

74HC123; 74HCT123

Dual retriggerable monostable multivibrator with reset

Rev. 04 — 16 June 2006

Product data sheet

1. General description

The 74HC123; 74HCT123 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC123; 74HCT123 are dual retriggerable monostable multivibrators with output pulse width control by three methods:

1. The basic pulse time is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}).
2. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\bar{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period ($nQ = \text{HIGH}$, $n\bar{Q} = \text{LOW}$) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input $n\bar{RD}$, which also inhibits the triggering.
3. An internal connection from $n\bar{RD}$ to the input gates makes it possible to trigger the circuit by a HIGH-going signal at input $n\bar{RD}$ as shown in the function table.

Schmitt-trigger action in the $n\bar{A}$ and nB inputs, makes the circuit highly tolerant to slower input rise and fall times.

The 74HC123; 74HCT123 is identical to the 74HC423; 74HCT423 but can be triggered via the reset input.

2. Features

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100 % duty factor
- Direct reset terminates output pulse
- Schmitt-trigger action on all inputs except for the reset input
- ESD protection:
 - ◆ HBM EIA/JESD22-A114-C exceeds 2000 V
 - ◆ MM EIA/JESD22-A115-A exceeds 200 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

PHILIPS

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC123				
74HC123N	−40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74HC123D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC123DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC123PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC123BQ	−40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT123				
74HCT123N	−40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74HCT123D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT123DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT123PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

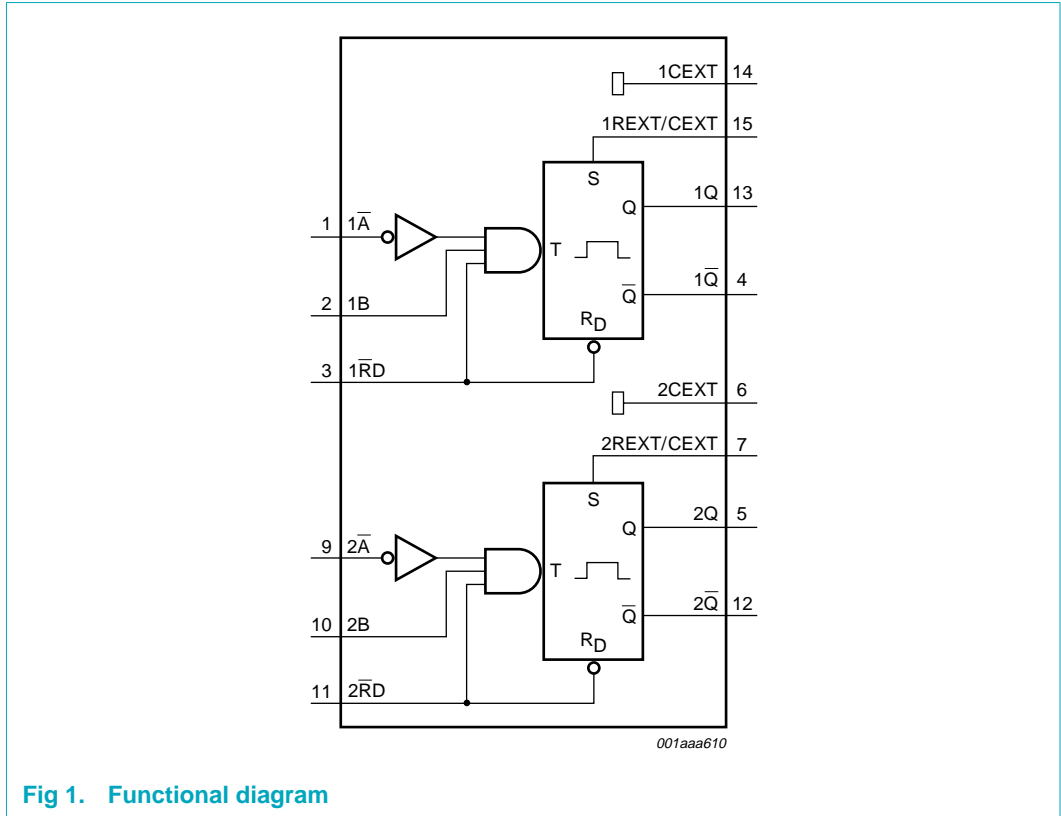


Fig 1. Functional diagram

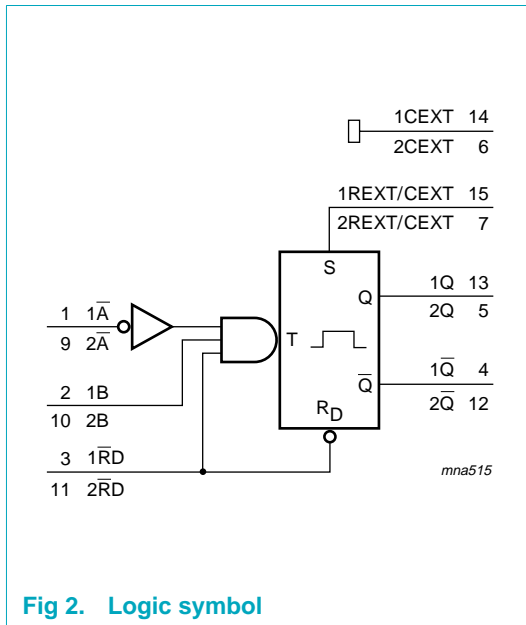


Fig 2. Logic symbol

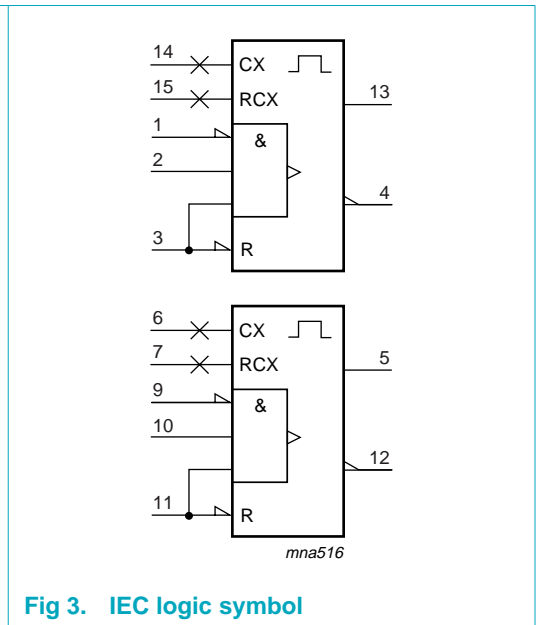


Fig 3. IEC logic symbol

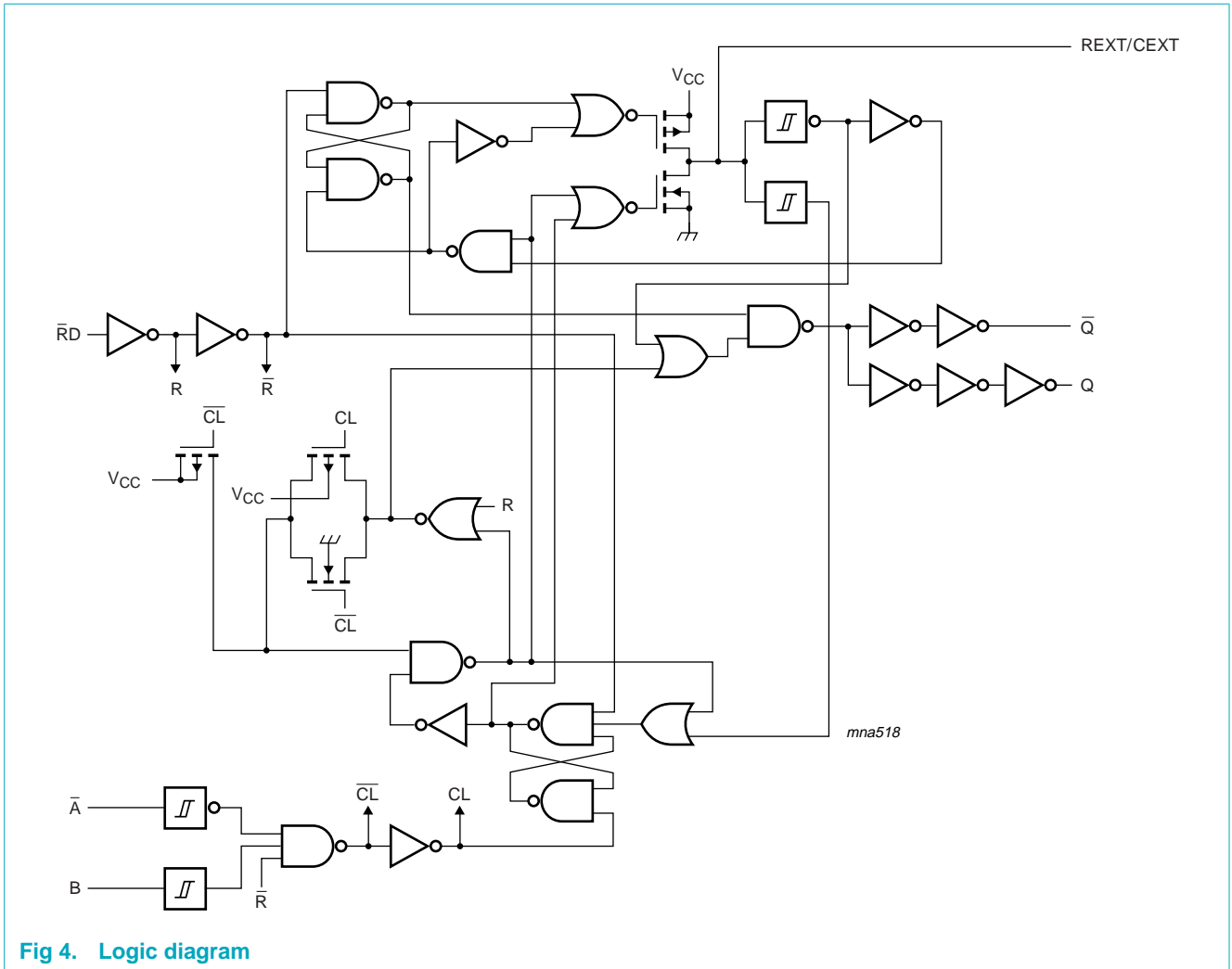
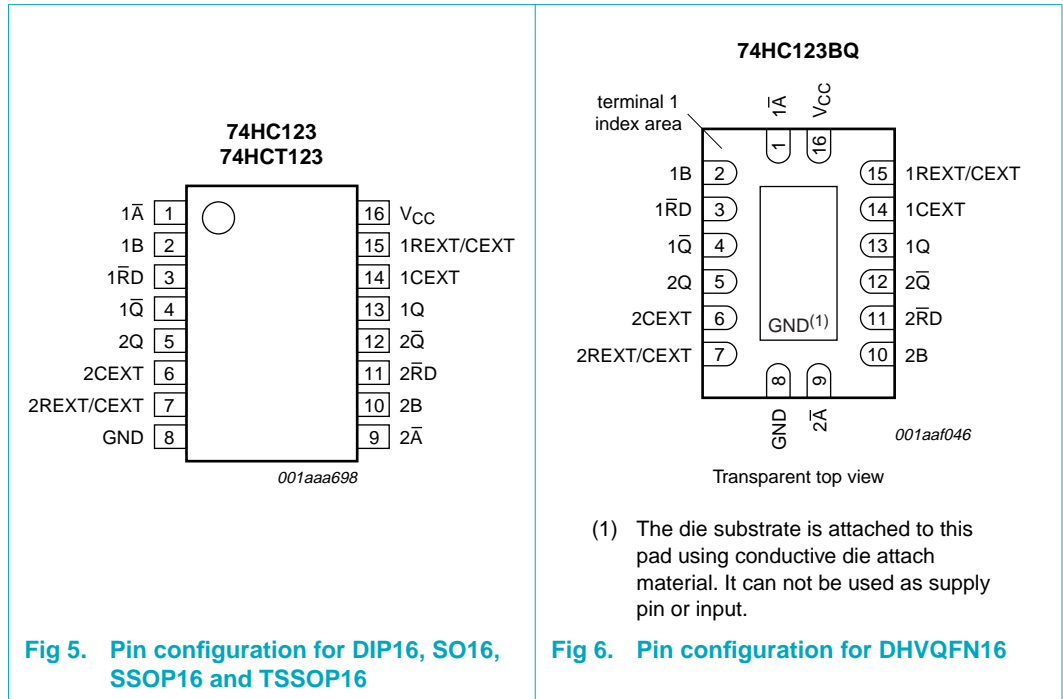


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning









5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1Ā	1	negative-edge triggered input 1
1B	2	positive-edge triggered input 1
1RD̄	3	direct reset LOW and positive-edge triggered input 1
1Q̄	4	active LOW output 1
2Q	5	active HIGH output 2
2CEXT	6	external capacitor connection 2
2REXT/CEXT	7	external resistor and capacitor connection 2
GND	8	ground (0 V)
2Ā	9	negative-edge triggered input 2
2B	10	positive-edge triggered input 2
2RD̄	11	direct reset LOW and positive-edge triggered input 2
2Q̄	12	active LOW output 2
1Q	13	active HIGH output 1
1CEXT	14	external capacitor connection 1
1REXT/CEXT	15	external resistor and capacitor connection 1
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table^[1]

Input			Output	
nRD	nA	nB	nQ	nQ
L	X	X	L	H
X	H	X	L ^[2]	H ^[2]
X	X	L	L ^[2]	H ^[2]
H	L	↑		
H	↓	H		
↑	L	H		


[1] H = HIGH voltage level


L = LOW voltage level

X = don't care

↑ = LOW-to-HIGH transition

↓ = HIGH-to-LOW transition

 = one HIGH level output pulse

 = one LOW level output pulse

[2] If the monostable was triggered before this condition was established, the pulse will continue as programmed.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_O	output current	except for pins nREXT/CEXT; $V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	± 25	mA
I_{CC}	quiescent supply current		-	50	mA
I_{GND}	ground current		-	-50	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation				
	DIP16 package		[1] -	750	mW
	SO16 package		[2] -	500	mW
	SSOP16 package		[3] -	500	mW
	TSSOP16 package		[3] -	500	mW
	DHVQFN16 package		[4] -	500	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[4] For DHVQFN16 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC123						
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
t_r, t_f	input rise and fall time	nRD input				
		$V_{CC} = 2.0\text{ V}$	-	-	1000	ns
		$V_{CC} = 4.5\text{ V}$	-	6.0	500	ns
		$V_{CC} = 6.0\text{ V}$	-	-	400	ns
T_{amb}	ambient temperature		-40	+25	+125	°C
74HCT123						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
t_r, t_f	input rise and fall time	nRD input; $V_{CC} = 4.5\text{ V}$	-	6.0	500	ns
T_{amb}	ambient temperature		-40	+25	+125	°C

9. Static characteristics

Table 6. Static characteristics 74HC123

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25\text{ °C}$						
V_{IH}	HIGH-state input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	V
V_{IL}	LOW-state input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 2.0\text{ V}$	1.9	2.0	-	V
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$	4.4	4.5	-	V
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 6.0\text{ V}$	5.9	6.0	-	V
		$I_O = -4\text{ mA}$; $V_{CC} = 4.5\text{ V}$	3.98	4.32	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 2.0\text{ V}$	-	0	0.1	V
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$	-	0	0.1	V
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 6.0\text{ V}$	-	0	0.1	V
		$I_O = 4\text{ mA}$; $V_{CC} = 4.5\text{ V}$	-	0.15	0.26	V
	$I_O = 5.2\text{ mA}$; $V_{CC} = 6.0\text{ V}$	-	0.16	0.26	V	
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\text{ V}$	-	-	± 0.1	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$; $V_{CC} = 6.0\text{ V}$	-	-	8.0	μA
C_i	input capacitance		-	3.5	-	pF
$T_{amb} = -40\text{ °C to }+85\text{ °C}$						
V_{IH}	HIGH-state input voltage	$V_{CC} = 2.0\text{ V}$	1.5	-	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	-	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	-	-	V
V_{IL}	LOW-state input voltage	$V_{CC} = 2.0\text{ V}$	-	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	-	1.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 2.0\text{ V}$	1.9	-	-	V
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$	4.4	-	-	V
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 6.0\text{ V}$	5.9	-	-	V
		$I_O = -4\text{ mA}$; $V_{CC} = 4.5\text{ V}$	3.84	-	-	V
	$I_O = -5.2\text{ mA}$; $V_{CC} = 6.0\text{ V}$	5.34	-	-	V	

Table 6. Static characteristics 74HC123 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OL}	LOW-state output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 2.0 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	-	0.33	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	-	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±1.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	80	μA
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-state input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-state input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V _{OH}	HIGH-state output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	-	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	-	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	-	-	V
		I _O = -4 mA; V _{CC} = 4.5 V	3.7	-	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.2	-	-	V
V _{OL}	LOW-state output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 2.0 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 4.5 V	-	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	-	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±1.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	160	μA

Table 7. Static characteristics 74HCT123

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{IH}	HIGH-state input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V _{IL}	LOW-state input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
V _{OH}	HIGH-state output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V				
		I _O = -20 μA	4.4	4.5	-	V
		I _O = -4 mA	3.98	4.32	-	V

Table 7. Static characteristics 74HCT123 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OL}	LOW-state output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V				
		I _O = 20 μA	-	0	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	μA
ΔI _{CC}	additional quiescent supply current	per input pin; V _I = V _{CC} - 2.1 V and other inputs at V _{CC} or GND; I _O = 0 A; V _{CC} = 4.5 V to 5.5 V				
		pins n \bar{A} , nB	-	35	125	μA
		pin n \bar{RD}	-	50	180	μA
C _i	input capacitance		-	3.5	-	pF
T_{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-state input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V _{IL}	LOW-state input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V _{OH}	HIGH-state output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V				
		I _O = -20 μA	4.4	-	-	V
		I _O = -4.0 mA	3.84	-	-	V
V _{OL}	LOW-state output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V				
		I _O = 20 μA	-	-	0.1	V
		I _O = 4.0 mA	-	-	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±1.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	80	μA
ΔI _{CC}	additional quiescent supply current	per input pin; V _I = V _{CC} - 2.1 V and other inputs at V _{CC} or GND; I _O = 0 A; V _{CC} = 4.5 V to 5.5 V				
		pins n \bar{A} , nB	-	-	160	μA
		pin n \bar{RD}	-	-	225	μA
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-state input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V _{IL}	LOW-state input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V _{OH}	HIGH-state output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V				
		I _O = -20 μA	4.4	-	-	V
		I _O = -4 mA	3.7	-	-	V
V _{OL}	LOW-state output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V				
		I _O = 20 μA	-	-	0.1	V
		I _O = 4.0 mA	-	-	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±1.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	160	μA

Table 7. Static characteristics 74HCT123 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔI_{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC} - 2.1$ V and other inputs at V_{CC} or GND; $I_O = 0$ A; $V_{CC} = 4.5$ V to 5.5 V				
		pins $n\bar{A}$, nB	-	-	170	μ A
		pin $n\bar{RD}$	-	-	245	μ A

10. Dynamic characteristics

Table 8. Dynamic characteristics 74HC123Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified.For test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C						
t_{PHL} , t_{PLH}	propagation delay	$C_{EXT} = 0$ pF; $R_{EXT} = 5$ k Ω ; see Figure 9				
	$n\bar{RD}$, $n\bar{A}$, nB to nQ or $n\bar{Q}$	$V_{CC} = 2.0$ V	-	83	255	ns
		$V_{CC} = 4.5$ V	-	30	51	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	26	-	ns
		$V_{CC} = 6.0$ V	-	24	43	ns
	$n\bar{RD}$ (reset) to nQ or $n\bar{Q}$	$V_{CC} = 2.0$ V	-	66	215	ns
		$V_{CC} = 4.5$ V	-	24	43	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	20	-	ns
		$V_{CC} = 6.0$ V	-	19	37	ns
t_{THL} , t_{TLH}	output transition time	see Figure 9				
		$V_{CC} = 2.0$ V	-	19	75	ns
		$V_{CC} = 4.5$ V	-	7	15	ns
		$V_{CC} = 6.0$ V	-	6	13	ns
t_W	pulse width					
	$n\bar{A}$ LOW	see Figure 10				
		$V_{CC} = 2.0$ V	100	8	-	ns
		$V_{CC} = 4.5$ V	20	3	-	ns
		$V_{CC} = 6.0$ V	17	2	-	ns
	nB HIGH	see Figure 10				
		$V_{CC} = 2.0$ V	100	17	-	ns
		$V_{CC} = 4.5$ V	20	6	-	ns
		$V_{CC} = 6.0$ V	17	5	-	ns
	$n\bar{RD}$ LOW	see Figure 11				
		$V_{CC} = 2.0$ V	100	14	-	ns
		$V_{CC} = 4.5$ V	20	5	-	ns
		$V_{CC} = 6.0$ V	17	4	-	ns
	nQ HIGH and $n\bar{Q}$ LOW	$V_{CC} = 5.0$ V; see Figure 10 and 11				
		$C_{EXT} = 100$ nF; $R_{EXT} = 10$ k Ω	-	450	-	μ s
		$C_{EXT} = 0$ pF; $R_{EXT} = 5$ k Ω	-	75	-	ns

Table 8. Dynamic characteristics 74HC123 ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified.

For test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rt}	retrigger time $n\bar{A}$, nB	$C_{EXT} = 0$ pF; $R_{EXT} = 5$ k Ω ; $V_{CC} = 5.0$ V; see Figure 10	[2][3]	-	110	- ns
R_{EXT}	external timing resistor	see Figure 7				
		$V_{CC} = 2.0$ V	10	-	1000	k Ω
		$V_{CC} = 5.0$ V	2	-	1000	k Ω
C_{EXT}	external timing capacitor	$V_{CC} = 5.0$ V; see Figure 7	[3]	no limits		pF
C_{PD}	power dissipation capacitance	per monostable	[4][5]	-	54	- pF
$T_{amb} = -40$ °C to $+85$ °C						
t_{PHL} , t_{PLH}	propagation delay $n\bar{RD}$, $n\bar{A}$, nB to nQ or $n\bar{Q}$	$C_{EXT} = 0$ pF; $R_{EXT} = 5$ k Ω ; see Figure 9				
		$V_{CC} = 2.0$ V	-	-	320	ns
		$V_{CC} = 4.5$ V	-	-	64	ns
	$n\bar{RD}$ (reset) to nQ or $n\bar{Q}$	$V_{CC} = 6.0$ V	-	-	54	ns
		$V_{CC} = 2.0$ V	-	-	270	ns
		$V_{CC} = 4.5$ V	-	-	54	ns
t_{THL} , t_{TLH}	output transition time	$V_{CC} = 6.0$ V	-	-	46	ns
		see Figure 9				
		$V_{CC} = 2.0$ V	-	-	95	ns
t_w	pulse width n \bar{A} LOW	$V_{CC} = 4.5$ V	-	-	19	ns
		$V_{CC} = 6.0$ V	-	-	16	ns
		see Figure 10				
	nB HIGH	$V_{CC} = 2.0$ V	125	-	-	ns
		$V_{CC} = 4.5$ V	25	-	-	ns
		$V_{CC} = 6.0$ V	21	-	-	ns
	n \bar{RD} LOW	see Figure 11				
		$V_{CC} = 2.0$ V	125	-	-	ns
		$V_{CC} = 4.5$ V	25	-	-	ns
	$V_{CC} = 6.0$ V	21	-	-	ns	

Table 8. Dynamic characteristics 74HC123 ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified.

For test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40$ °C to $+125$ °C						
t_{PHL} , t_{PLH}	propagation delay	$C_{EXT} = 0$ pF; $R_{EXT} = 5$ k Ω ; see Figure 9				
	$n\overline{RD}$, $n\overline{A}$, nB to nQ or $n\overline{Q}$	$V_{CC} = 2.0$ V	-	-	385	ns
		$V_{CC} = 4.5$ V	-	-	77	ns
		$V_{CC} = 6.0$ V	-	-	65	ns
	$n\overline{RD}$ (reset) to nQ or $n\overline{Q}$	$V_{CC} = 2.0$ V	-	-	325	ns
		$V_{CC} = 4.5$ V	-	-	65	ns
		$V_{CC} = 6.0$ V	-	-	55	ns
t_{THL} , t_{TLH}	output transition time	see Figure 9				
		$V_{CC} = 2.0$ V	-	-	110	ns
		$V_{CC} = 4.5$ V	-	-	22	ns
		$V_{CC} = 6.0$ V	-	-	19	ns
t_W	pulse width					
	$n\overline{A}$ LOW	see Figure 10				
		$V_{CC} = 2.0$ V	150	-	-	ns
		$V_{CC} = 4.5$ V	30	-	-	ns
		$V_{CC} = 6.0$ V	26	-	-	ns
	nB HIGH	see Figure 10				
		$V_{CC} = 2.0$ V	150	-	-	ns
		$V_{CC} = 4.5$ V	30	-	-	ns
		$V_{CC} = 6.0$ V	26	-	-	ns
	$n\overline{RD}$ LOW	see Figure 11				
		$V_{CC} = 2.0$ V	150	-	-	ns
		$V_{CC} = 4.5$ V	30	-	-	ns
		$V_{CC} = 6.0$ V	26	-	-	ns

[1] For other R_{EXT} and C_{EXT} combinations see [Figure 7](#). If $C_{EXT} > 10$ nF, the next formula is valid.

$t_W = K \times R_{EXT} \times C_{EXT}$, where:

t_W = typical output pulse width in ns;

R_{EXT} = external resistor in k Ω ;

C_{EXT} = external capacitor in pF;

K = constant = 0.45 for $V_{CC} = 5.0$ V and 0.55 for $V_{CC} = 2.0$ V.

The inherent test jig and pin capacitance at pins 15 and 7 ($nREXT/CEXT$) is approximately 7 pF.

[2] The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT} . The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time. If $C_{EXT} > 10$ pF, the next formula (at $V_{CC} = 5.0$ V) for the setup time of a retrigger pulse is valid:

$t_{rt} = 30 + 0.19 \times R_{EXT} \times C_{EXT}^{0.9} + 13 \times R_{EXT}^{1.05}$, where:

t_{rt} = retrigger time in ns;

C_{EXT} = external capacitor in pF;

R_{EXT} = external resistor in k Ω .

The inherent test jig and pin capacitance at pins 15 and 7 ($nREXT/CEXT$) is 7 pF.

[3] When the device is powered-up, initiate the device via a reset pulse, when $C_{EXT} < 50$ pF.

- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) + 0.75 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 16 \times V_{CC}$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 D = duty factor in %;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 C_{EXT} = timing capacitance in pF;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ sum of outputs.
- [5] The condition is $V_I = GND$ to V_{CC} .

Table 9. Dynamic characteristics 74HCT123

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified.
 For test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25\text{ }^\circ\text{C}$						
t_{PHL}	propagation delay	$C_{EXT} = 0$ pF; $R_{EXT} = 5$ k Ω ; see Figure 9				
	$n\bar{R}D$, $n\bar{A}$, nB to $n\bar{Q}$	$V_{CC} = 4.5$ V	-	30	51	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	26	-	ns
	$n\bar{R}D$ (reset) to nQ	$V_{CC} = 4.5$ V	-	27	46	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	23	-	ns
t_{PLH}	propagation delay	$C_{EXT} = 0$ pF; $R_{EXT} = 5$ k Ω ; see Figure 9				
	$n\bar{R}D$, $n\bar{A}$, nB to nQ	$V_{CC} = 4.5$ V	-	28	51	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	26	-	ns
	$n\bar{R}D$ (reset) to $n\bar{Q}$	$V_{CC} = 4.5$ V	-	23	46	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	23	-	ns
t_{THL} , t_{TLH}	output transition time	$V_{CC} = 4.5$ V; see Figure 9	-	7	15	ns
t_W	pulse width	$V_{CC} = 4.5$ V				
	$n\bar{A}$ LOW	see Figure 10	20	3	-	ns
	nB HIGH	see Figure 10	20	5	-	ns
	$n\bar{R}D$ LOW	see Figure 11	20	7	-	ns
	nQ HIGH and $n\bar{Q}$ LOW	$V_{CC} = 5.0$ V; see Figure 10 and 11	[1]			
		$C_{EXT} = 100$ nF; $R_{EXT} = 10$ k Ω	-	450	-	μs
		$C_{EXT} = 0$ pF; $R_{EXT} = 5$ k Ω	-	75	-	ns
t_{rt}	retrigger time $n\bar{A}$, nB	$C_{EXT} = 0$ pF; $R_{EXT} = 5$ k Ω ; $V_{CC} = 5.0$ V; see Figure 10	[2][3]	-	110	ns
R_{EXT}	external timing resistor	$V_{CC} = 5.0$ V; see Figure 7	2	-	1000	k Ω
C_{EXT}	external timing capacitor	$V_{CC} = 5.0$ V; see Figure 7	[3]	no limits		pF
C_{PD}	power dissipation capacitance	per monostable	[4][5]	-	56	pF
$T_{amb} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$						
t_{PHL}	propagation delay	$C_{EXT} = 0$ pF; $R_{EXT} = 5$ k Ω ; see Figure 9				
	$n\bar{R}D$, $n\bar{A}$, nB to $n\bar{Q}$	$V_{CC} = 4.5$ V	-	-	64	ns
	$n\bar{R}D$ (reset) to nQ	$V_{CC} = 4.5$ V	-	-	58	ns

Table 9. Dynamic characteristics 74HCT123 ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified.

For test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	propagation delay	$C_{EXT} = 0$ pF; $R_{EXT} = 5$ k Ω ; see Figure 9				
	$n\overline{RD}$, $n\overline{A}$, nB to nQ	$V_{CC} = 4.5$ V	-	-	64	ns
	$n\overline{RD}$ (reset) to $n\overline{Q}$	$V_{CC} = 4.5$ V	-	-	58	ns
t_{THL} , t_{TLH}	output transition time	$V_{CC} = 4.5$ V	-	-	19	ns
t_W	pulse width	$V_{CC} = 4.5$ V				
	$n\overline{A}$ LOW	see Figure 10	25	-	-	ns
	nB HIGH	see Figure 10	25	-	-	ns
	$n\overline{RD}$ LOW	see Figure 11	25	-	-	ns
$T_{amb} = -40$ °C to $+125$ °C						
t_{PHL}	propagation delay	$C_{EXT} = 0$ pF; $R_{EXT} = 5$ k Ω ; see Figure 9				
	$n\overline{RD}$, $n\overline{A}$, nB to $n\overline{Q}$	$V_{CC} = 4.5$ V	-	-	77	ns
	$n\overline{RD}$ to nQ (reset)	$V_{CC} = 4.5$ V	-	-	69	ns
t_{PLH}	propagation delay	$C_{EXT} = 0$ pF; $R_{EXT} = 5$ k Ω ; see Figure 9				
	$n\overline{RD}$, $n\overline{A}$, nB to nQ	$V_{CC} = 4.5$ V	-	-	77	ns
	$n\overline{RD}$ to $n\overline{Q}$ (reset)	$V_{CC} = 4.5$ V	-	-	69	ns
t_{THL} , t_{TLH}	output transition time	$V_{CC} = 4.5$ V	-	-	22	ns
t_W	pulse width	$V_{CC} = 4.5$ V				
	$n\overline{A}$ LOW	see Figure 10	30	-	-	ns
	nB HIGH	see Figure 10	30	-	-	ns
	$n\overline{RD}$ LOW	see Figure 11	30	-	-	ns

- [1] For other R_{EXT} and C_{EXT} combinations see [Figure 7](#). If $C_{EXT} > 10$ nF, the next formula is valid.

$t_W = K \times R_{EXT} \times C_{EXT}$, where:

t_W = typical output pulse width in ns;

R_{EXT} = external resistor in k Ω ;

C_{EXT} = external capacitor in pF;

K = constant = 0.45 for $V_{CC} = 5.0$ V, see [Figure 8](#).

The inherent test jig and pin capacitance at pins 15 and 7 ($nREXT/CEXT$) is approximately 7 pF.

- [2] The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT} . The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time. If $C_{EXT} > 10$ pF, the next formula (at $V_{CC} = 5.0$ V) for the setup time of a retrigger pulse is valid:

$t_{rt} = 30 + 0.19 \times R_{EXT} \times C_{EXT}^{0.9} + 13 \times R_{EXT}^{1.05}$, where:

t_{rt} = typical retrigger time in ns;

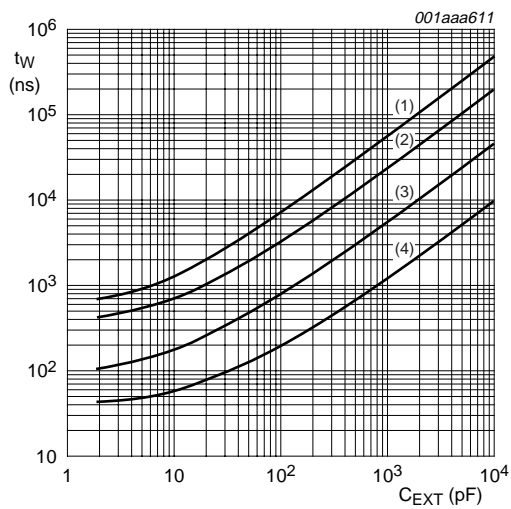
C_{EXT} = external capacitor in pF;

R_{EXT} = external resistor in k Ω .

The inherent test jig and pin capacitance at pins 15 and 7 ($nREXT/CEXT$) is 7 pF.

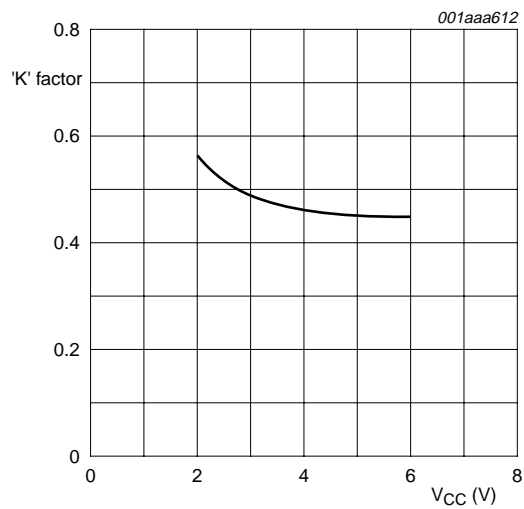
- [3] When the device is powered-up, initiate the device via a reset pulse, when $C_{EXT} < 50$ pF.

- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o) + 0.75 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 16 \times V_{CC}$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 D = duty factor in %;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 C_{EXT} = timing capacitance in pF;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ sum of outputs.
- [5] The condition is $V_I = GND$ to $V_{CC} - 1.5 V$.



$V_{CC} = 5.0 V$; $T_{amb} = 25\text{ }^\circ C$.
 (1) $R_{EXT} = 100\text{ k}\Omega$
 (2) $R_{EXT} = 50\text{ k}\Omega$
 (3) $R_{EXT} = 10\text{ k}\Omega$
 (4) $R_{EXT} = 2\text{ k}\Omega$

Fig 7. Typical output pulse width as a function of the external capacitor value



$C_X = 10\text{ nF}$; $R_X = 10\text{ k}\Omega$ to $100\text{ k}\Omega$

Fig 8. 74HCT123 typical 'K' factor as function of V_{CC}

11. Waveforms

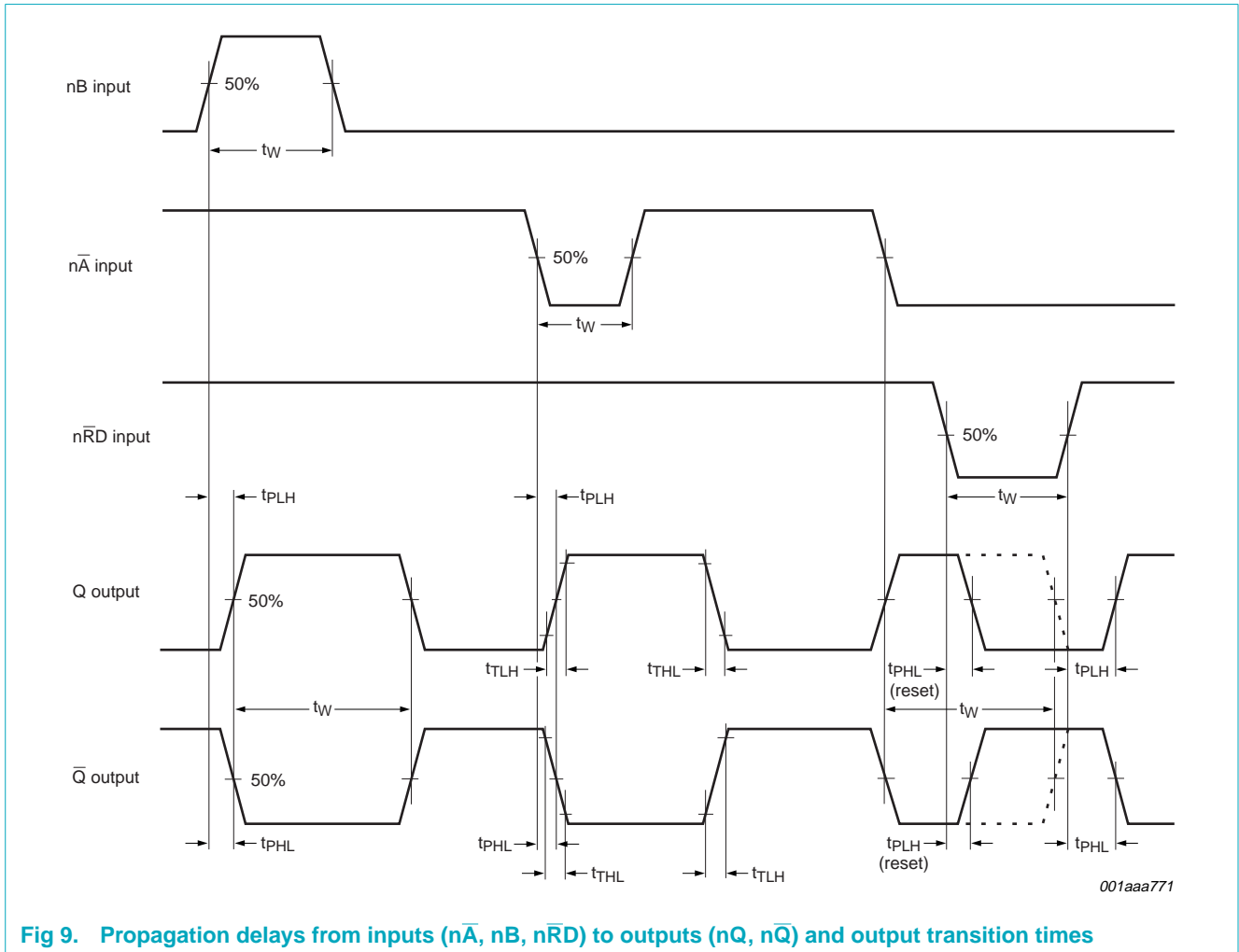


Fig 9. Propagation delays from inputs ($n\bar{A}$, nB , $n\bar{RD}$) to outputs (nQ , $n\bar{Q}$) and output transition times

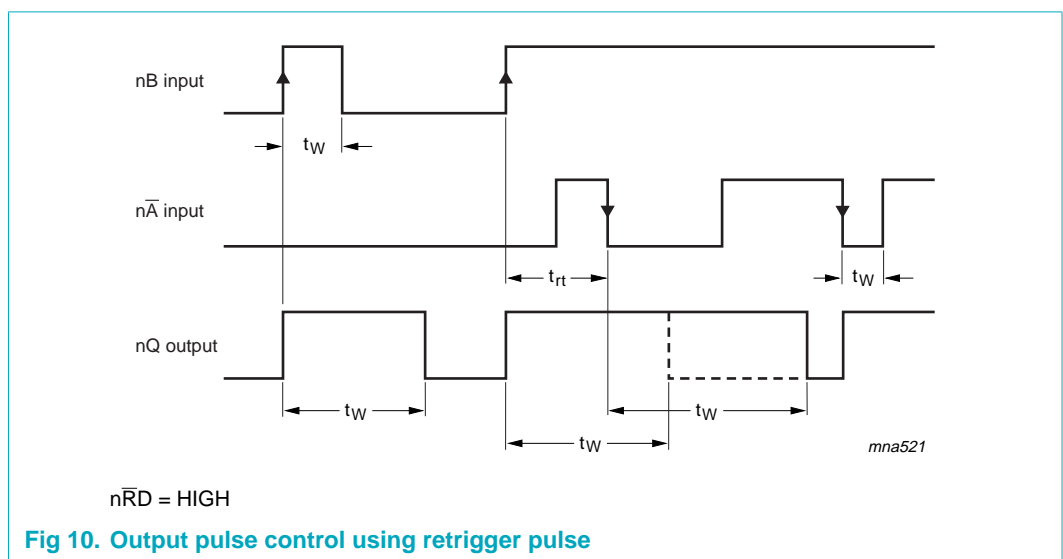


Fig 10. Output pulse control using retrigger pulse

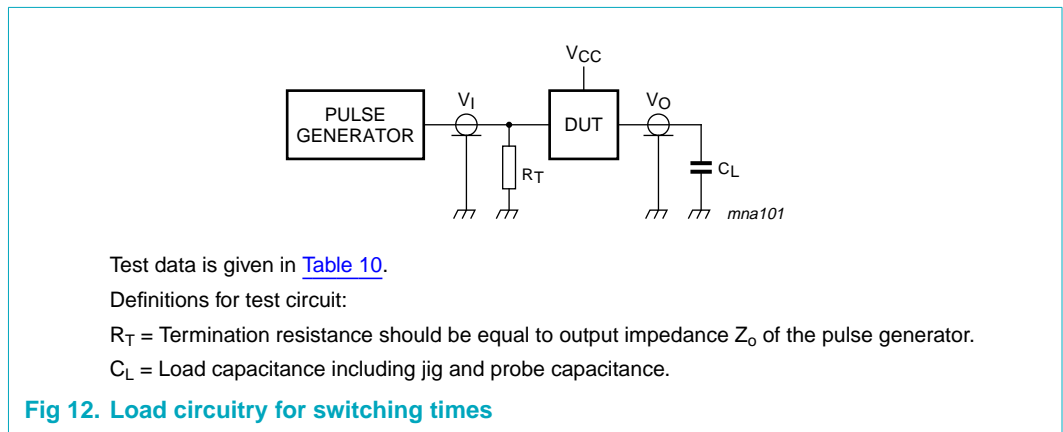
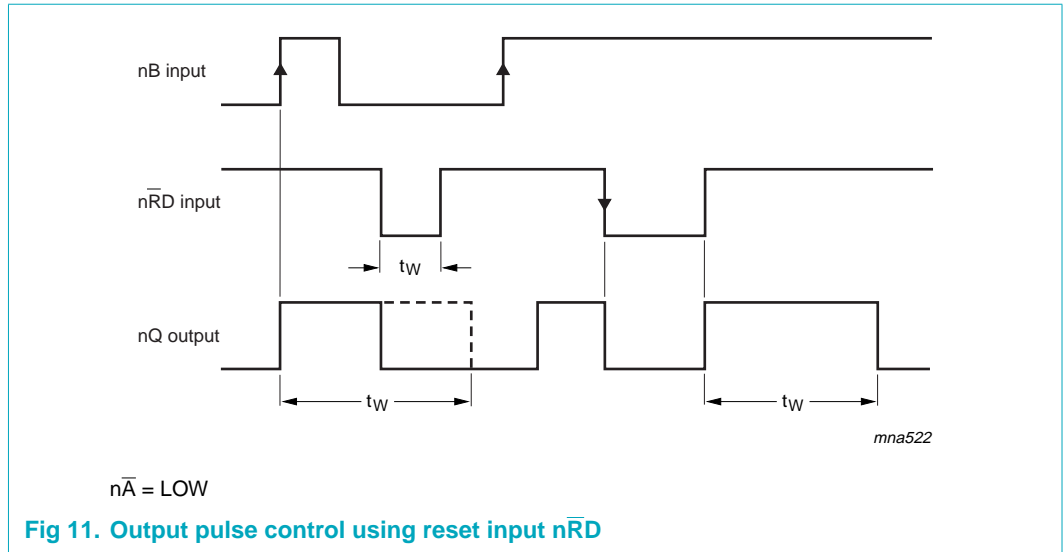


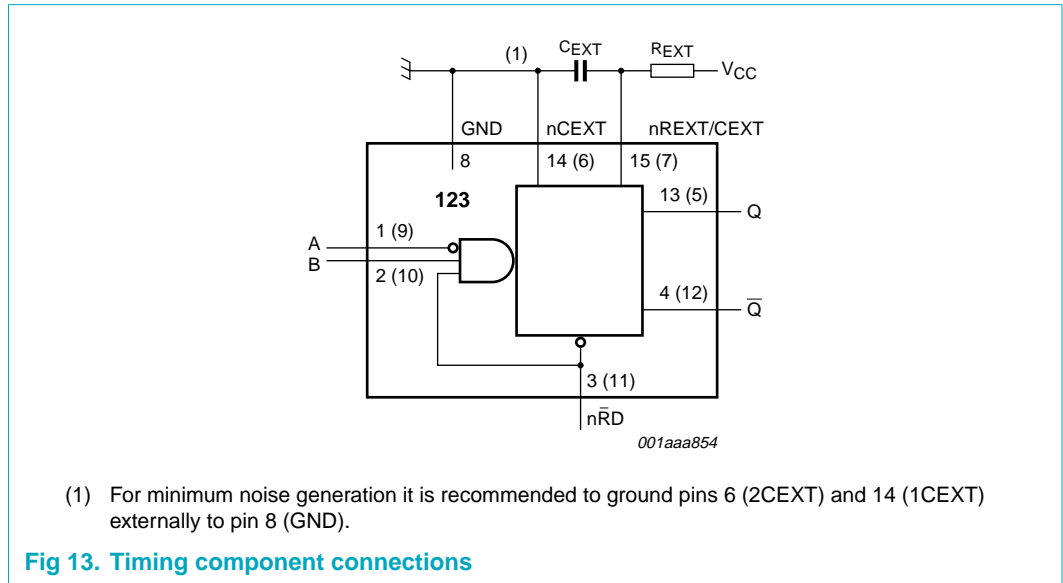
Table 10. Test data

Supply	Input		Load
V_{CC}	V_I	t_r, t_f	C_L
2.0 V to 6.0 V	V_{CC}	6 ns	15 pF or 50 pF

12. Application information

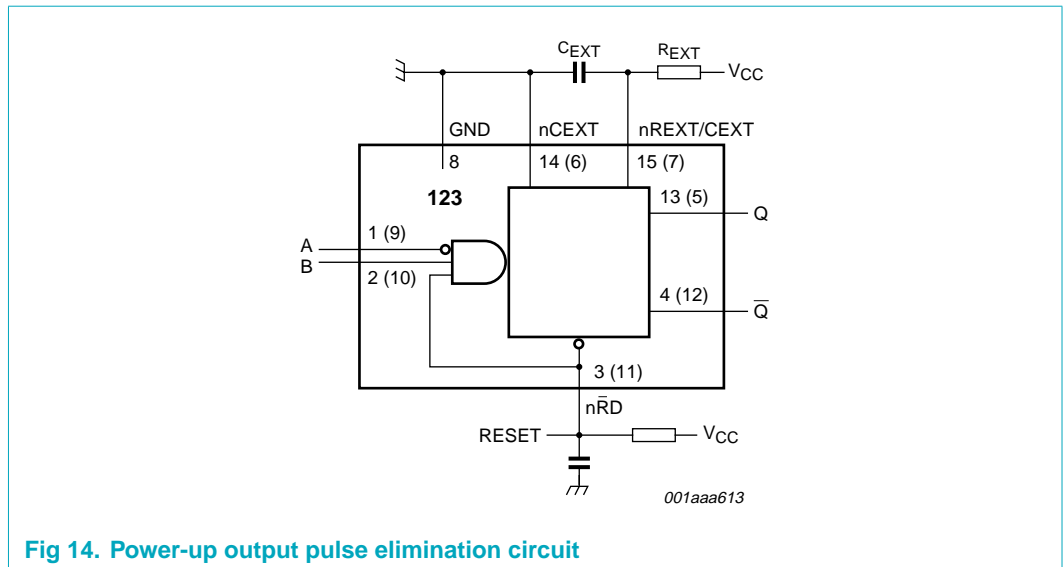
12.1 Timing component connections

The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT} .



12.2 Power-up considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of R_{EXT} and C_{EXT} . This output pulse can be eliminated using the circuit shown in [Figure 14](#).



12.3 Power-down considerations

A large capacitor C_{EXT} may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_{EXT}) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in [Figure 15](#).

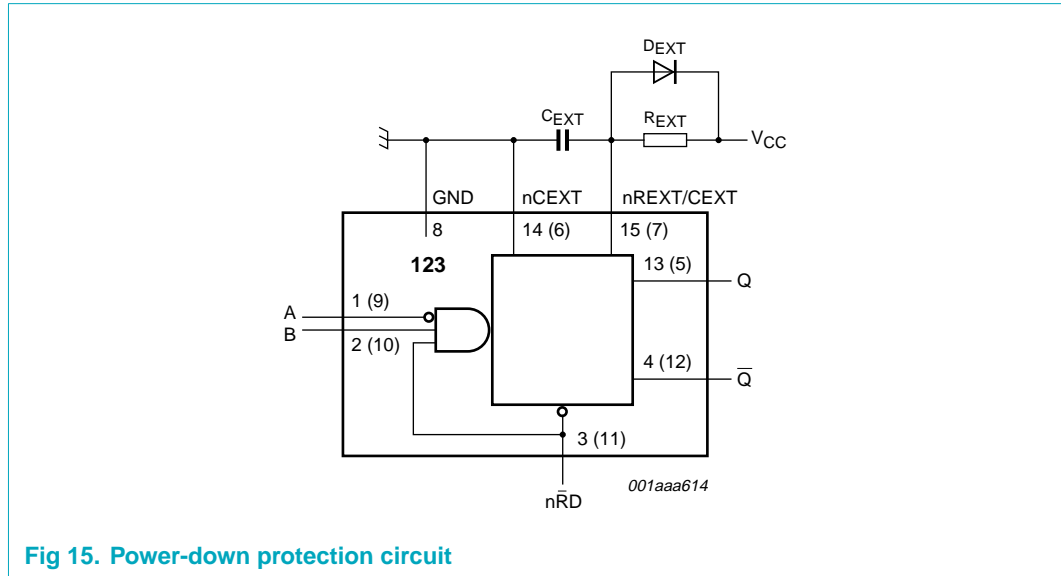


Fig 15. Power-down protection circuit

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil); long body

SOT38-1

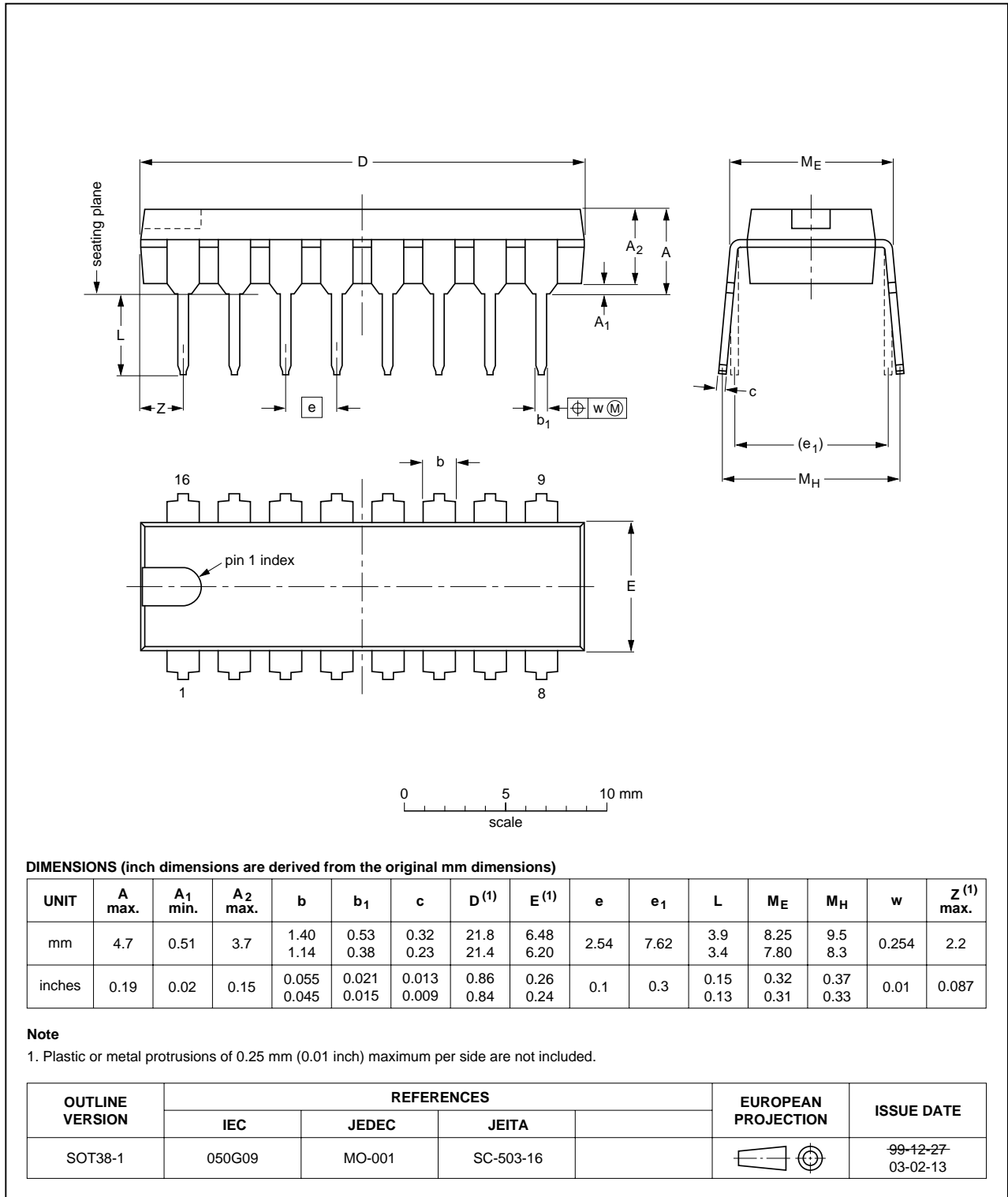


Fig 16. Package outline SOT38-1 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

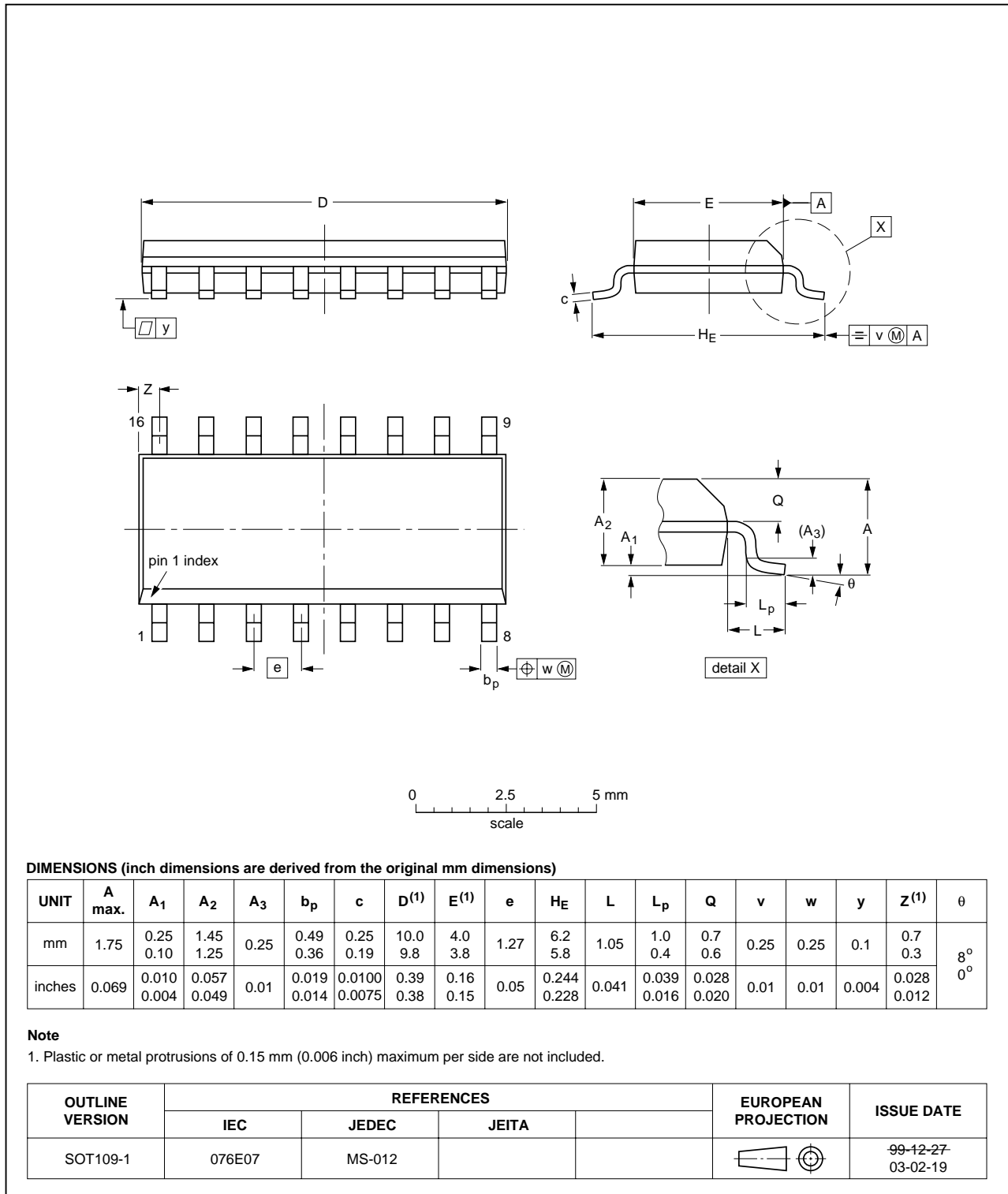


Fig 17. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

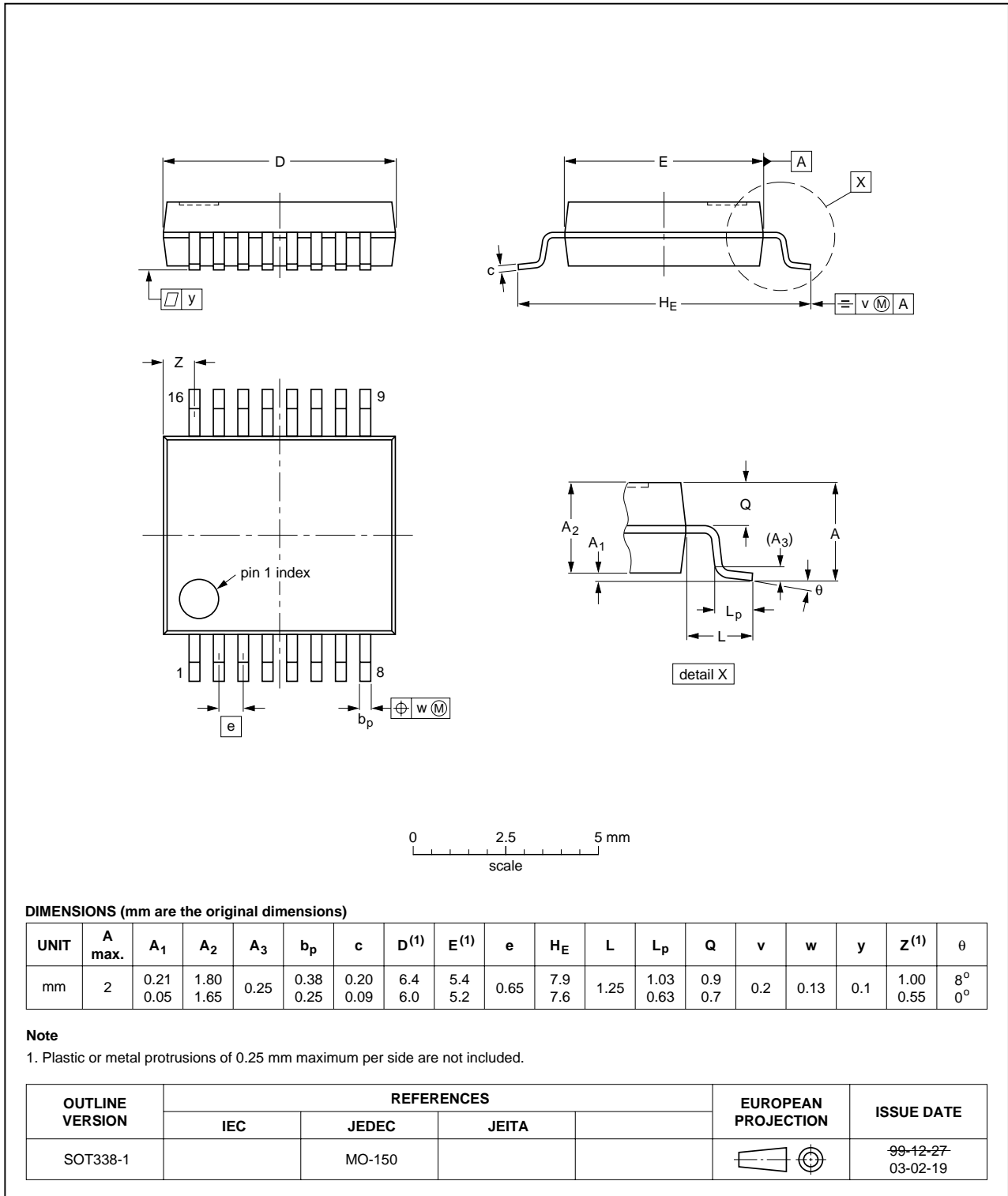


Fig 18. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

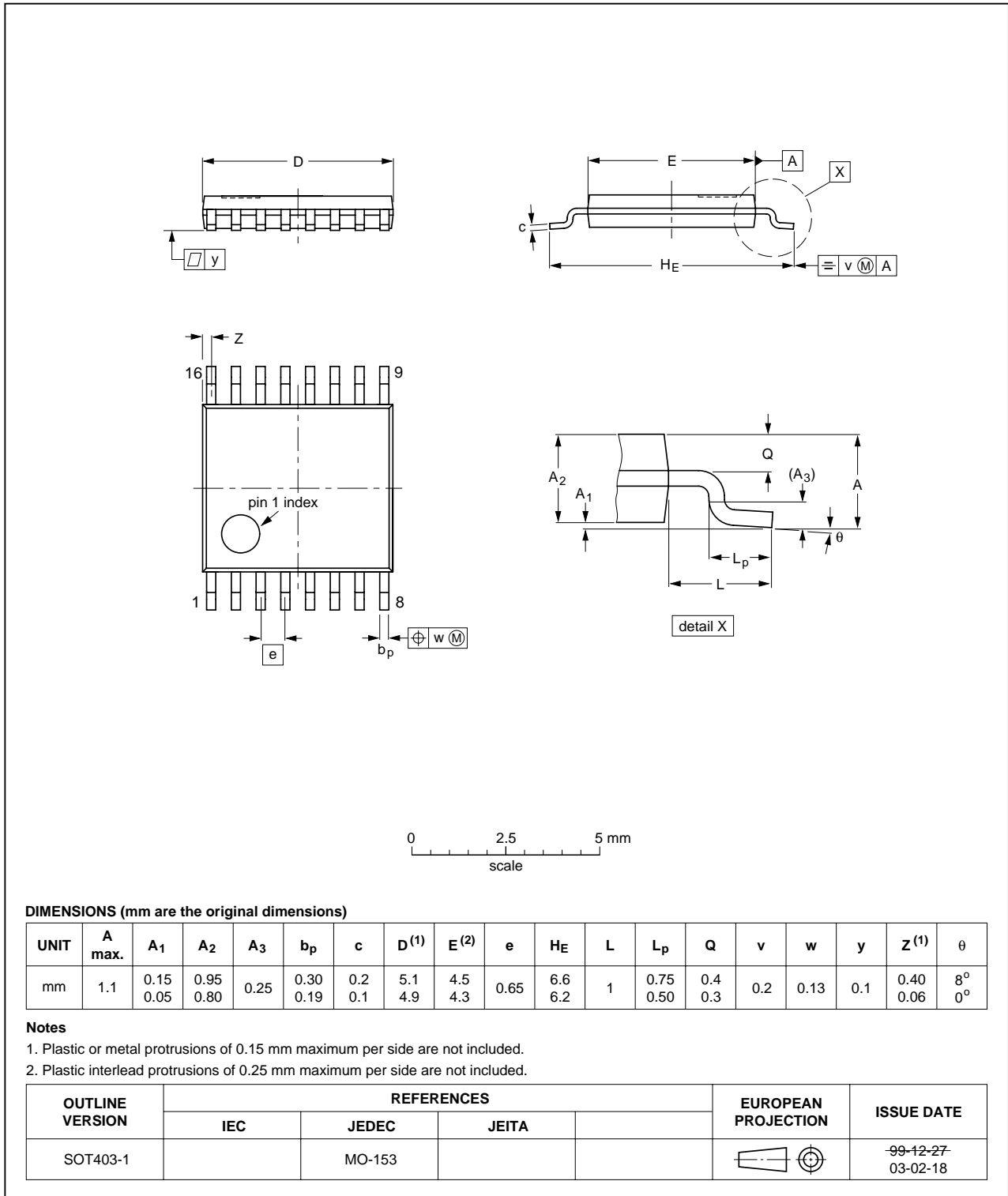


Fig 19. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

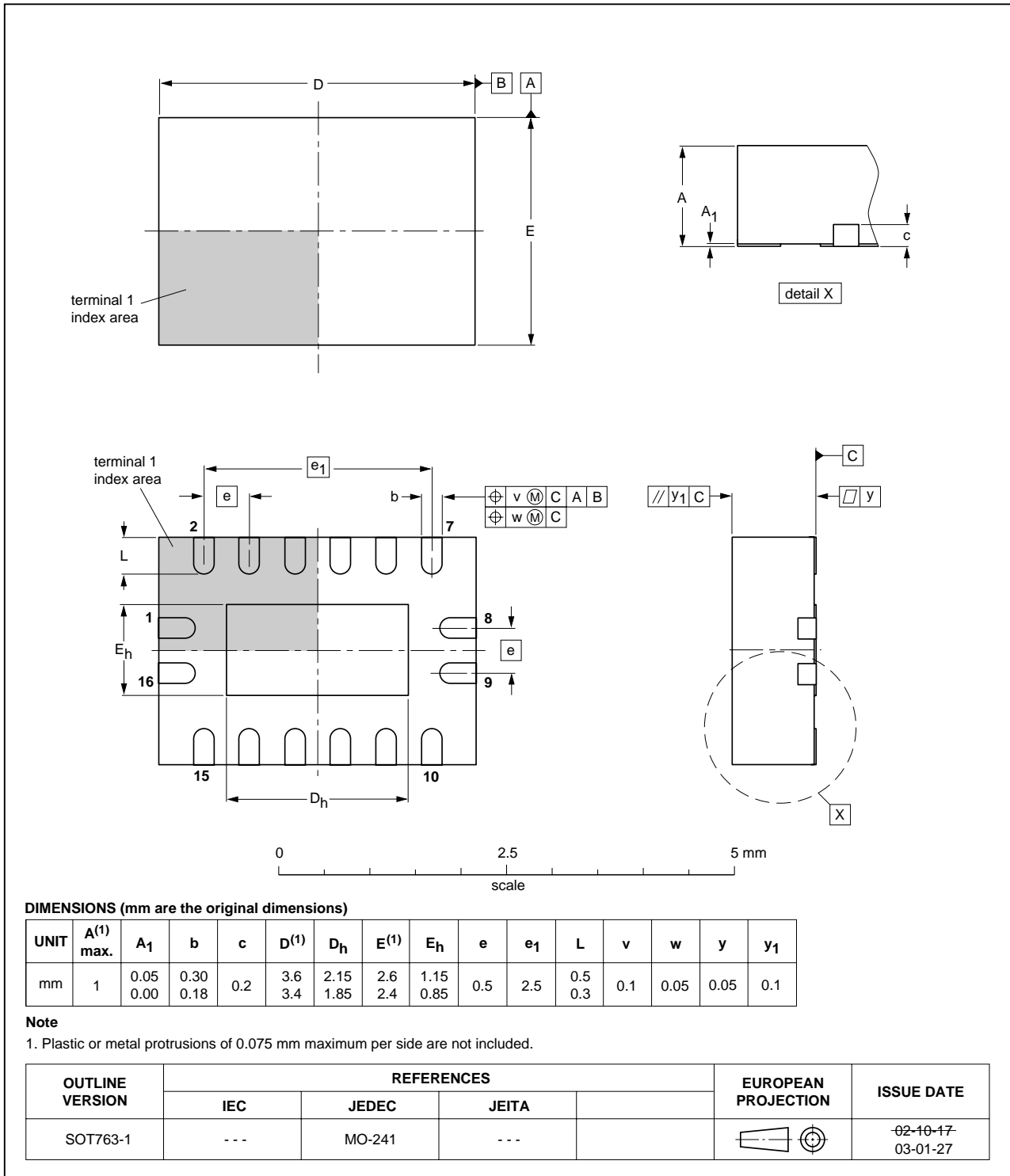


Fig 20. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 11. Abbreviations

Acronym	Abbreviation
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT123_4	20060616	Product data	-	74HC_HCT123_3
Modifications:	• Added: type number 74HC123BQ (DHVQFN16 package)			
74HC_HCT123_3 (9397 750 13024)	20040511	Product data	-	74HC_HCT123_2
74HC_HCT123_2	19980708	Product specification	-	74HC_HCT123_1

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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Date of release: 16 June 2006

Document identifier: 74HC_HCT123_4