FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27211-5E

ASSP For Power Supply Applications

BIPOLAR

Switching Regulator Controller
(Supporting External Synchronization)

MB3789

■ DESCRIPTION

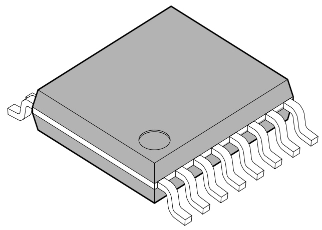
The MB3789 is a PWM (pulse width modulation) switching regulator controller supporting an external sync signal.
The MB3789 incorporates two error amplifiers which can be used respectively for voltage control and current control, allowing the IC to serve as a DC/DC converter with current regulating functions.
The MB3789 is the ideal IC for supplying power to the back-lighting fluorescent tube for a liquid crystal display (LCD) device such as a camera-integrated VTR.

■ FEATURES

- Wide range of operating power supply voltages: 3 V to 18 V
- Low current consumption: 1.5 mA (Typ)
- Wide input voltage range of error amplifier: –0.2 V to V_{CC} – 1.8 V
- Built-in two error amplifier
- Oscillator capable of operating with an external sync signal
- Built-in timer latch short protection circuit
- Variable dead time provides control over total operating range
- Output supporting a power MOSFET
- 16-pin SSOP package mountable at high density

■ PACKAGE

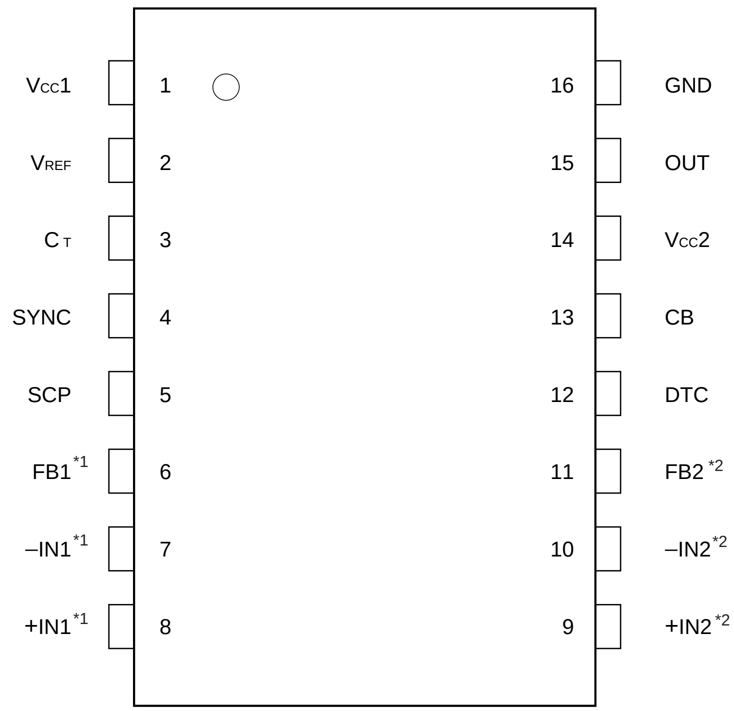
16-pin Plastic SSOP



(FPT-16P-M05)

■ PIN ASSIGNMENT

(TOP VIEW)



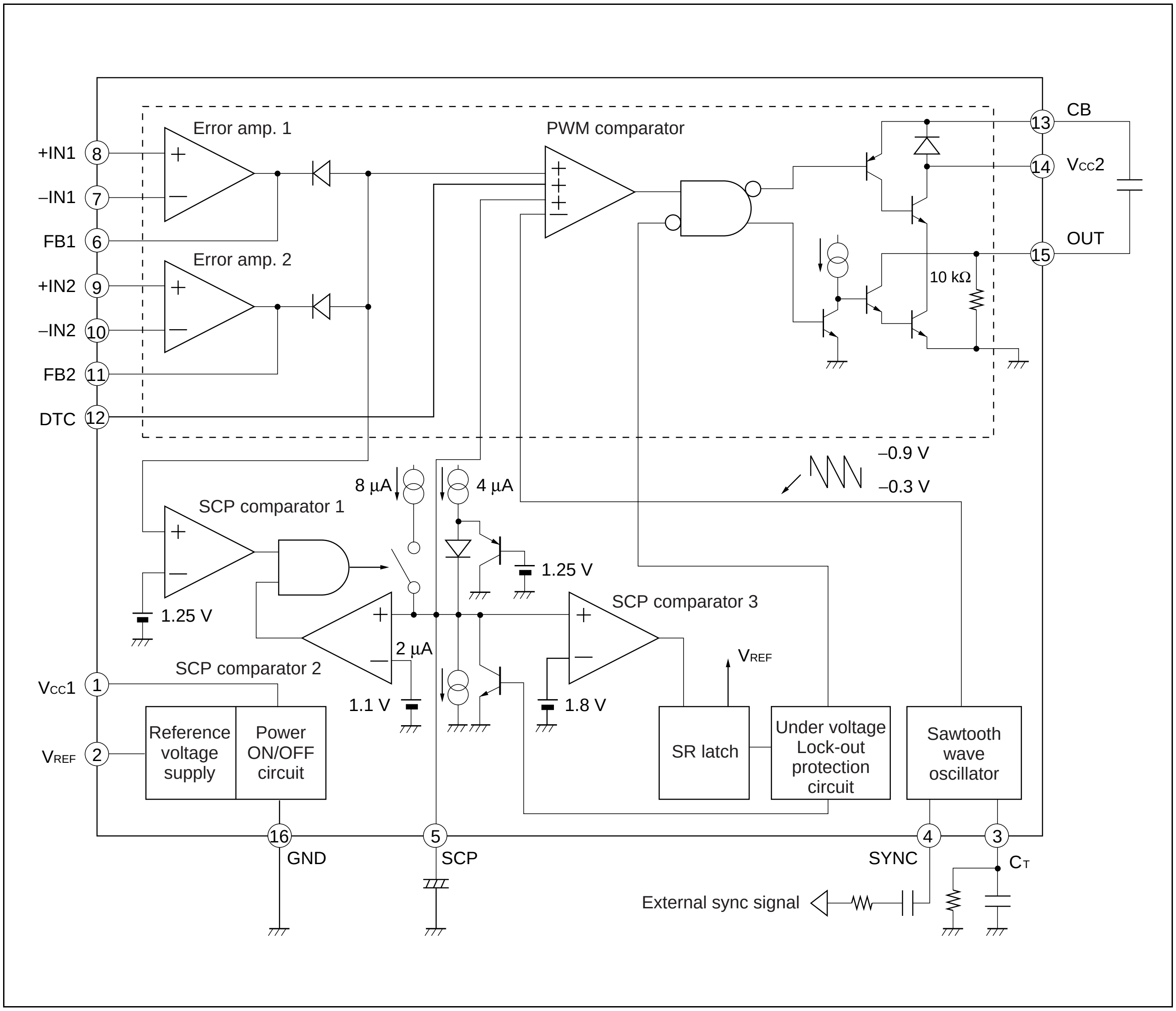
(FPT-16P-M05)

*1: Pins on error amplifier 1
*2: Pins on error amplifier 2

■ PIN DESCRIPTION

Pin no.		Pin symbol	I/O	Function
I/O control unit	7	–IN1	I	Error amplifier 1 inverting input pin
	8	+IN1	I	Error amplifier 1 noninverting input pin
	6	FB1	O	Error amplifier 1 output pin
	10	–IN2	I	Error amplifier 2 inverting input pin
	9	+IN2	I	Error amplifier 2 noninverting input pin
	11	FB2	O	Error amplifier 2 output pin
	13	CB	—	Output bootstrap pin. Connect a capacitor between the CB and OUT pins to bootstrap the output transistor.
	5	SCP	—	Capacitor connection pin for short-circuit protection circuit
	12	DTC	I	Dead time control pin
	15	OUT	O	Totem-pole output pin
Sawtooth waveform oscillator	3	C_T	—	Sawtooth waveform frequency setting capacitor/resistor connection pin
	4	SYNC	I	External sync signal input pin
Power-supply circuit	1	$V_{CC}1$	—	Reference power supply, control circuit power-supply pin
	14	$V_{CC}2$	—	Output circuit power-supply pin
	2	V_{REF}	O	Reference voltage output pin
	16	GND	—	Ground pin

■ BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTION

1. Switching Regulator Functions

(1) Reference voltage generator

The reference voltage generator uses the voltage supplied from the power supply pin (pin 1) to generate a temperature-compensated, reference voltage (about 2.50 V) as the reference supply voltage for the IC's internal circuitry.

The reference voltage can be output, up to 50 µA, to an external device through the V_{REF} pin (pin 2).

This regulated reference voltage can be used as the reference voltage for the switching regulator and also used for setting the dead time.

(2) Sawtooth waveform oscillator

With a timing capacitor and a timing resistor connected to the C_T pin (pin 3), the sawtooth waveform oscillator generates a sawtooth wave which remains stable even with supply voltage variations or temperature changes. The sawtooth wave is input to the PWM comparator. The amplitude of oscillating waveform is 0.3 V to 0.9 V.

In addition, the oscillator can be used for external synchronization, where it generates a sawtooth waveform synchronous to the input signal from the SYNC pin (pin 4).

(3) Error amplifiers

The error amplifiers detect the output voltage from the switching regulator and outputs the PWM control signal. Since they support a wide range of in-phase input voltages from –0.2 V to "V_{CC} – 1.8 V", they can be set easily from an external power supply.

An arbitrary loop gain can be set by connecting a feedback resistor and capacitor from the error amplifier output pin to the inverting input pin, enabling stable phase compensation to the system.

The MB3789 can make a current-regulated DC/DC converter using the two internal error amplifiers respectively for voltage control and current control.

(4) PWM comparator

The PWM comparator is a voltage comparator with one inverting input and three noninverting inputs, serving as a voltage-pulse width converter for controlling the output duty depending on the input voltage.

The PWM comparator turns on the output transistor during the interval in which the sawtooth wave voltage level is lower than the voltage levels at all of the error amplifier output pins, the SCP pin (pin 5), and at the DTC pin (pin 12).

(5) Output circuit

The output circuit is a power MOSFET driven, output circuit in a totem-pole configuration. It can drive the gate voltage up to near the supply voltage with a bootstrap capacitor connected between the OUT pin (pin 15) and CB pin (pin 13). (See "■ SETTING THE BOOTSTRAP CAPACITOR (C_{BS}).")

2. Protection Functions

(1) Timer-latch short-circuit protection circuit

SCP comparator 1 detects the output voltage levels of error amplifiers 1 and 2. When the output voltage level of both of the two error amplifiers reaches 1.25 V, the timer circuit is actuated to start charging the external protection-enable capacitor connected to the SCP pin (pin 5).

If the error amplifier output is not restored to the normal voltage level before the capacitor voltage reaches 1.8 V, the latch circuit is actuated to turn off the output transistor while making the dead time 100%.

To reset the actuated protection circuit, turn the power supply on back. (See "■ SETTING THE SOFT START/ SHORT-CIRCUIT DETECTION TIME.")

(2) Low input voltage malfunction preventive circuit

The transient state or a momentary decrease in supply voltage, which occurs when the power supply is turned on, may cause errors in the control IC, resulting in breakdown or degradation of the system. The low input voltage malfunction preventive circuit detects the internal reference voltage level according to the supply voltage level and, if the input voltage is low, turn off the output transistor and maintains the SCP pin (pin 5) at 0 V while making the dead time 100%.

The circuit restores voltage supply when the supply voltage reaches its threshold voltage.

■ ABSOLUTE MAXIMUM RATINGS

(Ta = +25°C)

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{CC}	—	—	20	V
Power dissipation	P_D	Ta ≦ +25°C	—	440*	mW
Operating temperature	Top	—	–30	+85	°C
Storage temperature	Tstg	—	–55	+125	°C

*: When mounted on a 10 cm-square double-side epoxy board.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

(Ta = +25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	$V_{CC}1$	—	3.0	5.0	18	V
	$V_{CC}2$		—	6.0	18	V
Reference voltage output current	I_{OR}	—	–50	–30	—	µA
Error amp. input voltage	V_I	—	–0.2	—	V_{CC} – 1.8	V
Output current	I_{O+}	CB = 4700 pF, t≦2 µs	–70	–40	—	mA
	I_{O-}	CB = 4700 pF, t≦2 µs	—	40	70	mA
Timing resistance	R_T	—	10	39	200	kΩ
Timing capacitance	C_T	—	470	1000	6800	pF
Oscillation frequency	f_{OSC}	—	1	20	200	kHz
Operating temperature	T_{OP}	—	–30	+25	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

($V_{CC}1$ = 5 V, $V_{CC}2$ = 6 V, Ta = +25°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Reference voltage block	Output voltage	V_{REF}	I_{OR} = 0 µA	2.400	2.500	2.600	V
	Output voltage temperature variation	$\Delta V_{REF}/V_{REF}$	Ta = –30°C to +85°C*	—	0.2	2	%
	Input stability	Line	V_{CC} = 3.0 V to 18 V	—	1	10	mV
	Load stability	Load	I_{OR} = 0 µA to –50 µA	—	2	10	mV
	Short output current	I_{OS}	V_{REF} = 0 V	–700	–450	–300	µA
Under voltage lockout protection circuit	Threshold voltage	V_{TH}	—	—	2.15	2.62	V
		V_{TL}	—	1.62	1.90	—	V
	Hysteresis width	V_{HYS}	—	80	250	—	mV
	Reset voltage (V_{CC})	V_R	—	1.0	1.4	—	V
Soft start block	Charge current	I_{CHG}	V_{SCP} 0.9 V	–2.8	–2.0	–1.2	µA
	Threshold voltage	V_{T0}	Duty cycle = 0%	0.2	0.3	0.4	V
		V_{T100}	Duty cycle = 100%	0.8	0.9	1.0	V
Short circuit detection block	Threshold voltage	V_{TH}	—	1.70	1.80	1.90	V
	Input standby voltage	V_{STB}	—	1.15	1.25	1.35	mV
	Input latch voltage	V_I	—	—	50	100	mV
	Input source current	I_I	V_{SCP} = 1.5 V	–8.4	–6.0	–3.6	µA
Triangular waveform oscillator block	Oscillator frequency	f_{OSC}	C_T = 1000 pF, R_T = 39 kΩ	17	20	23	kHz
	Frequency voltage variation	$\Delta f/f_{dv}$	V_{CC} = 3 V to 18 V	—	1	10	%
	Frequency temperature variation	$\Delta f/f_{dT}$	Ta = –30°C to +85°C*	—	3	—	%
	Synchronous pin input current	I_{SYNC}	V_{THSY} = 5 V	0.9	1.3	2.2	mA
	Synchronous pin threshold voltage	V_{THSY}	—	0.65	0.75	0.85	V

*: Standard design value

(Continued)

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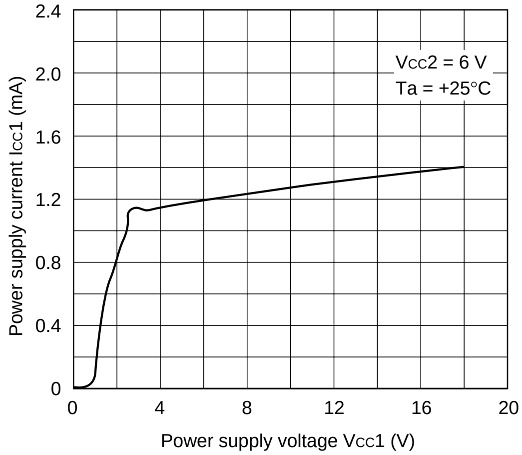
($V_{CC}1$ = 5 V, $V_{CC}2$ = 6 V, Ta = +25°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Error amplifier	Input offset voltage	V_{IO}	V_{FB} = 0.6 V	—	—	10	mV
	Input offset current	I_{IO}	V_{FB} = 0.6 V	—	—	100	nA
	Input bias current	I_B	V_{FB} = 0.6 V	–200	–30	—	nA
	Common mode input voltage range	V_{CM}	—	–0.2	—	V_{CC} – 0.8	V
	Common mode rejection ratio	C_{MRR}	—	60	100	—	dB
	Voltage gain	A_V	—	60	100	—	dB
	Frequency bandwidth	BW	A_V = 0 dB*	—	800	—	kHz
	Maximum output voltage range	V_{OM+}	—	V_{REF} – 0.3	2.4	—	V
		V_{OM-}	—	—	0.05	0.3	V
	Output sink current	I_{OM+}	V_{FB} = 0.6 V	30	60	—	µA
	Output source current	I_{OM-}	V_{FB} = 0.6 V	—	–2	–0.6	mA
Dead time control block	Threshold voltage	V_{T0}	Duty cycle = 0%	0.2	0.3	0.4	V
		V_{T100}	Duty cycle = 100%	0.8	0.9	1.0	V
	ON duty cycle	Dtr	V_{dt} = V_{REF}/4.2	45	55	65	%
	Input bias current	I_{Ibdt}	—	–500	–100	—	nA
PWM comparator block	Threshold voltage	V_{T0}	Duty cycle = 0%	0.2	0.3	0.4	V
		V_{T100}	Duty cycle = 100%	0.8	0.9	1.0	V
	Input sink current	I_{IN+}	—	30	60	—	µA
	Input source current	I_{IN-}	—	—	–2	–0.6	mA
Output block	Output voltage	V_{OH}	CL = 2000 pF, CB = 4700 pF	5.5	6.0	—	V
		V_{OL}	CL = 2000 pF, CB = 4700 pF	—	1.1	1.4	V
General	Power supply current when output off	$I_{CC}1$	—	—	1.15	1.65	mA
		$I_{CC}2$	—	—	350	500	µA

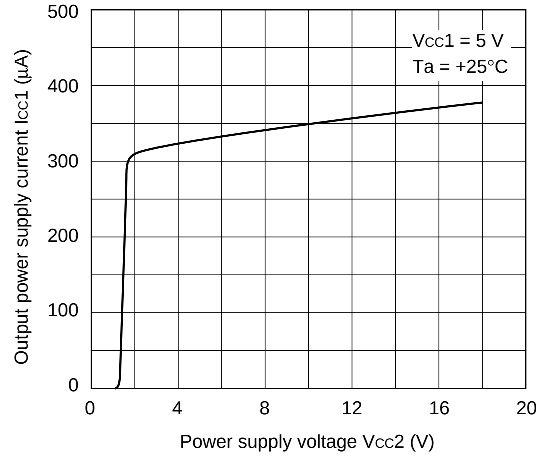
*: Standard design value

■ TYPICAL CHARACTERISTICS

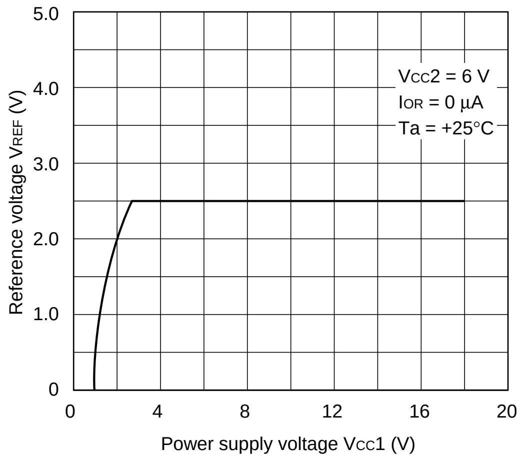
Power supply current vs.
power supply voltage characteristics



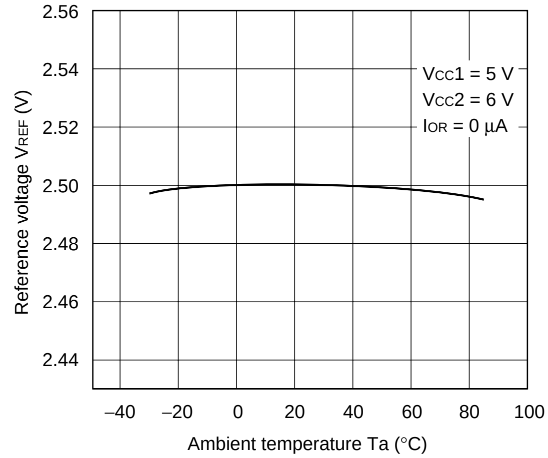
Output power supply current vs.
power supply voltage characteristics



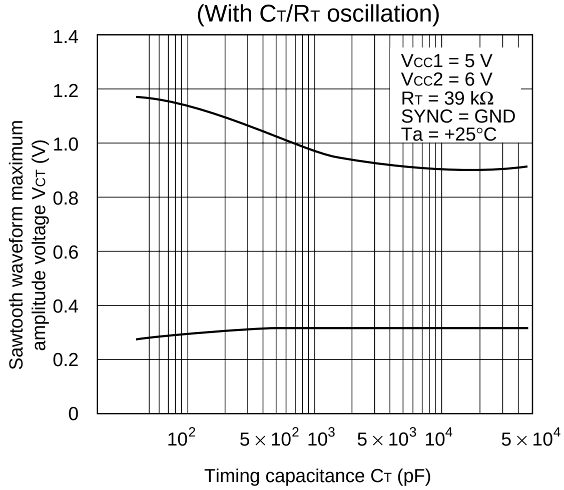
Reference voltage vs.
power supply voltage characteristics



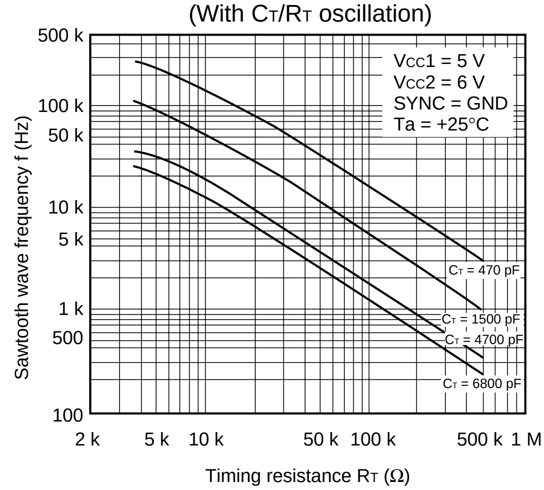
Reference voltage vs.
ambient temperature characteristics



Sawtooth waveform maximum amplitude voltage vs.
timing capacitance characteristics
(With CT/RT oscillation)



Sawtooth wave frequency vs.
timing resistance characteristics
(With CT/RT oscillation)



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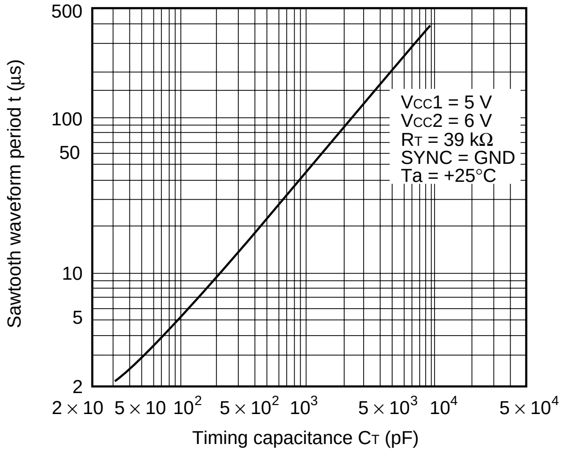
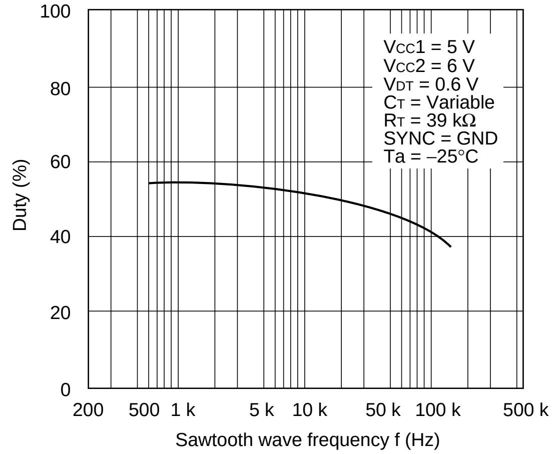
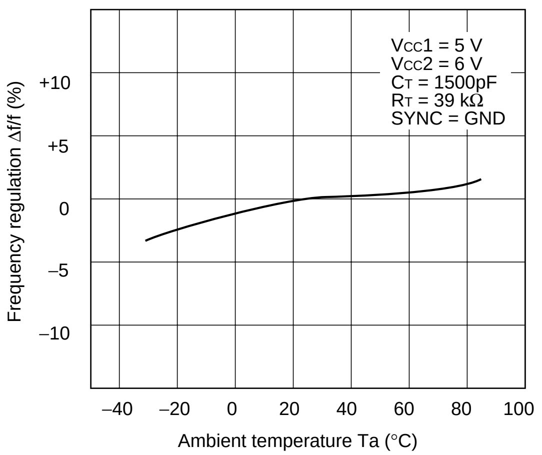
Sawtooth waveform period vs.
timing capacitance characteristics
(With CT/RT oscillation)



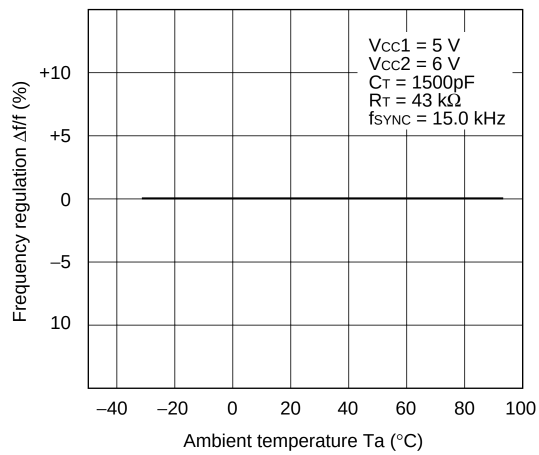
Duty vs. sawtooth wave
frequency characteristics
(With CT/RT oscillation)



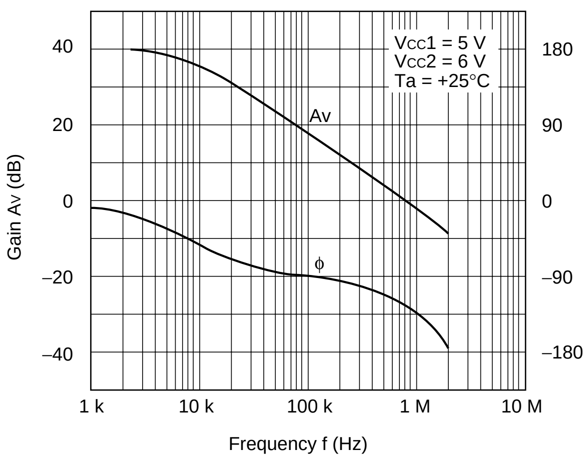
Sawtooth wave frequency vs.
ambient temperature characteristics
(With CT/RT oscillation)



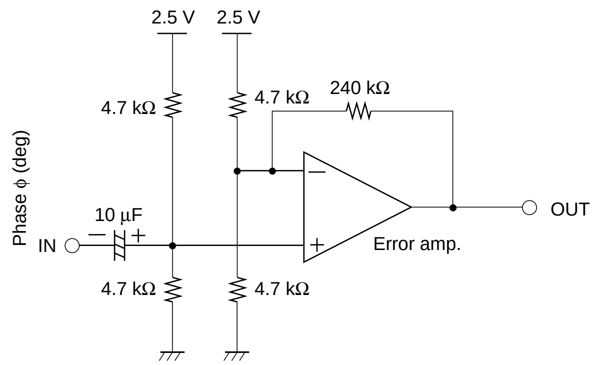
Sawtooth wave frequency vs.
ambient temperature characteristics
(In external synchronization)



Gain vs. frequency and phase vs.
frequency characteristics



Measurement circuit for gain-frequency
characteristics and phase-frequency characteristics



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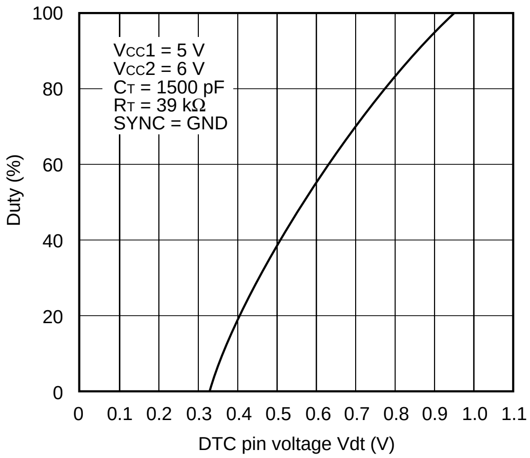
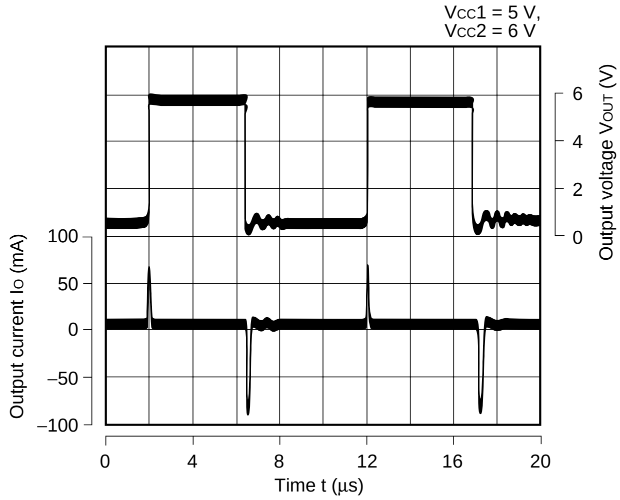
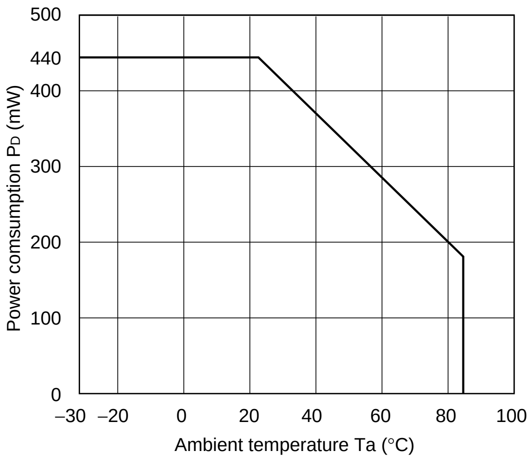
Duty vs. DTC pin voltage characteristics



Output pin (OUT) voltage and current waveforms



Power comsumption vs.
ambient temperature characteristics



■ SETTING THE OUTPUT VOLTAGE

Set the output voltage by connecting the input pins (+IN, –IN) and output pin (FB) of error amplifiers 1 and 2 as shown in Figures 1 and 2.

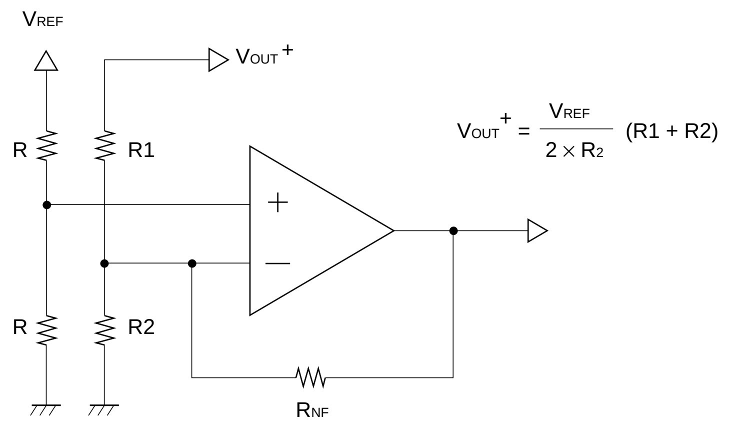


Figure 1 Setting the output voltage (positive output voltage (V_{OUT}))

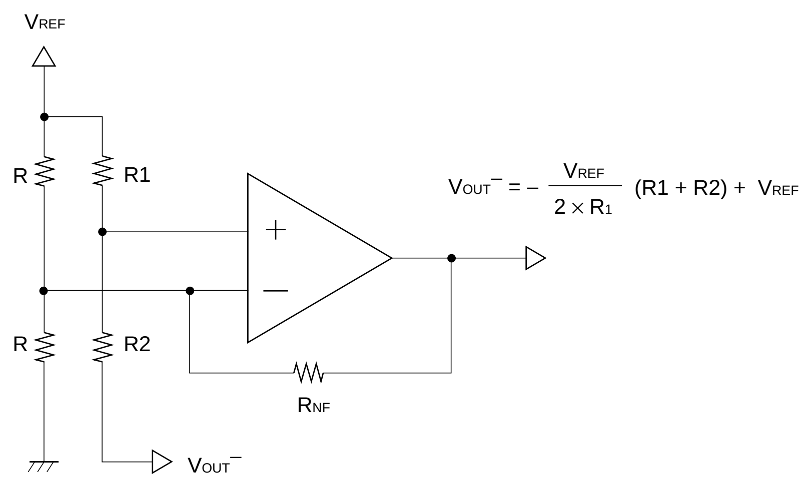


Figure 2 Setting the output voltage (negative output voltage (V_{OUT}))

■ SETTING THE OSCILLATION FREQUENCY

The oscillation frequency can be set by connecting the timing resistor (R_T) and the timing capacitor to the CT terminal (pin 3) .

Oscillation frequency : f_{OSC}

$$f_{OSC}\ (kHz) \fallingdotseq \frac{78000}{C_T(pF) \times R_T(k\Omega)}$$

■ CONNECTION FOR OUTPUT CONTROL WITH ONE ERROR AMPLIFIER

The MB3789 can make up a system using only one of the two error amplifiers. In this case, connect the +IN and –IN pins of the unused error amplifier to the V_{REF} and GND pins, respectively, and leave the FB pin open.

When V_{CC} – 1.8 V < V_{REF}, divide the V_{REF} voltage using a resistor and apply the voltage to the +IN pin.

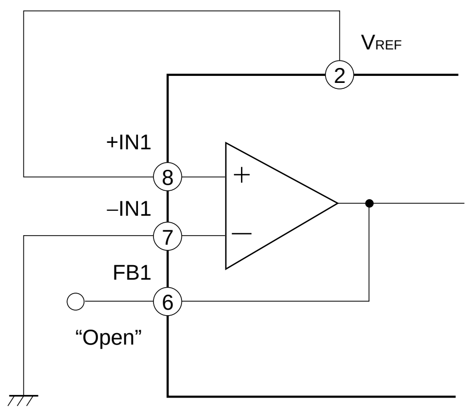


Figure 1 Connection without using error amplifier 1

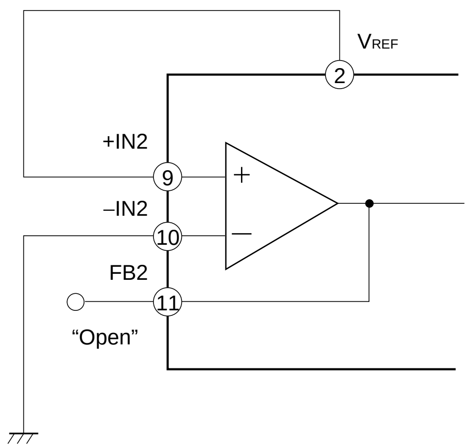


Figure 2 Connection without using error amplifier 2

■ CONNECTING THE SAWTOOTH WAVEFORM OSCILLATOR

1. Connection for internal oscillation

For internal oscillation, connect the frequency setting capacitor (C_T) and resistor (R_T) to the C_T pin (pin 3) and leave the SYNC pin (pin 4) open or connect it to GND.

The oscillation frequency can be set with the C_T and R_T constants.

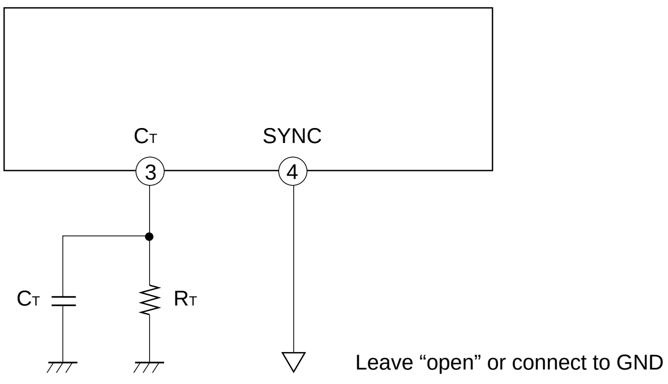


Figure 5 Connection for internal oscillation

2. Connection for external synchronous oscillation

For external synchronous oscillation, connect the frequency setting capacitor (C_T) and resistor (R_T) to the C_T pin (pin 3) and connect the external sync signal to the SYNC pin (pin 4).

In this case, select the C_T and R_T conditions so that the oscillation frequency is 5% to 10% lower than the frequency of the external sync signal excluding the setting error of the oscillation frequency.

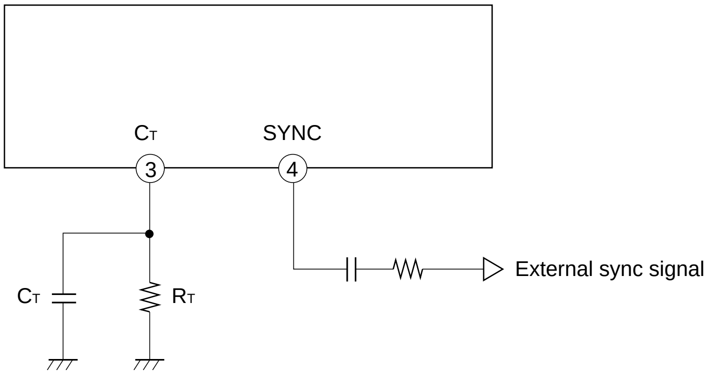


Figure 6 Connection for external synchronous oscillation

■ SETTING THE DEAD TIME

When the device is set for step-up inverting output based on the flyback method, the output transistor is fixed to a full-ON state (ON duty = 100%) when the power supply is turned on. To prevent this problem, you may determine the voltage at the DTC pin (pin 12) from the V_{REF} voltage so you can set the output transistor's dead time (maximum ON-duty period) as shown in Figure 7 below.

1. Setting the dead time

When setting the dead time, use resistors as shown in Figure 7 to connect the V_{REF} and DTC pins to GND. When the voltage at the DTC pin (pin 12) is lower than the sawtooth wave output voltage from the oscillator, the output transistor is turned off.

To set the dead time, see "Duty vs. DTC pin voltage" (in "■ STANDARD CHARACTERISTIC CURVES").

$$V_{dt} = \frac{R2}{R1 + R2} \times V_{REF}$$

2. Connection without setting the dead time

If you do not set the dead time, connect the V_{REF} and DTC pins as shown in Figure 8.

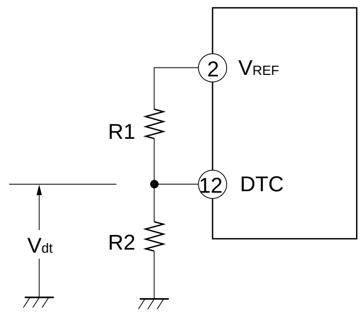


Figure 7 Connection for setting the dead time

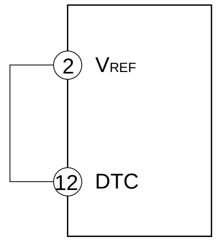


Figure 8 Connection without setting the dead time

■ SETTING THE SOFT START/SHORT-CIRCUIT DETECTION TIME

Connecting capacitor C_{PE} to the SCP pin (pin 5) as shown in Figure 9 enables a soft start and short-circuit protection.

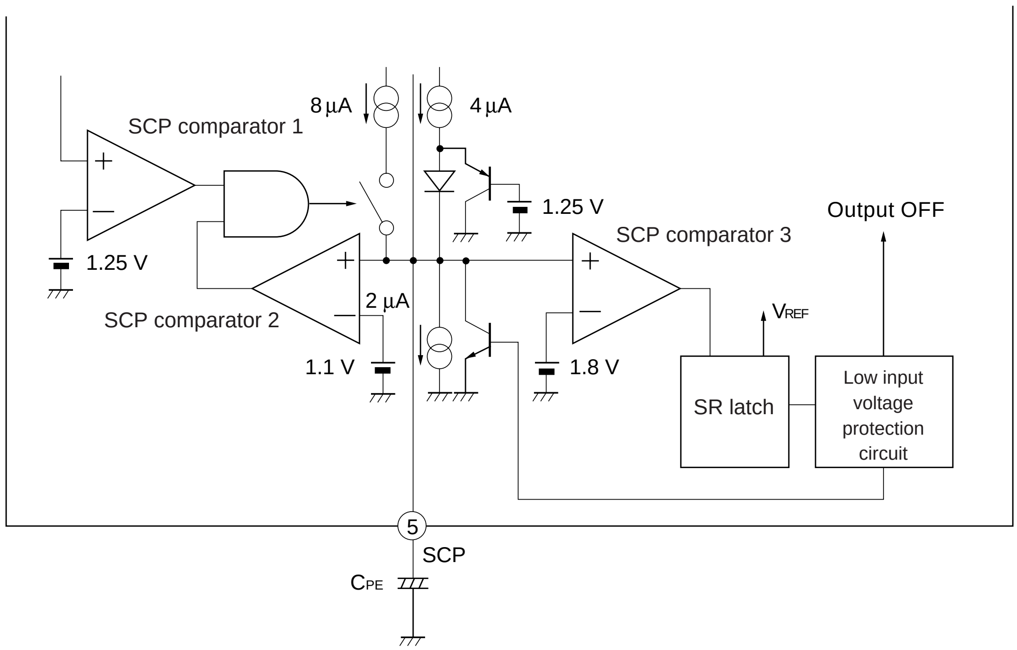


Figure 9 Soft start/short-circuit detection circuit

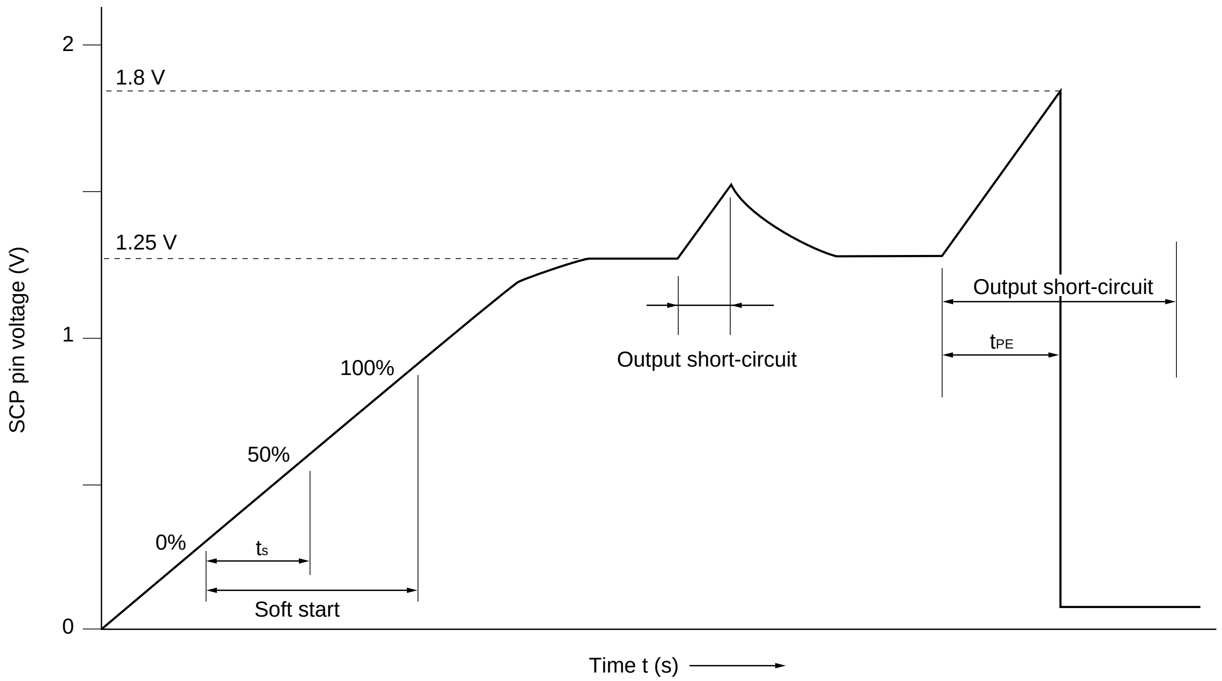


Figure 10 SCP pin operating waveform

1. Soft Start

To prevent surge currents when the IC is turned on, you can set a soft start by connecting capacitor C_{PE} to the SCP pin (pin 5).

•Softstart time(ts): Time required up to duty cycle ≃ 50% with output on

t_S (s) ≃ 0.15 × C_{PE} (µF)

2. Protection from short circuit

SCP comparator 1 always compares the output voltage levels at error amplifiers 1 and 2 with the 1.25 V reference voltage.

When the load conditions for the switching regulator are stable, the outputs from error amplifiers 1 and 2 do not vary and thus short-circuit protection control remains balanced. In this case, the SCP pin (pin 5) is held at the soft start end voltage (about 1.25 V).

If the load conditions change rapidly and the output voltage level of both of the two error amplifiers reaches 1.25 V, for example, because of a short-circuit of a load, capacitor C_{PE} is charged further. When capacitor C_{PE} is charged up to about 1.8 V, the SR latch is set and the output drive transistor is turned off. At this time, the dead time is set to 100%, capacitor C_{PE} is discharged, and the SCP pin becomes ≃ 50 mV.

•Short-circuit detection time (t_{PE})

t_{PE} (s) ≃ 0.09 × C_{PE} (µF)

3. Connection without using short-circuit protection

Add a clamp circuit as shown in Figure 11 so that the clamp voltage (V_{CRP}) falls within the following range when a short-circuit is detected: 1.0 V < V_{CRP} < 1.7 V

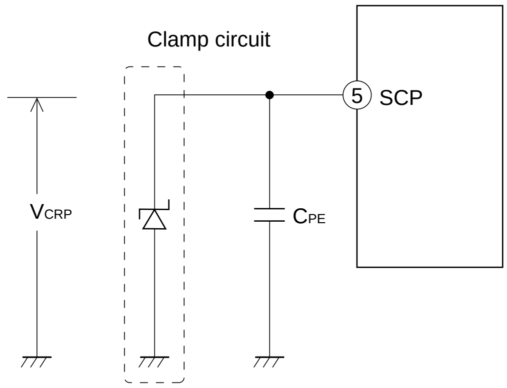


Figure 11 Connection without using short-circuit protection

■ SETTING THE BOOTSTRAP CAPACITOR

When a bootstrap capacitor is connected, it raises the output-ON voltage (at the OUT pin (pin 15) when the external MOS FET is turned "ON") to the ≃ $V_{CC}2$ level. It can therefore drive the MOS FET at a higher threshold voltage (V_{th}).

1. Connecting the bootstrap capacitor

Connect the bootstrap capacitor between the CB pin (pin 13) and OUT pin (pin 15).

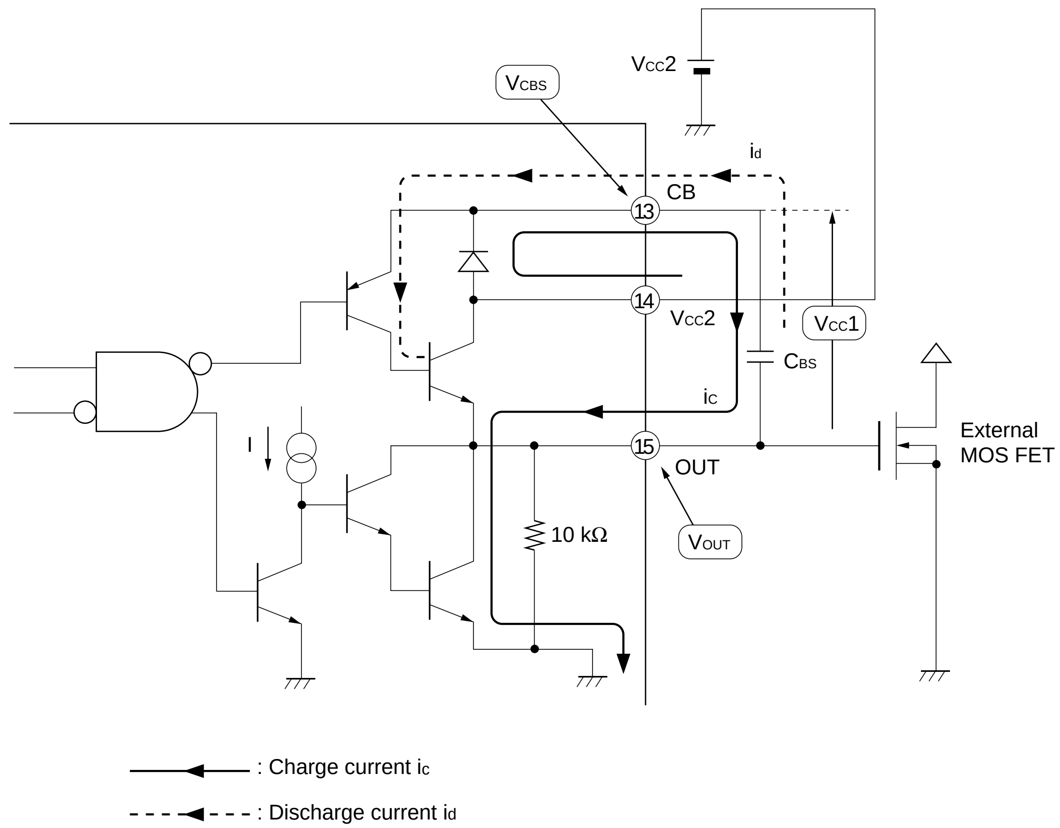


Figure 12 Circuit with a bootstrap capacitor connected and current flow

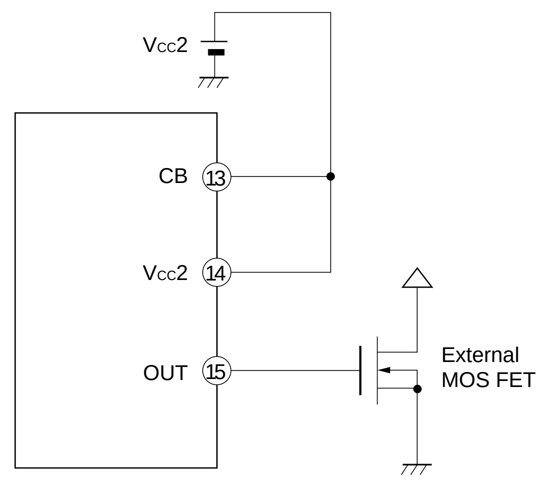
•Calculation of bootstrap capacitance

$$C_{BS} \geqq \frac{500 \times 10^6}{V_{CC}2 - 2.6} \times t_{ON}\ (\text{Max})\ [\text{pF}]$$

t_{ON} (Max): Maximum ON duty time

2. Connection with no bootstrap capacitor

Connect the CB pin (pin 13) and $V_{CC}2$ pin (pin 14) as shown in Figure 13.



Note: Under a condition of "$V_{CC}2 - V_{th} < 1.1$ V", bootstrap capacitor C_{BS} should be connected because the external MOS FET cannot be driven sufficiently.

V_{th}: External MOS FET threshold voltage

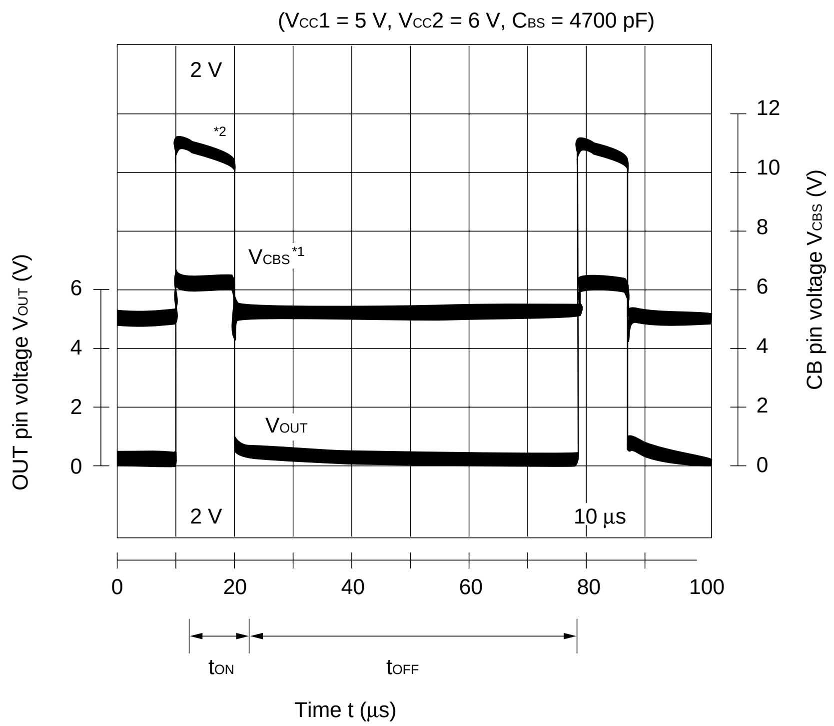
Figure 13 Connection with no bootstrap capacitor connected

3. Operation of the Bootstrap Capacitor

When voltage V_{OUT} at the OUT pin (pin 15) is "L" level, the voltages (V_{C1}) at both ends of the bootstrap capacitor C_{BS} is charged up to the $V_{CC}2$ voltage level by charge current (i_C).

When V_{OUT} changes from "L" level to "H" level, the CB pin (pin 13) voltage V_{CBS} rises to $\simeq 2 \times V_{CC}2$ and V_{OUT} reaches almost the $V_{CC}2$ level.

The charge accumulated at C_{BS} at this time is released by discharge current i_d (output unit supply current). See Figure 12 for circuit operation.



*1: Use the device with a setting of $V_{CBS} \leqq 18$ V.
*2: The slant of V_{CBS} is determined by the value of discharge current i_d (output unit supply current).

Figure 14 Bootstrap operating waveform

■ EQUIVALENT SERIES RESISTANCE OF SMOOTHING CAPACITOR AND SYSTEM STABILITY

The equivalent series resistance (ESR) value of a smoothing capacitor for the DC/DC converter largely affects the loop phase characteristic.

Depending on the ESR value, the phase characteristic causes the ideal capacitor in a high-frequency domain advance the loop phase (as shown in Figures 16 and 17) and thus the system is improved in stability. In contrast, using a smoothing capacitor with low ESR lowers system stability. Use meticulous care when a semiconductor electrolytic capacitor with low ESR (such as an OS capacitor) or a tantalum capacitor is used. (The next page gives an example of reduction in phase margin when an OS capacitor is used.)

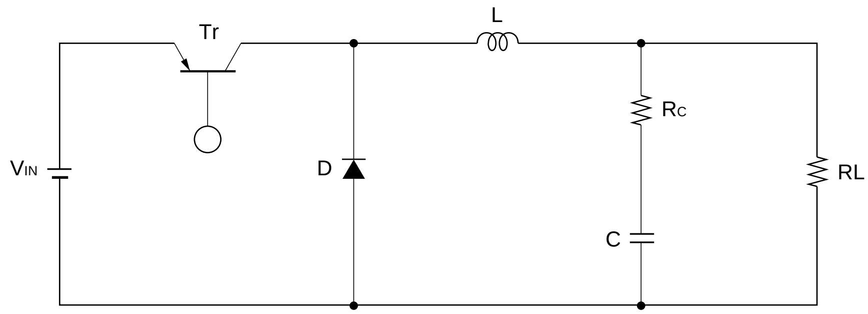


Figure 15 Basic circuit of step-down DC/DC converter

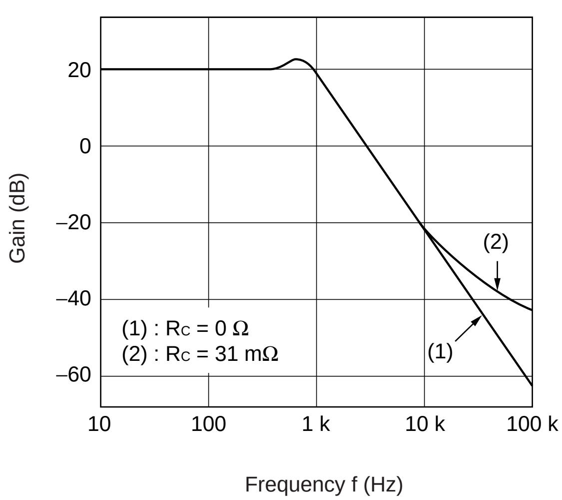


Figure 16 Gain vs. frequency

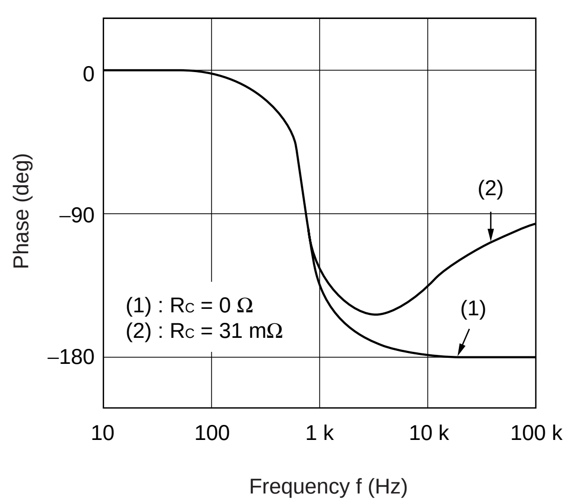


Figure 17 Phase vs. frequency

(Reference data)

Changing the smoothing capacitor from an aluminum electrolytic capacitor ($R_C \simeq 1.0\ \Omega$) to a low-ESR semiconductor electrolytic capacitor (OS capacitor: $R_C \simeq 0.2\ \Omega$) halves the phase margin. (See Figures 19 and 20.)

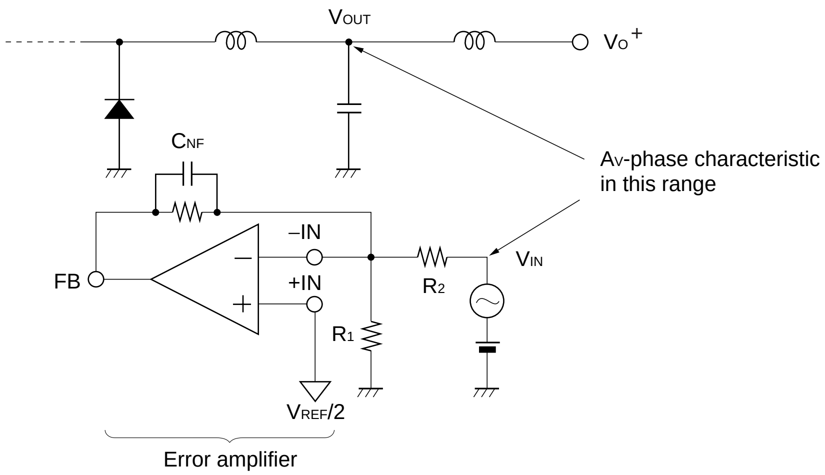


Figure 18 DC/DC converter Av vs. phase measurement diagram

Al electrolytic capacitor gain vs. frequency, phase vs. Frequency (DC/DC converter +5 V output)

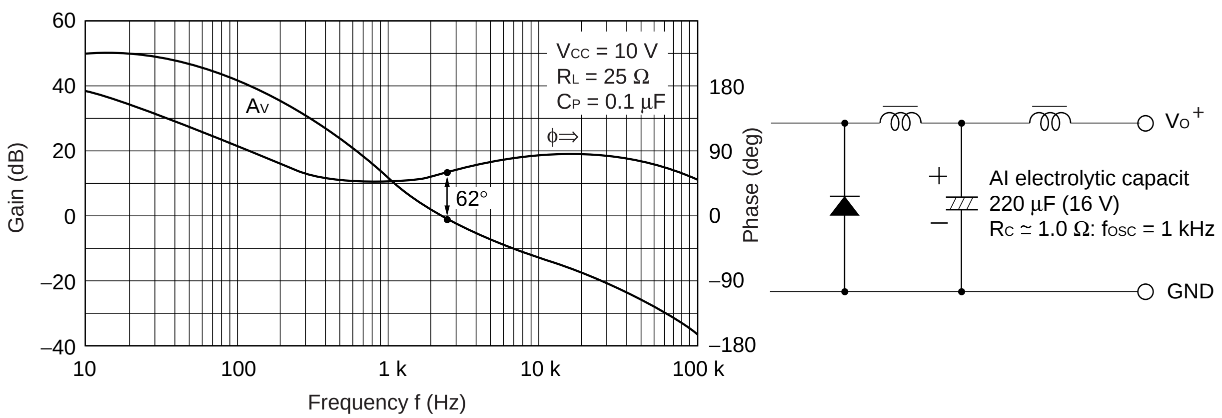


Figure 19 Gain vs. frequency

OS capacitor gain vs. frequency, phase vs. frequency (DC/DC converter +5 V output)

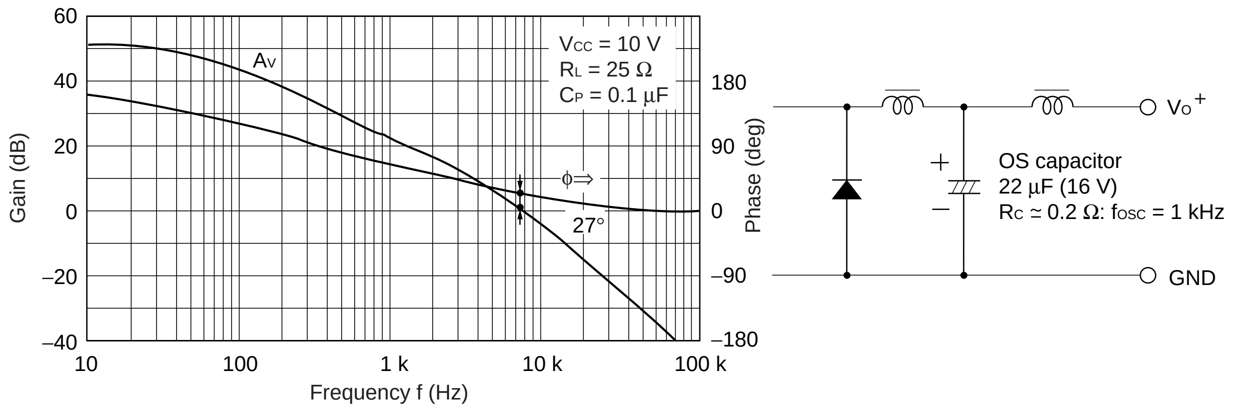
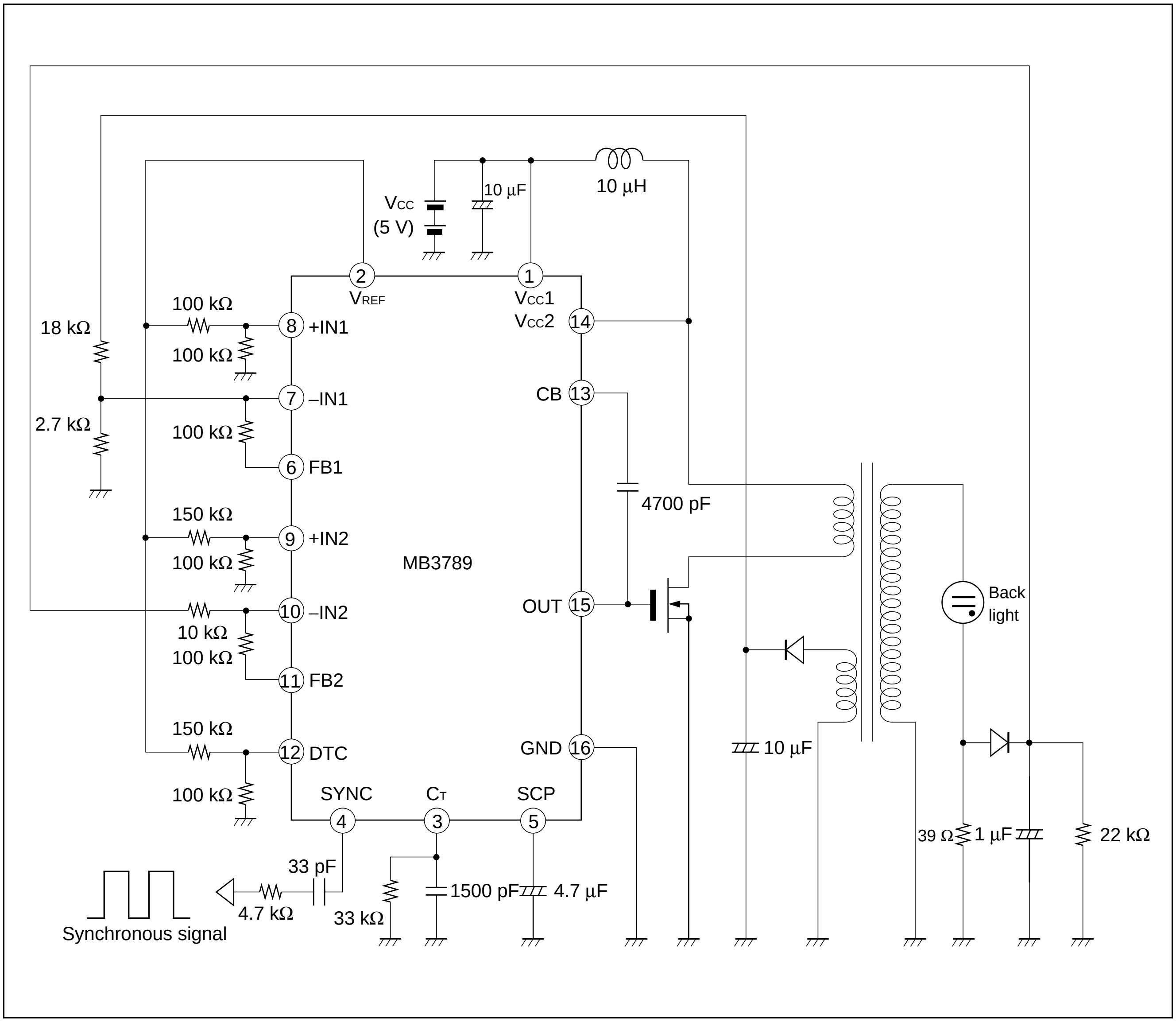


Figure 20 Phase vs. frequency characteristic curves

■ APPLICATION EXAMPLE



■ NOTES ON USE

- Take account of common impedance when designing the earth line on a printed wiring board.

- Take measures against static electricity.
  - For semiconductors, use antistatic or conductive containers.
  - When storing or carrying a printed circuit board after chip mounting, put it in a conductive bag or container.
  - The work table, tools and measuring instruments must be grounded.
  - The worker must put on a grounding device containing 250 kΩ to 1 MΩ resistors in series.

- Do not apply a negative voltage
  - Applying a negative voltage of –0.3 V or less to an LSI may generate a parasitic transistor, resulting in malfunction.

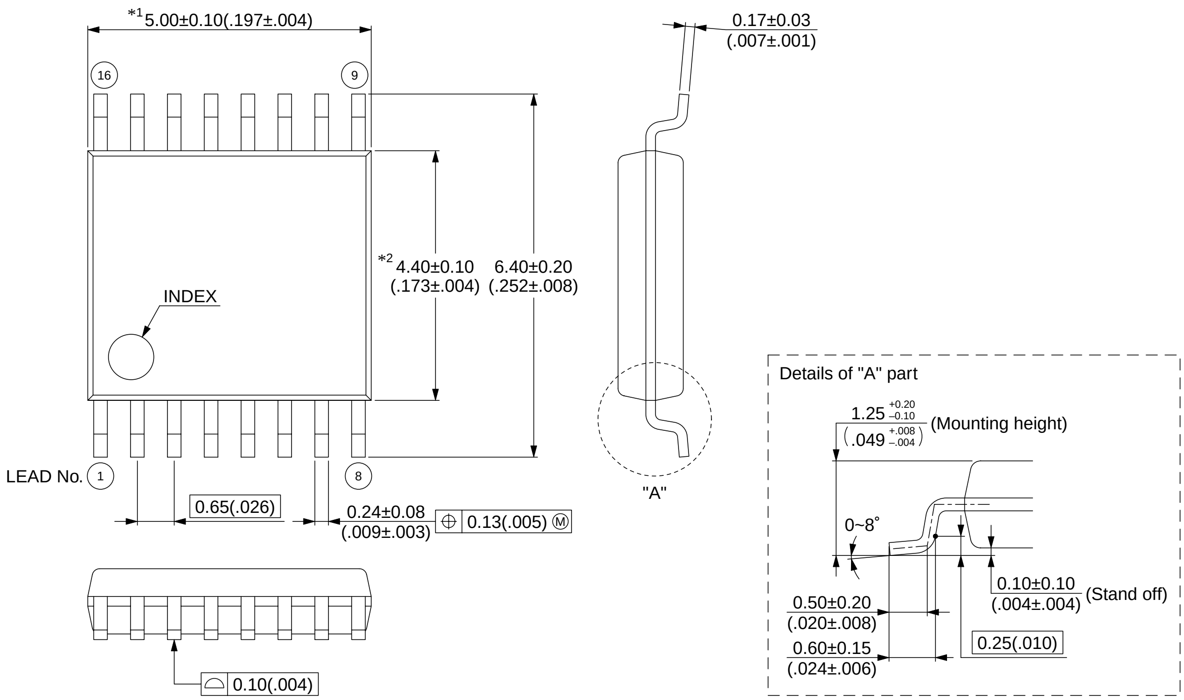
■ ORDERING INFORMATION

Part number	Package	Remarks
MB3789PFV	16-pin Plastic SSOP (FPT-16P-M05)	

■ PACKAGE DIMENSION

16-pin Plastic SSOP
(FPT-16P-M05)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max) .
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note : The values in parentheses are reference values.

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