SIEMENS

ICs for Communications

ISDN Echocancellation Circuit
IEC-Q

PEB 2091 Version 5.3
PEF 2091 Version 5.3

Data Sheet 01.99

DS 2

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Preface

The ISDN Echocancellation Circuit for the 2B1Q line code (IEC-Q) is a U-interface transceiver for level 1 basic access subscriber lines covering a wide range of applications related to this function.

This data sheet describes the properties of the IEC-Q needed for understanding its external connections, architecture and functions, and for designing circuits using this device.

Organization of this Document

This document follows a top-down approach in describing the IEC-Q and its features. It is application oriented, designed to maximize customers' effectivity in designing and debugging their boards. Numerous examples of programming code and application hints are included. An index is included. It consists of 11 chapters and an appendix.

- Chapter 1, Overview
  Describes the system related view of the device, i.e. features, system integration and typical applications.

- Chapter 2, Pin Descriptions
  Gives a detailed description of the device pins, their functions and their physical location for the different packages available.

- Chapter 3, Functional Description
  Provides a high level block diagram of the IEC-Q, describes setting its operational modes and gives an overview of the device architecture. All user's interfaces are described in detail. Interaction between these interfaces, however, is not in the scope of this chapter.

- Chapter 4, Operational Description
  Describes access means to the IEC-Q features and the resulting device behavior in all relevant operational modes. Interaction between the different interfaces is described.

- Chapter 5, Register Description
  Provides a detailed description of the registers used in the microprocessor mode.

- Chapter 6, Programming
  Gives an overview of important programming codes and provides numerous practical programming examples.

- Chapter 7, Application Hints
  Describes the external circuitry needed and gives useful hints for some applications.

- Chapter 8, Electrical Characteristics
  Specifies the statical and dynamical characteristics of the device's inputs and outputs, its maximum rating, power supply, power consumption and other important electrical characteristics.

- Chapter 9, Package Outlines
  Outlines the geometry of the three packages available.

- Chapter 10, Glossary.

- Chapter 11, Index.

- Appendix
  A listing of basic standards and some remarks are included.

1 Overview

Version 5.3 of the PEB/F 2091 (IEC-Q), is an optimized version of the IEC-Q, which features all functions needed for building basic rate digital subscriber line systems. It complies to all international and all important national standards (e.g. ITU, ANSI, ETSI, CNET, BT). The IEC-Q holds the Bellcore approval for "Layer 1 ISDN Basic Access Digital Subscriber Line Transceivers", including all objectives, and it is the de facto industrial standard for these applications.

The IEC-Q is one building stone of the Siemens U transceiver product family for the 2B1Q line code, which is divided into three groups of products

- IEC AFE/DFE-Q (PEB 24902 / PEB 24911)
- NTC-Q and INTC-Q (PEB 8091/PEB8191)
- IEC-Q

The IEC AFE/DFE kit is optimized to interface four metallic lines in the LT allowing cost effective design for line cards in the switch and in wireless local loop applications (LT).

The NTC-Q is a one chip solution for NT1 systems offering all needed level 1 functions for this application. The functions of the NTC-Q are a subset of these of the INTC-Q, which offers additional features for comfortable and cost effective implementation of intelligent NTs.

The IEC-Q provides numerous features supporting comfortable and cost effective implementation of

- Digital added main line (DAML) PCM-2 and PCM-4 applications
- Repeater applications
- Wireless local loop applications (base station)
- TE applications
- NT-PBX and Access Network applications

From the technical point of view, it can also be used in standard NT and LT applications.

The IEC-Q allows access to the U-interface via IOM®-2 interface, microprocessor interface or a combination of both. It also provides means to support monitoring transmission quality, monitoring power supply, activation and deactivation procedures for special modes, performing maintenance tests and other features.

Version 5.3 is available in three different packages and in two operational temperature ranges. It offers

- New features to support applications gaining increasing importance in the marketplace, e.g. wireless local loop, repeaters, dual mode S and U terminals and PC cards,
- Improved electrical behavior and functions (power consumption, ESD immunity, dynamic characteristics of the microprocessor interface) as well as
- Full compatibility to previous IEC-Q versions

ISDN Echocancellation Circuit
IEC-Q

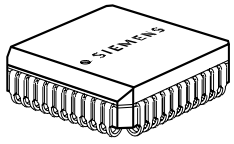
PEB 2091
PEF 2091

Version 5.3

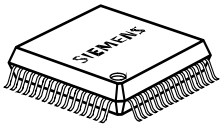
CMOS

1.1 Features

- ISDN U transceiver with IOM®-2 and microprocessor interface control
- Pin and functionally compatible to all previous PEB 2091 versions
- Perfectly suited to all LT, NT, TE, DAML, Repeater, NT-PBX and Wireless Local Loop applications.
- U-interface (2B1Q) conforms to all relevant international standardization norms (e.g. ITU, ANSI, ETSI) and all important national norms (e.g. CNET, BT), including all optional transmission requirements with sufficient margin.
- Application optimized DSP with adaptive echo cancellation and equalization, automatic polarity adaption, clock recovery, automatic gain control and build-in wake-up function.
- IOM®-2 interface for connection of e.g. EPIC®, ELIC®, IDEC®, SBC-X, ICC, SICOFI®-2/4, SICOFI®-2/4TE, ISAC®-S, ARCOFI®, ITAC®, HSCX-TE, ISAR, IPAC, 3PAC
- Automatic maintenance control features
- Multipurpose controller interface in stand-alone mode
- Single 5 Volt power supply
- Low power CMOS technology with power down mode
- Available in three packages: P-LCC-44, M-QFP-64 and T-QFP-64
- Available in the extended temperature range



P-LCC-44



M-QFP-64

T-QFP-64

In µP Mode

- Parallel or serial microprocessor interface
- Wake up function in NT mode without IOM®-2
- Undervoltage detection circuit
- Watchdog

- µP access to all data and control channels of the IOM®-2 interface
- Adjustable microcontroller clock source between 0.96MHz and 7.68MHz
- Selection between Bit clock (BCL) and Data clock (DCL)
- Supports synchronization of base stations in Wireless Local Loop applications
- Supports D-channel arbitration with ELIC® linecard (e.g. PBX)

1.2 Ordering Codes

Type	Ordering Code	Package
PEB 2091 N V5.3	Q67236-H1078	P-LCC-44
PEF 2091 N V5.3	Q67236-H1069	P-LCC-44
PEF 2091 H V5.3	Q67237-H1079	M-QFP-64
PEF 2091 F V5.3	Q67237-H1077	T-QFP-64

1.3 Logic Symbol for µP Mode

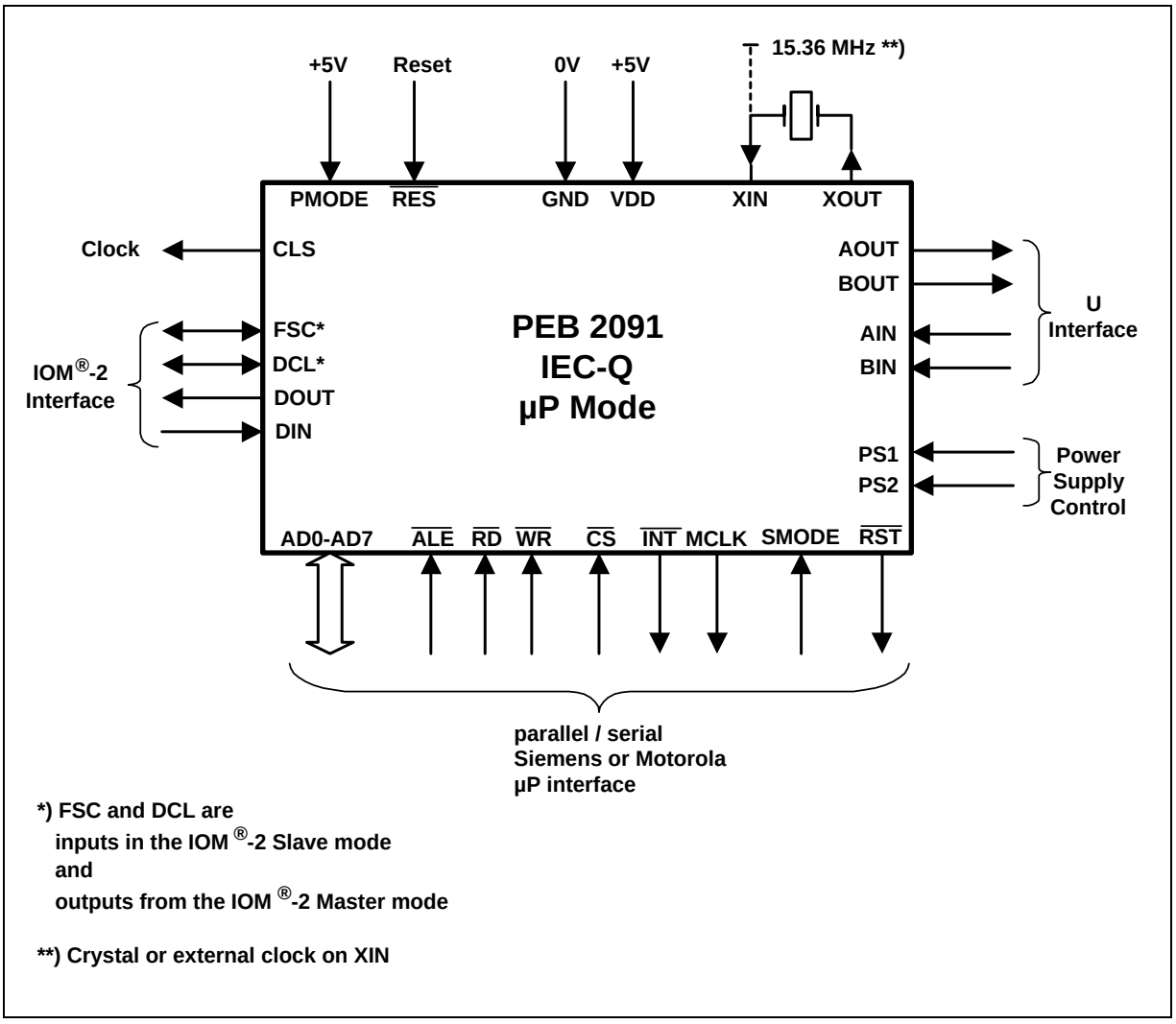


Figure 1 Logic Symbol for µP Mode

1.4 Logic Symbol for Stand-Alone Mode

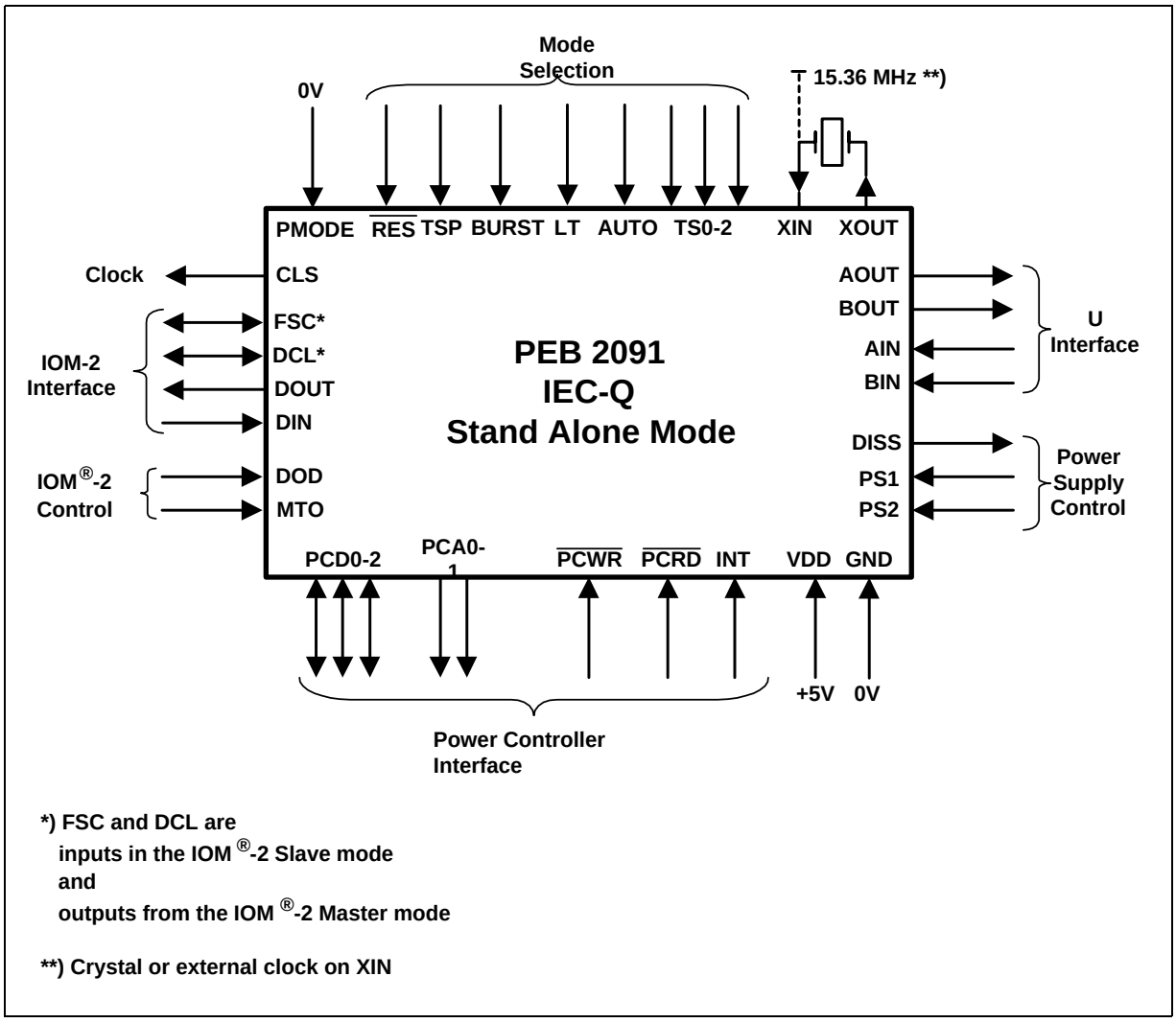


Figure 2 Logic Symbol for Stand-Alone Mode

1.5 System Integration

The PEB/F 2091 can be combined with a variety of other devices to fit in numerous applications. Some of the typical[1)] layer-1 applications are sketched below.

1.5.1 PCM 2 Systems

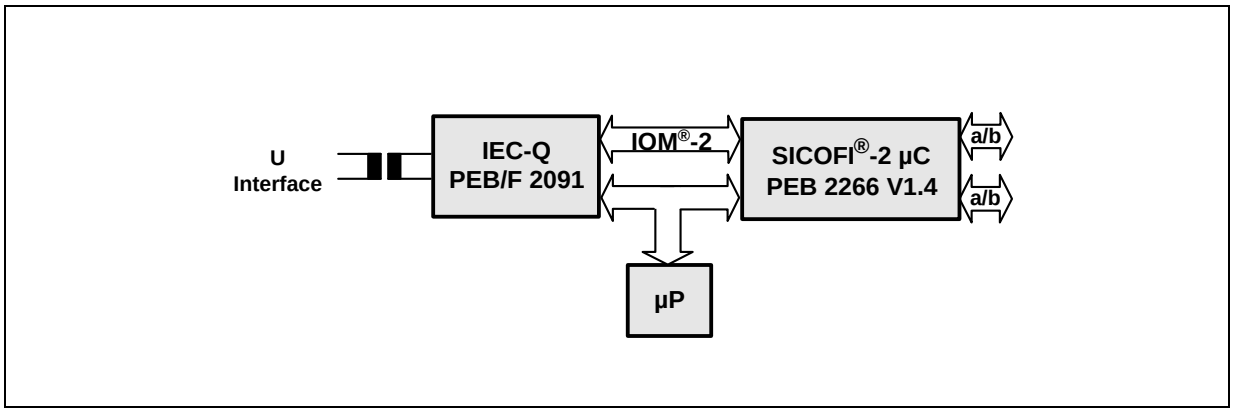


Figure 3 COT Application

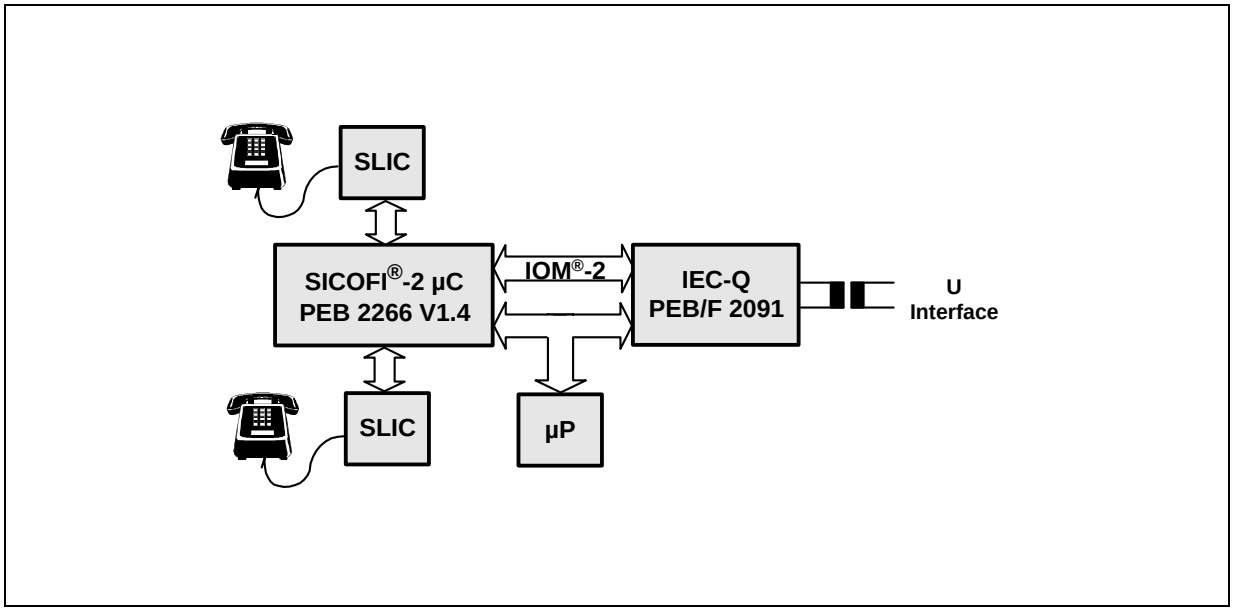


Figure 4 RT Application

1) Typical applications are not necessarily covered by system tests or reference designs performed by Siemens, and they may be subject to future changes

1.5.2 PCM 4 with FAX/Modem Features

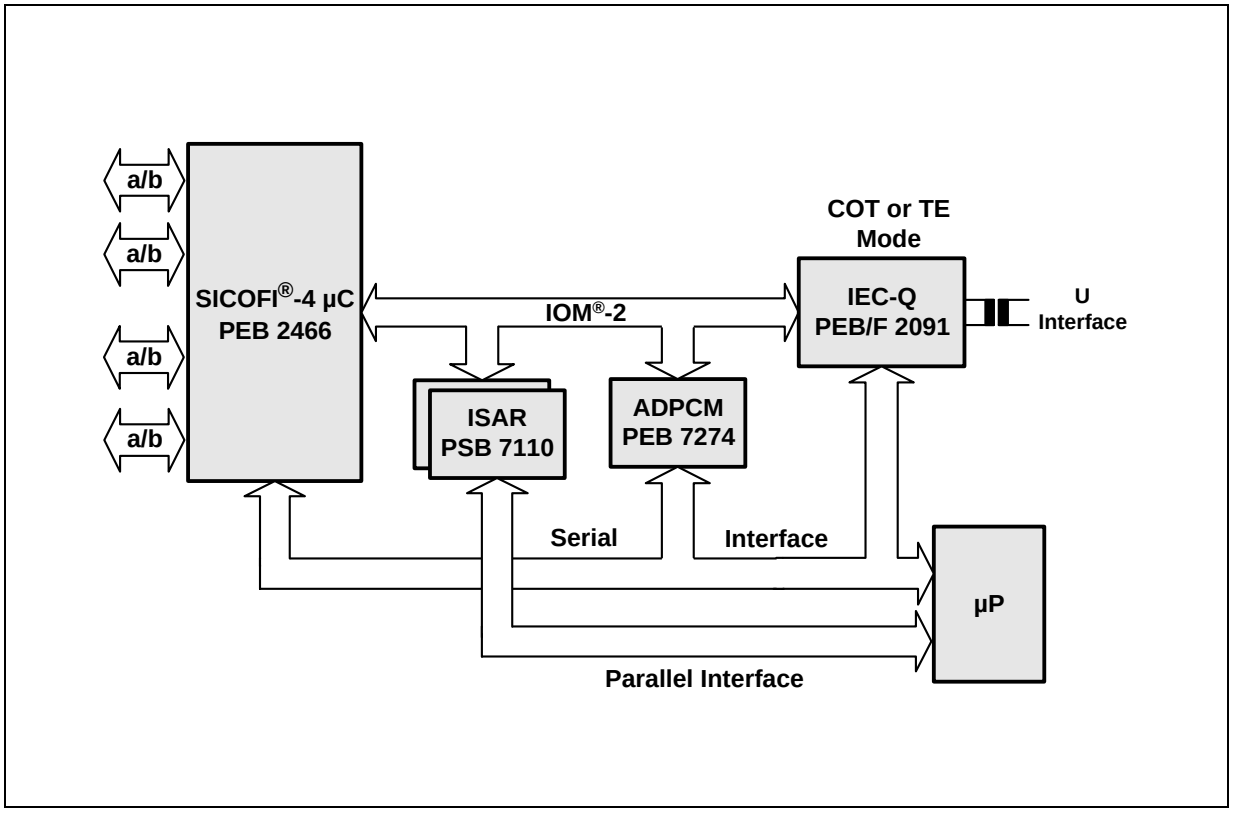


Figure 5 PCM 4 Application

1.5.3 Repeater

The IEC-Q offers several special features to allow simple and cost effective design of repeaters. Beside the microprocessor interface, free programming of maintenance bits and special state machines for activation and deactivation control, the following three features are of interest

- A wake-up tone from downstream is indicated directly on DOUT. No special circuit for wake tone detection is needed. See "Upstream Wake-Up Indication in the LT Repeater Mode", page 143.
- A master clock is delivered on pin CLS in the NT Repeater mode. This allows reducing power consumption to a minimum in power down. Furthermore, PLL architecture can be simplified. See "Clocks", page 45.
- The undervoltage detection function can be used to detect power supply level drops on the board and reduce external reset circuitry. Refer to "Undervoltage Detection", page 92.

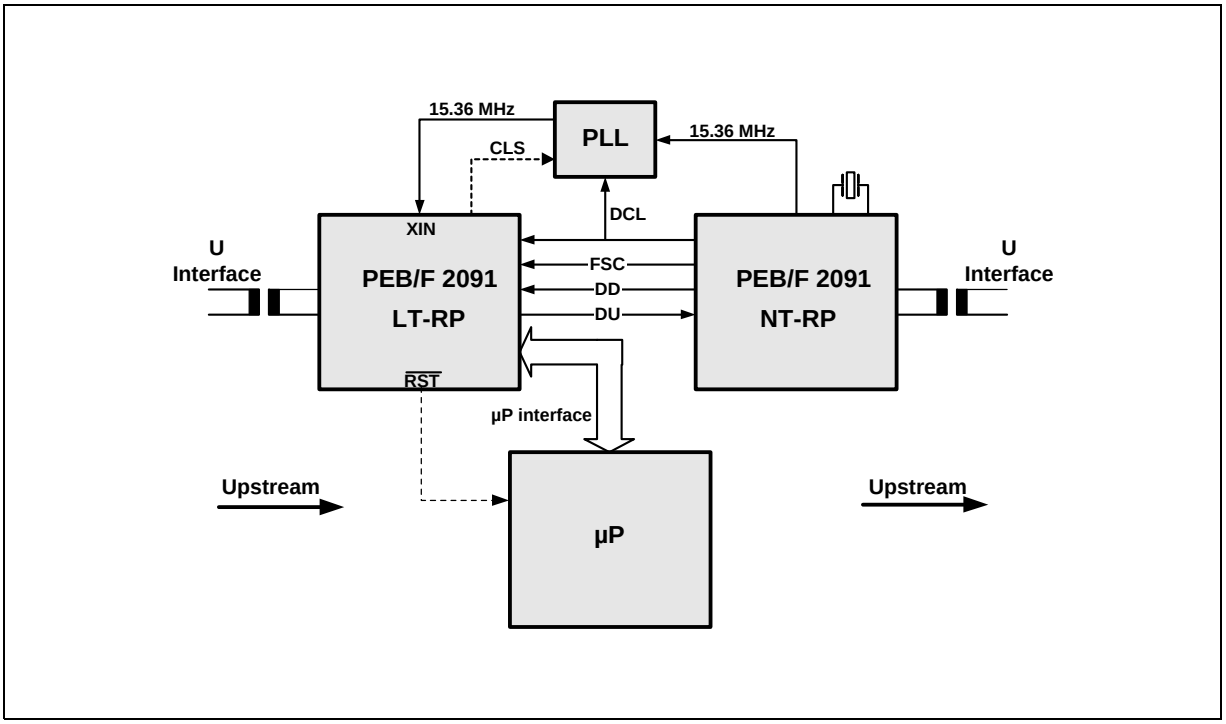


Figure 6 Architecture of Repeater Application

1.5.4 Wireless Local Loop

In Figure 7 an example for base station configuration is sketched. The PEB/F 2091 Version 5.3 is designed to suit to PEB 24911/PEB 24902 (DFE-Q/AFE) in the linecard, and to the PMB 2727 (Multichannel Burst Mode Controller) in the base station. Several special features concerning S/G bit control (see "S/G Bit and BAC Bit Operations", page 198) allow flexible and cost effective construction of base station boards without the need for external circuitry for S/G bit evaluation. Like the S/G bit, the S/G pin can be used for transmitting a common synchronization pulse to the burst mode controller. Moreover the undervoltage detection feature (see "Undervoltage Detection", page 92) can be used to monitor power supply drops on the board.

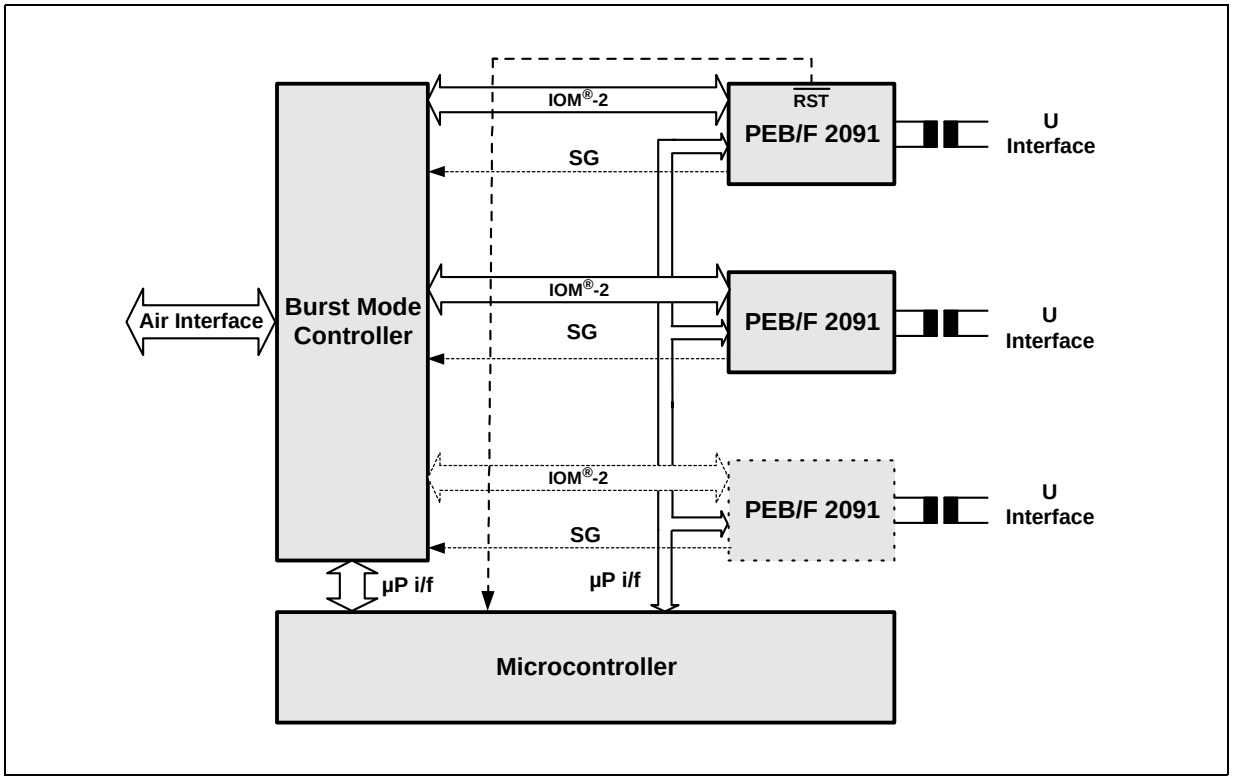


Figure 7 Architecture of the Wireless Local Loop Base Station

1.5.5 TE Applications

One example for terminal application is the ISDN feature phone.

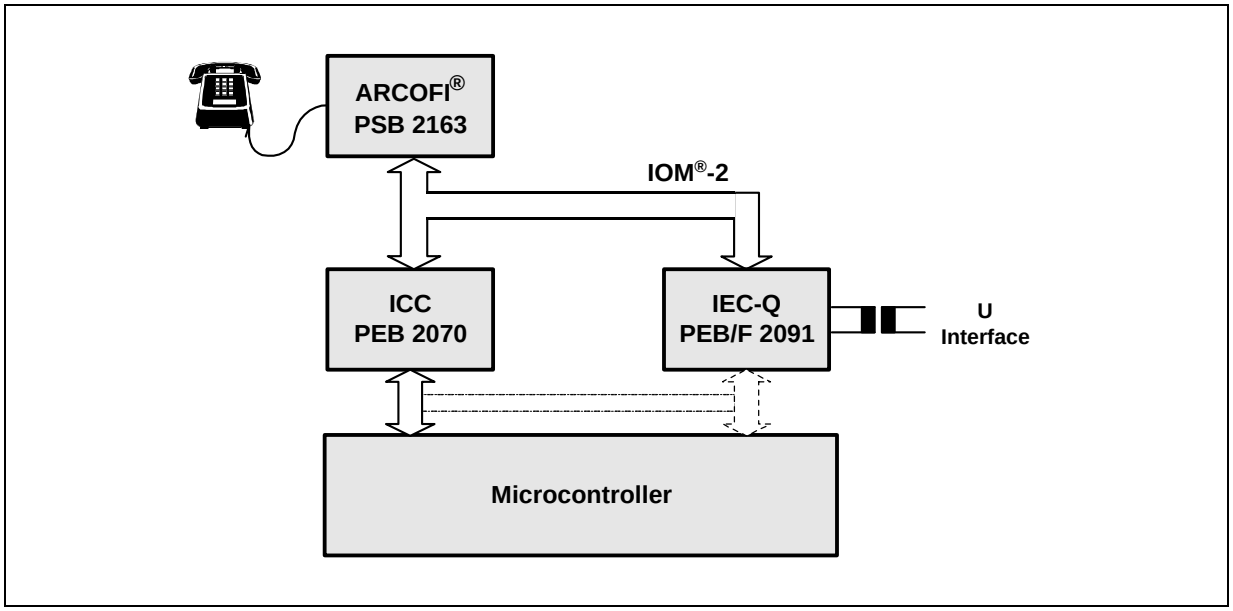


Figure 8 TE Application

1.5.6 Dual Mode U and S Terminals and PC Cards

In this application the IOM®-2 interface can be programmed to be inactive in the IOM®-2 master mode. This allows introduction of dual mode terminals and PC adapter cards using e.g. IPAC. See 3.2.4, page 53 for details.

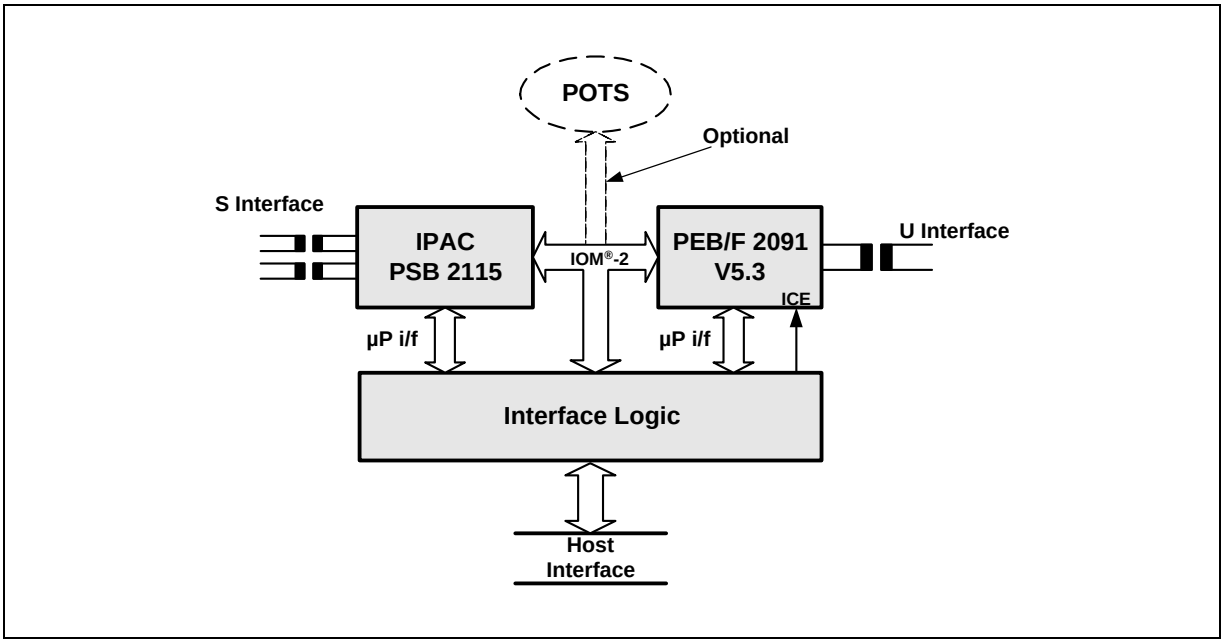


Figure 9 Dual Mode PC Adapter Card

1.5.7 NT-PBX

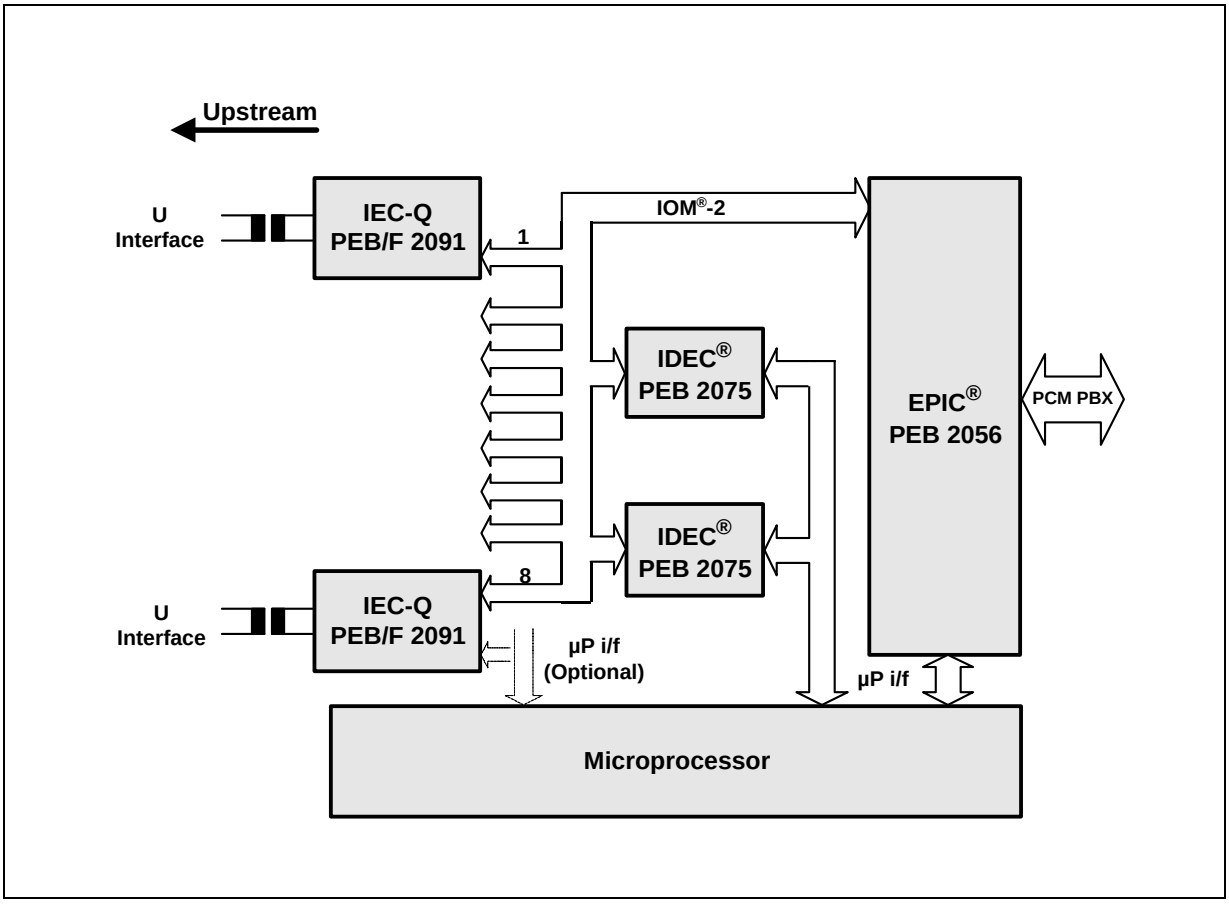


Figure 10 NT-PBX Application

1.5.8 LT Application and Access Network

Note 1: For LT applications in general it is recommended to use the device kit PEB 24911 / PEB/F 24902 (Quad IEC DFE-Q/AFE), which offers the same function for four metallic lines. In some special configurations, however, (e.g. line cards with 6 lines) it might be more cost effective to use the IEC-Q. In the configuration below system integration on existing boards is sketched.

An LT configuration with up to 8 IEC-Qs can be built with an EPIC® and two IDEC®s. The EPIC® controls the C/I-channel, the B-channel slot assignment and the Monitor channel handling. The IDEC® is a HDLC-controller for four independent D-channels.

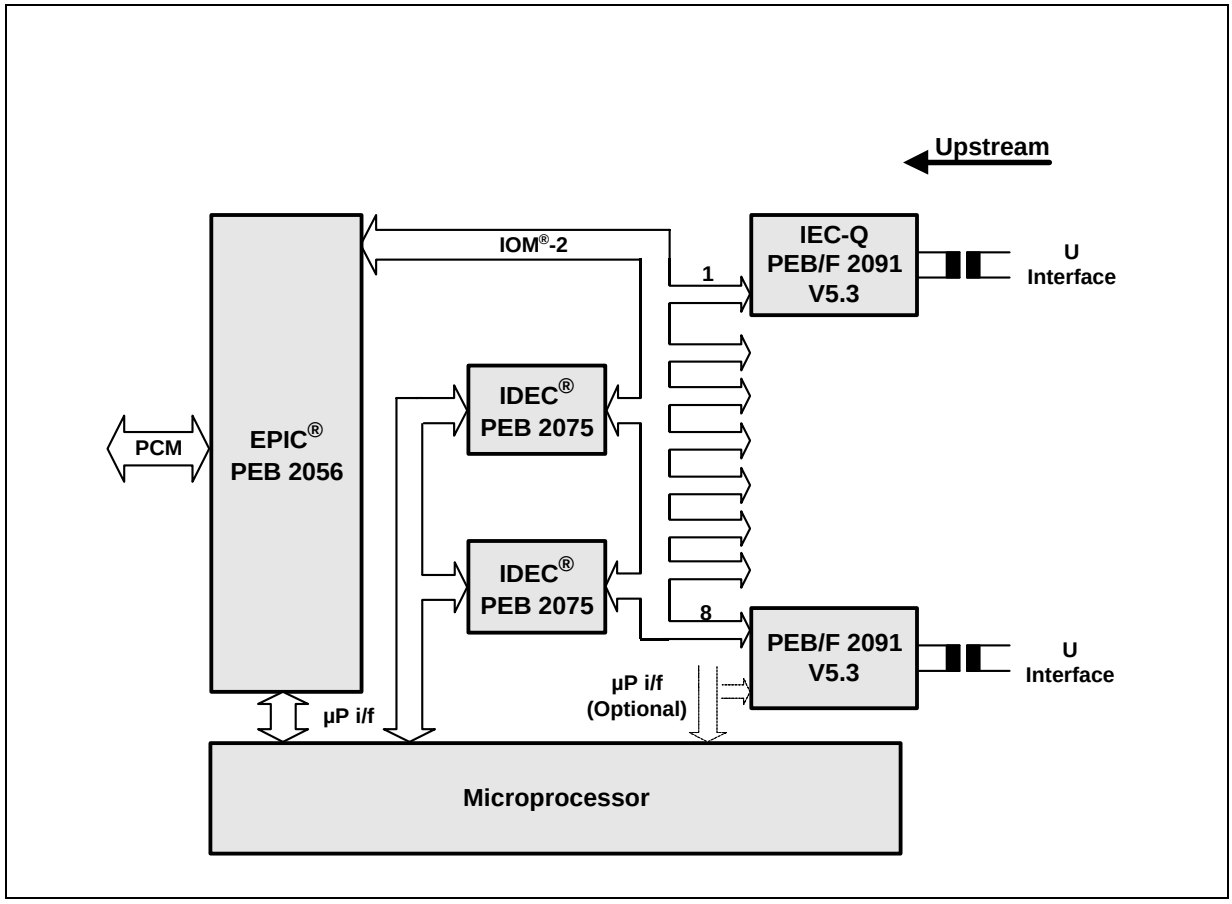


Figure 11 LT and Access Network Applications

1.5.9 NT1

Note 2: In new designs the IEC-Q is not recommended for this application. It is more cost effective and more convenient to use PEB/F 8091 in this application. As the PEB/F 8091 combines the functionality of SBC-X and IEC-Q in one device the combination below is sketched for reference only.

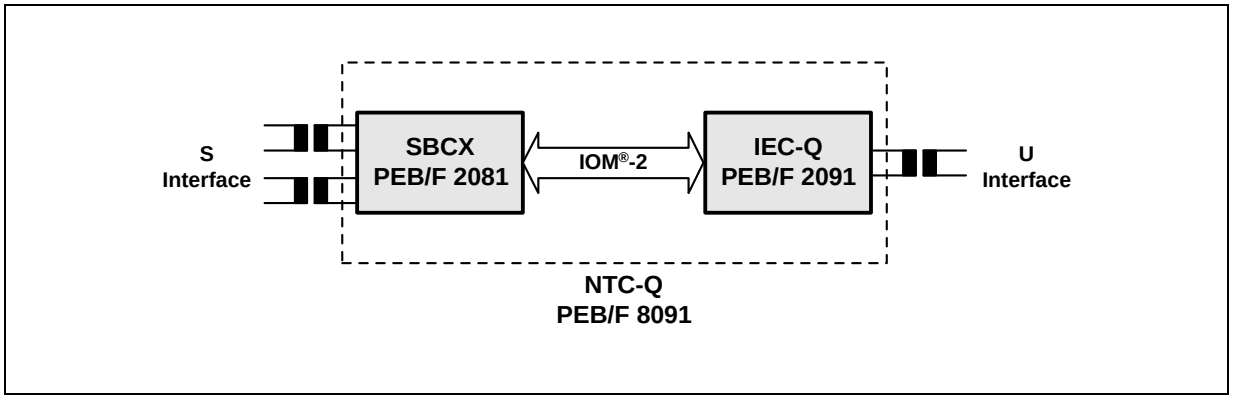


Figure 12 NT1 Application

2 Pin Descriptions

The PEB/F 2091 is available in three packages, P-LCC-44, T-QFP-64 and M-QFP-64. The detailed pin configurations of these three packages are given in section 2.1 below. Section 2.2 on page 32 provides a detailed definition and a brief functional description of all pins, for both stand-alone and microprocessor modes. Section 2.3 on page 48 closes this chapter with an overview of different µP interface modes supported by the IEC-Q.

2.1 Pin Configuration

2.1.1 P-LCC-44 Package

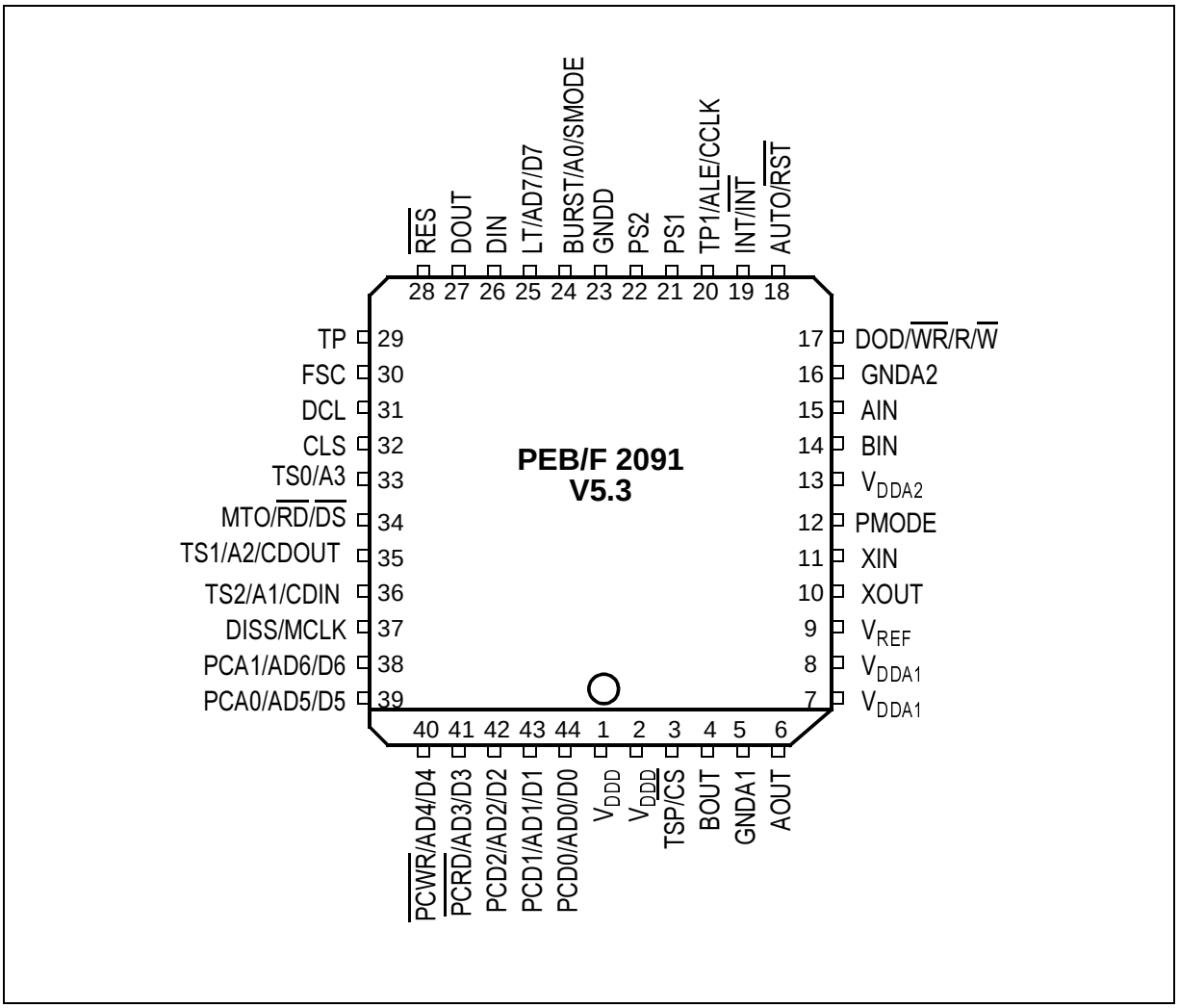


Figure 13 Pin Configuration for P-LCC-44 Package (top view)

2.1.2 T-QFP-64 and M-QFP-64 Packages

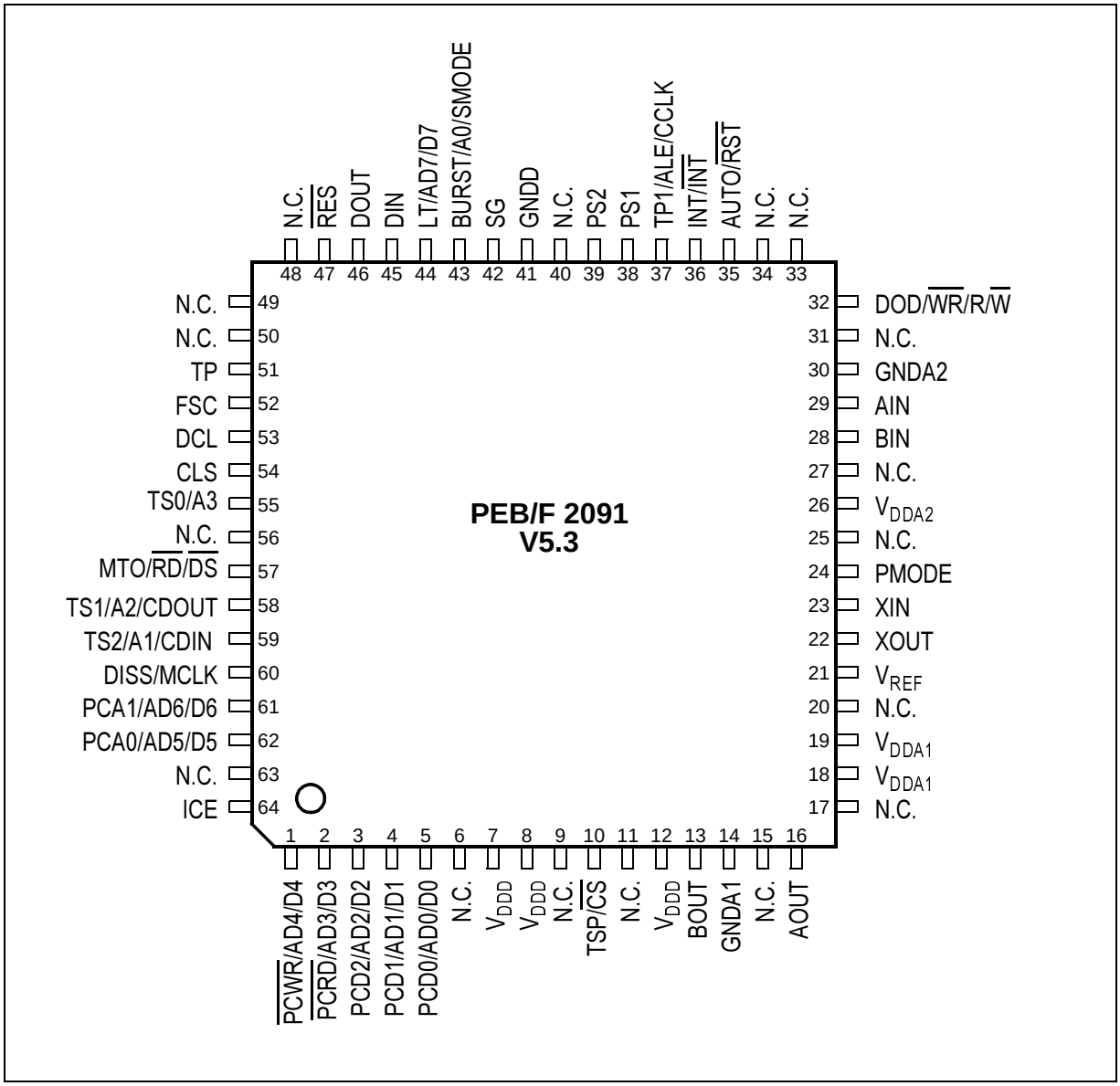


Figure 14 Pin Configuration for M-QFP-64 and T-QFP-64 Packages (top view)

2.2 Pin Definitions and Functions

The following tables group the pins according to their functions. They include pin name, pin number, type and a brief description of the function.

2.2.1 Pin Definition in Stand-Alone Mode

(i.e. PMODE="0" or unconnected)

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function

2.2.1.1 Mode Selection Pins

12	24	PMODE	I	Processor Interface Enable: Tie to GND or do not connect to select stand-alone mode. Setting PMODE to "1" enables the Processor Interface, see "Pin Definition in Microprocessor Mode", page 40. Internal pull down.
28	47	$\overline{\text{RES}}$	I	Reset: Low active, must be (0) at least for 30 ns, (see Table 4, page 53 for complete description of available mode configurations with this pin). The reset in the LT and NT-PBX mode will be carried out only after the clocks on the IOM®-2 have been applied to the IEC-Q. Tie to VDD if not used.
3	10	TSP	I	Single pulse test mode: For activation refer to Table 4, page 53. When active, alternating 2.5 V pulses are issued in 1.5 ms intervals. Tie to GND if not used.
25	44	LT	I/O	LT modes: Selects LT, COT 512/1536, LT-RP (1) and non LT modes NT, TE, NT-PBX, NT-RP (0). See Table 2, page 51 for details on mode selection.
24	43	BURST	I	Selection of burst modes (LT, NT-PBX) with (1) and non-burst modes (NT, TE, COT-512/1536, LT/NT-RP) with (0). See Table 2, page 51 for details on mode selection.

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
33	55	TS0	I	Time-slot: IOM®-2 channel selection for burst mode. LSB, active high. See Table 2, page 51 for details on mode selection.
35	58	TS1	I/O	Time-slot: IOM®-2 channel selection for burst mode. Active high. See Table 2, page 51 for details on mode selection.
36	59	TS2	I	Time-slot: IOM®-2 channel selection for burst mode. MSB, active high. See Table 2, page 51 for details on mode selection.
18	35	AUTO	I/O	Auto: Selection between auto and transparent mode for EOC channel processing. (Auto mode = (1))

2.2.1.2 Power Supply Pins

1, 2	7, 8, 12	V_{DDD}	I	5 V ± 5% digital supply voltage
5	14	GNDA1	I	0 V analog
7, 8	18, 19	V_{DDA1}	I	5 V ± 5% analog supply voltage
9	21	V_{REF}	O	V_{REF} pin to buffer internally generated voltage. Connect a capacitor of 100 nF to GND
13	26	V_{DDA2}	I	5 V ± 5% analog supply voltage
16	30	GNDA2	I	0 V analog
23	41	GNDD	I	0 V digital

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function

2.2.1.3 IOM®-2 Pins

31	53	DCL	I/O	Data clock: Clock range 512 kHz to 4096 kHz.
30	52	FSC	I/O	Frame synchronization clock: The start of the B1-channel in time-slot 0 is marked. FSC = (1) for one DCL-period indicates a superframe marker. FSC = (1) for at least two DCL-periods marks a standard frame.
26	45	DIN	I	Data in: Input of IOM®-2 data synchronous to DCL-clock. Corresponds to DD (data downstream) in LT and DU (data upstream) in NT applications.
27	46	DOUT	O	Data out: Output of IOM®-2 data synchronous to DCL-clock. Corresponds to DD (data downstream) in NT and DU (data upstream) in LT applications.

2.2.1.4 IOM®-2 Control Pins

17	32	DOD	I	DOUT open drain: Select open drain with DOD = (1) (external pull-up resistor required) and tristate with DOD = (0).
34	57	MTO	I	Monitor procedure time-out: Disables the internal 6 ms monitor time-out when set to (1). Internal pull-down resistor.

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function

2.2.1.5 U-Interface Pins

15	29	AIN	I	Differential U-Interface input: Connect to hybrid.
14	28	BIN	I	Differential U-Interface input: Connect to hybrid.
6	16	AOUT	O	Differential U-Interface output: Connect to hybrid.
4	13	BOUT	O	Differential U-Interface output: Connect to hybrid.

2.2.1.6 Power Controller Pins

44	5	PCD0	I/O	Data bus of power controller interface: LSB. Connect to VDD if not used.
43	4	PCD1	I/O	Data bus of power controller interface: Connect to VDD if not used.
42	3	PCD2	I/O	Data bus of power controller interface: MSB. Connect to VDD if not used.
39	62	PCA0	I/O	Address bus of power controller interface.
38	61	PCA1	I/O	Address bus of power controller interface.
41	2	$\overline{\text{PCRD}}$	I/O	Power controller interface read request: Low active.
40	1	$\overline{\text{PCWR}}$	I/O	Power controller interface write request: Low active.
19	36	INT	I/O	Interrupt: Change-sensitive. After a change of level has been detected the C/I code "INT" will be issued on IOM®-2. Tie to GND if not used.

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
37	60	DISS	O	Disable power supply: Different function in LT and NT modes. LT: the DISS pin is set to (1) with the C/I command "LTD". NT: the DISS pin is set to (1) after receipt of MON-0 LBBD in Auto mode.
21	38	PS1	I	Power status (primary): Different function in LT and NT mode. LT: (1) indicates that the remote power is switched off. (1) on PS1 results in C/I message "HI". Clamp to low if not used. NT: (1) indicates that prim. Power supply is OK. The pin value is identical to the overhead bit "PS1" value.
22	39	PS2	I	Power status (secondary): Different function in LT and NT mode. LT: the current feed value is transmitted (8 bit serially) from a power controller. Read the value with MON-8 "RPFC". NT: (1) indicates that secondary power supply is OK. The pin value is identical to the overhead bit "PS2" value.

2.2.1.7 Clocks

10	22	XOUT	O	Crystal OUT: 15.36-MHz crystal is connected. Suitable load capacitances should be connected in parallel. Their value depends on the crystal chosen and board Layout. See "Oscillator Circuit and Crystal", page 252 for details. Leave open if not used.

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
11	23	XIN	I	Crystal IN: External 15.36-MHz clock signal or 15.36-MHz crystal is connected. In case a crystal is connected, suitable load capacitances should be connected in parallel. Their value depends on the crystal chosen and board Layout. See "Oscillator Circuit and Crystal", page 252 for details
32	54	CLS	O	Clock Signal: In the NT modes this clock is synchronized to U-Interface. Used to synchronize external PLL or to clock S-Interface devices. In the NT , NT-Auto Activation, COT- and TE modes a 7.68 MHz clock is provided on this pin. In the PBX- and in the LT-RP modes a 512 kHz clock is provided. In the NT-RP mode a 15.36 MHz clock is provided (not synchronized to U-Interface). In the LT mode the clock on CLS is not defined and should therefore be left unconnected.

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function

2.2.1.8 Miscellaneous Function Pins

Not available	64	ICE	I	IOM®-2 Clocks Enable **In IOM®-2 Master modes:** '0': no FSC and DCL clocks are output. Clocks may be applied to pins FSC and DCL. However, they are ignored by the IEC-Q. Data on pin DIN is ignored. Pin DOUT is 'floating'. '1': Behavior as in former versions of the IEC-Q. The IOM®-2 clocks FSC and DCL are output on the corresponding pins. Due to an internal 100kOhm pull-up resistor this is the default configuration after reset if pin ICE is not connected. This pin can be overridden by the bit ADF2:ICEC. For more information see "IOM®-2 Enable/Disable Mode", page 53. **In IOM®-2 Slave modes:** Connect to VDD or leave open. Internal pull up.
Not available	42	SG	O	Undefined in stand-alone mode. Leave it open

2.2.1.9 Test Pins

29	51	TP	I	Test pin: Not available to user. Do not connect. Internal pull-down resistor.
20	37	TP1	I	Test pin: Not available to user. Do not connect. Internal pull-down resistor.

2.2.2 Pin Definition in Microprocessor Mode

(i.e. PMODE="1")

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
2.2.2.1 Mode Selection Pins				
12	24	PMODE	I	Processor Interface Enable: PMODE must be set to "1" to enable the Processor Interface (Multiplexed, demultiplexed and serial modes). Tie to GND or do not connect to select stand-alone mode, see "Pin Definition in Stand-Alone Mode", page 33. Internal pull down.
28	47	$\overline{\text{RES}}$	I	Reset: Low active, must be (0) at least for 30 ns, (see Table 4, page 53 for complete description of available mode configurations with this pin. The reset in the LT and NT-PBX mode will be carried out only after the IOM®-2 clocks have been applied to the IEC-Q. Tie to VDD if not used.
2.2.2.2 Data, Address and µP Selection Pins				
24	43	SMODE A0 SMODE	I	Serial mode pin: SMODE = 1 selects serial mode, SMODE = 0 enables the multiplexed mode. Address bus pin (Demultiplexed mode). (Multiplexed mode) tie to GND
36	59	CDIN A1 not used	I	Controller Data In (Serial mode): CCLK determines the data rate. Address bus pin (Demultiplexed mode). (Multiplexed mode) tie to GND.

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
35	58	CDOUT	I/O	Controller Data Out (Serial mode): CCLK determines the data rate. CDOUT is "high Z" if no data is transmitted.
		A2	I/O	Address bus pin (Demultiplexed mode).
		not used		(Multiplexed mode) tie to GND.
33	55	not used	I	(Serial mode) tie to GND.
		A3		Address bus pin (Demultiplexed mode).
		not used		(Multiplexed mode) tie to GND.
44	5	not used	I/O	(Serial mode) tie to GND.
		D0		Data bus pin (Demultiplexed mode)
		AD0		Address/Data bus pin (Multiplexed mode)
43	4	not used	I/O	(Serial mode) tie to GND.
		D1		Data bus pin (Demultiplexed mode)
		AD1		Address/Data bus pin (Multiplexed mode)
42	3	not used	I/O	(Serial mode) tie to GND.
		D2		Data bus pin (Demultiplexed mode)
		AD2		Address/Data bus pin (Multiplexed mode)
41	2	not used	I/O	(Serial mode) tie to GND.
		D3		Data bus pin (Demultiplexed mode)
		AD3		Address/Data bus pin (Multiplexed mode)
40	1	not used	I/O	(Serial mode) tie to GND.
		D4		Data bus pin (demultiplexed modes)
		AD4		Address/Data bus pin (Multiplexed mode)

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
39	62	not used D5 AD5	I/O	(Serial mode) tie to GND. Data bus pin (demultiplexed modes) Address/Data bus pin (Multiplexed mode)
38	61	not used D6 AD6	I/O	(Serial mode) tie to GND. Data bus pin (demultiplexed modes) Address/Data bus pin (Multiplexed mode)
25	44	not used D7 AD7	I/O	(Serial mode) tie to GND. Data bus pin (demultiplexed modes) Address/Data bus pin (Multiplexed mode)

2.2.2.3 µP Control Pins

19	36	$\overline{\text{INT}}$	I/O	Interrupt line (Multiplexed, demultiplexed and serial modes): Low active.
3	10	$\overline{\text{CS}}$	I	Chip select (Multiplexed, demultiplexed and serial modes): Low active.
17	32	not used $\overline{\text{WR}}$ R/$\overline{\text{W}}$	I	(Serial mode) tie to GND. Write (Siemens/Intel multiplexed and demultiplexed modes): indicates a write operation, active low. Read/Write (Motorola demultiplexed mode): indicates a read (high) or write (low) operation.

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
34	57	not used	I	(Serial mode) tie to GND.
		$\overline{RD}$		Read (Siemens/Intel multiplexed and demultiplexed modes): indicates a read operation, active low.
		$\overline{DS}$		Data Strobe (Motorola demultiplexed mode): indicates a data transfer, active low.
20	37	CCLK	I	Controller data clock (Serial mode): Shifts data from or to the device.
		(Mode Select)		Mode Selection (Demultiplexed mode): ALE tied to GND selects the Siemens/Intel type. ALE tied to VDD selects the Motorola type.
		ALE	I	Address Latch Enable (Multiplexed mode): In the Siemens/Intel µP interface modes a high indicates an address on the AD0..3 pins which is latched with the falling edge of ALE.

2.2.2.4 Power Supply Pins

1, 2	7, 8, 12	V_{DDD}	I	5 V ± 5% digital supply voltage
5	14	GNDA1	I	0 V analog
7, 8	18, 19	V_{DDA1}	I	5 V ± 5% analog supply voltage
9	21	V_{REF}	O	V_{REF} pin to buffer internally generated voltage. Connect a capacitor of 100 nF to GND
13	26	V_{DDA2}	I	5 V ± 5% analog supply voltage
16	30	GNDA2	I	0 V analog
23	41	GNDD	I	0 V digital

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function

2.2.2.5 IOM®-2 Pins

31	53	DCL	I/O	Data clock: Clock range 512 kHz to 4096 kHz.
30	52	FSC	I/O	Frame synchronization clock: The start of the B1-channel in time-slot 0 is marked. FSC = (1) for one DCL-period indicates a superframe marker. FSC = (1) for at least two DCL-periods marks a standard frame.
26	45	DIN	I	Data in: Input of IOM®-2 data synchronous to DCL-clock. Corresponds to DD (data downstream) in LT and DU (data upstream) in NT applications.
27	46	DOUT	O	Data out: Output of IOM®-2 data synchronous to DCL-clock. Corresponds to DD (data downstream) in NT and DU (data upstream) in LT applications.

2.2.2.6 U-Interface Pins

15	29	AIN	I	Differential U-Interface input: Connect to hybrid.
14	28	BIN	I	Differential U-Interface input: Connect to hybrid.
6	16	AOUT	O	Differential U-Interface output: Connect to hybrid.
4	13	BOUT	O	Differential U-Interface output: Connect to hybrid.

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
2.2.2.7 Power Controller Pins				
21	38	PS1	I	Power status (primary): Different function in LT and NT mode. LT: (1) indicates that the remote power is switched off. (1) on PS1 results in C/I message "HI". Clamp to low if not used. NT: (1) indicates that primary power supply is OK. The pin value is identical to the overhead bit "PS1" value.
22	39	PS2	I	Power status (secondary): Different function in LT and NT mode. LT: the current feed value is transmitted (8 bit serially) from a power controller. Read the value with MON-8 "RPFC". NT: (1) indicates that secondary power supply is OK. The pin value is identical to the overhead bit "PS2" value.
2.2.2.8 Clocks				
10	22	XOUT	O	Crystal OUT: 15.36-MHz crystal is connected. Suitable load capacitances should be connected in parallel. Their value depends on the crystal chosen and board Layout. See "Oscillator Circuit and Crystal", page 252 for details. Leave open if not used.

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
11	23	XIN	I	Crystal IN: External 15.36-MHz clock signal or 15.36-MHz crystal is connected. In case a crystal is connected, suitable load capacitances should be connected in parallel. Their value depends on the crystal chosen and board Layout. See "Oscillator Circuit and Crystal", page 252 for details
32	54	CLS	O	Clock Signal: In the NT modes this clock is synchronized to U-Interface. Used to synchronize external PLL or to clock S-Interface devices. In the NT, NT-Auto Activation, COT and TE modes a 7.68 MHz clock is provided on this pin. In the PBX- and in the LT-RP modes a 512 kHz clock is provided. In the NT-RP mode a 15.36 MHz clock is provided (not synchronized to U-Interface). In the LT mode the clock on CLS is not defined and should therefore be left unconnected.
37	60	MCLK	O	Microprocessor clock output (Multiplexed, demultiplexed and serial modes): provided with four programmable clock rates: 7.68 MHz, 3.84 MHz, 1.92 MHz and 0.96 MHz.

2.2.2.9 Miscellaneous Function Pins

18	35	$\overline{\text{RST}}$	O	Reset output (Multiplexed, demultiplexed and serial modes): Low active.

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
Not available	64	ICE	I	IOM®-2 Clocks Enable **In IOM®-2 Master modes:** '0': no FSC and DCL clocks are output. Clocks may be applied to pins FSC and DCL. However, they are ignored by the IEC-Q. Data on pin DIN is ignored. Pin DOUT is 'floating'. '1': Behavior as in former versions of the IEC-Q. The IOM®-2 clocks FSC and DCL are output on the corresponding pins. Due to an internal 100 kOhm pull-up resistor this is the default configuration after reset if pin ICE is not connected. This pin can be overridden by the bit ADF2:ICEC. For more information see "IOM®-2 Enable/Disable Mode", page 53. **In IOM®-2 Slave modes:** Connect to VDD or leave open. Internal pull up.
Not available	42	SG	O	Stop/Go Bit Status Pin Gives the status of the S/G bit in TE mode if the S/G bit control function is being used, see "Indication of S/G Bit Status on Pin SG", page 205, for details. In all other modes the SG pin in set to '1'.

2.2.2.10 Test Pin

29	51	TP	I	Test pin: Not available to user. Do not connect. Internal pull-down resistor.

2.3 Microprocessor Bus Interface (Overview)

The table below gives an overview of the different microprocessor bus modes.

Table 1 Microprocessor Bus Interface

Pin Number		Stand-Alone Mode	Symbol in Processor Mode			
P-LCC-44	T-QFP-64 and M-QFP-64		Siemens/ Intel multiplexed	Siemens/ Intel demultiplex.	Motorola demultiplex.	Serial
12	24	PMODE = 0	PMODE = 1			
44	5	PCD0	AD0	D0	D0	n.c.
43	4	PCD1	AD1	D1	D1	n.c.
42	3	PCD2	AD2	D2	D2	n.c.
41	2	$\overline{\text{PCRD}}$	AD3	D3	D3	n.c.
40	1	$\overline{\text{PCWR}}$	AD4	D4	D4	n.c.
39	62	PCA0	AD5	D5	D5	n.c.
38	61	PCA1	AD6	D6	D6	n.c.
25	44	LT	AD7	D7	D7	n.c.
19	36	INT	$\overline{\text{INT}}$	$\overline{\text{INT}}$	$\overline{\text{INT}}$	$\overline{\text{INT}}$
24	43	BURST	SMODE=0	A0	A0	SMODE=1
36	59	MS2	n.c.	A1	A1	CDIN
35	58	MS1	n.c.	A2	A2	CDOUT
33	55	MS0	n.c.	A3	A3	n.c.
20	37	TP1	ALE	ALE=0	ALE=1	CCLK
34	57	MTO	$\overline{\text{RD}}$	$\overline{\text{RD}}$	$\overline{\text{DS}}$	n.c.
17	32	DOD	$\overline{\text{WR}}$	$\overline{\text{WR}}$	R/$\overline{\text{W}}$	n.c.
3	10	TSP	$\overline{\text{CS}}$	$\overline{\text{CS}}$	$\overline{\text{CS}}$	$\overline{\text{CS}}$
37	60	DISS	MCLK			
18	35	AUTO	$\overline{\text{RST}}$			

3 Functional Description

Interfaces and functional blocks of the PEB/F 2091 V5.3 differ depending on the mode used, i.e. depending on whether the stand-alone mode or the microprocessor mode is being used.

Section 3.1 defines these two modes and gives an overview of device function.

As mentioned in section 1.1, page 19 the IEC-Q can be used in various functional modes, including LT, NT, TE, Repeater and others. Section 3.2 gives an overview of available modes, and describes how these modes can be set. In addition an overview is given about setting special modes, e.g. test modes, and EOC Auto and Transparent modes and different mode settings related to the IOM®-2 interface.

In Section 3.3 device architecture is discussed. Block diagrams for both stand-alone and microprocessor modes are illustrated.

Section 3.4 describes the architecture of the U-interface core (transceiver core). It provides a brief description of its functions and properties.

The device's interfaces defined in section 3.3 are described in the subsequent sections 3.5 through 3.14. All relevant functional information about these interfaces, especially those related to user's handling are given. The interaction between these interfaces, however, is out of the scope of this section (e.g. operations between the IOM®-2 and the U-interface). This is the scope of the chapter "Operational Description", page 96.

Section 3.15 gives an overview of the reset behavior of the IEC-Q.

3.1 Functional Overview

The IEC-Q fulfills all U transceiver functions required by all national and international standardization institutes. It also provides simple and flexible access to data and control bits on the U-interface, activation and deactivation, monitoring transmission quality and other useful general as well as application specific functions. This access can be achieved using the IOM®-2 interface, the microprocessor interface or a combination of both. If the microprocessor interface is not being used we refer to this mode as 'stand-alone mode'. This mode can be selected by leaving pin PMODE opened or setting it to '0' (see "Mode Selection Pins", page 33). In stand-alone mode the PEB/F 2091 V5.3 is controlled exclusively via the IOM®-2 interface and mode selection pins (see Figure 15 below). In this mode a 'Power Controller Interface' is available, allowing direct access to e.g. peripheral power controller devices.

If the microprocessor interface (PI) is being used we refer to this mode as the 'µP mode'. This mode can be selected by setting pin PMODE to '1' (see "Mode Selection Pins", page 40). The PI of the PEB/F 2091 V5.3 establishes the access of a microprocessor between U-interface and IOM®-2. It's main function is illustrated in Figure 15.

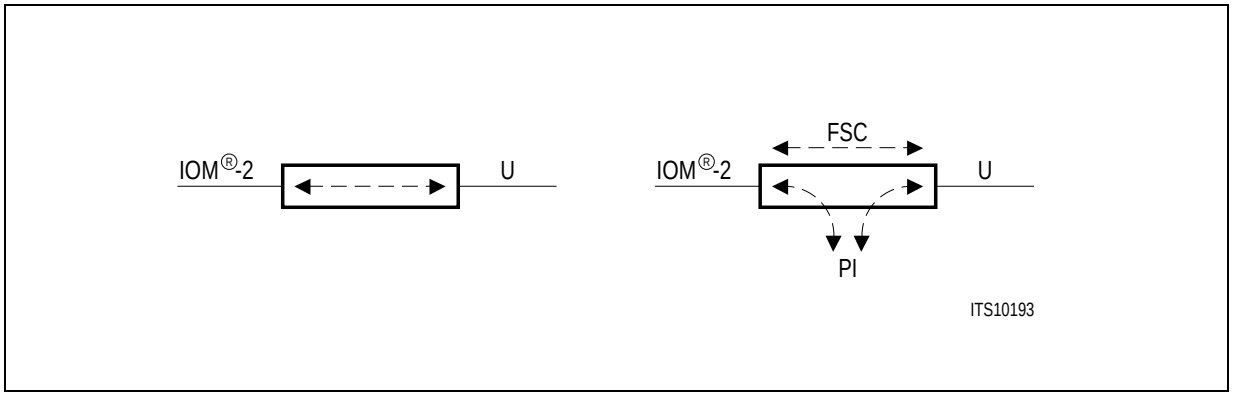


Figure 15 Stand-Alone Mode (left) and µP Mode (right)

In µP mode B channels, D channel, C/I codes and Monitor commands can either be passed between the U transceiver and IOM®-2 directly, or they can be looped through the µP via the PI. Any selection of "passed" or "looped" channels can be programmed via a control register.

3.2 Setting Operating Modes

Mode setting of the PEB/F 2091 V5.3 will be described in several subsections below. This includes setting basic operation modes (e.g. LT, NT, Repeater), as well as setting special operating modes, i.e. test modes, DOUT driver modes, IOM®-2 enable/disable, EOC Auto/Transparent and monitor time-out on/off.

Setting operation modes of the PEB/F 2091 V5.3 will be different in stand-alone and in µP mode. These two cases will be distinguished.

3.2.1 Basic Operating Mode

µP Mode

In µP mode a microprocessor interface gives access to the configuration registers. The basic operating mode is selected via bits STCR:BURST,LT, TS2,TS1,TS0, according to Table 2, page 51 . The STCR register is described on page 212.

Stand-Alone Mode

In stand-alone mode the operating mode is selected via pin strapping of pins LT, Burst, TS2, TS1 and TS0 according to Table 2, page 51. It is possible to change the mode of a device during operation (e.g. for test purposes) if the mode change is followed by a reset.

Table 2 Setting Modes of Operation (Stand-Alone and µP Mode)

	Mode Selection Stand-Alone Mode/µP Mode						Output Pins U Synchronized		
Mode	**Burst[1)]**	**LT[1)]**	**TS2[1)]**	**TS1[1)]**	**TS0[1)]**	**DCL IN**	**DCL OUT (kHz)**	**CLS OUT (kHz)**	**Super frame marker[2)]**
NT	0	0	0	0	0	_	512	7680[3)]	no
NT	0	0	1	0	0	_	512	7680[3)]	yes
NT-Auto Activation	0	0	0	0	1	_	512	7680[3)]	no
TE	0	0	0	1	0	_	1536	7680[3)]	no
TE	0	0	1	1	0	_	1536	7680[3)]	yes
NT-PBX	1	0	IOM®-2 channel assignment (Table 3)			512-4096	_	512[3)]	_
LT	1	1	IOM®-2 channel assignment (Table 3)			512-4096	_	not defined	_
COT-512	0	1	0	0	0	_	512	7680[4)]	no
COT-1536	0	1	0	1	0	_	1536	7680[4)]	no
LT-RP	0	1	1	0	1	512	_	512[4)]	_
NT-RP	0	0	1	0	1	_	512	15360[4)]	yes

1) In stand-alone mode this name refers to the corresponding pin
In µP mode this name refers to the corresponding bit in register STCR

2) 1 DCL-period high-phase of FSC at superframe position
2 DCL-periods high-phase of FSC at normal position

3) CLS-clock signal not available while device is in power-down. Synchronized to the U-interface

4) CLS-clock signal available while device is in power-down. Not synchronized to the U-interface

Table 3 Setting IOM®-2 Channel Assignment

IOM®-2 Channel No.	TS2[1)]	TS1[1)]	TS0[1)]	Bit No.	Min. Frequency of DCL (kHz)
CH 0	0	0	0	0 … 31	512
CH 1	0	0	1	32 … 63	1024
CH 2	0	1	0	64 … 95	1536
CH 3	0	1	1	96 … 127	2048
CH 4	1	0	0	128 … 159	2560
CH 5	1	0	1	160 … 191	3072
CH 6	1	1	0	192 … 223	3584
CH 7	1	1	1	224 … 255	4096

1) In **stand-alone mode** this name refers to the corresponding pin. The pin value is read continuously (non-latching) after the supply voltage has reached its nominal value
In **µP mode** this name refers to the corresponding bit in register STCR

3.2.2 Test Modes

µP Mode

Test modes Send Single Pulses, Quiet Mode or Data Through are invoked via the corresponding C/I Channel command (see "C/I Channel Codes", page 224) or via bits STCR:TM2,TM1 (Table 4). See also "STCR-Register", page 212.

Stand-Alone Mode

The test modes Send Single Pulses (SSP), Quiet Mode (QM) and Data Through (DT) are invoked via the corresponding C/I Channel command ("C/I Channel Codes", page 224) or via pins $\overline{\text{RES}}$ and TSP (Table 4).

Table 4 Setting Test Modes

	Mode Selection Stand-Alone Mode/µP Mode	
Test-Mode	**Pin $\overline{\text{RES}}$/ Bit TM1**	**Pin TSP/ Bit TM2**
Master-Reset[1)]	0	0
Send Single-Pulses[2)]	1	1
Data-Through[3)]	0	1
Normal Operation	1	0

1) Used for Quiet Mode and Return Loss measurements

2) Used for Pulse Mask measurements

3) Used for Insertion Loss, Power Spectral Density and Total Power measurements

3.2.3 DOUT Driver Modes

Mode setting of pin DOUT will be given in the following two tables

Table 5 Setting DOUT Driver in Stand-Alone Mode

Mode	Pin $\overline{\text{RES}}$	Pin TSP	Pin DOD	Pin DOUT Output Driver		
				Value	DOUT in active IOM®-2 Channel[1)]	DOUT in passive IOM®-2 Channel[1)]
Normal (Tristate)	1	0	0	0	low	high Z
				1	high	
Normal (Open Drain [2)])	1	0	1	0	low	floating
				1	floating	

1) Refer to Notes 10, page 72, 12, page 72, and 15, page 73 for explanation about active and passive channels

2) External pull-up resistors required (typ.1 kΩ)

3.2.4 IOM®-2 Enable/Disable Mode

Note 3: This mode setting is only available in the master mode of the IEC-Q, i.e. modes in which the IOM®-2 clocks FSC and DCL are delivered by the

Table 6 Setting DOUT Driver in µP Mode

Mode	Pin RES	Bit ADF2: DOD[1]	Pin DOUT Output Driver		
			Value	DOUT in active IOM®-2 Channel[2]	DOUT in passive IOM®-2 Channel
Normal (Tristate)	1	0	0	low	high Z[3]
			1	high	
Normal (Open Drain [4])	1	1	0	low	floating
			1	floating	

1) See also "ADF2-Register", page 214

2) Refer to Notes 10, page 72, 12, page 72, and 15, page 73 for explanation about active and passive channels

3) In TE mode bit number 27 of channel 2 (S/G bit) may be driven if the 'S/G bit control' function is being used (see "S/G Bit and BAC Bit Operations", page 198)

4) External pull-up resistors required (typ.1 kΩ)

IEC-Q. See Table 2, page 51. For a detailed description of the IOM®-2 interface refer to section 3.6, page 70.

Applications in which the IEC-Q is not the only potential IOM®-2 clock master on the board have to deal with IOM®-2 clock conflicts during and after reset. Among these applications are dual mode S- or U-terminals and circuits (see "Dual Mode U and S Terminals and PC Cards", page 27). Typical applications would include the ISAC®-S TE (PSB 2186) or the IPAC (PSB 2115) in TE mode. Both devices output FSC and DCL during and after reset.

The PEB/F 2091 V5.3 in the 64 pin packages (T-QFP-64 or M-QFP-64) has a pin (pin 64, ICE) which allows to enable or disable the IOM®-2 clocks and the data-lines. It is possible to change the status of pin ICE without the need of a reset signal being applied. In µP mode the status of pin ICE can be overridden by bit ADF2:ICEC. Basically, the value of pin ICE and the bit-value are EXORed (see Table 7 below).

This function can also be controlled in the P-LCC-44 package in the microprocessor mode (PMODE = "1") by bit ADF2:ICEC, see "ADF2-Register", page 214.

The following table gives an overview of the control mechanisms of this function in different settings. The terms "Idle" and "active" of the IOM®-2 interface in Table 7 are defined as follows:

Idle means that no FSC and DCL clocks are output. Clocks may be applied to pins FSC and DCL. However, they are ignored by the IEC-Q. Data on pin DIN is ignored. Internally, the DIN signal will be clamped to '1'. Pin DOUT is 'floating', which is the same behavior as described in "DOUT Driver Modes", page 53.

Active means that the behavior is as in former versions of the IEC-Q. The IOM®-2 clocks FSC and DCL are output on the corresponding pins.
Due to the 100 kOhm pull-up resistor this is the default configuration after reset if pin ICE is not connected.

Table 7 Setting IOM®-2 Clock Enable/Disable Mode

Mode	Package	ADF2:ICEC bit polarity	ICE pin polarity	IOM®-2 interface
stand-alone mode (PMODE= "0" or unconnected)	P-LCC-44	Not available	Not available	Active
	M-QFP-64 or T-QFP-64	Not available	"1" or not connected	Active
			"0"	Idle
µP mode (PMODE="1")	P-LCC-44	"0" (default)	Not available	Active
		"1"		Idle
	M-QFP-64 or T-QFP-64	"0" (default)	"1" or not connected	Active
			"0"	Idle
		"1"	"1" or not connected	Idle
			"0"	Active

3.2.5 EOC Auto/Transparent Mode

The U-interface EOC (Embedded Operations Channel) allows transmission of commands and informations in either direction of the U-interface. For details on EOC structure and commands, see "Predefined EOC Codes", page 231. If the EOC "Transparent" mode is selected EOC channel informations will be given transparently on the IOM®-2 interface independently of the content of the EOC channel. In the EOC "AUTO" mode an EOC processor is activated for EOC command interpretation and handling. For operational details of the EOC in both modes see "Access to EOC of U-Interface", page 110.

In stand-alone mode the EOC mode will be set by the input pin AUTO. In µP mode the EOC mode will be set by bit AUTO of register STCR (see "STCR-Register", page 212).

3.2.6 Monitor Procedure Time-Out (MTO)

The IEC-Q offers an internal reset (monitor procedure "Time-out") for the monitor procedure (see 3.6.3, page 76 for description of the IOM®-2 Monitor Channel). This reset

Table 8 Setting EOC Mode

	Mode Selection Stand-Alone Mode / µP Mode
EOC Mode	**Pin AUTO/Bit STCR:AUTO**
Transparent	0
Automatic	1

function transfers the Monitor Channel into the idle state thereby resolving possible lock-up situations. It therefore is to be used in all systems where no µP is capable of detecting and solving hang-up situations in the monitor procedure. For a detailed description of the time-out procedure see "Monitor Procedure Time-Out", page 80.

Note 4: ***The Monitor Channel Time-Out feature is only available after the complete receive frame structure has been detected on U (see Figure 30, page 81). I.e. this feature is available if the following signals have been received:***
In LT modes, the signals SN3 or SN3T
In NT modes, the signals SL2, SL3, SL3T
See "U-Interface Signals", page 125 for definition of these signals.

In stand-alone mode the MTO mode will be set by the input pin MTO. In µP mode the MTO mode will be set by bit MTO of register ADF2 (see "ADF2-Register", page 214).

Table 9 Setting MTO Mode

	Mode Selection Stand-Alone Mode / µP Mode
MTO Mode	**Pin MTO/Bit ADF2:MTO**
Time-out Enabled	0[1)]
Time-out Disabled	1

1) In stand-alone mode the pin MTO can be left unconnected. Due to an internal pull-down the Monitor Channel time-out feature will be enabled.

3.2.7 Setting IOM®-2 Bit Clock Mode

Note 5: ***This section applies only if the microprocessor mode and the IOM®-2 Master mode are used (see Note 8, page 70 for definition).***

The default frequency of the IOM®-2 clock DCL will always be two times the bit frequency (see Note 7, page 70). In some non standard applications it might be more convenient to have IOM®-2 bit rate on DCL, instead. The IEC-Q supports this in the microprocessor mode. In this mode it is possible to change the DCL frequency if the IOM®-2 master

mode is being used. Setting the ADF:BCL bit to ’1’ will change DCL frequency to the bit data rate, dividing the default DCL frequency by 2.

Note 6: Setting this mode will change the output frequency on pin DCL. Internally, the IEC-Q will continue to work with the default DCL frequency.

3.3 Block Diagram

Microprocessor Mode

In the microprocessor mode the following interfaces and functional blocks are used. For an overview of block functions refer to sections 3.4 through 3.15.

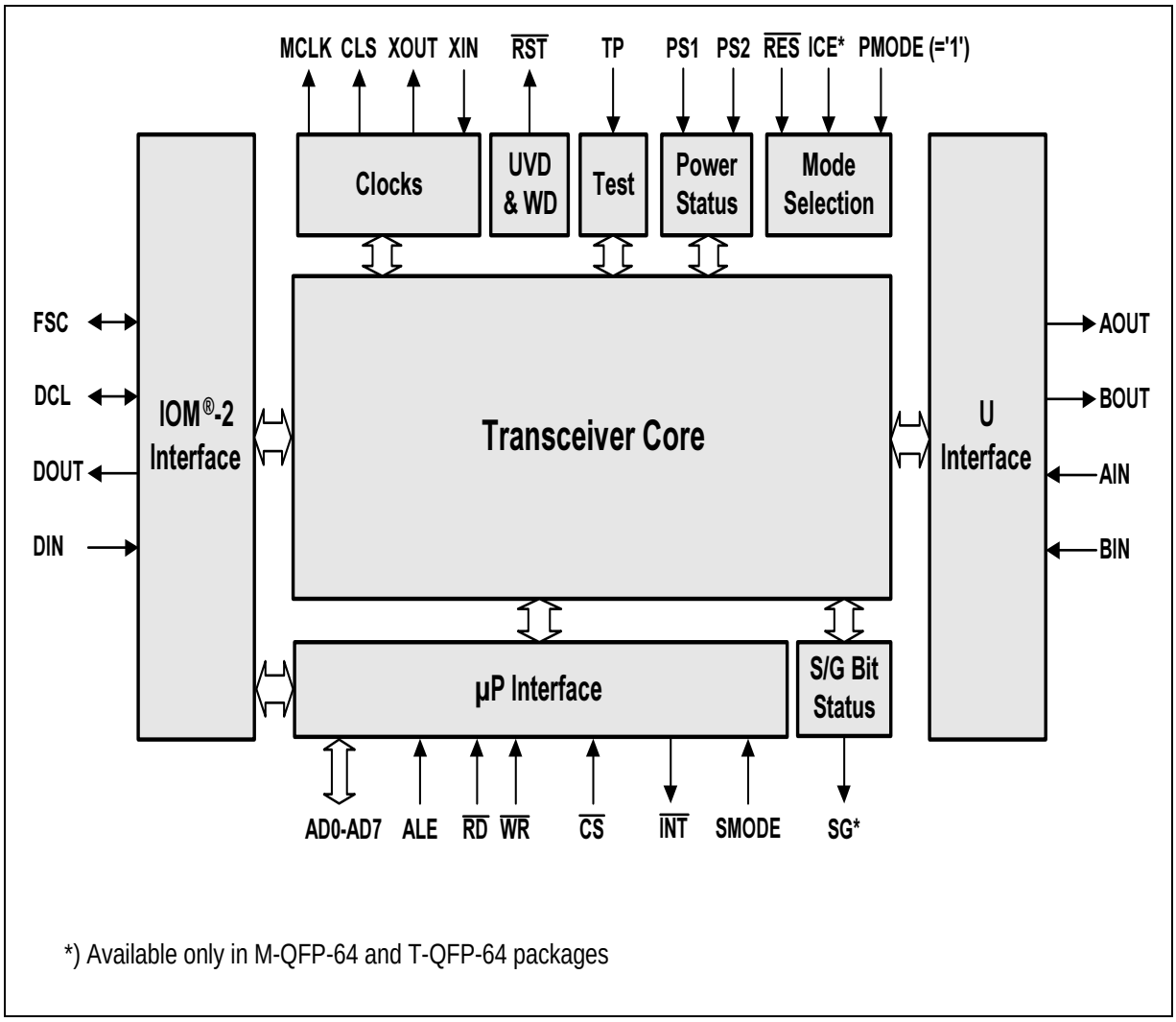


Figure 16 Device Architecture in µP Mode

Stand-Alone Mode

In stand-alone mode the following interfaces and functional blocks are used. For an overview of block functions refer to sections 3.4 through 3.15.

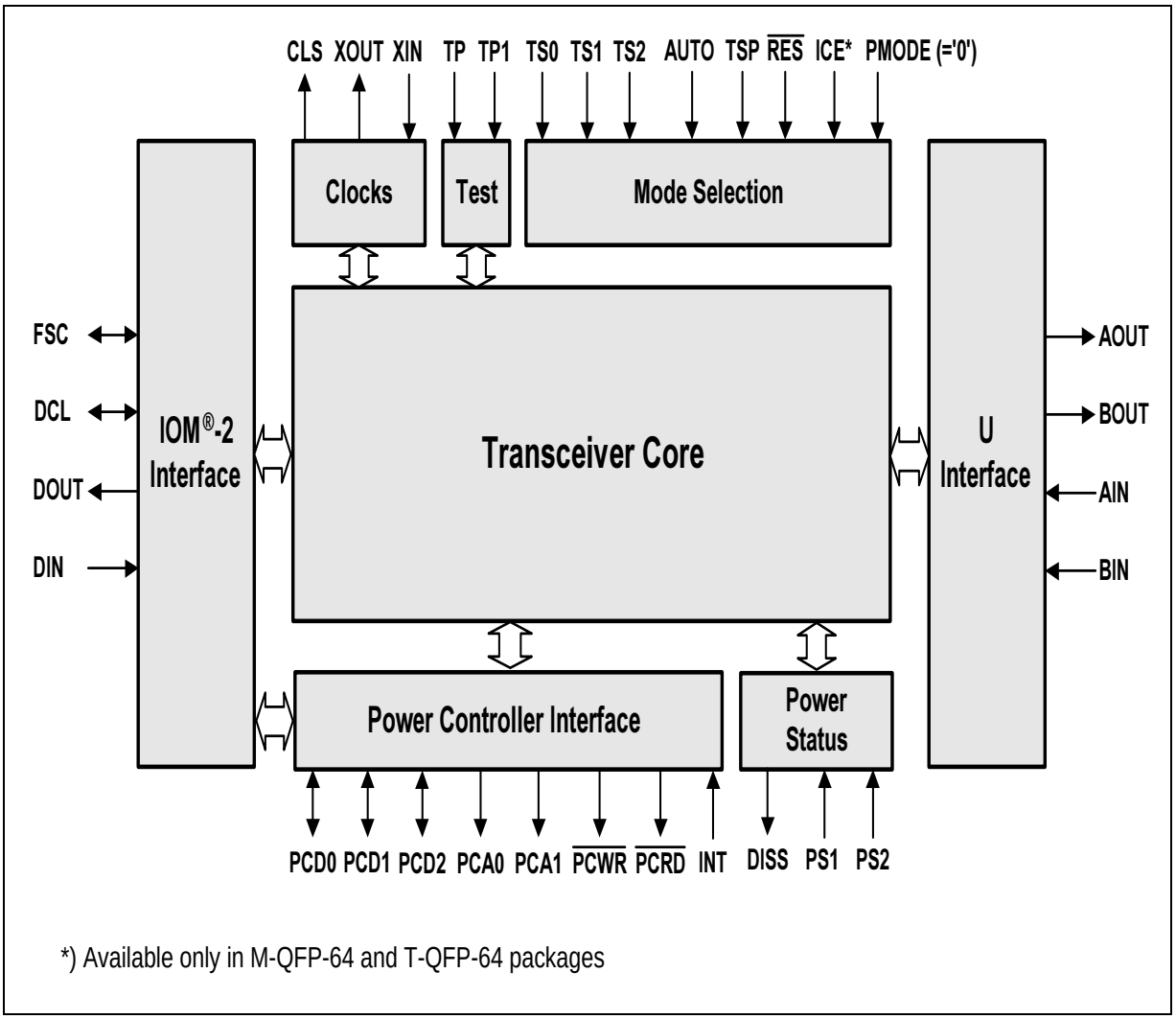


Figure 17 Device Architecture in Stand-Alone Mode

3.4 Transceiver Core

The U transceiver establishes the direct link between the exchange and the terminal side over two copper wires. Transmission over the U-interface is performed at a rate of 80 kBaud. Two binary informations are coded into one quaternary symbol (2B1Q) resulting in a total of 160 kbit/s to be transmitted. 144 kbit/s are user data (2B + D), 16 kbit/s are used for maintenance and synchronization information. For the structure of the U-interface, see "U-Interface", page 67. User access to the transceiver core will be established via one of the IEC-Q interfaces, e.g. IOM®-2 or µP interface (see Figure16 and 17 above). The access method to the transceiver core and to other blocks of the IEC-Q will be the scope of chapter 4, "Operational Description", page 96 ff.

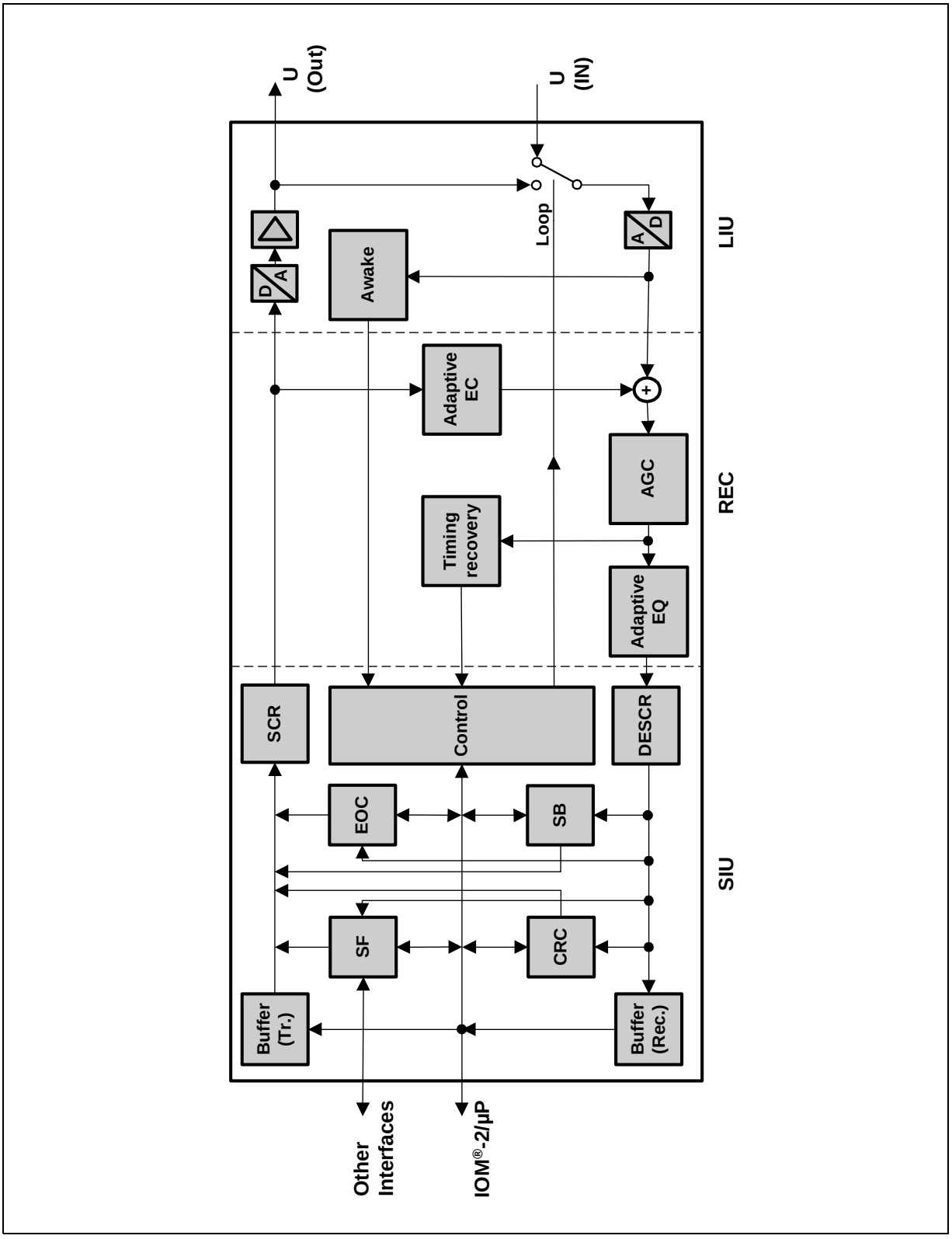


Figure 18 U Transceiver Block Diagram

the U transceiver can be subdivided in three main blocks:

SIU	System Interface Unit
REC	Receiver
LIU	Line Interface Unit

3.4.1 System Interface Unit

The System Interface Unit (SIU) provides the link between the different interfaces of the IEC-Q, e.g. IOM®-2 to the U- interface.

Transmit Buffer

This block is a 'first in first out' (FIFO) buffer which stores the user data (2B+D) given to the IEC-Q via IOM®-2 or µP interface. These data are then transmitted to the D/A converter (LIU) and to the adaptive echocanceller (REC) with the appropriate U-interface timing.

Receive Buffer

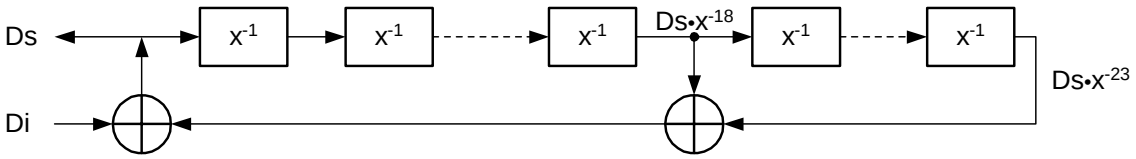
This is a 'first in first out' (FIFO) buffer which stores the user data (2B+D) received from the U-interface. These data are then transmitted to the user interface (IOM®-2 or µP) with the appropriate interface timing.

Scrambler / Descrambler

The scrambling and descrambling algorithms are implemented in these blocks (SCR and DESCR in Figure 18, page 61). These algorithms ensures that no sequences of permanent binary 0s or 1s are transmitted.

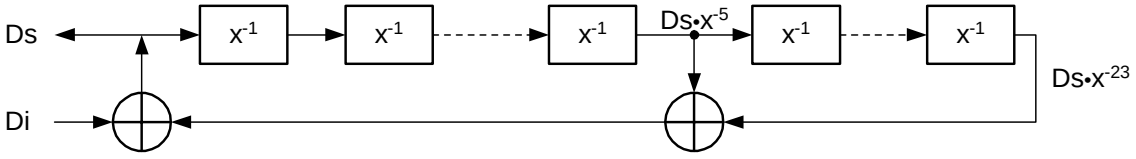
The algorithms used for scrambling and descrambling in LT and NT modes are described in Figure 19. Note that one wrong bit decision in the Receiver automatically leads to at least three bit errors.

Transmitter Scrambler in NT, NT-PBX and TE Mode without Loop-Back 3



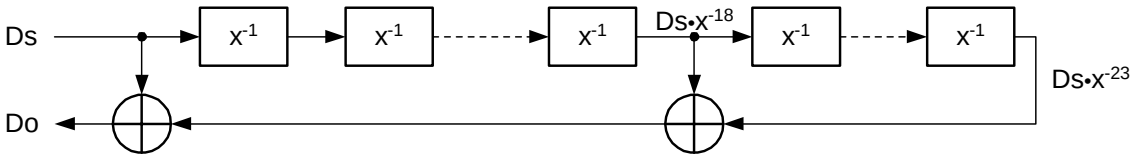
$Ds = Di \oplus Ds \bullet x^{-18} \oplus Ds \bullet x^{-23}$

Transmitter Scrambler for all LT Modes and for Loop-Back 3 in all NT Modes



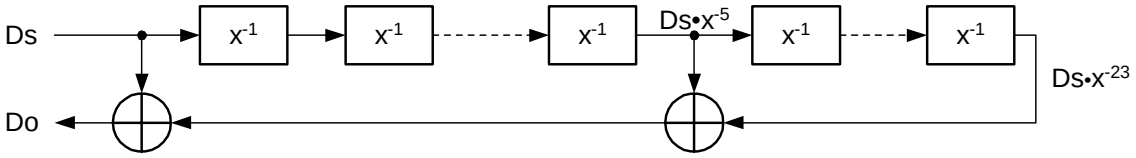
$Ds = Di \oplus Ds \bullet x^{-5} \oplus Ds \bullet x^{-23}$

Receiver Descrambler for all LT Modes and for Loop-Back 3 in all NT Modes



$Do = Ds (1 \oplus x^{-18} \oplus x^{-23})$

Receiver Descrambler in NT, NT-PBX and TE Mode without Loop-Back 3



$Do = Ds (1 \oplus x^{-5} \oplus x^{-23})$

Figure 19 Scrambler / Descrambler Algorithms

Control Block

Complete activation and deactivation procedures are implemented, which are controlled by activation and deactivation indications from U, IOM®-2 or µP interfaces. State transition of the procedures depend on the actual status of the Receiver (adaptation and synchronization) and timing functions to watch fault conditions.

Embedded Operational Channel (EOC) Processor

Two different modes can be selected for maintenance functions: In the Auto mode all EOC procedure handling and executing as specified by ANSI is performed. In the Transparent mode all bits are transferred transparently to the user's interfaces without any internal processing.

See "Embedded Operations Channel (EOC)", page 69 for definition, and "Access to EOC of U-Interface", page 110 for informations about programming and monitoring the EOC.

Single Bits (SB) Processor

The single bits are used mainly to communicate status and maintenance functions between the transceivers. The meaning of a bit position depends upon the direction of transmission (upstream/downstream) and the operation mode (repeater or NT/LT). The SB processor interprets these bits and gives access to some of them according to the mode used. It also provides several filtering methods for SB indications.

See "Single Bits Channel", page 69 for definition, and "Access to the Single Bits of U-Interface", page 115 for informations about programming and monitoring the SB.

Special Functions (SF)

This block provides miscellaneous functions of the SIU, like the power controller function in stand-alone mode, access to internal chip data, test loops control, S/G bit control in µP mode and others. These will be discussed in detail in chapter 4.

Cyclic Redundancy Check (CRC)

The cyclic redundancy check provides a possibility to verify the correct transmission of data. The check sum of a transmitted U-superframe is calculated from the bits in the D-channel, both B-channels, and the M4 bits according to the CRC polynomial

$$G(u) = u^{12} + u^{11} + u^3 + u^2 + u + 1$$

(+ modulo 2 addition)

The check digits (CRC bits CRC1, CRC2, …, CRC12) generated are transmitted at position M5 and M6 in the U-superframe (see "U-Frame Structure", page 68). At the receiving side this value is compared with the value calculated from the received superframe.

In case these values are not identical a CRC-error will be indicated to both sides of the U-interface. In chapter 4.5, page 176, different methods of monitoring transmission quality are discussed in detail.

3.4.2 Receiver

The Receiver block (REC) performs the filter algorithmic functions using digital signal processing techniques. Modules for echo cancellation, pre- and post-equalization, phase adaptation and frame detection are implemented in a modular multi-processor concept.

3.4.3 Line Interface Unit

The Line Interface Unit (LIU) contains the crystal oscillator and all of the analog functions, such as the A/D-converter and the awake unit in the receive path, the pulse-shaping D/A-converter, and the line driver in the transmit path. Furthermore it provides an analog test loop-back function. Refer also to "Analog Characteristics", page 266 for detailed information about the electrical characteristics of the LIU.

Analog-to-Digital Converter

The ADC was especially developed for the IEC-Q. It is a sigma-delta modulator of second order using a clock rate of 15.36-MHz.

The peak input signal measured between AIN and BIN must be below 4 Vpp. In case the signal input is too low (long range), the received signal is amplified internally by 6 dB. The maximum signal to noise ratio is achieved with 1.3 Vpp (long range) and 2.6 Vpp (short range) input signal voltage.

The impedance measured between AIN and BIN is at least 50 kΩ.

Awake Block

The Awake circuit evaluates the differential signal between AIN and BIN. The differential threshold level is between 4 mV and 28 mV. The DC-level (common mode level) may be between 0 V and 3 V. Level detect is not effected by the range setting.

Digital-to-Analog Converter

The output pulse is shaped by a special DAC. The DAC was optimized for excellent matching between positive and negative pulses and high linearity. It uses a fully differential capacitor approach. The staircase-like output signal of the DAC drives the

output buffers. The shape of a DAC-output signal is shown below, the peak amplitude is normalized to one. This signal is fed to an RC-lowpass of first order with a corner frequency of 1 MHz ± 50%.

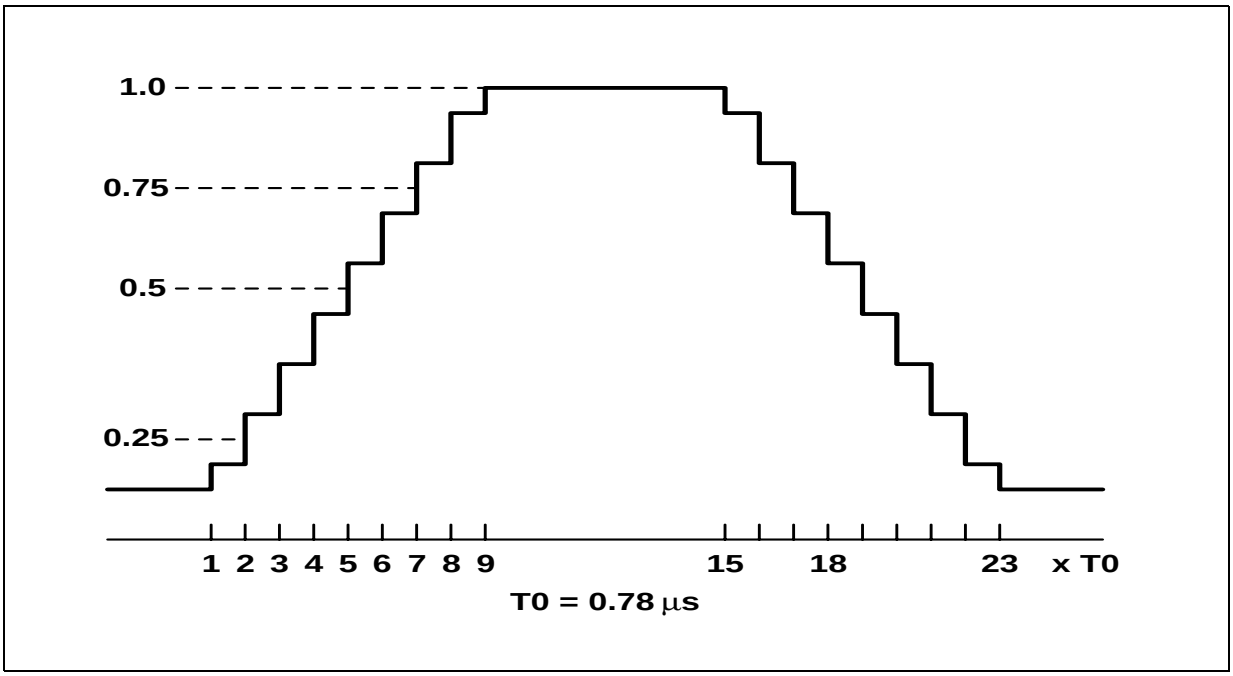


Figure 20 DAC-Output for a Single Pulse

The duration of each pulse is 24 steps, with T0 t = 0.78 µs per step. On the other hand, the pulse rate is 80-kHz or one pulse per 16 steps. Thus, the subsequent pulses are overlapping for a duration of 8 steps.

Line Driver

The Line Driver is optimized for

– High output swing
– High linearity
– Low quiescent current to minimize power consumption

The output jitter produced by the transmitter (with jitter-free input signals) is below 0.02 UIpp (Unit interval = 12.5 µs, peak-peak) measured with a high-pass filter of 30-Hz cutoff frequency. Without the filter the cutoff jitter is below 0.1 UIpp.

Analog Loop-Back Function

An internal analog loop-back function can be activated (see "Analog Loop-Back (No. 1/No. 3)", page 187). This loop-back is closed near the U-interface. If it is active all signals received on AIN / BIN will neither be evaluated nor recognized.

3.5 U-Interface

The IEC-Q interfaces with the metallic line through this block. Both are linked by an external circuitry consisting of a transformer and a hybrid circuitry (refer to Figure 93, page 250 for details).

3.5.1 Output and Input Signals

The output stage comes out of two identical buffers operating in differential mode. This concept allows an output swing of 6.4 Vpp between the output pins AOUT and BOUT of the IEC-Q. The nominal peak values of ± 3 correspond to a 3.2 Vpeak chip output and 2.5 Vpeak on the metallic line.

The input signal from the metallic line is detected on the differential inputs AIN and BIN. The swing of the input signal measured must be below 4 Vpp.

3.5.2 U -Frame Structure

Transmission on the U-interface is performed at a rate of 80 kBaud. The code used is reducing two binary informations to one quaternary symbol (2B1Q).

Data is grouped together into U-superframes of 12 ms each. The beginning of a new superframe is marked with an inverted synchronization word (ISW). Each superframe consists of eight basic frames which begin with a standard synchronization word (SW) and contain 222 bits of information. The structure of one U-superframe is illustrated in Figure 21, and 22. For a detailed description of one complete superframe see Table 10, page 68.

ISW	**1. Basic Frame**	**SW**	**2. Basic Frame**	**. . .**	**SW**	**8. Basic Frame**
<---12 ms--->						

Figure 21 U-Superframe Structure

(I) SW **(Inverted) Synch Word** **18 Bit (9 Quat)**	**12 × 2B + D** **User Data** **216 Bits (108 Quat)**	**M1 – M6** **Maintenance Data** **6 Bits (3 Quat)**
<---1,5 ms--->		

Figure 22 U-Basic Frame Structure

Out of the 222 information bits 216 contain 2B + D user data, the remaining 6 bits are used to transmit maintenance bits. Thus 48 maintenance bits are available per U-superframe. They are used to transmit two EOC-messages (24 bit), 12 overhead bits and one check sum (12 bit).

Table 10 U-Frame Structure

		Framing	2B + D	Overhead Bits (M1 – M6)					
	Quat Positions	1 – 9	10 – 117	118s	118m	119s	119m	120s	120m
	Bit Positions	1 – 18	19 – 234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B + D	M1	M2	M3	M4	M5	M6
1	1	ISW	2B + D	EOCa1	EOCa2	EOCa3	ACT/ ACT	1	1
	2	SW	2B + D	EOC d/m	EOCi1	EOCi2	DEA / PS1	1	FEBE
	3	SW	2B + D	EOCi3	EOCi4	EOCi5	1/ PS2	CRC1	CRC2
	4	SW	2B + D	EOCi6	EOCi7	EOCi8	1/ NTM	CRC3	CRC4
	5	SW	2B + D	EOCa1	EOCa2	EOCa3	1/ CSO	CRC5	CRC6
	6	SW	2B + D	EOC d/m	EOCi1	EOCi2	1	CRC7	CRC8
	7	SW	2B + D	EOCi3	EOCi4	EOCi5	UOA / SAI	CRC9	CRC10
	8	SW	2B + D	EOCi6	EOCi7	EOCi8	AIB / NIB	CRC11	CRC12
2,3…									
						LT to NT dir. >	/	< NT to LT dir.	

– ISW Inverted Synchronization Word (quat): – 3 – 3 + 3 + 3 + 3 – 3 + 3 – 3 – 3
– SW Synchronization Word (quat): + 3 + 3 – 3 – 3 – 3 + 3 – 3 + 3 + 3
– CRC Cyclic Redundancy Check
– EOC Embedded Operation Channel
a = address bit
d/m = data / message bit
i = information (data / message)
– ACT Activation bit ACT = (1) –> Layer 2 ready for communication
– DEA Deactivation bit DEA = (0) –> LT informs NT that it will turn off
– CSO Cold Start Only CSO = (1) –> NT activation with cold start only
– UOA U-Only Activation UOA = (0) –> U-only activated
– SAI S-Activity Indicator SAI = (0) –> S-interface is deactivated
– FEBE Far-end Block Error FEBE = (0) –> Far-end block error occurred
– PS1 Power Status Primary Source PS1 = (1) –> Primary power supply ok
– PS2 Power Status Secondary Source PS2 = (1) –> Secondary power supply ok
– NTM NT Test Mode NTM = (0) –> NT busy in test mode
– AIB Alarm Indication Bit AIB = (0) –> Interruption (according to ANSI)
– NIB Network Indication Bit NIB = (1) –> no function
(reserved for network use)

Embedded Operations Channel (EOC)

EOC-data are available in the U-frame at the positions M1, M2 and M3 thereby permitting the transmission of two complete EOC-messages (2 × 12 bits) within one U-superframe.

The EOC contains an address field, a data/message indicator (d/m) and an eight-bit information field (see Table 10, page 68).

With the address field the destination of the transmitted message/data is defined. Addresses are defined for the NT, 6 repeater stations and broadcasting.

The data/message indicator needs to be set to (1) to indicate that the information field contains a message. If set to (0), numerical data is transferred to the NT. Currently no numerical data transfer to or from the NT is required.

From the 256 codes possible in the information field 64 are reserved for non-standard applications, 64 are reserved for internal network use and eight are defined by ANSI/ETSI for diagnostic and loop-back functions. All remaining 120 free codes are available for future standardization. For information about EOC channel commands and programming refer to "Access to EOC of U-Interface", page 110.

Cyclic Redundancy Check Channel

The check digits (CRC bits CRC1, CRC2, …, CRC12) are transmitted at position M5 and M6 in the U-superframe. This value is compared with the value calculated from the previously received superframe. For more detailed functional information about the CRC feature see "Cyclic Redundancy Check (CRC)", page 64.

Single Bits Channel

The Single Bits in the U-frame are defined to be bits M41 to M48 (eight bits) in addition to the three bits M51, M52 and M61 and the bit FEBE. Bits M41 through M48 will be referred to as M4 bits. The three bits M51, M52 and M61 will be referred to as "Additional Overhead Bits". The single bits are used mainly to communicate status and maintenance functions between the transceivers. The meaning of a bit position depends upon the direction of transmission (upstream/downstream) and the operation mode (repeater or NT/LT). For details about access to these bits, see "Access to the Single Bits of U-Interface", page 115.

3.6 IOM®-2 Interface

The IOM®-2 interface is used to interconnect telecommunication ICs. It provides a symmetrical full-duplex communication link, containing user data, control/programming and status channels. The structure used follows the 2B + 1D-channel structure of ISDN. The ISDN user data rate of 144 kbit/s (B1 + B2 + D) is transmitted in both directions over the interface.

The IOM®-2 interface is a generalization and enhancement of the IOM®-1 interface.

3.6.1 IOM®-2 Frame Structure

The IOM®-2 interface comprises two clock lines for synchronization and two data lines.

Data is carried over Data Upstream (DU) and Data Downstream (DD) signals. The downstream and upstream direction are always defined with respect to the exchange. Downstream refers to information flow from the exchange to the subscriber and upstream vice versa respectively. The IOM®-2 Interface Specification describes open drain data lines with external pull-up resistors. However, if operation is logically point-to-point, tristate operation is possible as well. For IOM®-2 mode setting refer to "Setting Operating Modes", page 50.

The data is clocked by a Data Clock (DCL) that operates at twice the data rate.

Note 7: This is the default setting. If the microprocessor mode and the master mode are being used, DCL frequency can be set to the bit data rate, see "Setting IOM®-2 Bit Clock Mode", page 56 for details. This section will deal with the default setting. Nevertheless, it applies to the bit clock mode as well if DCL frequencies are adjusted.

Frames are delimited by an 8-kHz Frame Synchronization Clock (FSC). Incoming data is sampled on every second falling edge of the DCL clock.

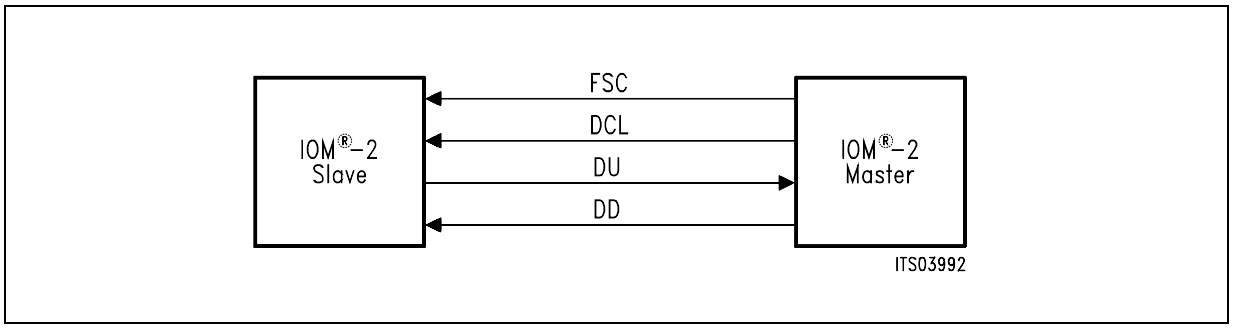


Figure 23 IOM®-2 Clocks and Data Lines

Note 8: A device with an IOM®-2 interface is said to be in the 'IOM®-2 Master Mode' or sometimes just 'Master Mode' if the IOM®-2 clocks FSC and DCL are delivered by this device. It is said to be in the 'IOM®-2 Slave Mode' or sometimes just 'Slave Mode' if the IOM®-2 Clocks are input to this device.

Within one FSC-period, 32 bit up to 256 bit are transmitted, corresponding to DCL-frequencies ranging from 512 kHz up to 4096 kHz.

Three optimized IOM®-2 timing modes exist for:

Multiplexed Timing Mode[1)] (LT and NT-PBX)

Plain Timing Mode (NT, NT-Auto Activation, COT-512, NT-RP and LT-RP)

Terminal Timing Mode (TE and COT1536)

All applications utilize the same basic frame and clocking structure, but differ in the number and usage of the individual channels.

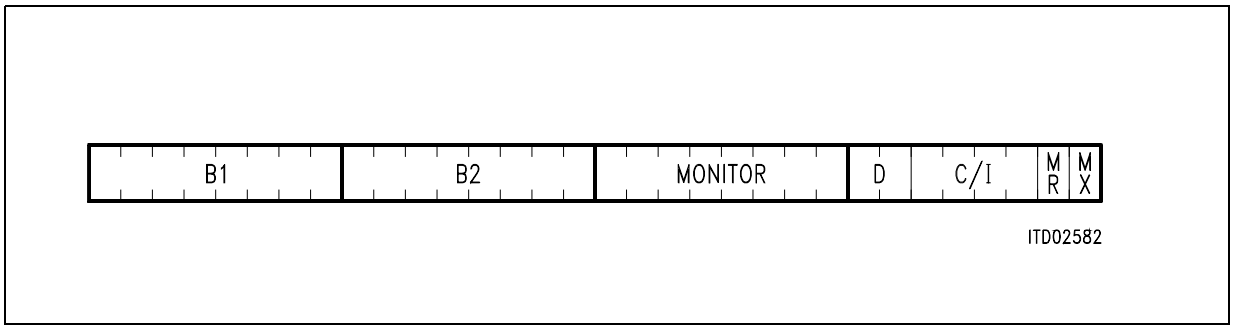


Figure 24 Basic Channel Structure of IOM®-2

Each frame consists of

- two 64 kbit/s channels B1 and B2
- the Monitor Channel for transferring maintenance information
- two bits for the 16 kbit/s D-channel
- four command/indication (C/I) bits for controlling of layer-1 functions (activation/deactivation and other control function) by i.e., layer-2 controller.
- two bits MR and MX for the handshake procedure in the Monitor Channel

3.6.1.1 Multiplexed Timing Mode

Note 9: This section applies to the LT and the NT-PBX modes.

In multiplexed timing mode the IEC-Q supports bit rates from 256 kbit/s up to 2048 kbit/s corresponding to DCL-frequencies from 512 kHz up to 4096 kHz.

The typical IOM®-2 line card or NT-PBX application comprises a DCL-frequency of 4096 kHz with a nominal bit rate of 2048 kbit/s. Therefore eight channels are available, each consisting of the basic frame with a nominal data rate of 256 kbit/s. In LT mode the downstream data (DD) are transferred on pin DIN, the upstream data (DU) on pin DOUT. In NT-PBX mode the downstream data (DD) are transferred on pin DOUT, the upstream

1) This mode is also referred to as "Burst Mode"

data (DU) on pin DIN. The IEC-Q is assigned to an individual channel by pin strapping (see "Setting Operating Modes", page 50).

Note 10: This assigned channel is called the 'active channel' of the IEC-Q. All other channels, if available, are called the 'passive channels' of the IEC-Q.

The IOM®-2 signals are:

DIN, DOUT	256 to 2048 kbit/s
DCL	512 to 4096 kHz, input
FSC	8 kHz, input

I

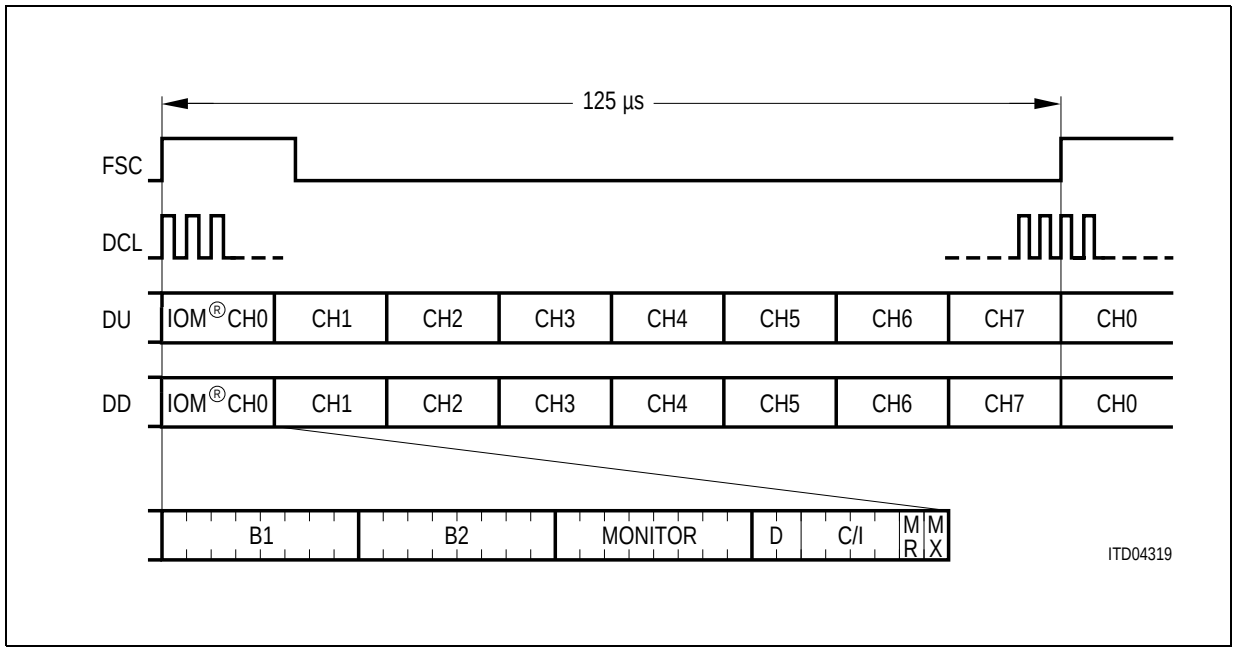


Figure 25 Multiplexed Frame Structure of the IOM®-2 Interface

3.6.1.2 Plain Timing Mode

Note 11: This timing applies to the NT, NT-Auto Activation, COT-512, LT-RP and NT-RP modes.

Note 12: Note also that the multiplexed mode timing described in 3.6.1.1 will reduce to this timing if the bit rate 256 kbit/s is chosen. In this mode there is therefore only one active IOM®-2 channel. No passive IOM®-2 channels are available.

In this timing mode the IEC-Q provides a data clock DCL with a frequency of 512 kHz. As a consequence the IOM®-2 interface provides only one channel with a nominal data rate of 256 kbit/s.

The IOM®-2 signals are:

DIN, DOUT	256 kbit/s
DCL	512 kHz
FSC	8 kHz

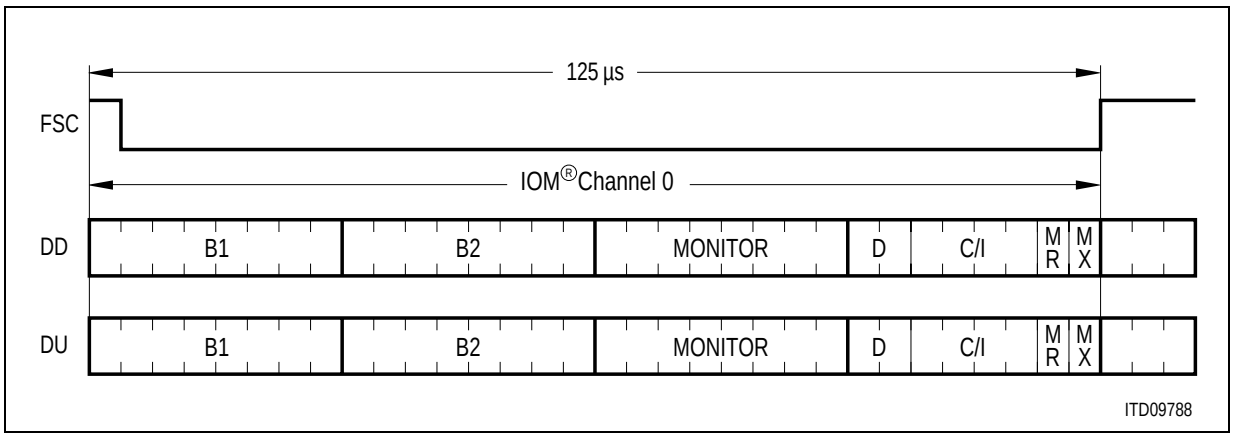


Figure 26 Plain Frame Structure of the IOM®-2 Interface

3.6.1.3 Terminal Timing Mode

Note 13: This timing applies to the TE and the COT-1536 modes.

In the terminal timing mode the IEC-Q provides a data clock DCL with a frequency of 1536 kHz. As a consequence the IOM®-2 interface provides three channels each with a nominal data rate of 256 kbit/s.

- Channel 0 contains 144 kbit/s (for 2B+D) plus Monitor and Command/Indication channels for the layer-1 device.
- Channel 1 contains two 64-kbit/s intercommunication channels plus Monitor and Command/Indication channels for other IOM®-2 devices.
- Channel 2 is used for IOM®-2 bus arbitration (access to the TIC bus). Only the Command/Indication bits are used in channel 2.

Note 14: Channels 1 and 2 can be used only in the TE mode. The description above for these two channels doesn't apply to the COT-1536 mode.

Note 15: Channel 0 is called the 'active channel' of the IEC-Q. Channels 1 and 2 are called the 'passive channels' of the IEC-Q.

The IOM®-2 signals are:

DIN, DOUT	768 kbit/s
DCL	1536 kHz output
FSC	8 kHz output

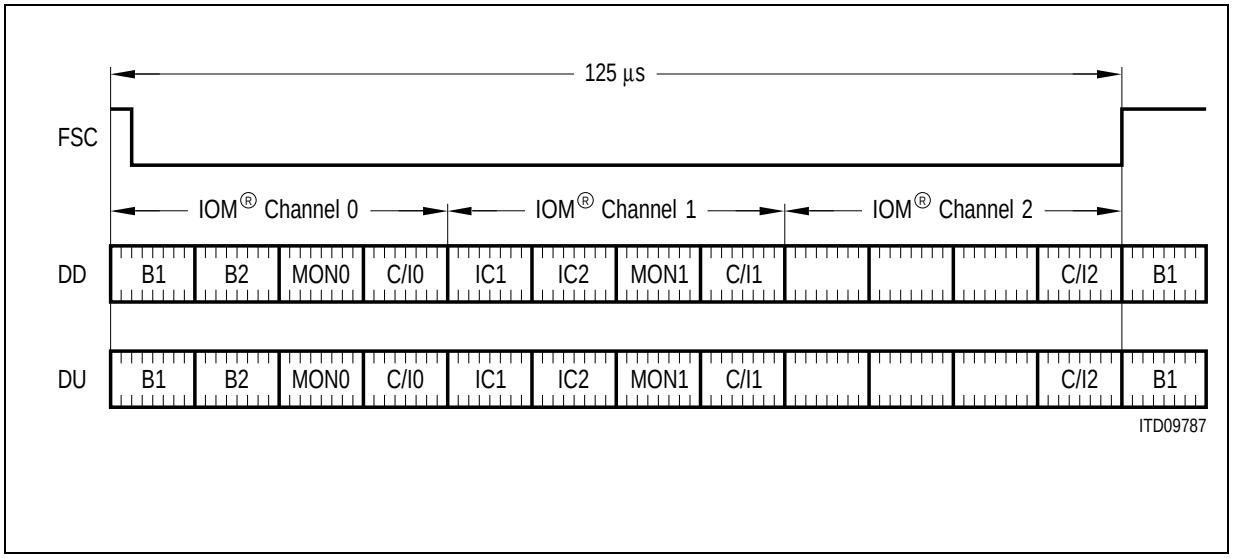


Figure 27 Terminal Frame Structure of the IOM®-2 Interface

– **C/I0 in IOM®-2 Channel 0:**

DU / DD	D	D	C/I4	C/I3	C/I2	C/I1	MR	MX

D: two bits for the 16 kbit/s D-channel

C/I: The four command/indication (C/I) bits are used for control of the U transceiver (activation/deactivation and additional control functions).

MR, **MX:** two bits MR and MX for the handshake in the Monitor Channel 0

– **C/I1 in IOM®-2 Channel 1:**

DU / DD	C/I6	C/I5	C/I4	C/I3	C/I2	C/I1	MR	MX

C/I1 to C/I6 are used for control of a transceiver or an other device in IOM®-2 channel 1 (activation/deactivation and additional control functions).

MR, **MX:** two bits MR and MX for handshake in the Monitor Channel 1

– **C/I2 in IOM®-2 Channel 2:**

E: D-echo bits

BAC-bit (Bus ACcessed). When the TIC bus is occupied the BAC-bit is low.

DU	1	1	BAC	TBA2	TBA1	TBA0	1	1
DD	E	E	S/G	A/B	1	1	1	1

S/G-bit (Stop/Go), available to a connected HDLC controller to determine if it can access the D-channel (S/G = 1: stop, S/G = 0: go).

A/B-bit (available/blocked), supplementary bit for D-channel control. (A/B = 1: D-channel available, A/B = 0: D-channel blocked).

TBA0-2: TIC Bus Address

3.6.2 IOM®-2 Command / Indication Channels

The Command/Indication channels carry real-time control and status information over the IOM®-2 interface.

3.6.2.1 Active C/I Channel

The active C/I Channel of the IEC-Q is available in all operational modes. The channel consists of four bits in each direction. Activation and deactivation of the IEC-Q is always controlled via the active C/I Channel. The C/I codes going to the IEC-Q are called ’commands’, those originating from it are referred to as ’indications’.

The IEC-Q verifies C/I commands with a double last-look criterion, i.e. a new command will be recognized as valid only after it has been correctly detected by the IEC-Q for two consecutive IOM®-2 frames.

If the microprocessor interface is not being used for controlling the C/I Channel, commands have to be applied continuously on DIN until the command is validated by the IEC-Q and the desired action has been initiated. Afterwards the command may be changed which would initiate another action by the IEC-Q. An indication is issued permanently by the IEC-Q on DOUT until a new indication needs to be forwarded.

In stand-alone mode the active C/I Channel is controlled by an external device, e.g. the ICC, 3PAC, IPAC or ISAR, EPIC®, ELIC®.

In µP mode the active C/I Channel can either be controlled by an external device or via the microprocessor interface. For a description on how to access the active C/I Channel via the µP-interface please refer to chapter "Microprocessor Access to IOM®-2 Channels", page 97.

All available C/I codes of the IEC-Q are listed and explained in "C/I Channel Codes", page 224.

3.6.2.2 C/I Channel 1

C/I Channel 1 (C/I1) is only available in TE mode (DCL = 1.536 MHz). The channel consists of six bits in each direction.

In stand-alone mode the C/I1 channel is ignored by the U transceiver.

In µP mode it can be accessed via registers CIWI/U and CIRI/U (see "C/I Channel Access", page 100).

3.6.3 IOM®-2 Monitor Channel

The Monitor Channel protocol is a full duplex handshake protocol used for programming and monitoring devices in the active Monitor Channel or on Monitor Channel 1 in the TE mode. These can include the IEC-Q itself as well as external devices connected to the IOM®-2 interface.

The Monitor Channel consists of 8 bits, located at position 17-24 of every time slot. For handshake control bits MR and MX at positions 31 and 32 of every time slot are used (see Figure 24, page 71).

3.6.3.1 Active Monitor Channel

The active Monitor Channel is available in all operational modes. The IEC-Q is always controlled and monitored via active Monitor Channel.

In stand-alone mode the Monitor Channel is controlled by an external device, e.g. the ICC, 3PAC, IPAC or ISAR, EPIC®, ELIC®.

In µP mode the Monitor Channel can either be controlled by an external device or via the microprocessor interface. For a description on how to access the active Monitor Channel via the µP-interface please refer to "Monitor Channel Access", page 101.

Structure of Monitor messages

Monitor messages sent to the IEC-Q are always 2 bytes long, monitor messages returned by the IEC-Q are 2 or 4 bytes long depending on the command. 4 byte long return messages (internal register data) are issued via 2 messages containing 2 bytes each. Table 11 below shows the general structure of 2 bytes monitor messages.

Table 11 General Monitor Channel Structure

1. Byte		2. Byte	
A3 A2 A1 A0	D11 D10 D9 D8	D7 D6 D5 D4	D3 D2 D1 D0
Address	Data	Data	data

The first four bits of this two byte message gives the address of the Monitor message. This address defines the type of the Monitor message.

Example: A Monitor message with an address '0_H', i.e. Address= '0000' will be called MON-0 message. A Monitor message with an address '8_H', i.e. Address= '1000' will be called MON-8 message.

The IEC-Q will respond only to MON-0, MON-1, MON-2 and MON-8 messages in the active channel. All other messages will be ignored.

The 12 Bits D0-D11 of a Monitor message will have different meanings, depending on message type and on the function used. An overview of Monitor Channel commands and indications of the IEC-Q are listed in section 6.2, page 226.

Priority

In the receive direction Monitor Channel commands (given to the IEC-Q) will be handled sequentially.

In the transmit direction messages will be handled according to the following priority if several of them are pending (to be issued by the IEC-Q):
MON-0 will have the first priority and will be therefore issued first. MON-1 will have the second, MON-2 the third and MON-8 the last priority. However, an already running message will not be aborted, even if a higher priority message is pending.

Verification

The monitor message on DIN is considered valid only if it consists of exactly two bytes. Longer messages or single-byte messages will be discarded.

A double last-look criterion is implemented for both bytes of the monitor message. If the received bytes are not identical in the first two received frames the message will be aborted.

Handshake Procedure

Figure 28 illustrates a Monitor Channel transfer of a 2-byte monitor command followed by a 2-byte IEC-Q-response. This requires a minimum of 15 IOM®-2 frames (reception 7 frames + transmission 8 frames = 1.875 ms). In case the controller is able to confirm the receipt of first IEC-Q-response byte in the frame immediately following the MX-transition on DOUT from high to low (i.e. in frame No. 9), 1 byte may be saved[1)] (7 frames + 7 frames).

Note 16: Transmission and reception of monitor messages can be performed simultaneously by the IEC-Q. In the procedure depicted in figure 28 it would be possible for the IEC-Q to transmit monitor data in frames 1–5 (excluding EOM-indication) and receive monitor data from frame 8 onwards.

1) This is referred to as the "fast handshake"

M 1/2:Monitor message 1. and 2. byte
R 1/2:Monitor response 1. and 2. byte
EOM:End of message: MX=’1’ and MR=’1’ in two consecutive IOM®-2-Frames.

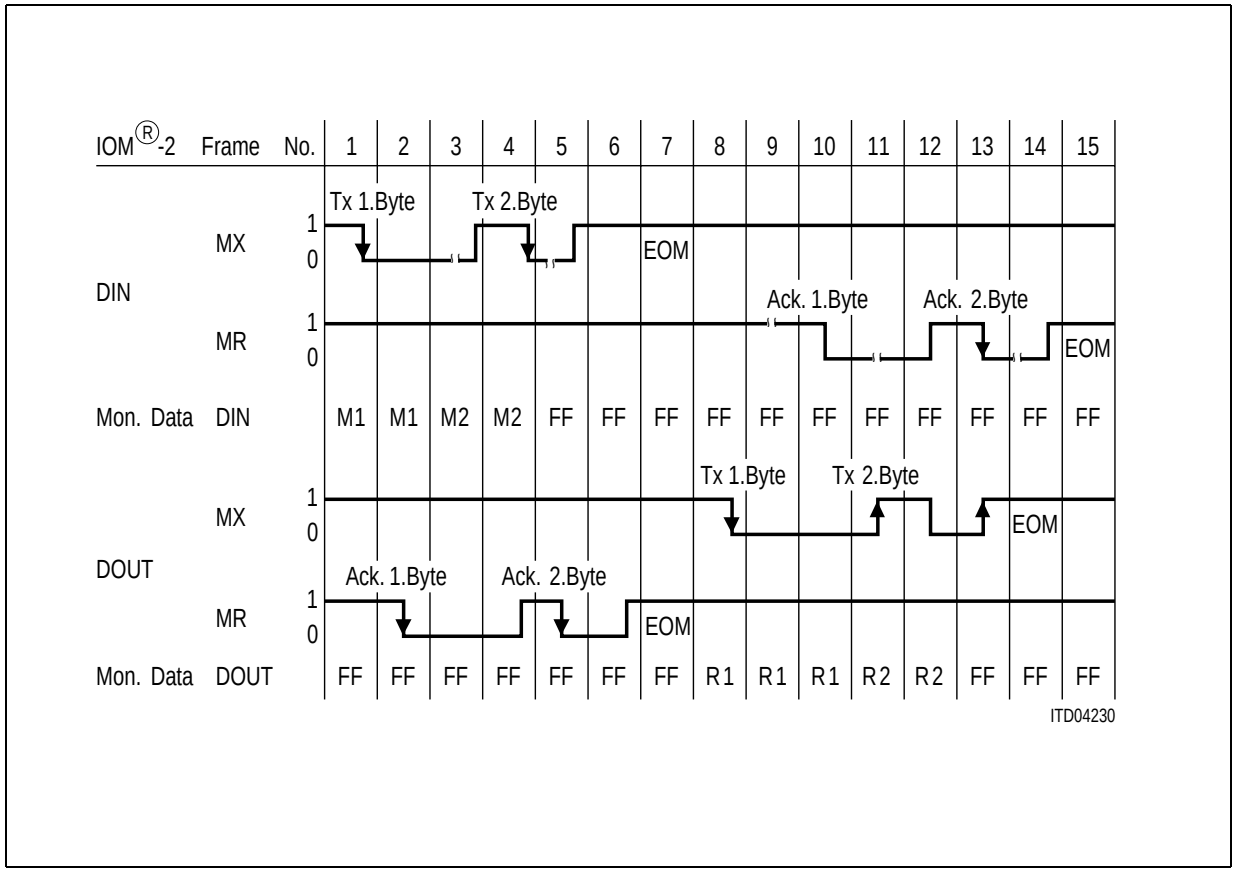


Figure 28 Handshake Protocol with a 2-Byte Monitor Message/Response

Idle State

After the bits MR and MX have been held inactive (i.e. high) for two or more successive IOM®-2-frames, the channel is considered idle in this direction.

Transmission Abortion

If no EOM is detected after the first two monitor bytes, or received bytes are not identical in the first two received frames, transmission will be aborted through receiver by setting the MR-bit inactive for two or more IOM®-2-frames. The controller reacts with EOM. This situation is illustrated in figure 29 below.

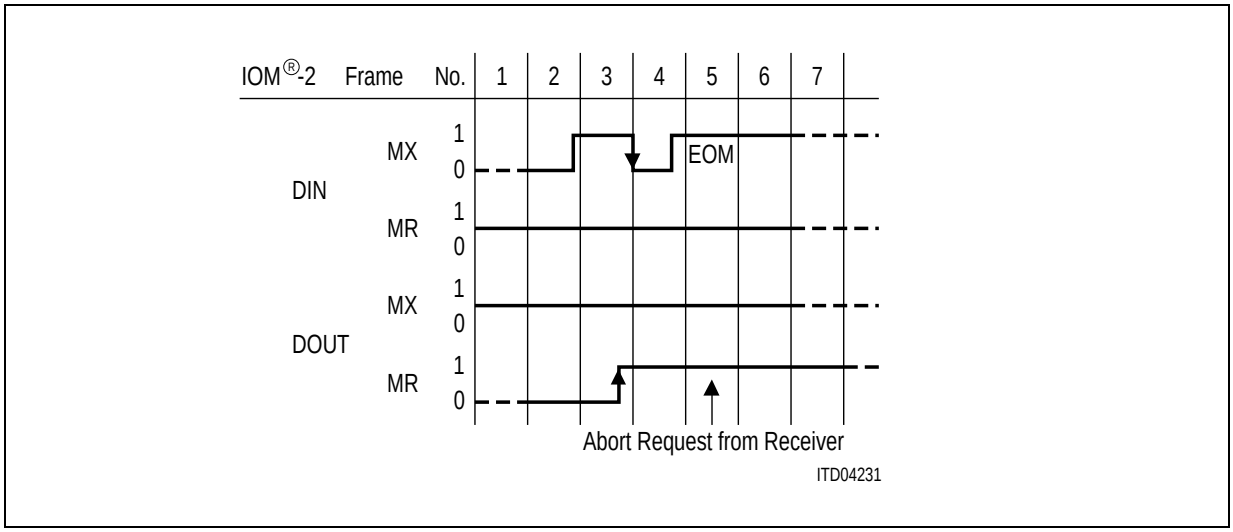


Figure 29 Abortion of Monitor Channel Transmission

Example: Standard Transmission Procedure in stand-alone mode

1. The first byte of monitor data is placed by the external controller (e.g. ICC, EPIC®) on the DIN line of the IEC-Q and MX is activated (low; frame No. 1).
2. The IEC-Q reads the data of the Monitor Channel and acknowledges by setting the MR-bit of DOUT active if the transmitted bytes are identical in two received frames (frame No. 2 because the IEC-Q reads and compares data already while the MX-bit is not activated).
3. The second byte of monitor data is placed by the controller on DIN and the MX-bit is set inactive for one single IOM®-2-frame. This is performed at a time convenient to the controller.
4. The IEC-Q reads the new data byte in the Monitor Channel after the rising edge of MX has been detected. In the frame immediately following the MX-transition active-to-inactive, the MR-bit of DOUT is set inactive. The MR-transition inactive-to-active exactly one IOM®-2-frame later is regarded as acknowledgment by the external controller (frame No. 4–5).
   The acknowledgment by the IEC-Q will always be sent two IOM®-2-frames after the activation of a new data byte.
5. After both monitor data bytes have been transferred to the IEC-Q, the controller transmits "End Of Message" (EOM) by setting the MX-bit inactive for two or more IOM®-2-frames (frame No. 5–6).
6. In the frame following the transition of the MX-bit from active to inactive, the IEC-Q sets the MR-bit inactive (as was the case in step 4). As it detects EOM, it keeps the MR-bit inactive (frame No. 6). The transmission of the monitor command by the controller is complete.
7. If the IEC-Q is requested to return an answer it will commence with the response as soon as possible. In case the "monitor time-out" function is enabled it may have to

postpone the answer until after the internal reset, see "Monitor Procedure Time-Out (MTO)", page 55. Figure 28, page 78 illustrates the case where the response can be sent immediately.
The procedure for the response is similar to that described in points 1 – 6 except for the transmission direction. It is assumed that the controller does not latch monitor data. For this reason one additional frame will be required for acknowledgment.
Transmission of the 2nd monitor byte will be started by the IEC-Q in the frame immediately following the acknowledgment of the first byte. The IEC-Q does not delay the monitor transfer.

3.6.3.2 Monitor Channel 1

Monitor Channel 1 is only available in TE mode (DCL = 1.536 MHz).

In stand-alone mode the Monitor 1 channel is ignored by the IEC-Q.

In µP mode it can be accessed via the microprocessor interface to control an external device (e.g. SICOFI®, ARCOFI®). For a detailed description of the microprocessor interface access to the Monitor Channel see "Monitor Channel Access", page 101.

3.6.3.3 Monitor Procedure Time-Out

Note 17: This feature is only available for the active Monitor Channel, see "Active Monitor Channel", page 76.

The IEC-Q can operate with or without the "Monitor Procedure Time-out" feature. For mode setting see "Monitor Procedure Time-Out (MTO)", page 55.

With the MTO-function enabled, the monitor routine is reset twice per U-superframe (see "U -Frame Structure", page 67 for definition). The resets are performed at the start of the first and 49th IOM®-2-frame (see Figure 30). Every reset sets both handshake bits of DOUT to the idle state (MR and MX set to high) thereby preventing lock-up situations. Monitor Channel transmitter and receiver are reset synchronously.

With the MTO-function disabled no internal resets are performed. This eliminates the restrictions described in the following paragraphs, requires however an external controller to prevent lock-up situations in the Monitor Channel.

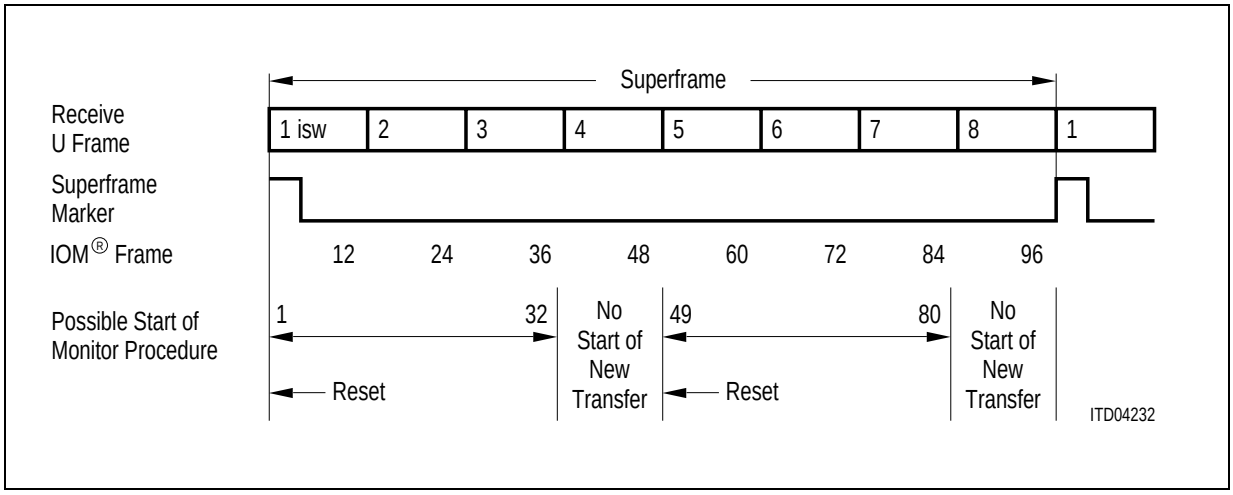


Figure 30 Monitor Access with MTO Enabled

Monitor Channel Transmitter and MTO Enabled

The transmitter is reset in 6 ms intervals in the frames shown above. In case the transmission of a monitor message has not been completed before the transmitter is reset, the complete message will be lost. A message that has been lost due to the interruption of a monitor reset will not be retransmitted.

To prevent this loss of monitor messages, the IEC-Q will only commence a monitor transmission if more than 16 IOM®-2 frames will be available for transmission before the next reset occurs. Transmission thus does not start during frame numbers 33 … 48 and 81 … 96. To ensure correct transmission the receiver must not delay the receive procedure for more than the following value:

- 2-byte transmission: max. speed = 8 frames => max. controller (receive) delay = 8 frames.

Monitor Channel Receiver and MTO Enabled

The receiver is reset in 6 ms intervals in the frames shown above. In case the reception of a monitor message has not been completed before the receiver is reset, the complete message can be lost because the generation of an abort request can not be guaranteed.

To prevent this loss of monitor messages the PEB 2091 will only commence a monitor reception (i.e. acknowledge the 1st received byte) if more than 16 IOM®-2 frames will be available for reception before the next reset occurs. Reception thus does not start during frame numbers 33 … 48 and 81 … 96. To ensure correct reception, the transmitter must not delay the receive procedure for more than the following value:

- 2-byte reception: max. speed = 7 frames => max. controller (transmit) delay = 9 frames.

3.6.4 Activation/Deactivation of IOM®-2 Clocks

Note 18: This section applies only in the NT, NT-Auto Activation, NT-RP and TE modes.

The IOM®-2 clocks may be switched off if the IEC-Q is in state 'Deactivated' (see "State Machine in NT Modes", page 160). This reduces power consumption to a minimum. In this deactivated state the clock lines are low and the data lines are high. The power-down condition within the 'Deactivated' state will only be entered if no Monitor messages are pending on IOM®-2.

For information on how to keep the IOM®-2 clocks active in all states please refer to the application note 'Providing Clocks in Deactivated State'.

The deactivation procedure is shown in Figure 31. After detecting the code DI (Deactivation Indication) the IEC-Q responds by transmitting DC (Deactivation Confirmation) during subsequent frames and stops the timing signals after the fourth frame.

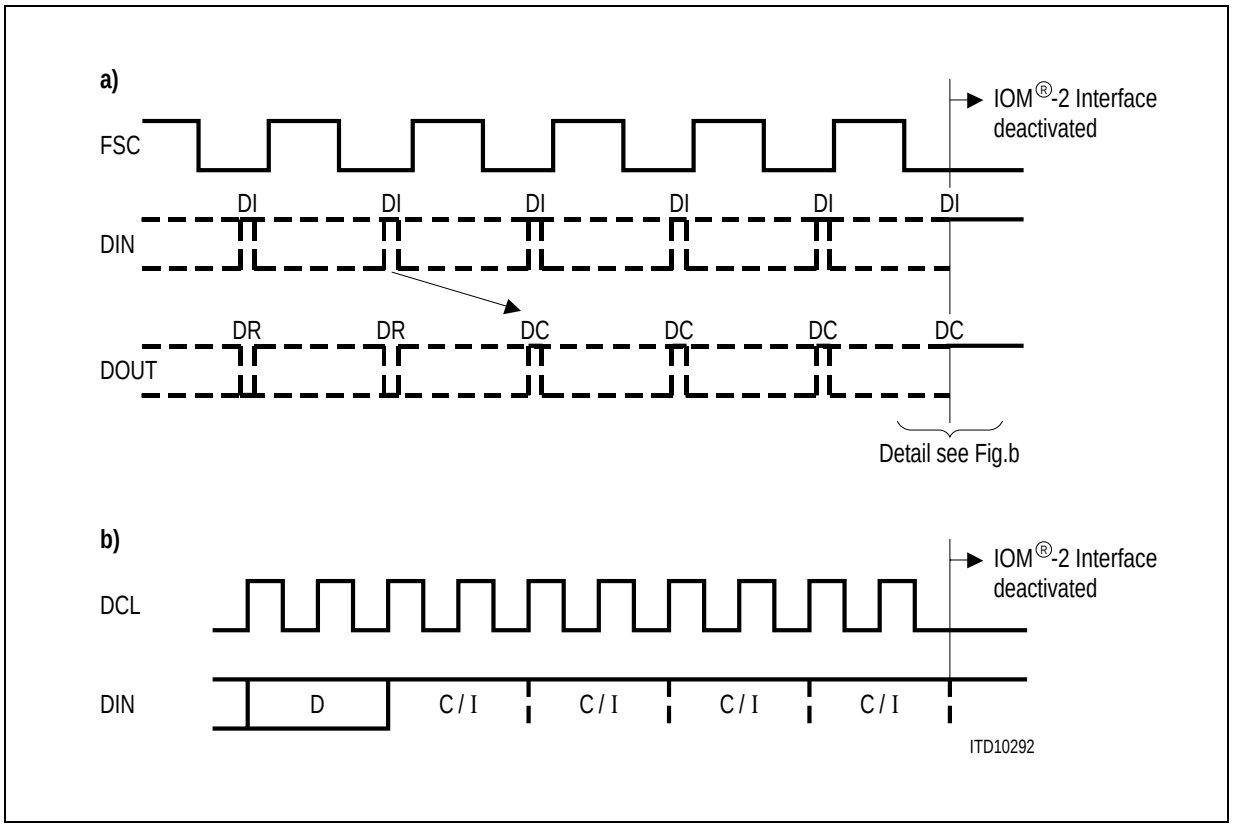


Figure 31 Deactivation of the IOM®-2 Clocks

The IOM®-2 clocks are activated automatically when one of the following conditions apply

- the DIN line is pulled low

- the bit CIWU:SPU is set to ’0’ or
- a wake-up tone is detected on the U-interface

DCL is activated such that its first rising edge occurs with the beginning of the bit following the C/I0 channel. After the clocks have been enabled this is indicated by the PU code in the C/I0 channel.

For detailed operational description, see "State Machine in NT Modes", page 160 ff.

3.7 Clocks

Clock generation of the IEC-Q depends on the mode used. The following sections will describe the properties of these clocks in each mode. For better understanding of the clock scheme in the different applications the properties of the IOM®-2 clocks will also be outlined.

3.7.1 LT Mode

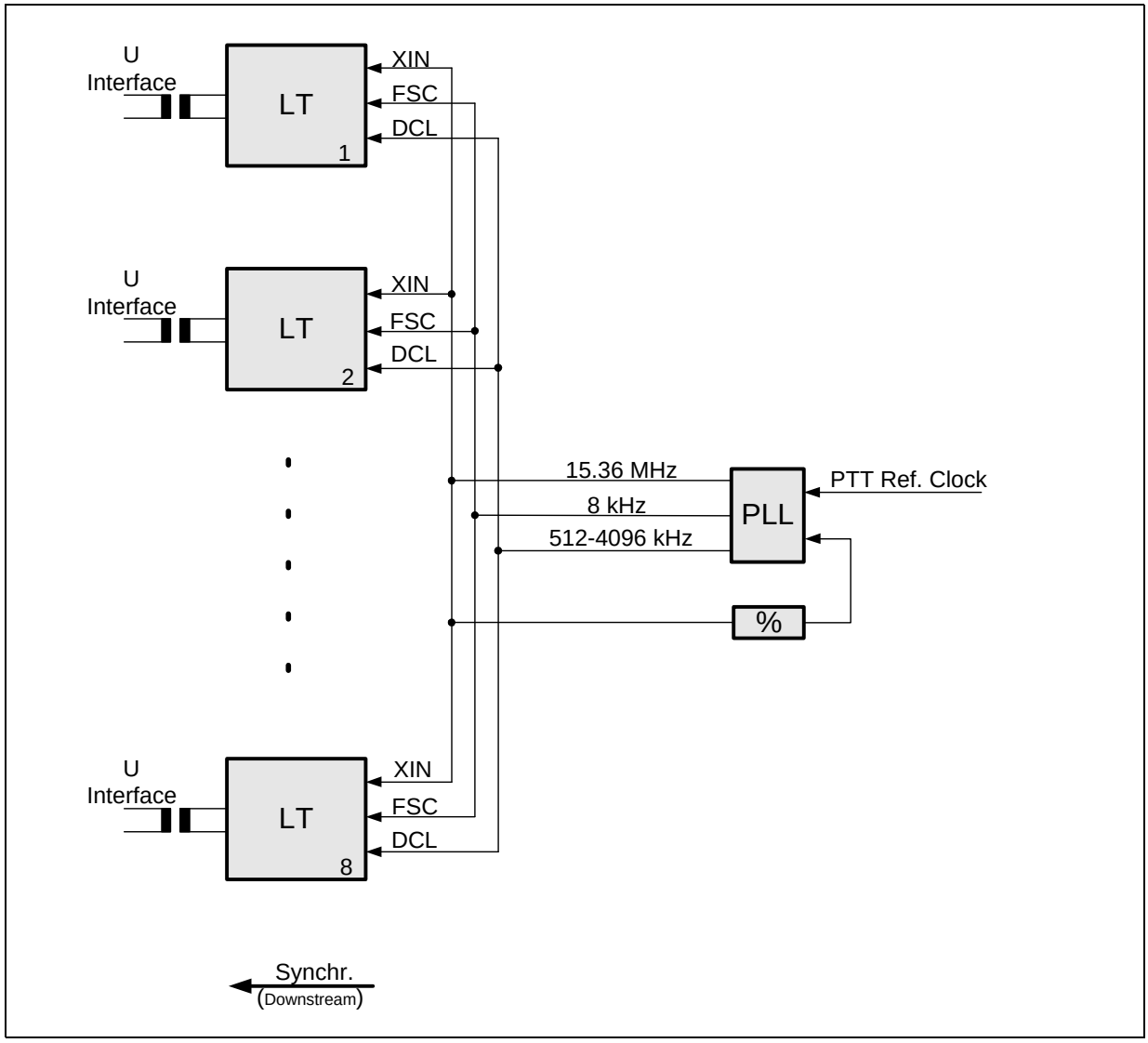


Figure 32 Clock Generation for LT Mode

The LT mode is typically chosen for ISDN-line card applications. The U transceiver has to synchronize onto an externally provided PTT-master clock. A phase locked loop (PLL) is required to generate the IOM®-2 clock signals FSC (Frame Synchronization) and DCL (Data Clock) as well as the 15.36 MHz IEC-Q master clock.

XIN/XOUT

Pin XOUT should be left open.

The synchronized 15.36 MHz clock should be provided on pin XIN. A synchronized IEC-Q system clock guarantees that U-interface transmission will be synchronous to the PTT-master clock.

The dynamic characteristics of this clock are described in "LT Modes", page 281.

Clock CLS

This clock is not defined in this mode.

3.7.2 NT and TE Mode

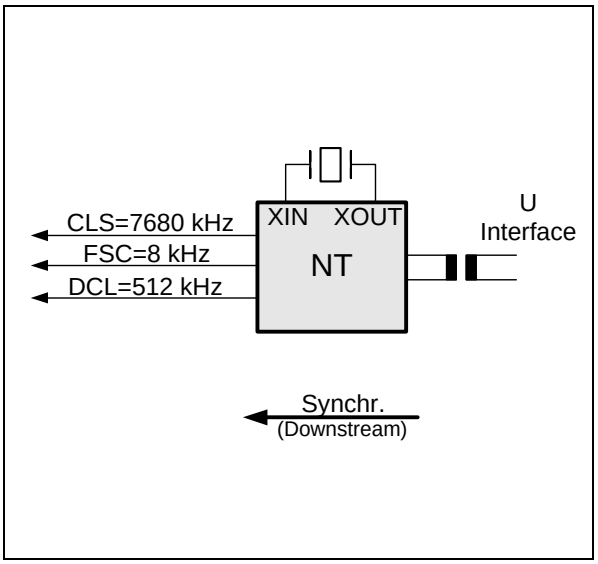


Figure 33 Clock in NT Mode

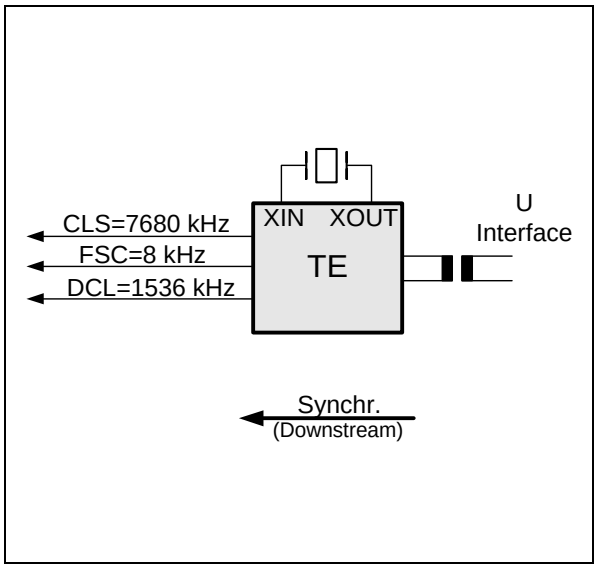


Figure 33 Clocks in TE Mode

In NT and TE modes the IEC-Q recovers the timing directly from the U-interface. Synchronization to the U-interface is achieved by including correction steps in the divider of the 15.36-MHz base clock. Thus the issued IOM®-2 clock signals are synchronous to the PTT-master clock on LT side.

XIN/XOUT

A free running crystal or other clock source should provide a 15.36-MHz base clock (see also “External Circuitry” on page 249 for more informations about crystal properties).

CLS Clock

In these modes the IEC-Q issues a 7.68-MHz clock signal. This clock signal is synchronous to the received U-interface signal. In order to achieve synchronism the free running 15.36-MHz master clock is not permanently divided by 2. Adjustment steps are included by division with 1 or 3. It is not available in power down.

3.7.3 NT-PBX

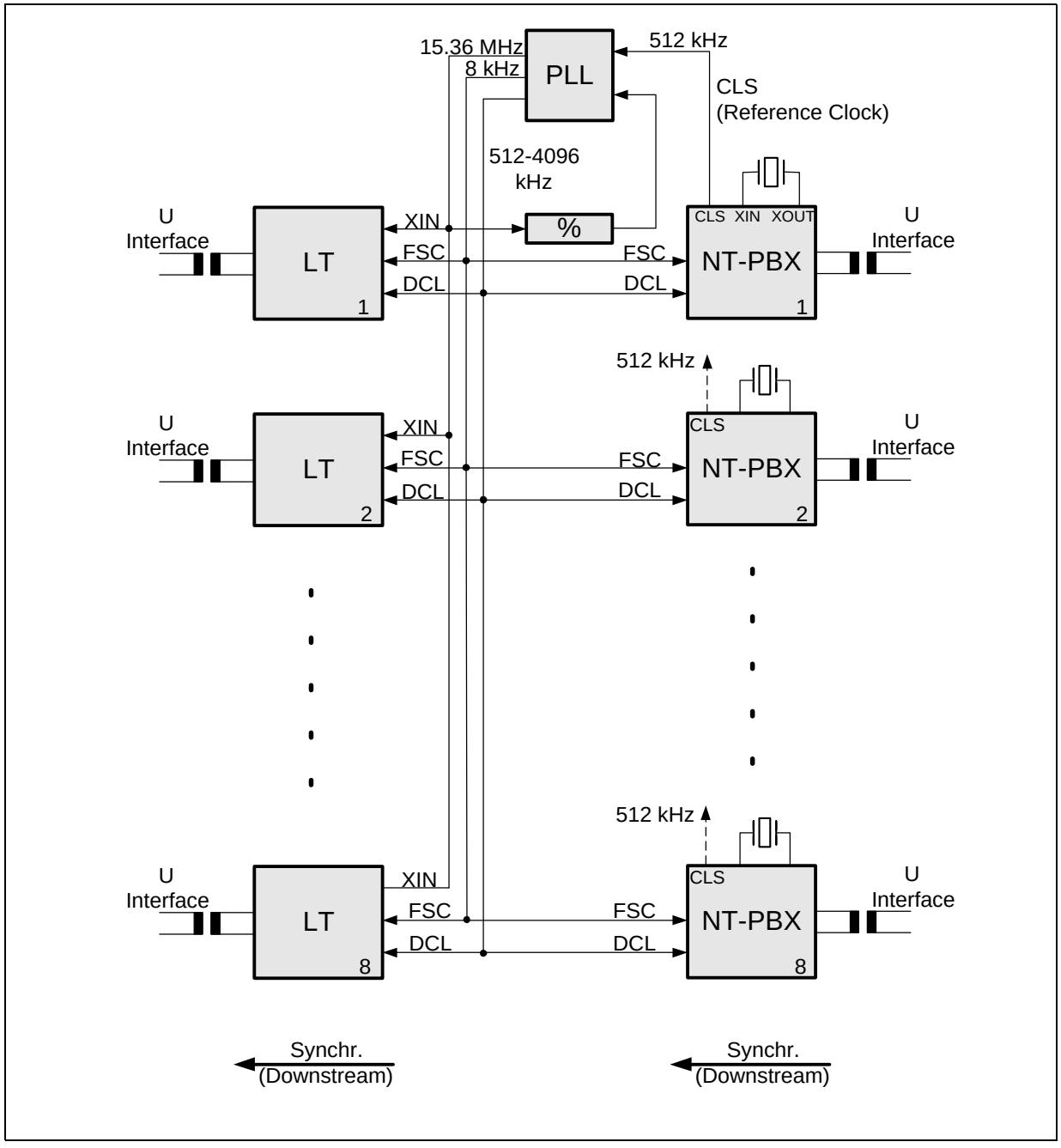


Figure 34 Clock Generation in NT-PBX Mode

In NT-PBX mode IOM®-2 clock signals are not issued by the device but need to be generated externally. In order to ensure synchronous timing to the PTT-master clock, a PLL is used for generation of FSC and DCL (supplied to NT-PBX and LT devices) as well as of the 15.36-MHz system clock (LT only).

Note 19: It may be necessary to use a multiplexer for the PLL-reference clock because the CLS-signal is available only if the corresponding line is active. If the referenced line is not active the PLL must be supplied by the CLS of another active IEC-Q of the PBX.

XIN/XOUT

A free running crystal or other clock source should provide a 15.36-MHz base clock (see also "External Circuitry", page 249 for more informations about crystal properties).

CLS

A 512 kHz clock synchronous to the PTT is provided. This clock should be used as the reference clock for the PLL. It is not available in power down.

3.7.4 Repeater Modes

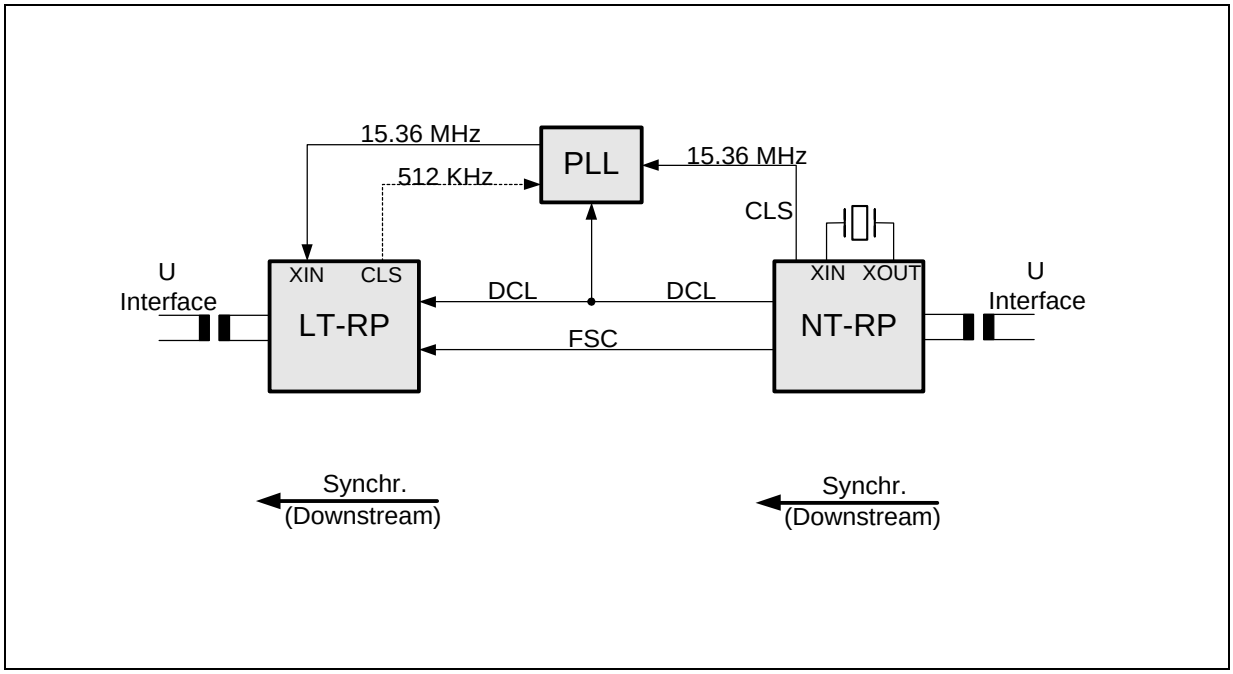


Figure 35 Clock Generation in Repeater Mode

In repeater applications the NT repeater issues IOM®-2 clocks for direct use in the LT repeater. The LT repeater is synchronized to the upstream unit through the NT repeater. To achieve this, a PLL is required to provide a synchronized 15.36 MHz master clock to the LT repeater.

3.7.4.1 NT Repeater

XIN/XOUT

A free running crystal or other clock source shall provide a 15.36-MHz base clock (see also "External Circuitry", page 249 for more informations about crystal properties).

CLS

In this mode version 5.3 provides an unsychronized 15.36 MHz clock on CLS. This clock can be used by the PLL as a base clock. It is also available in power down.

3.7.4.2 LT Repeater

XIN/XOUT

Pin XOUT should be left open.

The synchronized 15.36 MHz clock should be provided on pin XIN.

The dynamic characteristics of this clock are described in "LT Modes", page 281.

Clock CLS

In this mode a 512 kHz clock is provided on CLS. This clock signal is not synchronous to the received U-interface signal. It is also available in power down.

3.7.5 COT-512 and COT-1536 Mode

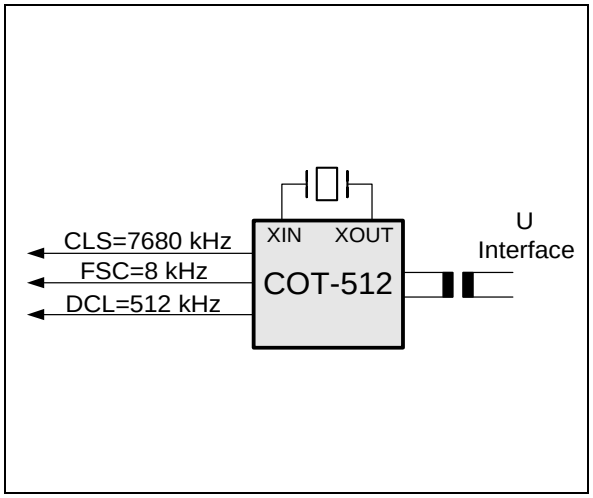


Figure 36 Clocks in COT-512 Mode

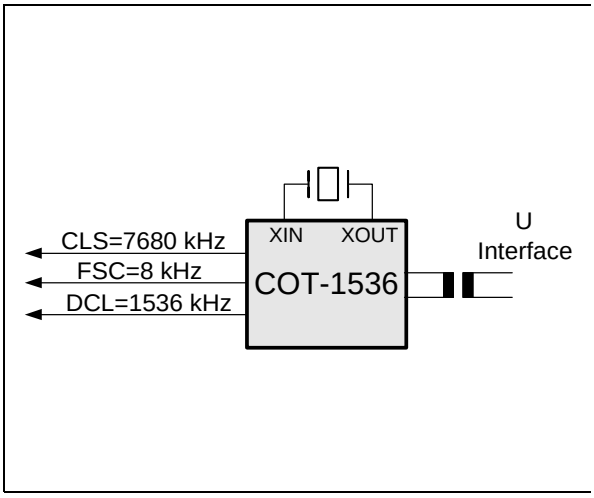


Figure 36 Clocks in COT-1536 Mode

Because pair gain systems do not need to synchronize onto a PTT-master clock, a free running 15.36-MHz system clock may be used at the exchange side. In COT mode the

IEC-Q issues all IOM®-2 clocks. An external clock generation circuit is not required. Information on the U-interface is transmitted synchronous to the system clock.

XIN/XOUT

A free running crystal or other clock source should provide a 15.36-MHz base clock (see also “External Circuitry” on page 249 for more informations about crystal properties).

CLS Clock

In these modes the IEC-Q issues a 7.68-MHz clock signal. This clock signal is not synchronous to the received U-interface signal. It is also available in power down.

3.7.6 Microprocessor Clock Output

Note 20: This clock is only available in the µP mode.

The microprocessor clock on the MCLK-output. Four clock rates are provided by a programmable prescaler in the ADF register (see "ADF-Register", page 219). These are 7.68 MHz, 3.84 MHz, 1.92 MHz and 0.96 MHz. The default value after reset is 3.84 MHz. Switching between the clock rates is realized without spikes. The oscillator remains active all the time. The clock is synchronized to the 15.36 MHz clock at the XIN pin.

3.8 Microprocessor Interface

Note 21: This Interface is only available in the microprocessor mode.

The parallel/serial microprocessor interface can be selected to be either of the

1. Siemens/Intel non-multiplexed bus type with control signals $\overline{CS}$, $\overline{WR}$, $\overline{RD}$
2. Motorola type with control signals $\overline{CS}$, R/$\overline{W}$, $\overline{DS}$
3. Siemens/Intel multiplexed address/data bus type with control signals $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, ALE
4. Serial mode using control signals CDIN, CDOUT, CCLK and $\overline{CS}$.

The selection is performed via pins ALE/CCLK and SMODE as follows:

Table 12 Microprocessor Interface Modes

	ALE	SMODE
Siemens/Intel non-Mux	0	x
Motorola	1	x
Siemens/Intel Mux	edge	0
Serial	edge	1

The occurrence of an edge on ALE/CCLK, either positive or negative, at any time during the operation immediately selects interface type 3 or 4. A return to one of the other interface types is possible only if a hardware reset is issued.

The timing of the different microprocessor bus types is given in sections 8.7.1, page 269 for the parallel bus type and in section 8.7.2, page 273, for the serial bus type.

3.9 S/G Bit and BAC bit Control

Note 22: This chapter applies only in the µP-TE mode (see "Basic Operating Mode", page 50).

If DCL = 1.536 MHz the IOM®-2 interface consists of three IOM®-2 channels (see "Terminal Timing Mode", page 73). The last octet of an IOM®-2 frame includes the S/G and the BAC bit. Either or both bits can be used in various applications including

- the D-channel arbitration in a PBX via an ELIC® on the line card
- the synchronization of a base station in wireless local loop applications

The S/G bit is always written and never read by the IEC-Q. Its value depends on the last received EOC-command and on the status of the BAC bit. The processing mode for the S/G bit is selected via bits SWST:BS, SWST:SGL and ADF:CBAC (see "ADF-Register", page 219). A detailed operational description of the S/G bit control in all modes is provided in "S/G Bit and BAC Bit Operations", page 198.

S/G Status Indication on Pin SG

If one of the packages M-QFP-64 or T-QFP-64 is being used the S/G bit status information will be additionally provided on pin SG, see "Miscellaneous Function Pins", page 46. This feature is not available in the package P-LCC-44.

3.10 Power Controller Interface

Note 23: This chapter applies only in stand-alone mode.

A power controller interface is implemented in the IEC-Q to provide comfortable access to peripheral circuits which are not connected directly to the microprocessor. Because this interface was specifically designed to support the ISDN Exchange Power Controller IEPC (PEB 2025) it is referred to as "Power Controller Interface". Despite this dedication to the IEPC, the controller interface is just as suited for other general-purpose applications.

The interface structure consists of

– 3 bit data bus PCD0 ... 2
– 2 bit address bus PCA0,1
– 3 control signals $\overline{\text{PCRD}}$ and $\overline{\text{PCWR}}$
– 1 interrupt facility INT

See also "Power Controller Pins", page 36, for information about pin configurations.

The address bits are latched, they may therefore in general interface applications be used as output lines. For general interface inputs each of the three data bits is suitable. Read and write operations are performed via MON-8 commands. Three inputs and two outputs are thus available to connect external circuitry.

The interrupt pin is edge sensitive. Each change of level at the pin INT will initiate a C/I-code INT lasting for four IOM®-2-frames. Interpretation of the interrupt cause and resulting actions need to be performed by the control unit.

For informations about communication with the power controller interface, see "Access to Power Controller Interface", page 196.

For informations about dynamic characteristics of the power controller interface, see "Power Controller Interface Timing", page 277.

3.11 Power Status

Two pins PS1 and PS2 are available for comfortably surveying and controlling the power status.

In addition, if the stand-alone mode is being used, a third pin (DISS) is also available.

In NT mode, power status bits 1 and 2 (PS1/2) are used to monitor both primary and secondary NT power supply. This information is transferred via the overhead bit channel to the exchange side. For operational details, see "Monitoring Primary and Secondary NT Power Supply", page 194.

In LT mode the first power status bit (PS1) is used to monitor the remote power feed circuit of the subscriber line. For operational details, see "Monitoring Remote Power Feed Circuit in LT Modes", page 194.

The pin PS2 provides a serial interface in order to read in the value of the current fed to the subscriber line by the power controller. This function is available only in combination with a power controller which supports this feature (the IEPC does not). For operational details, see "Monitoring Power Feed Current in LT Modes", page 194.

If the stand-alone mode is being used the following features are also available.

In the NT and TE modes the output pin disable (DISS) is set to (1) if the EOC-command "close complete loop" (LBBD) has been detected by the NT. This function is only available in EOC Auto mode. It may be used to test a secondary power source (e.g. battery check). For operational details, see "Access to Pin DISS", page 195.

In the LT modes the DISS-pin is used for switching off the remote power supply of the subscriber line. For operational details, see "Access to Pin DISS", page 195.

3.12 Undervoltage Detection

Note 24: This chapter applies only in the microprocessor mode (PMODE = "1").

The undervoltage detector is enabled by setting the ADF:UVD bit to "1", see "ADF-Register", page 219. Note that the default setting of this bit after power on will be "1", i.e. the undervoltage detection feature will be activated. It activates the reset signal if the supply voltage drops below the threshold U_L (typically 4.21 V, see Figure 37 below and "Undervoltage Detection Timing", page 280).
It also acts as power on reset by creating a reset pulse on pin $\overline{RST}$ if the supply voltage rises above U_H (typically 4.30 V). It then stays inactive until the supply voltage drops again below the threshold level U_L (see also "Power On Reset (POR)", page 93, for more information).

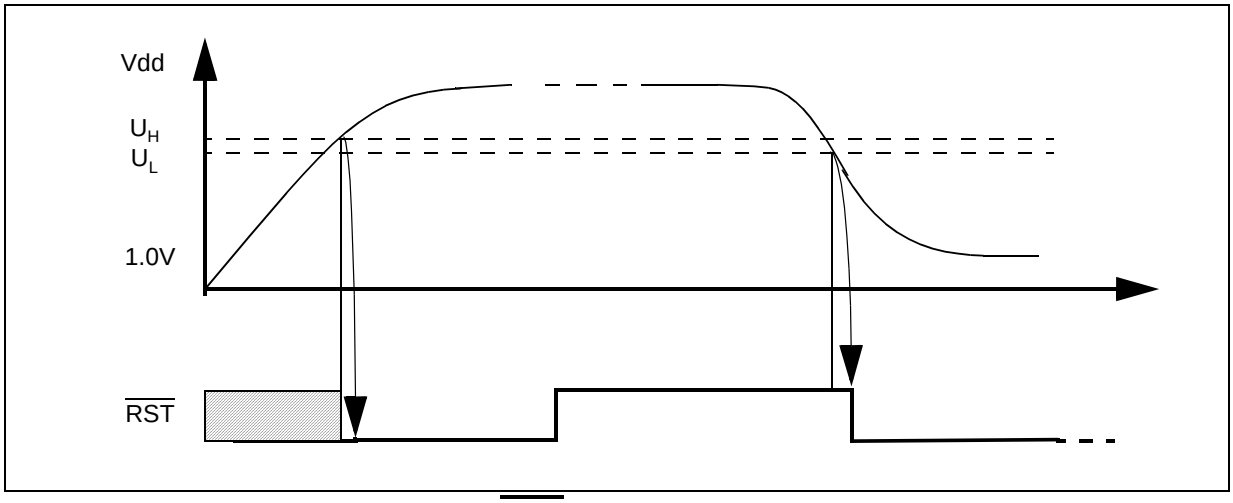


Figure 37 UVD Control of Pin $\overline{RST}$

While the supply voltage is below threshold U_L, the microcontroller clock MCLK is stopped and the MCLK output remains low[1)]. If the supply voltage falls below threshold U_L, the clock is stopped immediately which may result in one shorter high period of the clock signal.

Note 25: For power saving reasons, this function is not available in power down. Still pin RST will not float in this state and the power on reset function is still available, see 3.14 below.

3.13 Watchdog Timer

Note 26: This chapter applies only in the microprocessor mode (PMODE = "1").

The watchdog is enabled by setting the SWST:WT bit to "1", see "SWST-Register", page 220. The value of SWST:WT after hardware reset ($\overline{RES}$ = '0') is "0".

After the microcontroller has enabled the watchdog timer it has to write the bit patterns "10" and "01" in ADF:WTC1 and ADF:WTC2 within a period of 132 ms, see "ADF-Register", page 219. If it fails to do so, a reset signal of 5 ms at pin $\overline{RST}$ is generated. The clock at pin MCLK remains active during this reset.

3.14 Power On Reset (POR)

The PEB/F 2091 is equipped with a POR feature. During power on or power off, an internal reset will be generated if the POR threshold (between 2.5 V and 4.5 V) is

1) The behavior of the microcontroller clock MCLK is not specified below the supply voltage of 4.0 Volt.

reached. This is independent of mode setting. However there is a difference in reset duration and indication between the stand-alone mode and the microprocessor mode. In stand-alone mode this internal reset (POR) will be fully equivalent to the hardware reset generated by activating the pin $\overline{\text{RES}}$. The duration of the reset pulse will be some value between 10 and 30 µs.

The processor mode (PMODE="1") has two additional properties:
- The POR will be given on the pin $\overline{\text{RST}}$
- The POR will also reset the register STCR. See "STCR-Register", page 212.

The duration of POR in this mode will be some value between 60 and 70 ms.

3.15 Reset Behavior

Several resets are provided in the IEC-Q (see chapters 3.12, 3.13 and 3.14 above). Their effects are summarized in Table 13.

Definition

The transceiver core is said to be reset if the Receiver coefficients, the awake unit, the Monitor Channel procedure and the state machine are reset.

Table 13 Reset

Reset	Condition	Effect	Pin $\overline{\text{RST}}$ active[1)]
Power-On	Power-on	Resets the transceiver core[2)]. Resets all registers in the microprocessor mode	yes
UVD	Power supply drop	Resets the transceiver core[2)]. Resets all registers in the microprocessor mode	yes
Hardware Reset	Pin $\overline{\text{RES}}$ = 0	Resets the transceiver core[2)]. Resets all registers except for register STCR in the microprocessor mode	no
Watchdog	Watchdog expired	No internal effect	yes
Software Reset	C/I = 0001	Resets the transceiver core	no

1) Applies only in the microprocessor mode

2) In all IOM®-2 slave modes this reset will be carried out only after the IOM®-2 clocks has been applied to the IEC-Q

The clock MCLK is delivered during reset (except for power-on and undervoltage detection).

Table 13 shows that the output pin $\overline{\text{RST}}$ is controlled by power-on reset, undervoltage detection and the watchdog timer. Figure 38 illustrates the reset sources that have an impact on pin $\overline{\text{RST}}$.

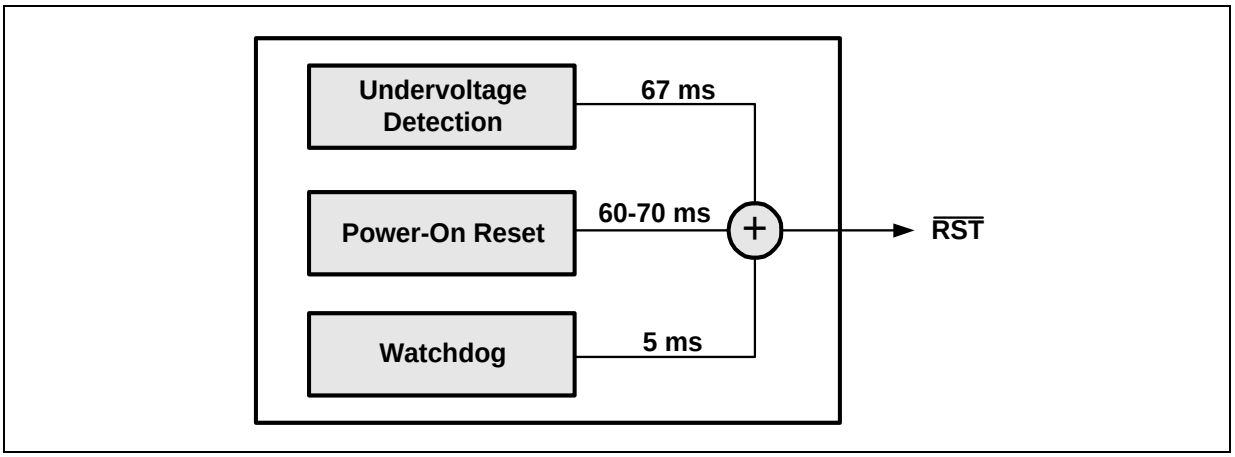


Figure 38 Reset Sources

3.16 Test Block

In stand-alone mode the two pins TP and TP1 are used for internal manufacturing device tests. In microprocessor mode only pin TP is used for device test. Test pins are not defined for normal system operation, as described in this document, and should therefore be left unconnected.

4 Operational Description

In chapters 2 and 3 the pins and user's interfaces of the IEC-Q are described in detail. Using this information, this chapter describes the interaction between these interfaces in detail. The approach used is to describe how IEC-Q features can be accessed using the different user interfaces, described in chapter 3.

Most of the IEC-Q features can be accessed via IOM®-2 interface. In the microprocessor mode the processor interface provides almost unlimited access to the IOM®-2 channels in upstream and downstream directions, and consequently to most of the IEC-Q features. This µP access to the IOM®-2 interface is described in section 4.1.

Access to the U-interface is the scope of section 4.2. A detailed description is given about the possibilities of (always indirect) access to each channel of the U-interface and the behavior of the IEC-Q in each mode (e.g. NT, LT, EOC Auto and Transparent modes).

Sections 4.3 and 4.4 cover the whole issue of activation and deactivation procedures and control. Section 4.3 describes layer 1 activation and deactivation procedures of different configurations. Section 4.4 describes the activation and deactivation control of the different modes of the IEC-Q itself.

Access to numerous maintenance features is discussed in sections 4.5 through 4.9. This includes monitoring transmission quality, features supporting test loop-backs defined by the national PTTs, power status monitoring features as well as chip internal testing features.

Features of the power controller interface are described in section 4.10 which applies only in the stand-alone mode.

Section 4.11 applies only to the microprocessor mode if used in the NT or the TE mode, and describes how to program and access the S/G and BAC bit features which can be used in applications like Wireless Local Loop and D-Channel arbitration.

4.1 Microprocessor Access to IOM®-2 Channels

Note 27: This chapter applies only in µP mode.

In µP mode the microcontroller has access to the IOM®-2 channels via the processor interface (PI) and registers.

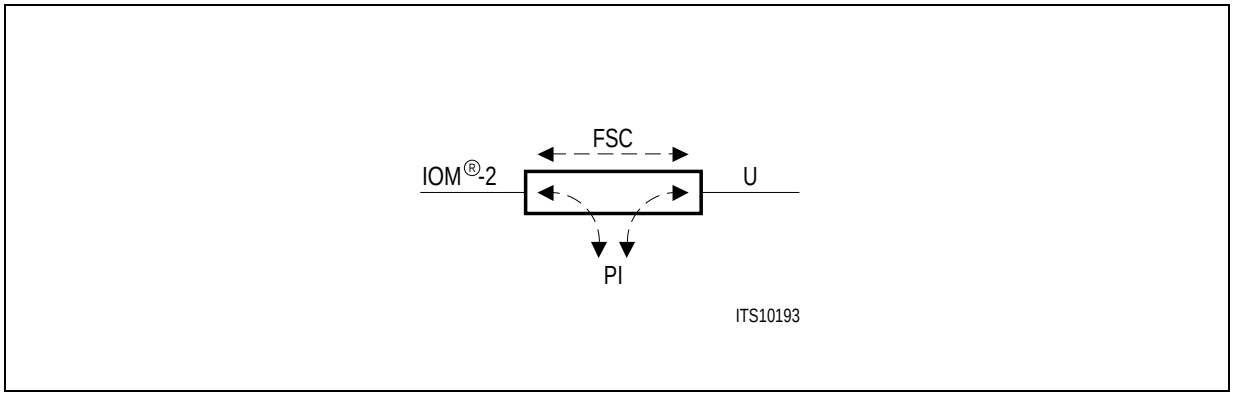


Figure 39 Access to IOM®-2 Channels (µP mode)

The processor interface can be understood as an intelligent switch between IOM®-2 and the transceiver core. It handles D, B1, B2, C/I and Monitor-channel data. The data can either be transferred directly between IOM®-2 and the transceiver core, or be controlled via the PI. The PI acts as an additional participant to the Monitor Channel.

Switching directions are selected by setting the register SWST as indicated below:

SWST-Register

WT	B1	B2	D	CI	MON	BS	SGL

- Setting one of the 5 bits B1, B2, D, CI, or MON of SWST to "1" enables the µP access to the corresponding data.
- Setting the bits listed above to "0" directly passes the corresponding data from IOM®-2 to the transceiver core and vice versa.

Refer also to "SWST-Register", page 220 for more details. The default value after hardware reset is "0" at all 8 positions.

Note 28: ***The microprocessor interface provides almost unlimited access possibilities to the active IOM®-2 channel. One important consequence is that all actions described in this document involving the active channel of the IOM®-2 interface or parts of it (e.g. B, D, Monitor and C/I channels) can be also performed using the PI.***
In the IOM®-2 Master mode proper function using the microprocessor interface is possible even if the IOM®-2 interface is omitted. In this case pin DIN should be clamped to '1'.
In the IOM®-2 Slave mode the IOM®-2 clocks can not be omitted. They are needed for internal data synchronization reasons. If pin DIN is not used, it should be clamped to '1'. If pin DOUT is not used it should be left open.

4.1.1 B-Channel Access

Setting SWST:B1 (B2) to "1" enables the microprocessor to access B1 (B2)-channel data between IOM®-2 and the transceiver core.

Eight registers (see Table 14) handle the transfer of data from IOM®-2 to the µP, from the µP to IOM®-2, from the µP to transceiver core and from transceiver core to the µP:

Table 14 B1/B2-Channel Data Registers

Register	Function
WB1U	write B1-channel data to transceiver core
RB1U	read B1-channel data from transceiver core
WB1I	write B1-channel data to IOM®-2
RB1I	read B1-channel data from IOM®-2
WB2U	write B2-channel data to transceiver core
RB2U	read B2-channel data from transceiver core
WB2I	write B2-channel data to IOM®-2
RB2I	read B2-channel data from IOM®-2

For more informations about these registers, refer to "B-Channel Access Registers", page 221. Every time B-channel bytes arrive, an interrupt ISTA:B1 or ISTA:B2 respectively is created. It is cleared after the corresponding registers have been read. ISTA:B1 is cleared after RB1U and RB1I have been read. ISTA:B2 is cleared after RB2I and RB2U have been read. After an interrupt the data in RB1U and RB1I is stable for 125µs. For more informations, refer to "Interrupt Structure", page 209.

4.1.2 D-Channel Access

Setting SWST:D to "1" enables the microprocessor to access D-channel data between the IOM®-2 and the transceiver core.

Four registers (see Table 15) handle the transfer of data from IOM®-2 to the µP, from the µP to IOM®-2, from the µP to transceiver core and from transceiver core to the µP. See "D-Channel Access Registers", page 221 for more details about these registers.

Table 15 D-Channel Data Registers

Register	Function
DWU	write D-channel data to transceiver core
DRU	read D-channel data from transceiver core
DWI	write D-channel data to IOM®-2
DRI	read D-channel data from IOM®-2

Two 2-bit FIFOs of length 4 collect the incoming D-channel packets from IOM®-2 and U. Every fourth IOM®-2-frame when they are filled, an interrupt ISTA:D is generated and the contents of the FIFOs are shifted in parallel to DRU and DRI respectively. DRU and DRI have to be read before the next interrupt ISTA:D can occur, otherwise 8 bits will be lost. DWU and DWI have to be loaded with data for 4 IOM®-2-frames. Data in DWU and DWI is assumed to be valid at the time ISTA:D occurs (see also "Interrupt Structure", page 209). The register contents are shifted in parallel into two 2-bit FIFOs of length four, from where the data is put to IOM®-2 and transceiver core respectively during the following 4 IOM®-2-frames. During this time, new data can be placed on DWU and DWI. DWU and DWI are not cleared after the data was passed to the FIFOs. That is, a byte may be put into DWU or DWI once and continuously passed to IOM®-2 or transceiver core, respectively. Figure 40 illustrates this procedure:

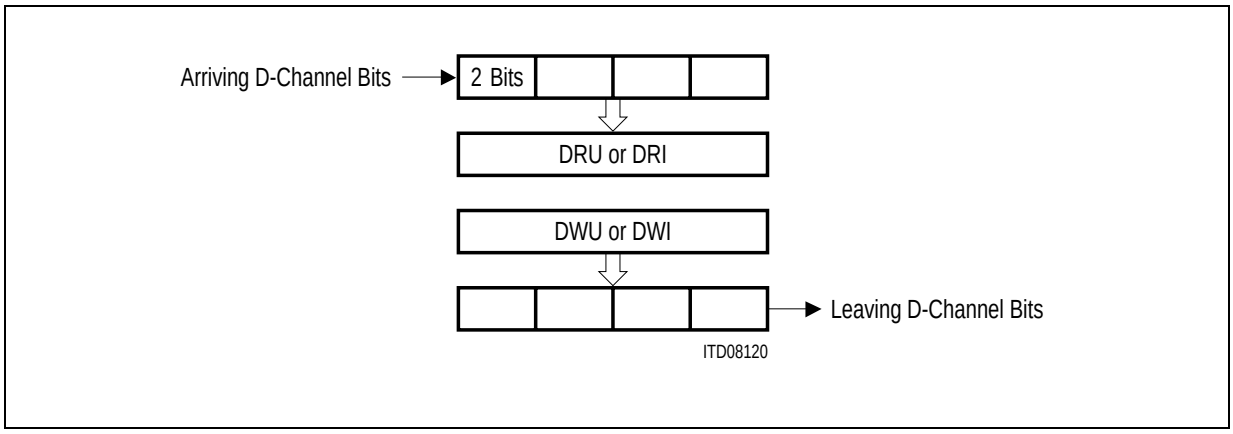


Figure 40 Procedure for the D-Channel Processing

Note 29: Default of DWU, DWI, DRU and DRI after reset is "FF_H".

4.1.3 C/I Channel Access

Setting SWST:CI to "1" enables the microprocessor to access C/I-commands and indications between IOM®-2 and the transceiver core.

A change in two consecutive frames (double last look) in the C/I-channel on IOM®-2 is indicated by an interrupt ISTA:CICI. The received C/I-command can be read from register CIRI. A change in the C/I-channel coming from the transceiver core is indicated by an interrupt ISTA:CICU. The new C/I-indication can be read from register CIRU.

Note 30: The term C/I-indication always refers to a C/I-code coming from the transceiver core, whereas the term C/I-command refers to a C/I-code going into the transceiver core.

A C/I-code going to the transceiver core has to be written into the CIWU-register. A C/I-code to IOM®-2 has to be written into the CIWI-register. The contents of both registers (CIWU and CIWI) will be transferred at the next available IOM®-2 frame. The registers are not cleared after the transfer. Therefore, it is possible to continuously send C/I codes to IOM®-2 or the transceiver core by only writing the code into the register once.

C/I-commands to the transceiver core have to be applied at least for two IOM®-2 frames (250 µs) to be considered as valid.

For more information see section 5.2.7, page 217 and thereafter. See also "Interrupt Structure", page 209.

In TE mode (i.e. 1.536 MHz DCL), the ADF2:TE1 bit is used to direct the C/I-channel access either to IOM®-2 channel 0 (ADF2:TE1 = 0, default) or to IOM®-2 channel 1 of the IOM®-2 terminal structure (ADF2:TE1 = 1), see Figure 41. This allows to program terminal devices such as the ARCOFI® via the processor interface of the IEC-Q. The C/I code going to IOM®-2 is 4 bits long if it is written to IOM®-2 channel 0 (ADF2:TE1 = 0). If written to IOM®-2 channel 1 this C/I code is 6 bits long (ADF2:TE1 = 1). If the ADF2:TE1 bit is 1, the C/I Channel on IOM®-2 channel 0 is passed transparently from the IOM®-2 interface to the transceiver core.

See also "ADF2-Register", page 214 for more information about this register.

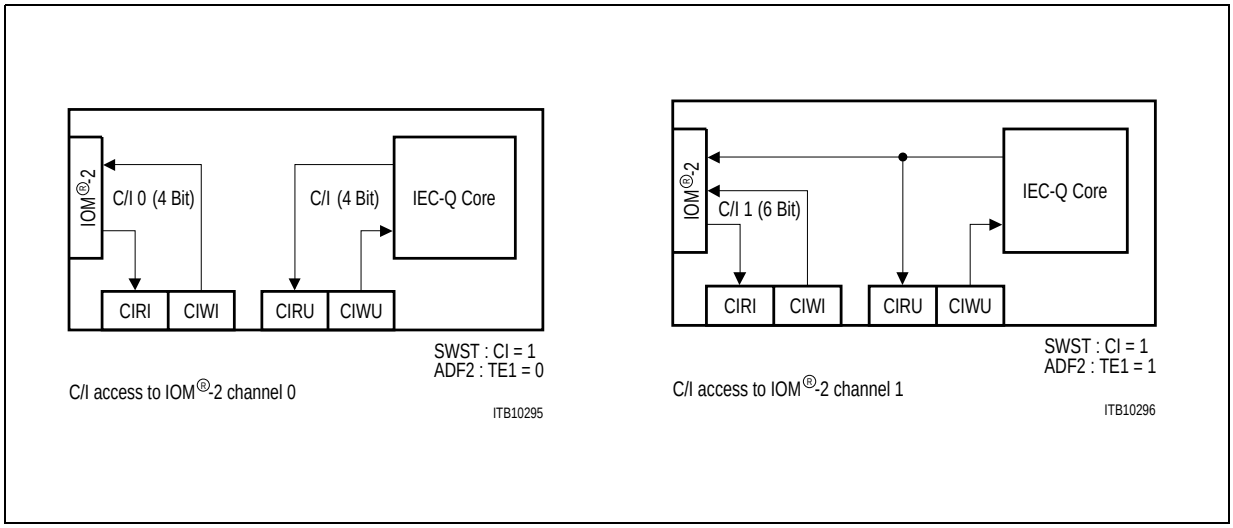


Figure 41 C/I Channel Access

4.1.4 Monitor Channel Access

Setting SWST:MON to "1" enables the microprocessor to access Monitor-channel messages at IOM®-2 interface and the transceiver core. Monitor-channel access can be performed in three different IOM®-2 channels (see Figure 42).

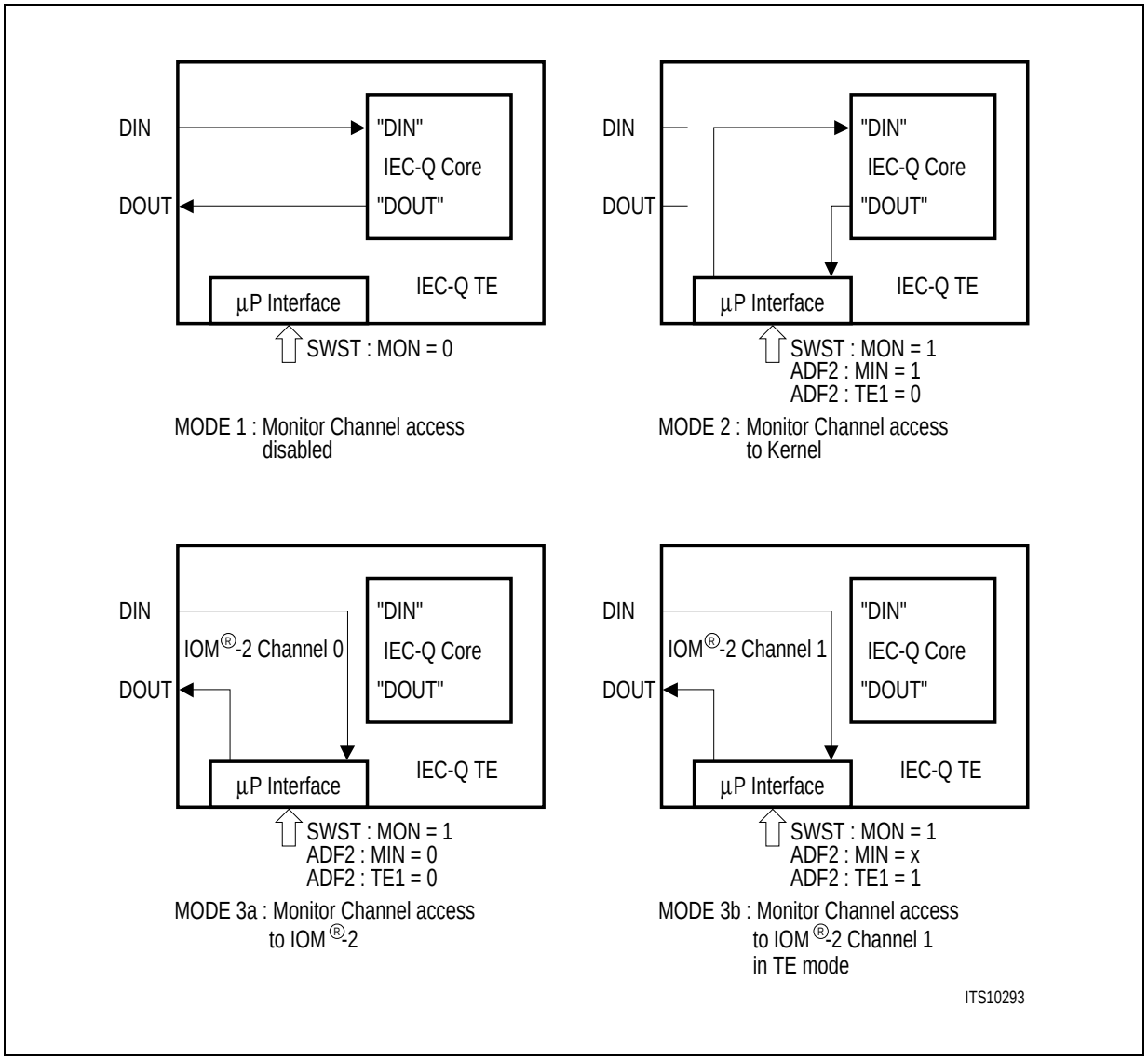


Figure 42 Monitor Channel Access Directions

Setting SWST:MON to ’0’ disables the controller access to the Monitor Channel (Figure 42 upper left part).

Setting SWST:MON to ’1’ enables three different ways of controller access to the Monitor Channel. ADF2:TE1 set to ’0’ allows to access either the transceiver core of the IEC-Q (see Figure 42 upper right part, ADF2:MIN = ’1’) or the IOM®-2 interface of the IEC-Q (Figure 42 lower left part, ADF2:MIN = ’0’).

Setting ADF2:TE1 to ’1’ in TE mode gives access to IOM®-2 channel 1 rather than IOM®-2 channel 0 directed out of the IEC-Q. This allows to program devices linked to IOM®-2 channel 1 (e.g. ARCOFI®) via the processor interface of the IEC-Q.

4.1.4.1 Monitor Channel Protocol

The PI allows to program the IEC-Q Monitor Channel in the way known from the PEB 2070 (ICC).

The Monitor Channel operates on an *asynchronous* basis. While data transfers on the IOM®-2-bus occur synchronized to frame sync FSC, the flow of data is controlled by a handshake procedure using the Monitor Channel Receive (MR) and Monitor Channel Transmit (MX) bits. For example: data is placed onto the Monitor Channel and the MX bit is activated. This data will be transmitted repeatedly once per 8-kHz frame until the transfer is acknowledged via the MR bit.

The microprocessor may either enforce a "1" (idle) in MR, MX by setting the control bit MOCR:MRC or MOCR:MXC to "0", or enable the control of these bits internally by the IEC-Q according to the Monitor Channel protocol. Thus, before a data exchange can begin, the control bits MRC or MXC should be set to "1" by the microprocessor.

The Monitor Channel protocol is illustrated in Figure 43. The relevant control and status bits for transmission and reception are:

Table 16 Monitor Transmit Bits

Register	Bit	control / status	Function
MOCR	MXC	control	MX Bit Control
	MXE		Transmit Interrupt Enable
MOSR	MDA	status	Data Acknowledged
	MAB		Data Abort
STAR	MAC		Transmission Active

Table 17 Monitor Receive Bits

Register	Bit	control / status	Function
MOCR	MRC	control	MR Bit Control
	MRE		Receive Interrupt Enable
MOSR	MDR	status	Data Received
	MER		End of Reception

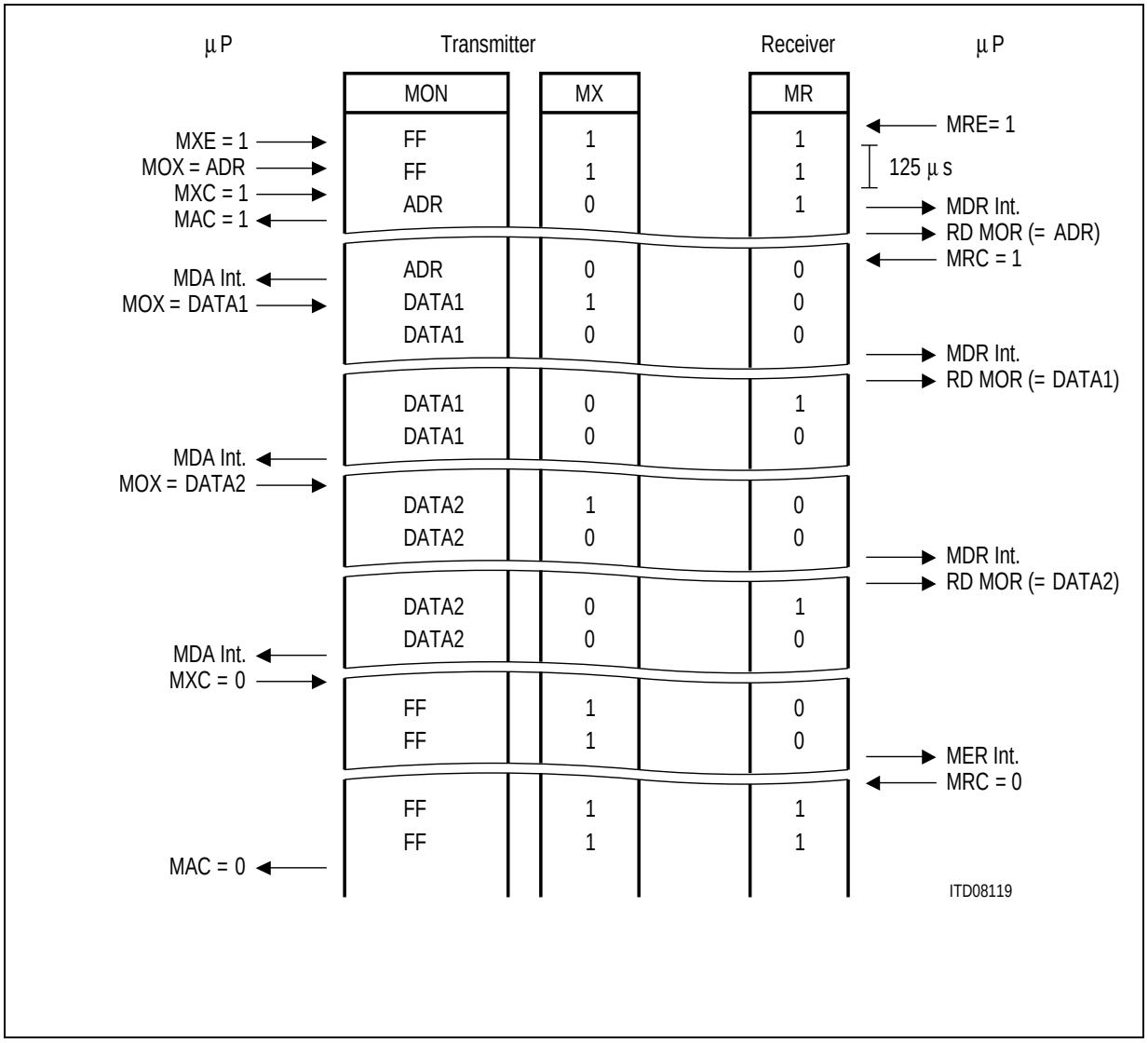


Figure 43 Monitor Channel Protocol

Before starting a transmission, the microprocessor should verify that the transmitter is inactive, i.e. that a possible previous transmission has been terminated. This is indicated by a "0" in MOSR:MAC, the Monitor Channel Active status bit.

To enable interrupts for the transmitter the MOCR:MXE bit must be set to "1" (For details see "Monitor-Channel Interrupt Logic", page 209). After having written the Monitor Data Transmit (MOX) register, the microprocessor sets the Monitor Transmit Control bit MXC to "1". This enables the MX bit to go active ("0"), indicating the presence of valid Monitor data (contents of MOX) in the corresponding frame. As a result, the receiving device stores the Monitor byte in its Monitor Receive (MOR) register and generates an MDR interrupt status.

Alerted by the MDR interrupt, the microprocessor reads the Monitor Receive (MOR) register. When it is ready to accept data (e.g. based on the value in MOR, which in a point-to-multipoint application might be the address of the destination device), it sets the MR control bit MRC to "1" to enable the receiver to store succeeding Monitor Channel bytes and acknowledge them according to the Monitor Channel protocol. In addition, it enables other Monitor Channel interrupts by setting Monitor receive Interrupt Enable (MRE) to "1".

As a result, the first Monitor byte is acknowledged by the receiving device setting the MR bit to "0". This causes a Monitor Data Acknowledge (MDA) interrupt status at the transmitter.

A new Monitor data byte can now be written by the microprocessor in MOX. The MX bit is still in the active ("0") state. The transmitter indicates a new byte in the Monitor Channel by returning the MX bit active after sending it once in the inactive state. As a result, the receiver stores the Monitor byte in MOR and generates a new MDR interrupt status. When the microprocessor has read the MOR register, the receiver acknowledges the data by returning the MR bit active after sending it once in the inactive state. This in turn causes the transmitter to generate an MDA interrupt status.

This "MDA interrupt – write data – MDR interrupt – read data – MDA interrupt" handshake is repeated as long as the transmitter has data to send. Note that the Monitor Channel protocol imposes no maximum reaction times to the microprocessor.

When the last byte has been acknowledged by the receiver (MDA interrupt status), the microprocessor sets the Monitor Transmit Control bit (MXC) to "0". This enforces an inactive ("1") state in the MX bit. Two frames of MX inactive signifies the end of a message. Thus, a Monitor Channel End of Reception (MER) interrupt status is generated by the receiver when the MX bit is received in the inactive state in two consecutive frames. As a result, the microprocessor sets the MR control bit MRC to "0", which in turn enforces an inactive state in the MR bit. This marks the end of the transmission, making the Monitor Channel Active (MAC) bit return to "0".

During a transmission process, it is possible for the receiver to ask for a transmission to be aborted by sending an inactive MR bit value in two consecutive frames. This is effected by the microprocessor writing the MR control bit MRC to "0". An aborted transmission is indicated by a Monitor Channel Data Abort (MAB) interrupt status at the transmitter.

In TE mode, the ADF2:TE1 bit is used to direct the Monitor access either to IOM®-2-channel 0 (ADF2:TE1 = "0", default) or to IOM®-2-channel 1 of the IOM®-2-Terminal structure. This allows to program terminal devices such as the ARCOFI® via the processor interface of the IEC-Q. If the ADF2:TE1 bit is "1", the Monitor Channel on IOM®-2-channel 0 is passed transparently from the IOM®-2 interface to the transceiver core.

4.2 Access to U-Interface

The U-frame is not directly accessible by the user. Communication with the U-interface will be established using the user interfaces IOM®-2, µP (if used) or pins. This chapter shows how this can be done for both receive and transmit directions. Figures 44 and 45 sketch the available ways of access to the different channels of the U-interface data in both directions. For more details about the structure of the U-frame, see "U -Frame Structure", page 67. For blocks' functions, see "System Interface Unit", page 62.

In addition, Section 4.2.4, page 124, describes how the U-interface superframe marker can be set and indicated.

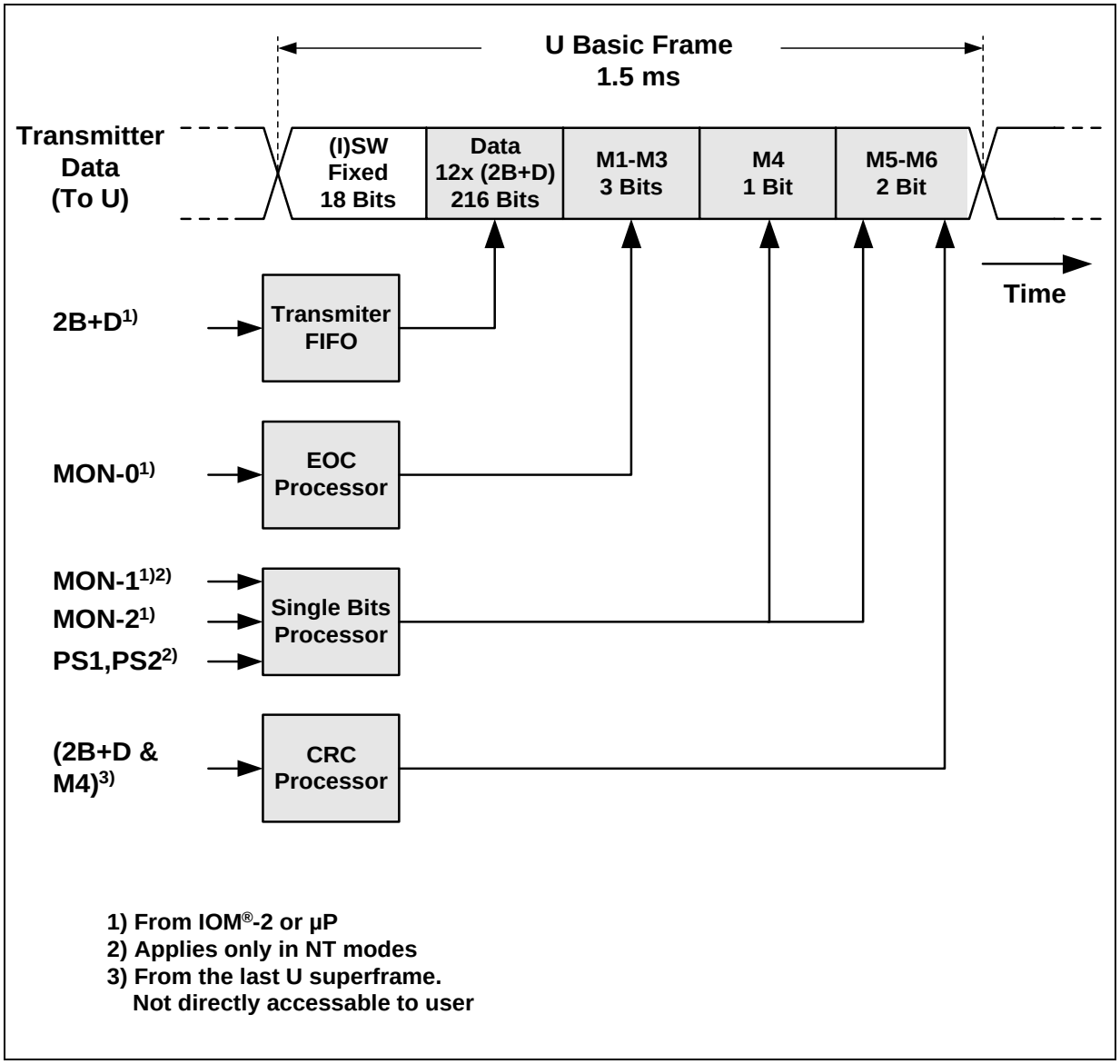


Figure 44 Channels of Access to U-Interface (Transmitter)

Data

During normal operation (i.e. transparent transmission and no test mode) the 2B+D channels can be accessed via the IOM®-2 or the µP interface, if used. See section 4.2.1, page 108 for details.

EOC

Basically the EOC channel can be accessed via MON-0 messages. However, internal processing, manipulation and filtering of the EOC messages could take place automatically, depending on the mode chosen. For details see section 4.2.2, page 110.

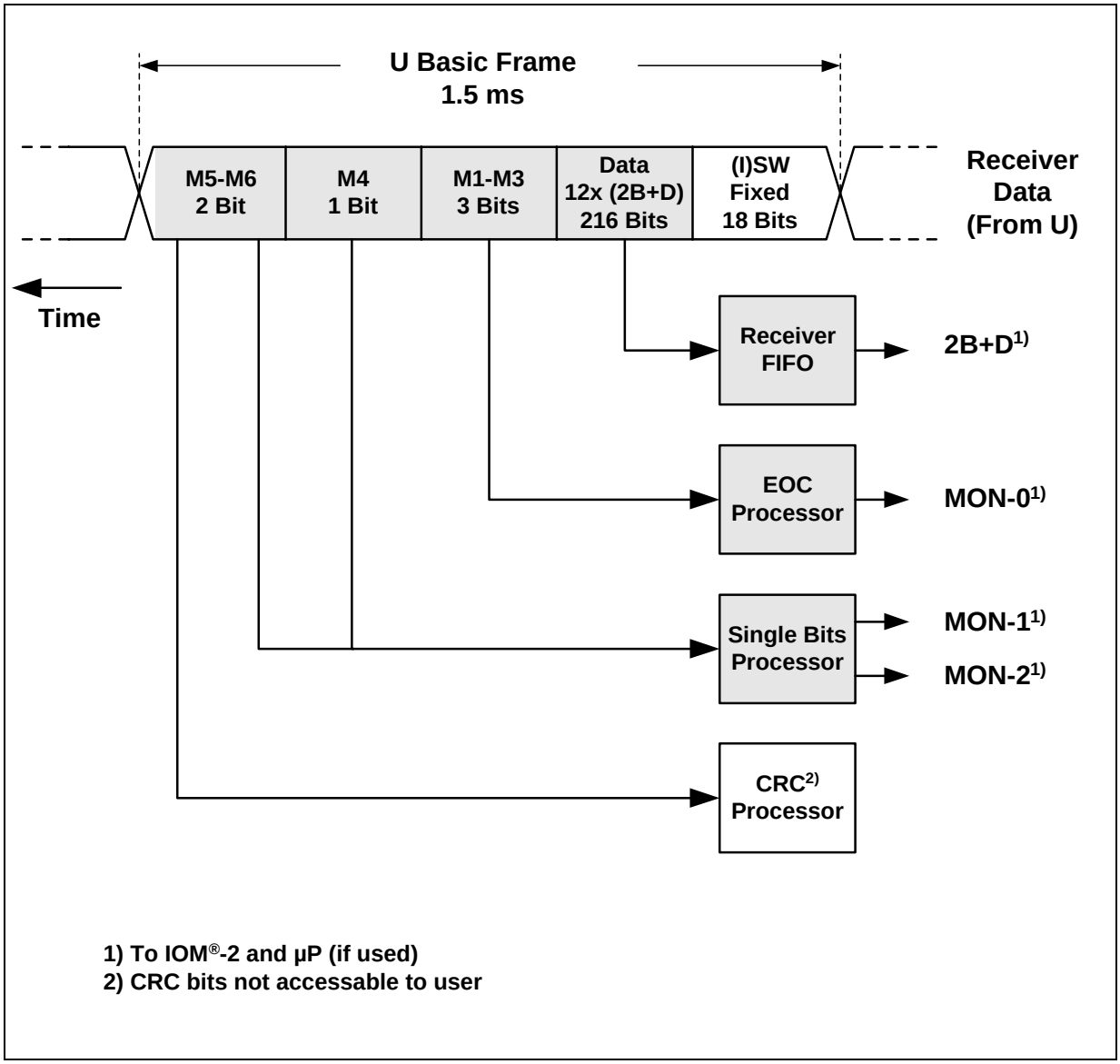


Figure 45 Channels of Access to U-Interface (Receiver)

Single Bits

User access to the Single Bits (SB) channel is mode dependent.
In transmit direction there are five possible sources for setting (different) SB: MON-1 messages, MON-2 messages, MON-8 messages, the pins PS1 and PS2 and the state machine. MON-1, MON-2 and pins PS1 and PS2 can be manipulated directly by the user. Bits controlled by the state machine can not be manipulated by the user in a direct way.
In the receive direction the SB are given via MON-1 and MON-2 messages. Several filtering methods are available. For details see section 4.2.3, page 115.

Note 31: ***U-interface data is scrambled before it is send to the U-interface and descrambled when they are received from the U-interface (see "Scrambler / Descrambler", page 62).***

Note 32: ***The synchronization words (bits 1-18 of each U basic frame) are set by the transceiver core and can not be manipulated by the user.***

Note 33: ***The CRC channel can not be accessed by the user. These bits are calculated and set by the transceiver core automatically (see "Cyclic Redundancy Check (CRC)", page 64). However there are several methods of monitoring CRC violations, which are discussed in detail in chapter 4.5, page 176.***

4.2.1 Access to Data Channels of U-Interface

Figures 46 and 47 below sketch how data can generally be accessed by the user.

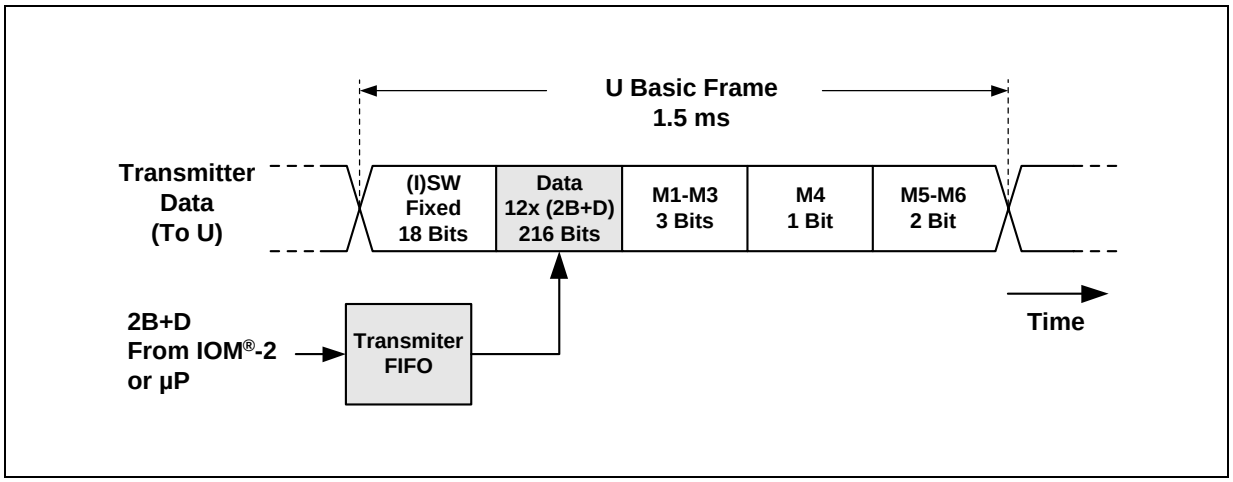


Figure 46 Access to Data Transmission on U

Data Access in LT Mode

In LT modes (see "Setting Operating Modes", page 50) transparent data access is available in both directions in the states:

LT	LT-RP
Pending Transparent	Pending Transparent
Transparent	Transparent
Pending Deactivation	Pending Deactivation
Line Active	
S/T Deactivated	

i.e. when the IEC-Q issues the signal SL3T on U, and the Receiver is synchronized (see "State Transition Diagram in LT Modes", page 147). In these states data from upstream is handed over via transmit FIFO to the U-Frame in the same order it is received. Data from downstream is handed over via receive FIFO to the IOM®-2 interface and to the microprocessor interface (if used) in the same order it is received.

Data Access in NT Mode

In NT modes (see "Setting Operating Modes", page 50) transparent data access will be available in both directions in the states "Transparent", "Error S/T" and "Pending Deactivation U", i.e. when the IEC-Q issues the signal SN3T on U (see "State Transition Diagram in NT, TE and NT-PBX Modes", page 161). If test loop #2 is not closed in the IEC-Q (see "Test Loop-Backs", page 186) data from downstream is handed over via transmit FIFO to the U-Frame in the same order it is received. Data from upstream is handed over via receive FIFO to the IOM®-2 interface and to the microprocessor interface (if used) in the same order it is received.

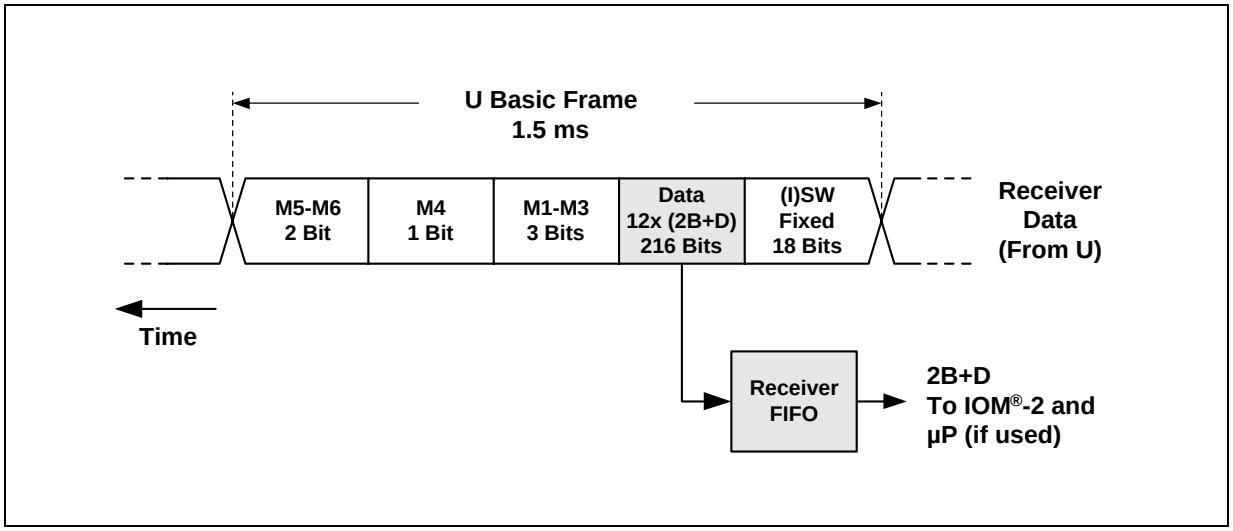


Figure 47 Access to Data Received from U

4.2.2 Access to EOC of U-Interface

The MON-0-commands provide access to device internal EOC-registers. Via MON-0 the EOC overhead bits of the U-interface are controlled. This access is only possible in states where the IEC-Q transmits superframe indications (ISW) and the Receiver is synchronized. This is the case in the following states:

LT Modes	NT Modes
EC-Converged	Synchronized
EQ-Training	Wait for ACT
Line Active	Transparent
Pend. Transparent	Error S/T
Transparent	Pend. Deac. U
Pend. Deactivation	
S/T Deactivated	

Figures 48 and 49 sketch EOC access in these states.

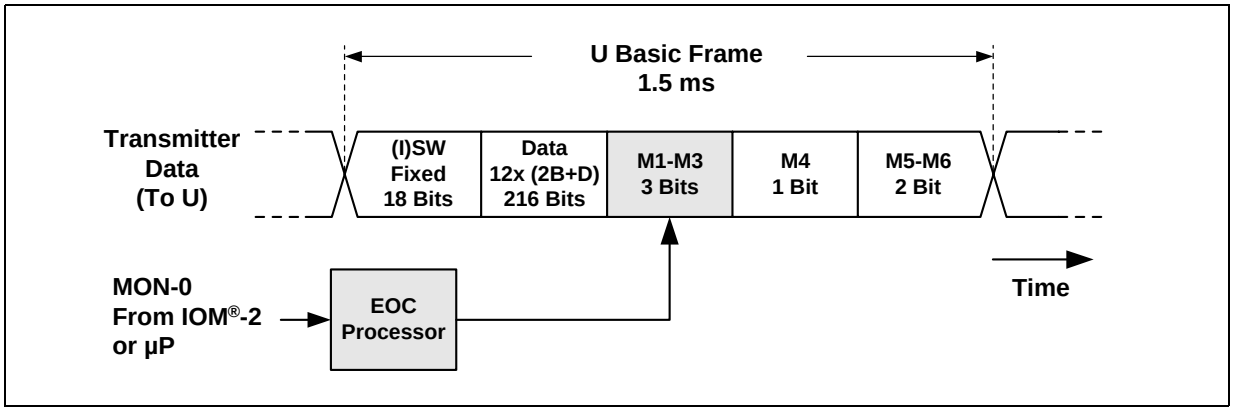


Figure 48 Access to EOC Transmission on U

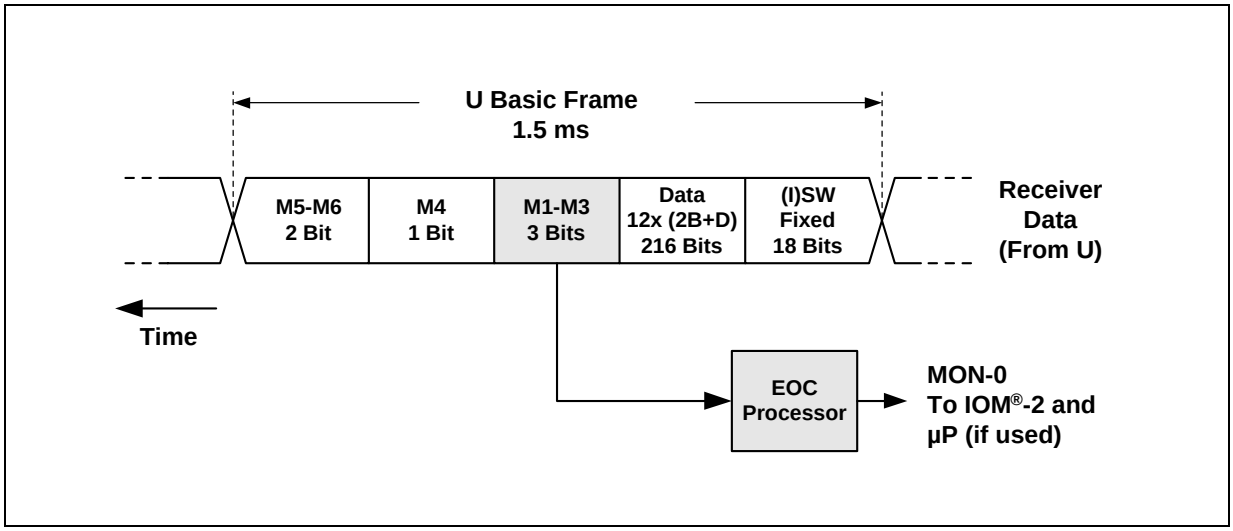


Figure 49 Access to EOC Received from U

In other states the EOC-processor clamps all EOC-maintenance bits to high when EOC-bits are transmitted.

The address bits, d/m bit and the EOC code of the two byte MON-0 message (see Table 18 below) corresponds to the address bits , d/m bits and EOC code in the EOC channel of the U-interface (see "U-Frame Structure", page 68). For more information on Monitor Channel handling, see "IOM®-2 Monitor Channel", page 76 and for the microprocessor mode "Monitor Channel Access", page 101. For a complete list of the available Monitor Channel commands, see "MON-0 Codes", page 226.

Table 18 Content of MON-0 Message

1. Byte		2. Byte	
0 0 0 0	A A A | 1	E E E E	E E E E
MON-0	Addr. | d/m	EOC Code	

MON-0-commands may be passed at any instant and need to be transferred only once (applicable for Auto and Transparent mode). Code repetition is performed within the chip by the EOC processor.

A summery of the EOC procedure in EOC Auto and Transparent modes is given in Figure 50, page 114. If the microprocessor mode is used, the IOM®-2 interface in Figure 50 can be replaced by the µP interface.

EOC Access in LT-Auto Mode

In LT-Auto mode the "return message" reception is enabled after an EOC-command has been transmitted downstream. The activation of this function causes the LT IEC-Q to watch the EOC of the U-interface and to issue a MON-0-message after an identical EOC-message has been received during three consecutive frames. Thus in LT-Auto mode an acknowledgment of the MON-0-command is even possible if the new message is not different from the previous one.

If no MON-0-command has been transmitted downstream, a MON-0-message is issued only after the "triple-last-look" criterion is fulfilled and if this message is different from the one previously accepted. New messages will be passed upstream independently of the address used, i.e. not only messages addressed with (000) or (111) but all received EOC-messages will be transmitted with MON-0-messages.

LT-Transparent Mode

In LT-transparent mode every 6 ms a MON-0-message containing the last received EOC-message is issued. This occurs even if no change occurred in the EOC-channel. No "triple-last-look" is performed before a MON-0-message is sent.

NT-EOC-Auto Mode

The seven defined EOC-commands listed in Table 19 will be executed automatically by the IEC-Q if they were sent with the address (000) or (111) and the d/m bit was set to message (1). Every new EOC-command will be acknowledged immediately, i.e. no triple-last-look (e.g. acknowledgment of LB1 command reads 01_H, 51_H) before the acknowledgment is transmitted.

Table 19 Predefined EOC Messages

Code Hex.	Symbol	Function
00	H	Hold
50	LBBD	Close complete loop
51	LB1	Close loop B1
52	LB2	Close loop B2

Table 19 Predefined EOC Messages

53	RCC	Request corrupt CRC
54	NCC	Notify of corrupt CRC
AA	UTC	Unable to comply
FF	RTN	Return to normal
XX		Acknowledge

If a command is declared as data (d/m = (0)), the IEC-Q will acknowledge with "UTC" (i.e. $01AA_H$). Commands addressed different from (000_B) or (111_B) will be acknowledged with the "Hold" message and the correct NT address (i.e. 0100_H), see "Predefined EOC Codes", page 231, for a complete list. All detected EOC-commands on U are latched, i.e. they are valid as long as they are not explicitly disabled with the EOC "RTN" command or a deactivation.

Each new EOC-command will be indicated with one single MON-0-message after the triple-last-look criterion has been met (also if other addresses than (000) or (111) or d/m = (0) are used). The verified message is not compared to the last accepted message (triple-last-look). Instead a MON-0-message will be issued every time the new verified message is different from the last. E.g. in case bit errors corrupted an EOC-command the correct command will be reissued after error free transmission is resumed. The execution of a correctly addressed command (000_B or 111_B) is performed only after the "triple-last-look" criterion is met.

MON-0-commands given via IOM®-2 (DIN) or microprocessor interface will be ignored.

NT-Transparent Mode

Every 6 ms a MON-0-message is issued on IOM®-2. It contains the last received EOC-message. No acknowledgment, no triple-last-look, no execution of the received commands is performed in EOC Transparent mode. All these actions have to be initiated by a control unit. With MON-8-messages all defined test functions (close/open loops, send corrupted CRCs) can be executed in the NT, see "Test Loop-Backs", page 186.

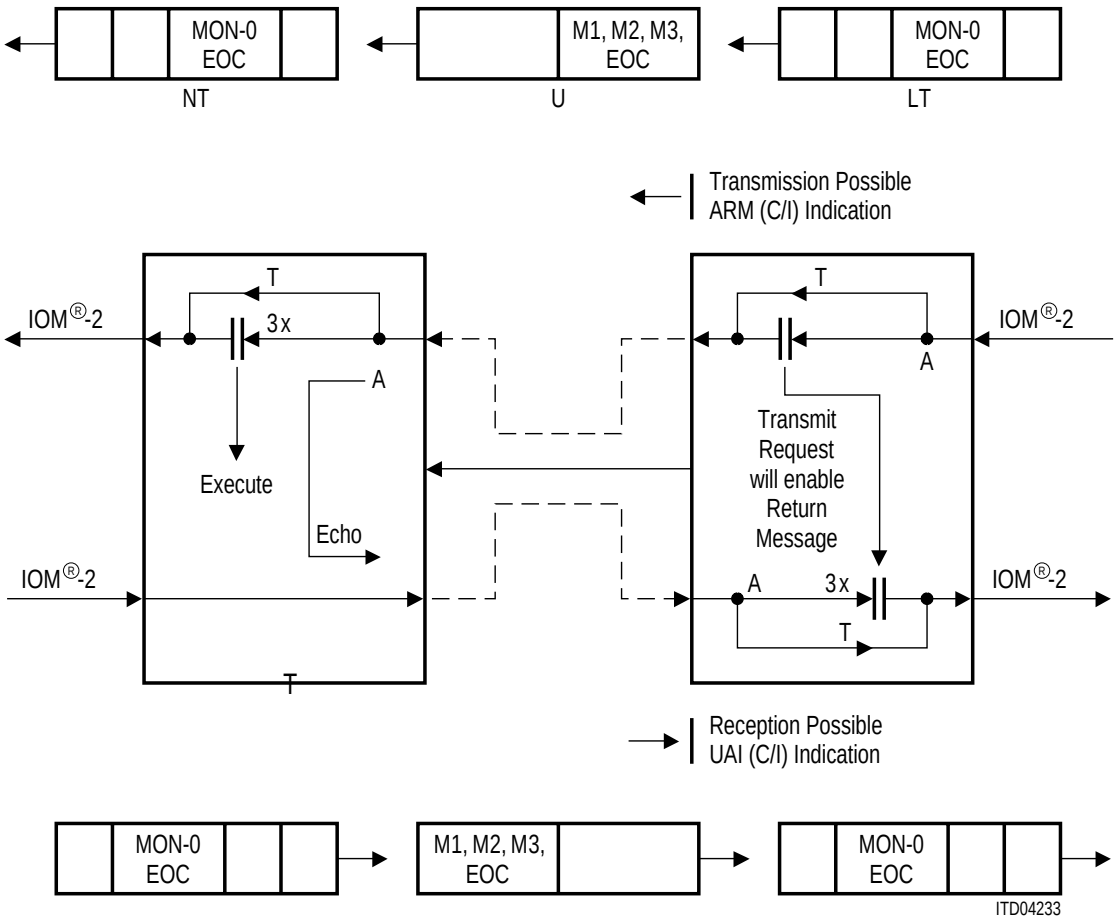


Figure 50 EOC-Procedure in Auto and Transparent Mode

4.2.3 Access to the Single Bits of U-Interface

The transmission procedure of the Single Bits (SB) on the U-interface is mode dependent. The reception procedure of the SB from the U-interface is independent[1)] of the mode used. Transmission and reception of SB will therefore be discussed in to different sections below. For definition of Single Bits, see "Single Bits Channel", page 69. For more information on Monitor Channel handling, see "IOM®-2 Monitor Channel", page 76, and for the microprocessor mode "Monitor Channel Access", page 101.

Correspondence between MON-2 Messages and SB

The content of the MON-2 message (Table 20) corresponds to the Single Bits in the U-frame (see "U-Frame Structure", page 68). Bit M46 in the MON-2 message, for example, will be inserted at position M46 in the U-frame.

Table 20 Content of MON-2 Message

1. Byte		2. Byte
0 0 1 0	M41 M51 M61 M42	M52 M62 M43 M44 M45 M46 M47 M48
MON-2	Overhead Bits	Overhead Bits

4.2.3.1 Single Bits Transmission on U

Figure 51 sketches roughly how transmitted Single Bits can be accessed.

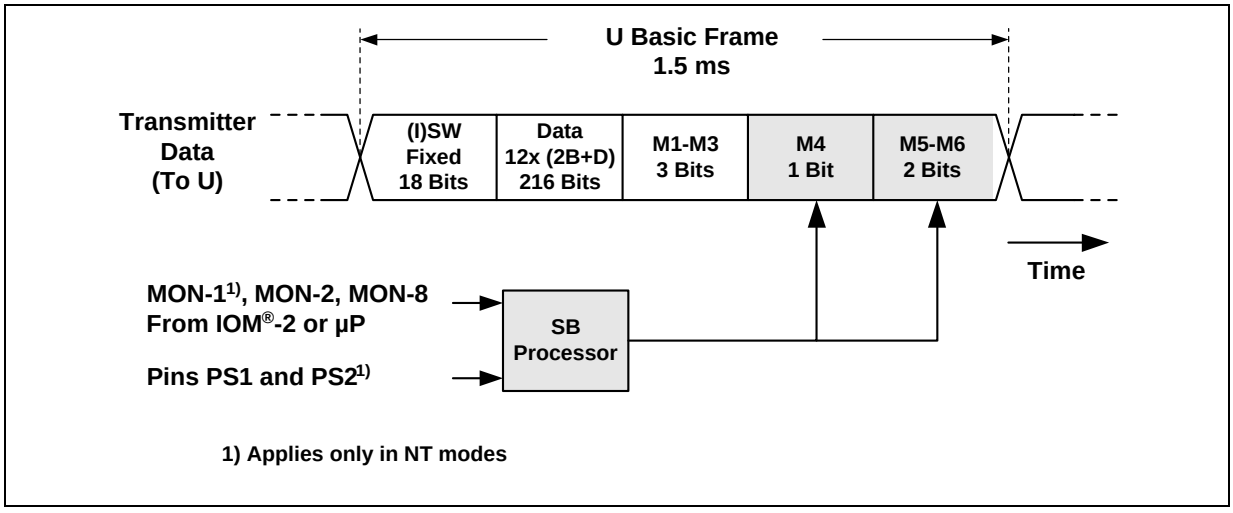


Figure 51 Access to Single Bits Transmission on U

The Single Bits defined by a MON-2 message are latched. I.e. they need to be issued only once. Repetition will be performed by the SB processor. If no MON-2 messages are

1) Exception: The default setting of the repeater modes for SB indication is different than the default setting in other modes, see "Single Bits Reception from U", page 120

issued, the corresponding position in the SB channel will be set to "1", which is the default value after the signal SL2 in the LT modes and SN3 in the NT modes are issued on the U-interface (see state machines, pages 146, 160 and 173).

SB Transmission in NT Modes

Note 34: This section applies if one of the modes NT, NT-Auto Activation, TE and NT-PBX is used (see "Basic Operating Mode", page 50).

The Single Bits will be set in the following manner:

- The Single bit ACT is controlled internally by the activation/deactivation state machine (see "State Machine in NT Modes", page 160)
- Two different ways are available to control the Single bit SAI:
  1- Internally by the activation/deactivation state machine (see "State Machine in NT Modes", page 160), which is the default setting after power up.
  2- By the MON-2 command.
  Control via MON-2 can be set by issuing the MON-8 command PACE. To change this setting back to IEC-Q internal control (1), the MON-8 command PACA can be issued. (See "MON-8 Codes", page 228, for details about codes and programming of these commands).
- The Single bit FEBE is controlled internally by the CRC processor (see "Monitoring Transmission Quality", page 176). In addition the MON-8 message SFB can be issued to set the FEBE bit to "0" once in the next available superframe (test mode, see "MON-8 Codes", page 228, for details MON-8 codes and programming).
- The Single bit CSO is set to "0".
- The Single Bits PS1 and PS2 are programmed directly by the pins PS1 and PS2 respectively (see "Power Controller Pins", page 36 and page 45). any change in the pin polarity will be indicated at the corresponding position and transmitted in the next available superframe (see "Monitoring Primary and Secondary NT Power Supply", page 194).
- The bit NTM is programmed via the M-bits of the MON-1 messages NTM and NORM (see "MON-8 Codes", page 228).
- All of other Single Bits, i.e. M46, M48 M51, M52 and M61 can be set by the user via MON-2 messages.

Table 21 gives an overview of SB control, and Table 22 gives a brief explanation of the function of the SB in this mode.

Table 21 Single Bits Control in NT Modes (Upstream)

Position MON-2/U	NT –> LT	
	Bit	**Control**
M41	ACT	State Machine (IEC-Q)
M51	1	MON-2

Table 21 Single Bits Control in NT Modes (Upstream)

M61	1	MON-2
M42	PS1	Pin PS1
M52	1	MON-2
M62	FEBE	CRC processor (IEC-Q) and MON-8
M43	PS2	Pin PS2
M44	NTM	MON-1
M45	CSO	"0" (IEC-Q)
M46	1	MON-2
M47	SAI	State Machine (IEC-Q) / MON-2
M48	1	MON-2

Table 22 Function of the Predefined SB in NT Modes

Bit	Function
ACT	(Activation bit) The ACT-bit is part of the start-up sequence and is used to indicate layer 2 to be ready for communication. In this case it is set to (1)
CSO	(Cold Start Only) The CSO-bit signals the network side whether the NT is only capable of being started via cold start
SAI	(S Activity Indicator) The SAI-bit informs the LT side about the state of the S-interface. With the S-interface deactivated (i.e. C/I-commands TIM or DI received), the SAI-bit is set to (0). Additionally the bit SAI is used (with SAI = (1)) in a terminal initiated activation (if the U-interface was active before) to request complete NT activation
FEBE	(Far-End Block Error) The FEBE-bit is used to inform the opposite U-interface station that the transmitted data could not be received free of errors. The device sets the FEBE-bit to (0) if errors were observed. Each time a FEBE = (0) is detected, the count of the internal far-end block error counter will be incremented. Additionally it is possible to control the FEBE-bit with the MON-8-message "SFB"

Table 22 Function of the Predefined SB in NT Modes

Bit	Function
PS1	(Power Status Primary Source) The PS1-bit is used to indicate the status of the primary NT power supply. It is set to (1) if the level at pin PS1 is high. PS1 = (1) indicates that the primary power supply is normal
PS2	(Power Status Secondary Source) The PS2 bit is used to indicate the status of the secondary NT power supply. It is set to (1) if the level at pin PS2 is high. PS2 = (1) indicates that the secondary power supply is normal
NTM	(NT Test Mode) This bit informs the network side that the NT is involved in terminal initiated tests and therefore is not available for transparent transmission. The NTM-bit set to (0) indicates that the NT is in a test mode. The NTM-bit is set to (0) with the MON-1 command "NTM" and is reset to (1) by "NORM"

SB Transmission in LT Modes

Note 35: This section applies in LT and COT modes (see "Basic Operating Mode", page 50).

The Single Bits will be set in the following manner:

- The Single Bits ACT and DEA are controlled internally by the activation/deactivation state machine (see "State Machine in LT Modes", page 146).
- Two different ways are available to control the Single bit UOA:
  1- Internally by the activation/deactivation state machine (see "State Machine in LT Modes", page 146), which is the default setting after power up.
  2- By the MON-2 command.
  Control via MON-2 can be set by issuing the MON-8 command PACE. To change this setting back to IEC-Q internal control (1), the MON-8 command PACA can be issued. (See "MON-8 Codes", page 228, for details about codes and programming of these commands).
- The Single bit FEBE is controlled internally by the CRC processor (see "Monitoring Transmission Quality", page 176). In addition the MON-8 message SFB can be issued to set the FEBE bit to "0" (test mode, see "MON-8 Codes", page 228, for details MON-8 codes and programming).
- All other Single Bits, i.e. M43-M46, M48 M51, M52 and M61 can be set by the user via MON-2 messages.

Table 21 gives an overview of SB control, and Table 22 gives a brief explanation of the function of the SB in this mode.

Table 23 Single Bits Control in LT Modes (Downstream)

Position MON-2/U	LT –> NT	
	Bit	Control
M41	ACT	State Machine (IEC-Q)
M51	1	MON-2
M61	1	MON-2
M42	DEA	State Machine (IEC-Q)
M52	1	MON-2
M62	FEBE	CRC processor (IEC-Q) and MON8
M43	1	Pin PS2
M44	1	MON-1
M45	1	"0" (IEC-Q)
M46	1	MON-2
M47	UOA	State Machine (IEC-Q) / MON-2
M48	1	MON-2

Table 24 Function of the Predefined SB in LT Modes

Bit	Function
ACT	(Activation bit) The ACT-bit is part of the start-up sequence and is used to indicate layer 2 to be ready for communication. In this case it is set to (1)
DEA	(Deactivation bit) By setting DEA to (0), the network informs the NT of its intention to turn-off
UOA	(Partial Activation) The UOA-bit is used by the network side to inform the NT that only the U-interface shall be activated (S-interface remains deactivated. If the UOA-bit is set to (0), only the U-interface will be activated
FEBE	(Far-End Block Error) The FEBE-bit is used to inform the opposite U-interface station that the transmitted data could not be received free of errors. The device sets the FEBE-bit to (0) if errors were observed. Each time a FEBE = (0) is detected, the internal far-end block error counter will be incremented. Additionally it is possible to control the FEBE-bit with the MON-8-message "SFB"

SB Transmission in Repeater Modes

Note 36: This section applies to NT-RP and NT-RP modes (see "Basic Operating Mode", page 50).

In these modes all of the Single Bits need to be controlled via MON-2-messages. This permits to implement national repeater specifications for overhead bit treatment. For a short explanation of the function of the SB in both NT and LT modes refer to Tables 22 and 24 above.

4.2.3.2 Single Bits Reception from U

The received Single Bits from the U-interface are forwarded via MON-2 messages to the controller unit[1)] to allow higher layer evaluation of these data.

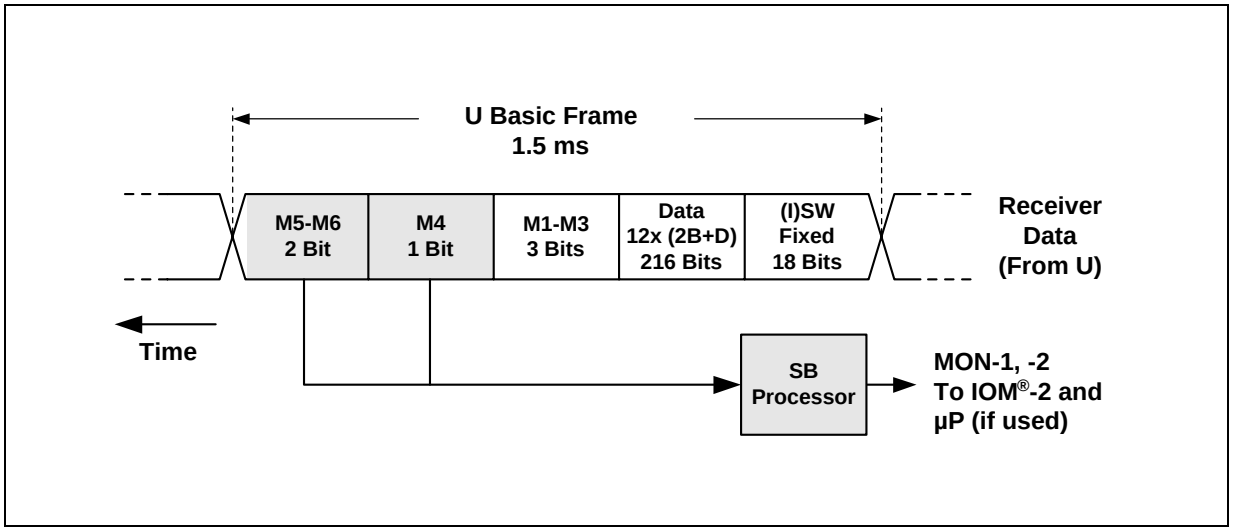


Figure 52 Access to Single Bits Received from U

The IEC-Q Version 5.3 allows almost free control of the conditions for Single Bits verification. Single Bits can be filtered and forwarded in one of the following ways:

- A MON-2 is issued if the polarity of at least one of the Single Bits, other than FEBE, has been changed. (Compatible to Version 5.1).
- A MON-2 message will be issued only if in addition no CRC violations have been detected in the completed last two superframes. (Compatible to all previous IEC-Q versions other than Version 5.1).
- Furthermore, verification of Single Bits changes can be chosen to be controlled by a triple last look processor. Choosing this filtering method will imply that a change in a Single Bit will be issued via MON-2 message only if an identical bit value has been received for three consecutive superframes.

1) Upstream in the LT modes and downstream in the NT modes

The last setting for the M4 bits complies with ANSI T1.601 without need for further software efforts. Note that this is the default setting for the M4 bits in all non repeater modes (see Table 26). Note also that this filtering method setting can be combined with the CRC filtering method.

In addition, the verification of the M4 bits is completely independent of the verification of bits M51, M52 and M61. This allows using the M4 bits in compliance with ANSI T1.601 (Triple Last Look), and still retain the freedom to use bits M51, M52 an M61 for other purposes (i.e. control functions, or even very low rate data transmission).

Control of the Single Bits is mode independent. This allows more flexibility, e.g. in repeater applications.

Selection of the filtering method is controlled via MON-8 messages. It is therefore available in stand-alone mode as well as in µP mode.

Definitions

As selection of the verification method for Single Bits is done via MON-8 messages, it is convenient to recall the format of MON-8 messages, which is given in Table 25 below. For more details on MON-8 messages, see "MON-8 Codes", page 228.

Table 25 Format of MON-8-Messages

1. Byte		2. Byte
1 0 0 0	r | 0 0 0	D7 D6 D5 D4 D3 D2 D1 D0
MON-8	Register | Addr.	Local Command (Message/Data)

r: Register address – 0 = local function register
– 1 = internal register

D0…7 Local command – 00 … FF_H = local function code
– 00 … FF_H = internal register address

The MON-8 commands used to control the verification method are all local functions. The Register bit "r" should therefore be always set to "0".

For definition of the Single Bits, see "Single Bits Channel", page 69. In what follows we will refer to Bits M41 to M48 as "M4 Bits". Bits M51, M52 and M61 will be referred to as "Additional Overhead Bits".

Verification Control for M4 Bits

Table 26 gives the available settings for M4 Bits filtering via MON-8 command.

Table 26 Setting Filtering Method for M4 Bits

Code D7-D0 (Bin)[1)]	Symbol	Function
1000 1110	TLL (Default, not RP)	A change in at least one of the M4 Bits will be passed via MON-2 only after valid triple last look. This is the default setting after reset in all non repeater modes
1000 1101	CRC (Default, RP)	A change in at least one of the M4 Bits will be passed via MON-2 only if the CRC is valid for the last two superframes, not including the current one. This is the default setting after reset in the repeater modes
1000 1111	TLL, CRC	A change in at least one of the M4 Bits will be passed via MON-2 only after valid triple last look, and if the CRC is valid for the last two superframes, not including the current one
1000 1100	On Change	Every change in at least one of the M4 Bits will be passed via MON-2

1) see Table 25 for definition

Verification Control for Additional Overhead Bits

Table 27 gives the available settings for Additional Overhead Bits (M51, M52, M61) filtering via MON-8 command.

Table 27 Setting Filtering Method for Additional Overhead Bits

Code D7-D0 (Bin)[1)]	Symbol	Function
1000 1010	TLL (Default, not RP)	A change in at least one of the Additional Overhead Bits will be passed via MON-2 only after valid triple last look. This is the default setting after reset in all non repeater modes
1000 1001	CRC (Default, RP)	A change in at least one of the Additional Overhead Bits will be passed via MON-2 only if the CRC is valid for the last two superframes, not including the current one. This is the default setting after reset in the repeater modes
1000 1011	TLL, CRC	A change in at least one of the Additional Overhead Bits will be passed via MON-2 only after valid triple last look, and if the CRC is valid for the last two superframes, not including the current one
1000 1000	On Change	Every change in at least one of the Additional Overhead Bits will be passed via MON-2

1) see Table 25 for definition

Reset behavior

MON-2 messages will be issued only if the Receiver is synchronized. This is done to avoid meaningless MON-2 messages if data transmission is not synchronized.

In other words, MON-2 messages will be issued **only** in the following states:

In the **LT Mode** (*page* 147): "Line Active", "Pend. Transparent", "S/T Deactivated", "Pend. Deactivation" and "Transparent".

In the **NT Mode** (page 161): "Synchronized 1", "Synchronized 2", "Wait for Act", "Transparent", "ERROR S/T", "Pend. Deact. S/T", "Pend. Deact. U" and "Analog Loop Back".

In the **LT-Repeater Mode** (*page* 174): "Pend. Transparent", "Transparent", "Pend. Deactivation".

In the **NT-Repeater Mode** (*page* 175): "Synchronized", "Transparent", "ERROR", "Pend. Deact." and "Analog Loop Back".

Mode setting via MON-8 will be reset only if the "Test" state is entered (see "State Machine in LT Modes", page 146), i.e. after UVD, Hardware Reset, Software Reset or Power-On Reset.

4.2.4 Setting Superframe Marker

In the NT and TE modes, with superframe marker selected (see "Setting Modes of Operation (Stand-Alone and µP Mode)", page 51) the start of a new superframe is indicated with a FSC high-phase lasting for one single DCL-period. A FSC high-phase of two DCL-periods is transmitted for all other IOM®-2-frame starts.

In LT modes the superframe marker can be indicated by a short frame synchronization signal (FSC) of the IOM®-2 interface. If the high phase of FSC lasts one DCL period or less, the U-interface frame will be reset and the Inverted Synchronization Word (ISW) will be inserted at the beginning of the next available basic frame. The remaining 95 FSC-clocks must be of at least two DCL-periods duration. If no superframe marker is to be used, all FSC high-phases need to be of at least two DCL-periods duration.

The relationship between the IOM®-2-superframe marker of the slave, the U-interface, and the IOM®-2 superframe marker of the master is fixed after activation of the U-interface. I.e. data inserted on LT side in the first B1-channel after the IOM®-2-slave superframe marker will always appear on the NT side with a fixed offset, e.g. in the 5th B1-channel after the master superframe marker. After a new activation this relationship (offset) may be different.

Superframe Marker Enable in µP Mode

Note 37: This feature is only available in the µP-LT Modes.

As mentioned above, in LT modes the superframe marker can be indicated by a short frame synchronization signal (FSC) of the IOM®-2 interface. Consequently, spikes on the FSC might be unintentionally recognized as superframe marker by the IEC-Q. In most cases (> 85%) such a spike will introduce permanent high bit error rate. It is therefore very important to make sure, that no spikes on pin FSC could occur. However, cases were reported where spikes on pin FSC couldn’t be avoided.

Version 5.3 of the IEC-Q offers a way to overcome this problem. Setting bit SFEN of register ADF2 (see "ADF2-Register", page 214) to "0" will disable the superframe marker function. This prevents spikes on FSC to trigger superframes. Bit errors caused by the additional FSC pulses will not last longer than 3 IOM®-2 frames.

Note 38: Setting ADF2:SFEN to "0" will introduce the same behavior as Version 5.2 (refer to the corresponding point in Delta Sheet of the PEB/F 2091 V5.2). However, the value of ADF2:SFEN after reset will be "1", which means that the superframe marker function is enabled by default and therefore compatible to all IEC-Q versions up to 5.1.

4.3 Layer 1 Activation and Deactivation

The IEC-Q is designed to meet the newest standards of ANSI and ETSI regarding status control. The following sections describe some of the most important protocols implemented in the IEC-Q. They illustrate the interaction between the stations involved. All information presented in this section is extracted from the state machines (see "State Machines", page 145).

Table 28 shows all U-interface signals as defined by ANSI.

Table 28 U-Interface Signals

Signal	Synch. Word (SW)	Superframe (ISW)	2B + D	M-Bits
NT –> LT				
TN[1)]	± 3	± 3	± 3	± 3
SN0	no signal	no signal	no signal	no signal
SN1	present	absent	1	1
SN2	present	absent	1	1
SN3	present	present	1	normal
SN3T	present	present	normal	normal
LT –> NT				
TL[1)]	± 3	± 3	± 3	± 3
SL0	no signal	no signal	no signal	no signal
SL1	present	absent	1	1
SL2	present	present	0	normal
SL3[2)]	present	present	0	normal
SL3T	present	present	normal	normal
Test Mode				
SP[3)]	± 3			

1) Alternating ± 3 symbols at 10 kHz

2) Must be generated by the exchange

3) Alternating ± 3 single pulses of 12.5 µs duration spaced by 1.5 ms, else no signal

4.3.1 Complete Activation Initiated by LT

Figure 53 depicts the procedure if the activation has been initiated by the exchange side. If activation is initiated with the C/I code AR, as shown in Figure 53, activation will fail if the signal SN3 hasn't been correctly received within 15 seconds. In this case the LT side will indicate the C/I code EI3 instead of UAI and the device should be reset (see "LT Modes State Diagram", page 147). In normal LT-NT configurations these 15 seconds are much longer than average activation time which lies between 1-7 seconds, depending on line characteristics, i.e. if this timer expires it is a strong indication for an error condition.

In some configurations, however, e.g. a line with several repeaters, this timer could expire under normal activation condition. For such configurations the IEC-Q provides the C/I command ARX which can be used instead of the command AR for activation. If activated with the ARX command the IEC-Q will continue the activation procedure, even if the 15 seconds timer has expired.

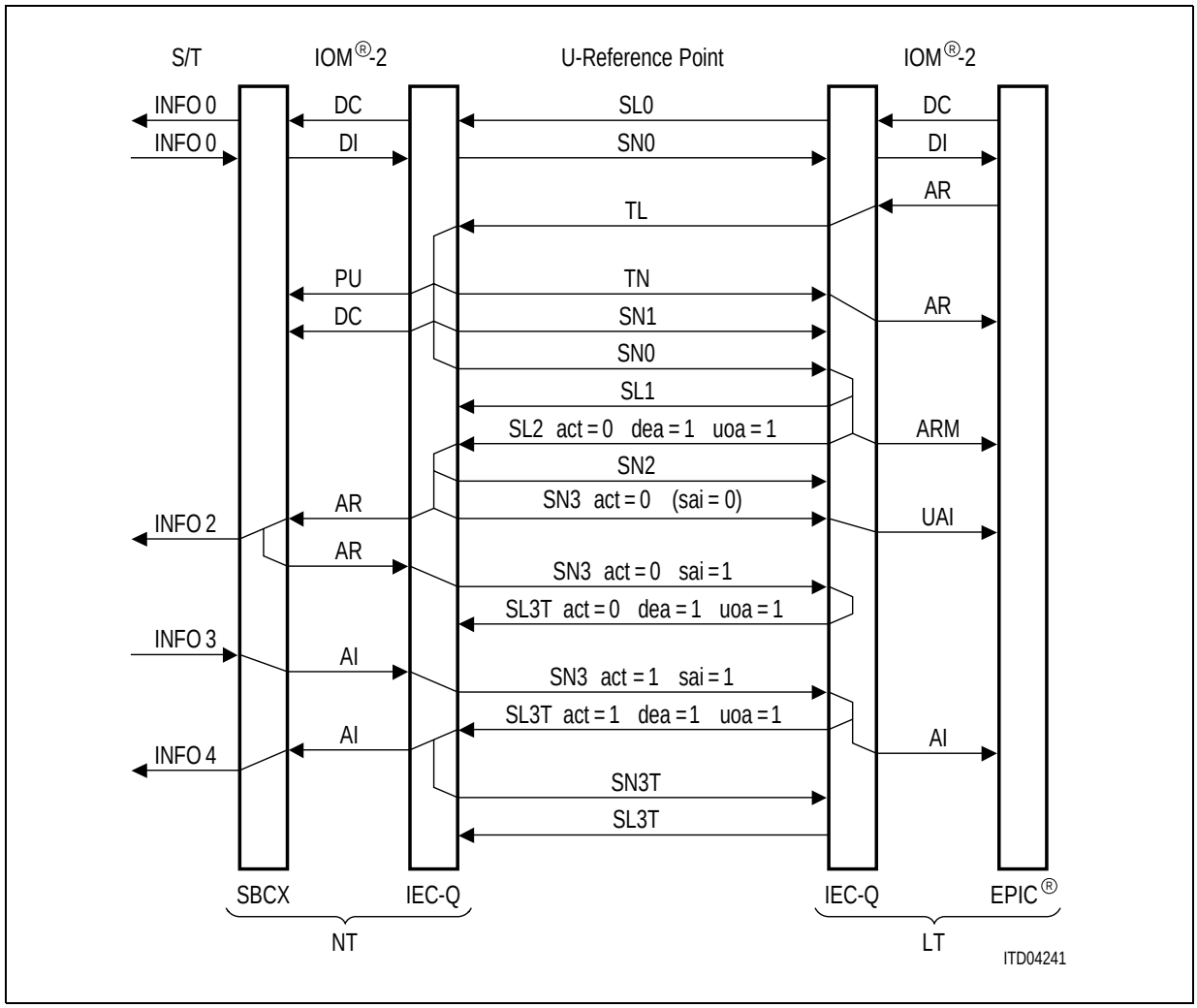


Figure 53 Complete Activation Initiated by LT

4.3.2 Activation with ACT-Bit Status Ignored by the Exchange Side

Activation with C/I-command "AR0" forces the state machine into the state "Line Active" independently of the ACT-bit status transmitted upstream from the network. Activation may be completed after the ACT-bit evaluation has been enabled with C/I-command "AR".

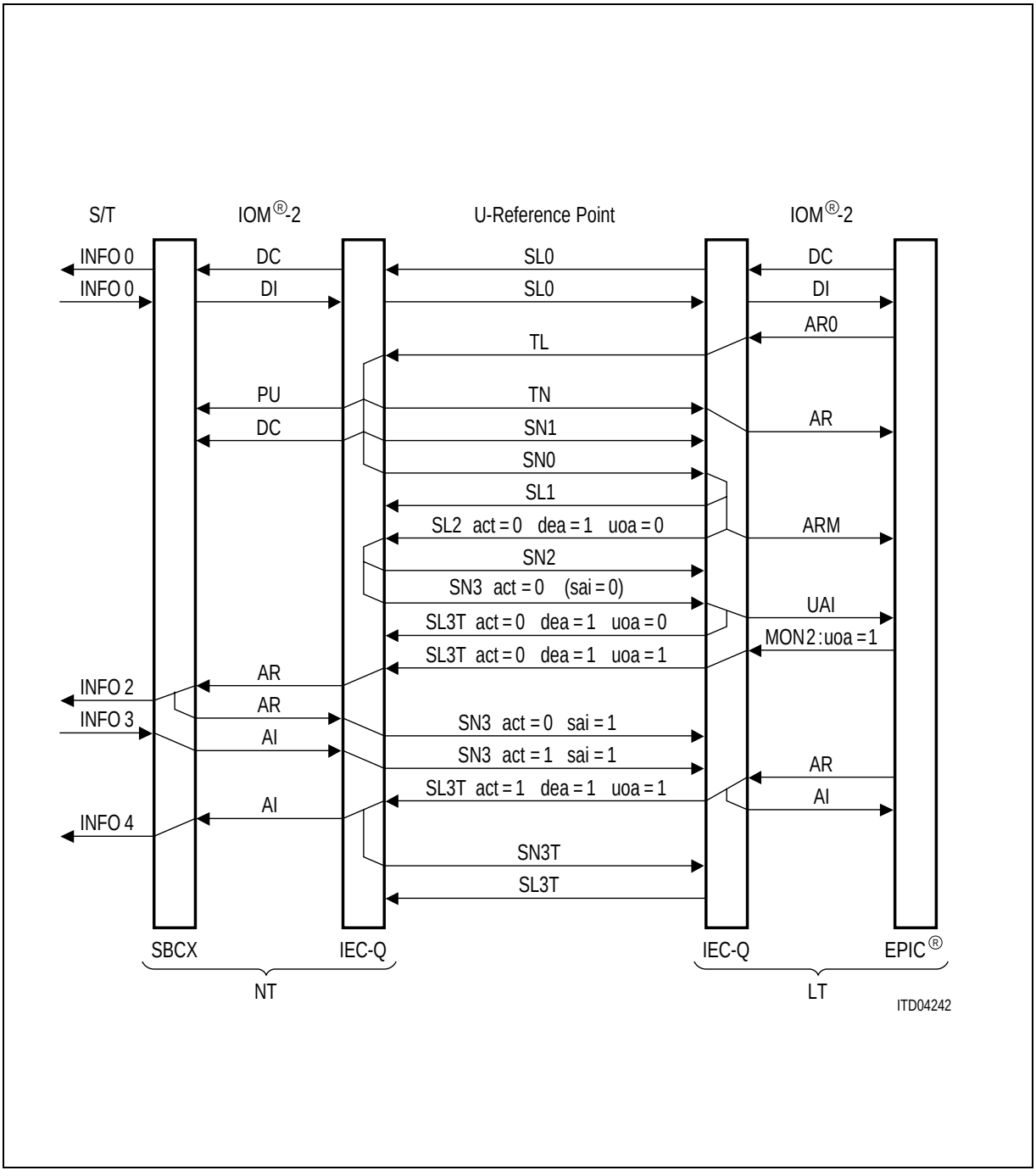


Figure 54 Activation with ACT-Bit Status Ignored by the Exchange

4.3.3 Complete Activation Initiated by TE

Figure 55 depicts the procedure if the activation has been initiated by the terminal side.

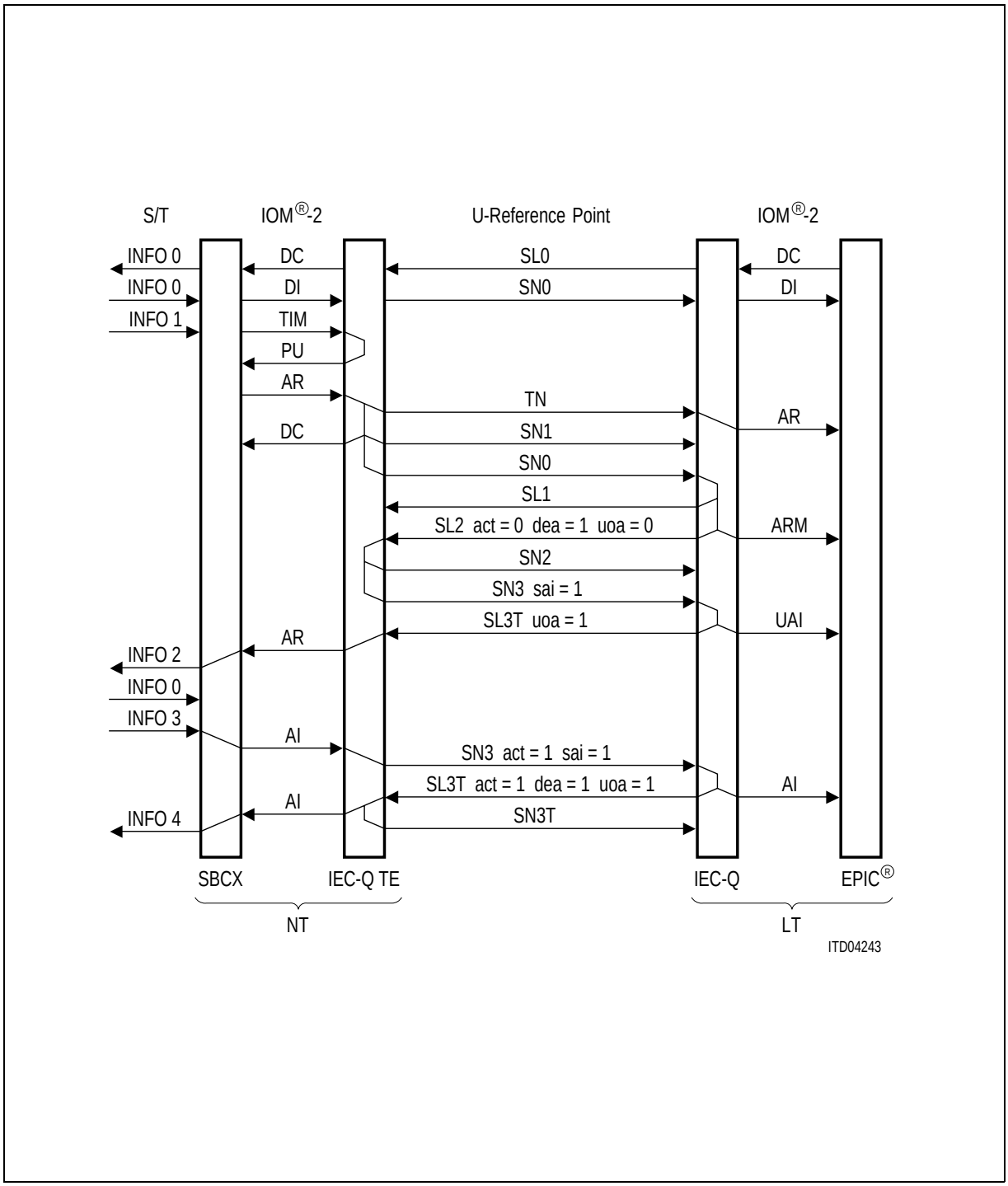


Figure 55 Complete Activation Initiated by TE

4.3.4 Complete Deactivation

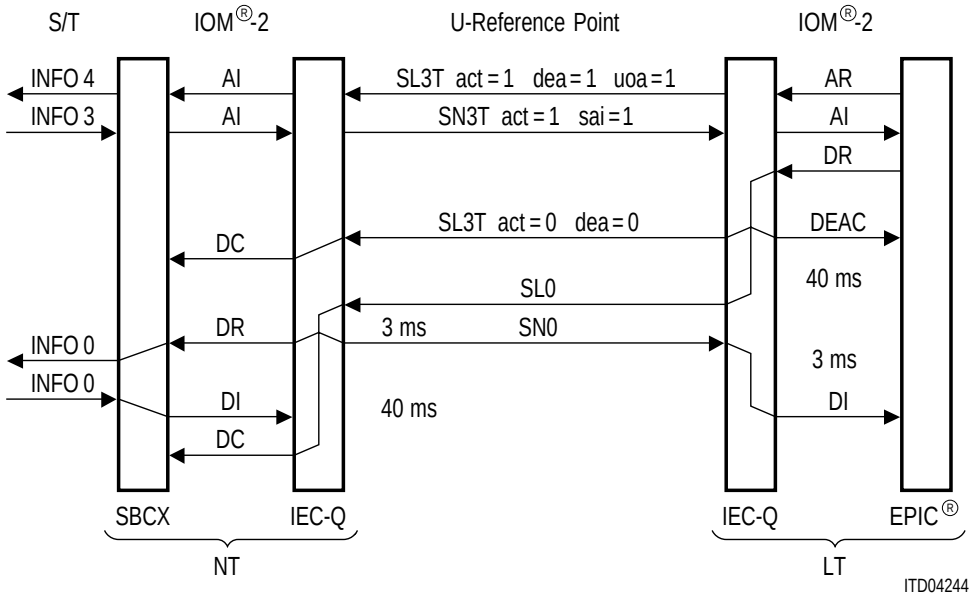


Figure 56 Complete Deactivation

4.3.5 Partial Activation (U Only)

The IEC-Q is in the "Synchronized 1" state (see "State Machine in NT Modes", page 160) after a successful partial activation. IOM®-2-clocks DCL and FSC are issued. On DOUT the C/I-message "DC" as well as the LT user data is sent.

While the C/I-messages "DI" (1111_B) or "TIM" (0000_B) are received on DIN, the IEC-Q will transmit "SAI" = (0) upstream. Any other code results in "SAI" = (1) to be sent. On the U-interface the signal SN3 (i.e. 2B + D = (1)) will be transmitted continuously regardless of the data on received from the downstream side.

The LT will transmit all user data transparently downstream (signal SL3T). In case the last C/I command applied is "UAR", the LT retains activation control when an activation request comes from the terminal (confirmation with C/I = "AR" required, see page 132 (case 1)). With C/I "DC" applied from the upstream device, TE initiated activations will be completed without the necessity of an exchange confirmation (page 133 (case 2)).

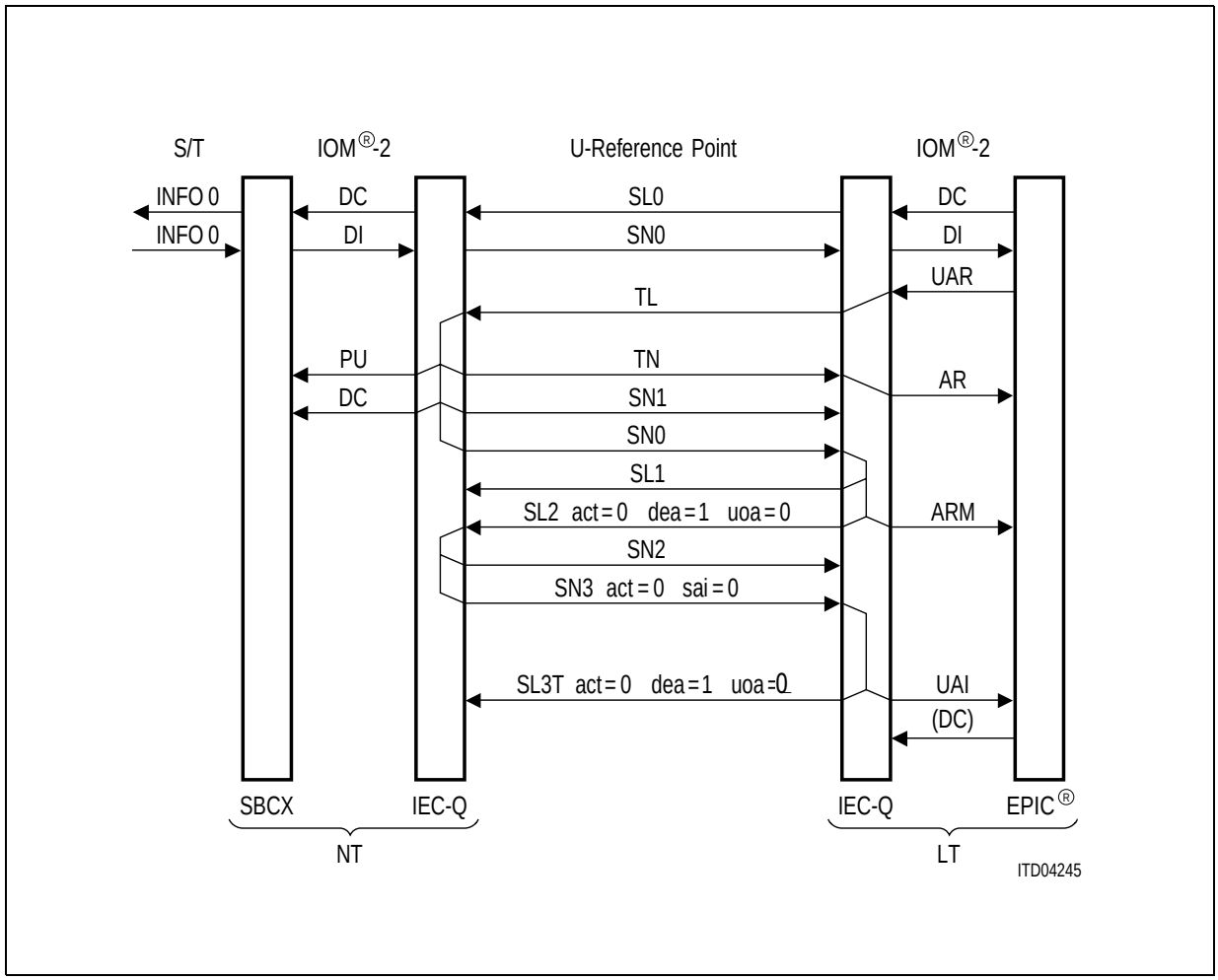


Figure 57 U Only Activation

4.3.6 Activation Initiated by LT with U Active

The S-interface is activated from the exchange with the command "AR". Bit "UOA" changes to (1) requesting S-interface activation.

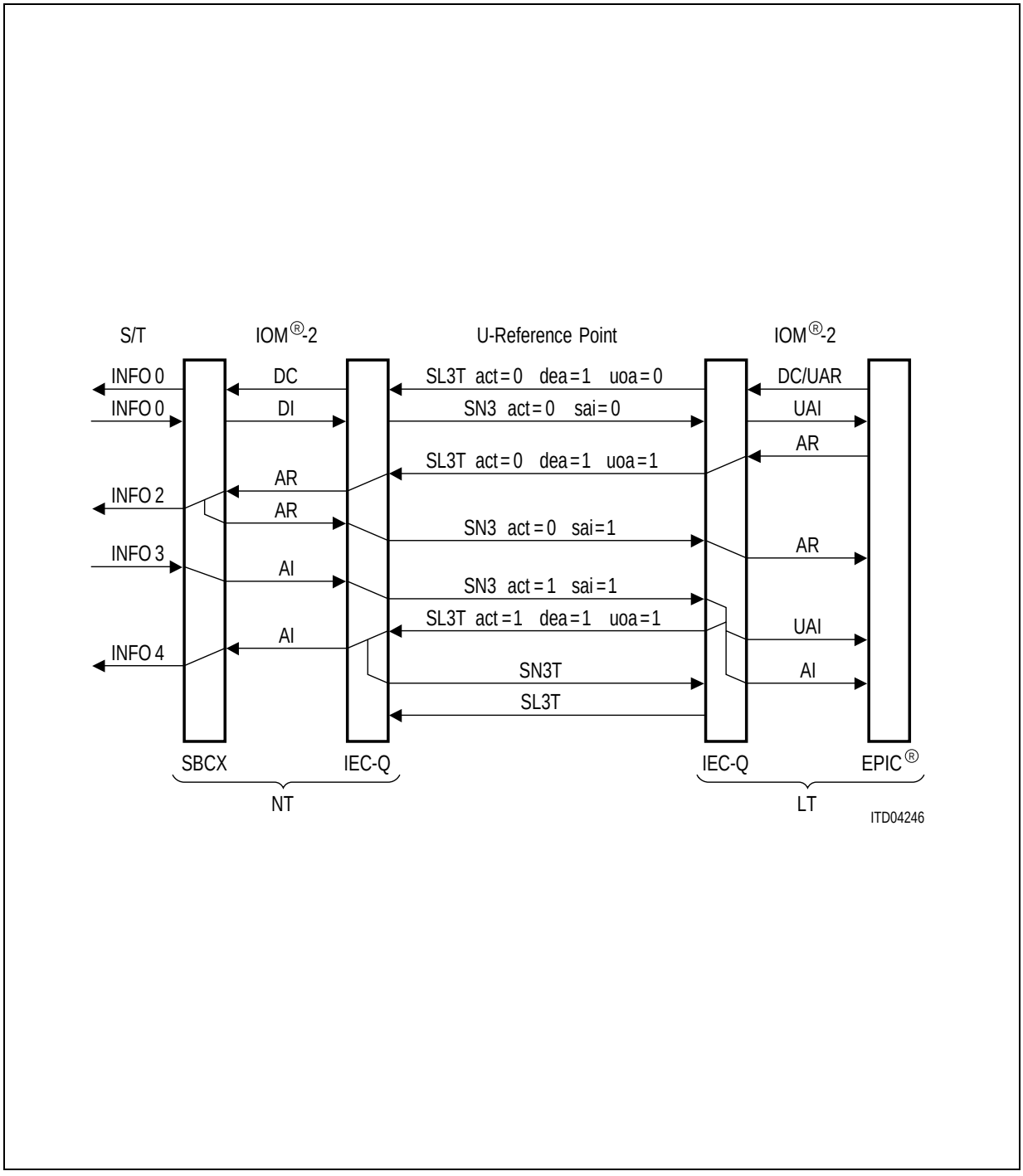


Figure 58 LT Initiated Activation with U-Interface Active

4.3.7 Activation Initiated by TE with U Active

The TE initiates complete activation with INFO 1 leading to "SAI" = (1). Case 1 requires the exchange side to acknowledge the TE activation by sending C/I = "AR", Case 2 activates completely without any LT confirmation.

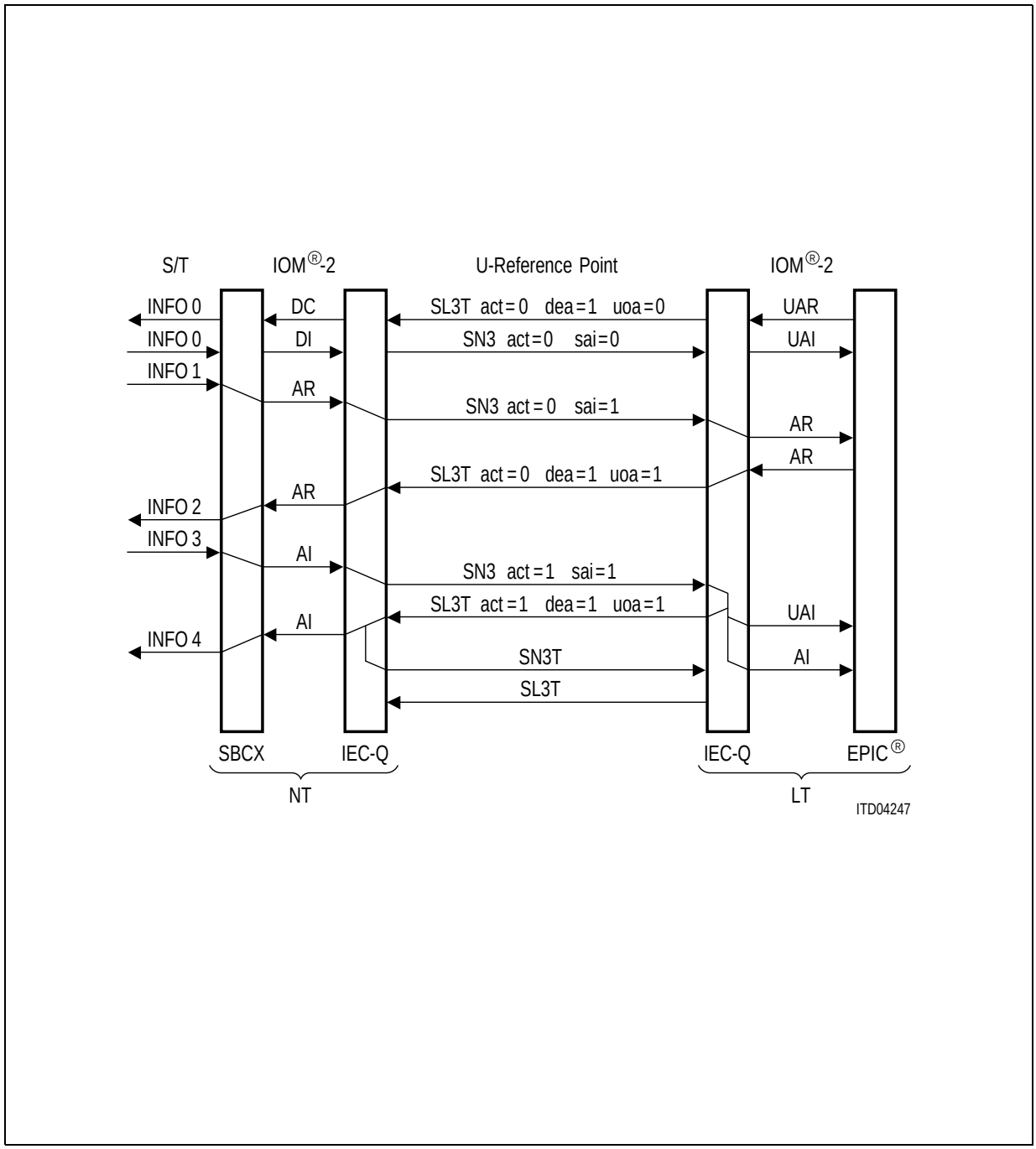


Figure 59 TE Activation with U Active and Exchange Control (case 1)

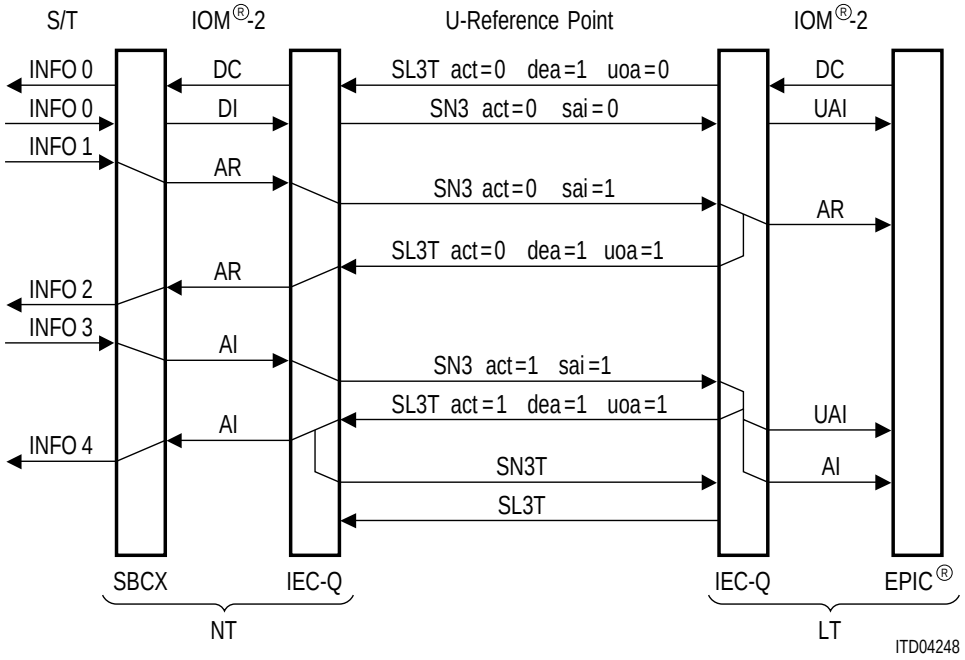


Figure 60 TE Activation with U Active and no Exchange Control (case 2)

4.3.8 Deactivating S/T-Interface Only

Deactivation of the S-interface without deactivating the U-interface is initiated from the exchange by setting the "UOA" bit = (0).

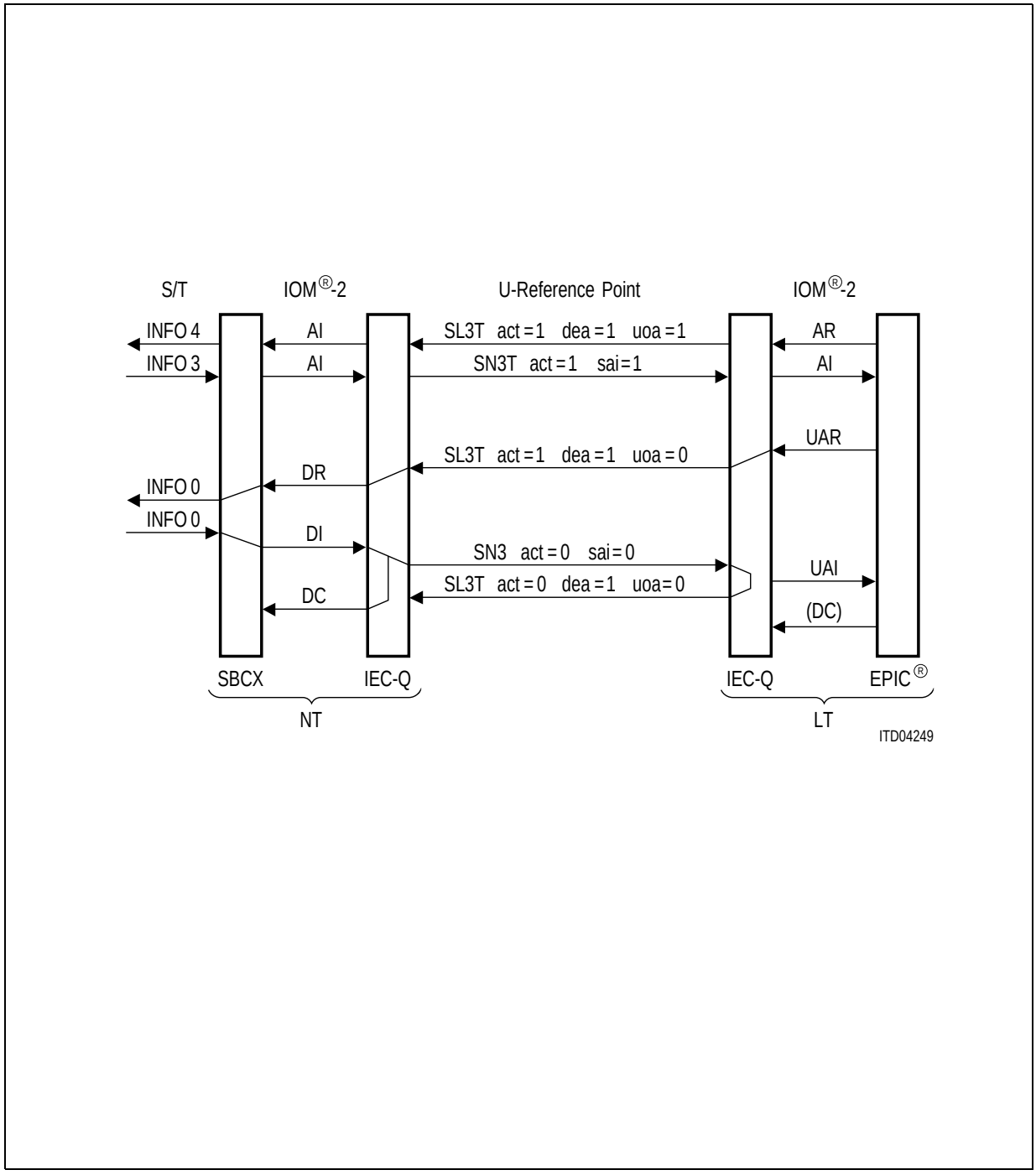


Figure 61 Deactivation of S/T Only

4.3.9 Activation Initiated by LT with Repeater

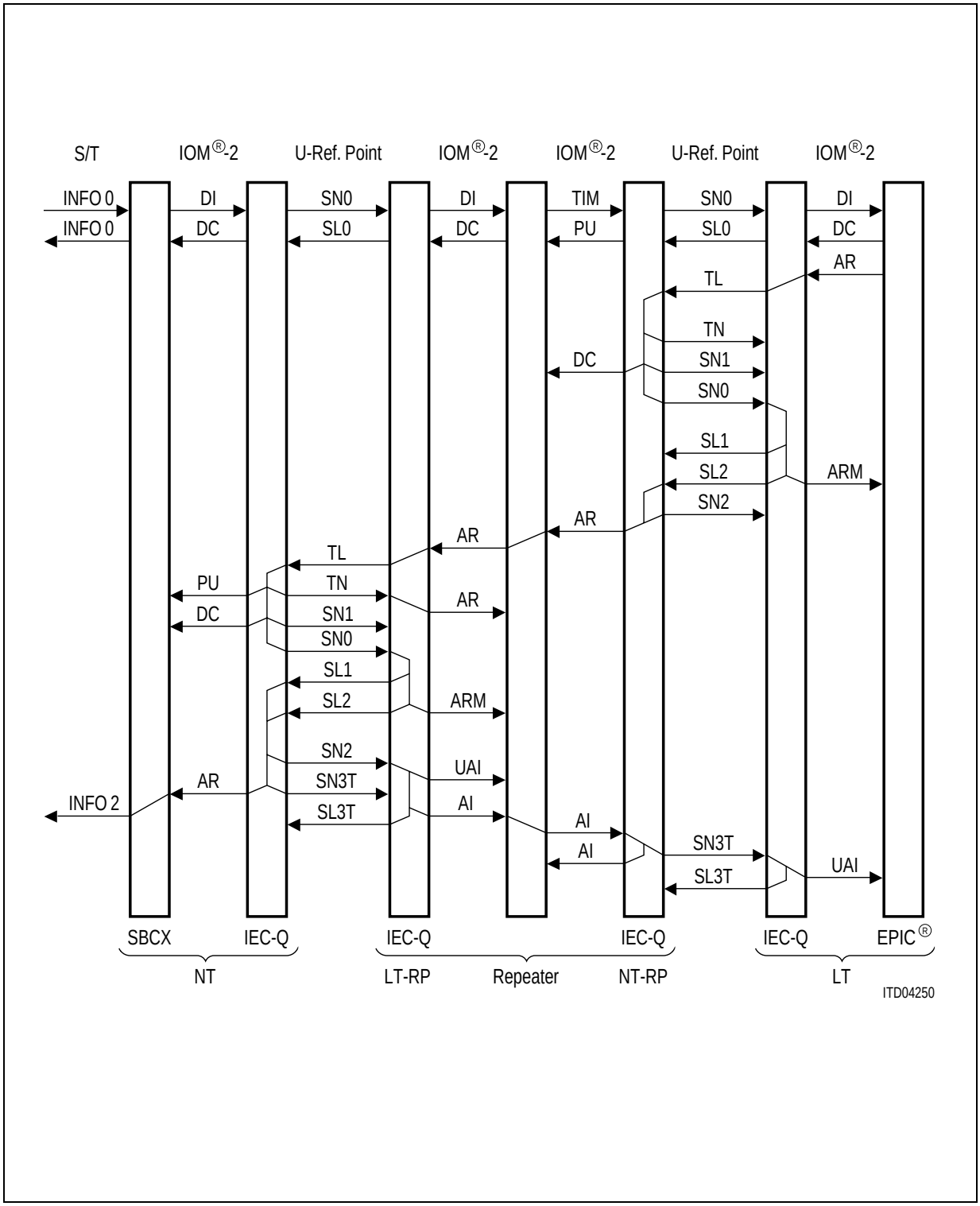


Figure 62 Activation with Repeater Initiated by LT

4.3.10 Activation Initiated by TE with Repeater

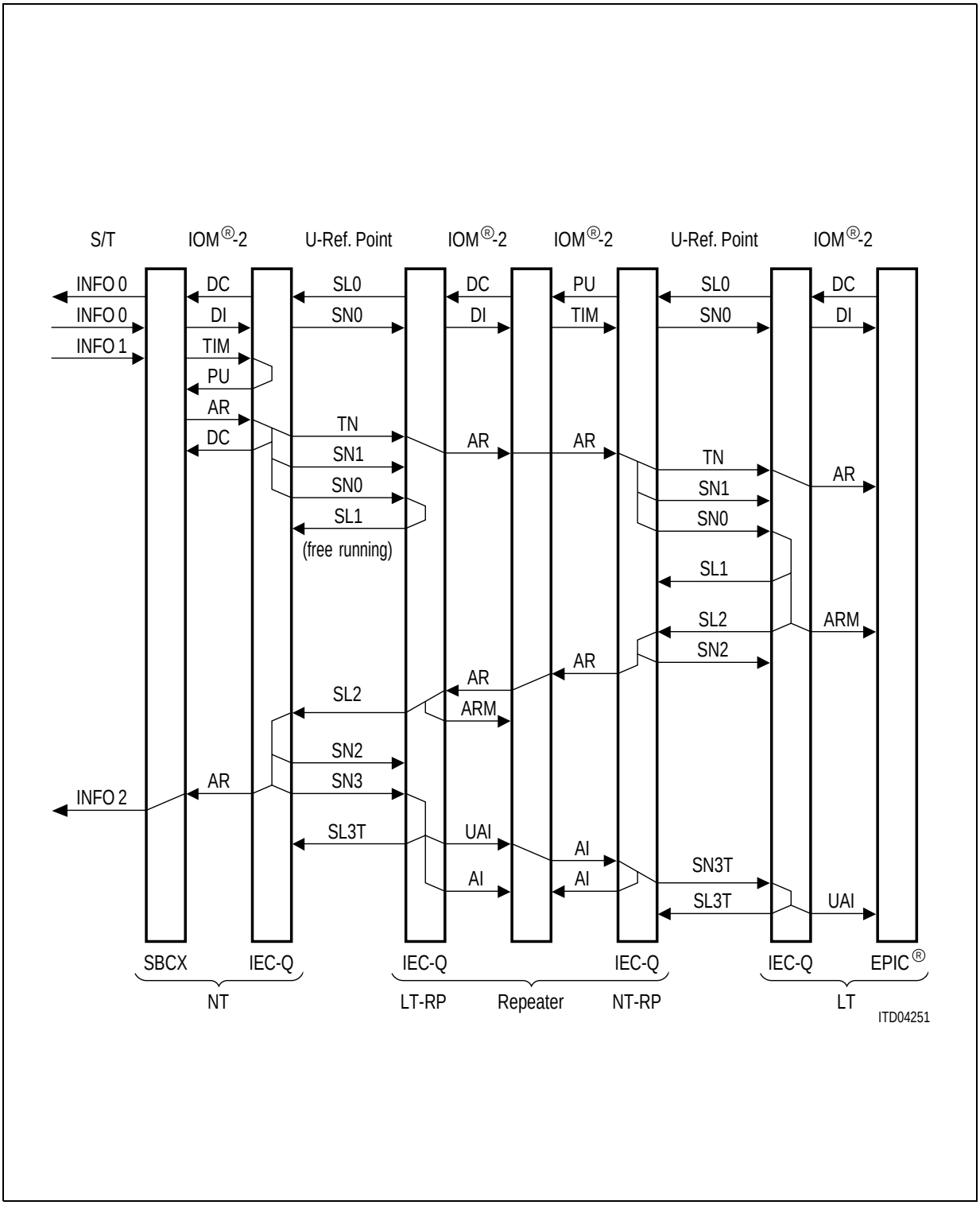


Figure 63 Activation with Repeater Initiated by TE

4.3.11 Loss of Synchronization / Signal at Repeater

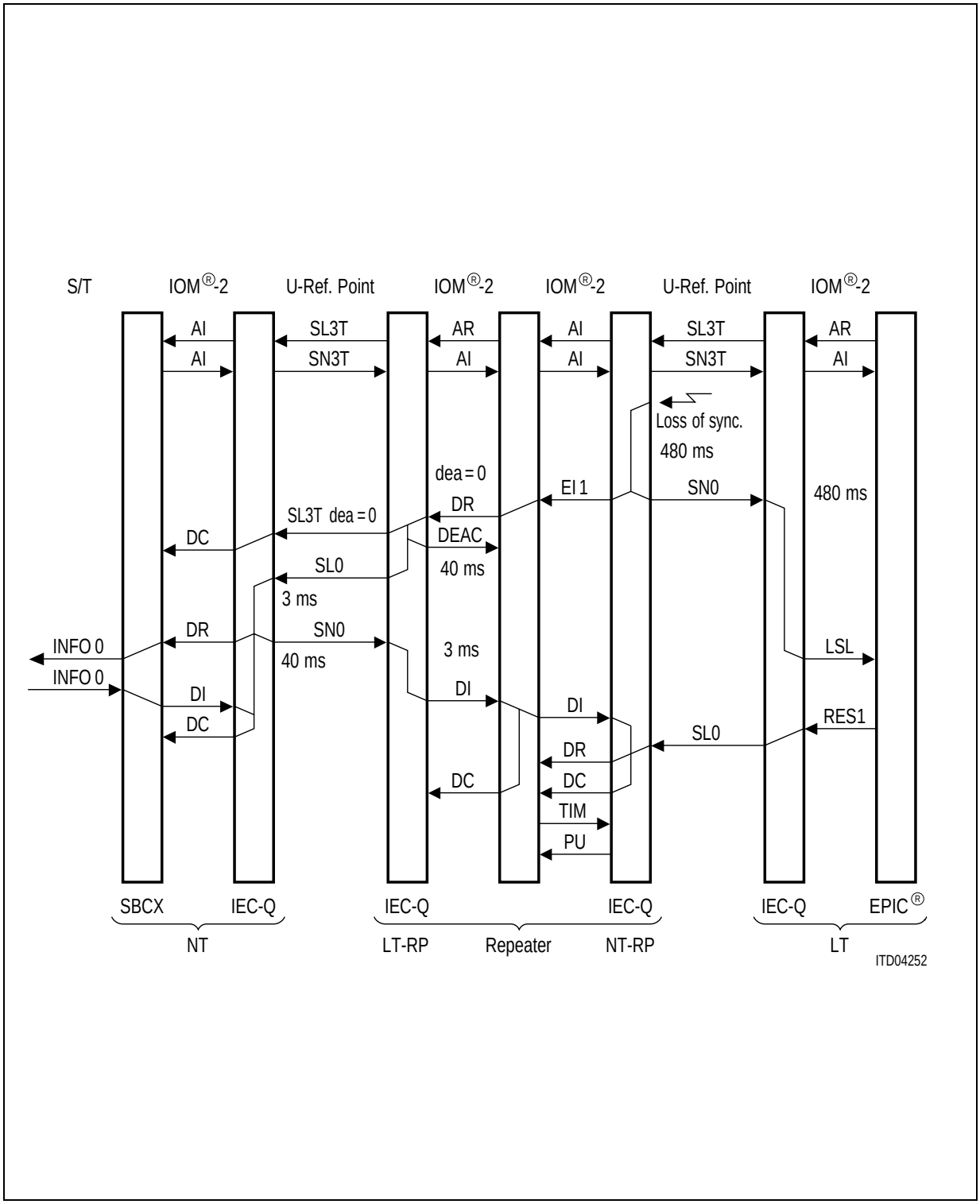


Figure 64 Loss of Synchronization at Repeater (LT Side)

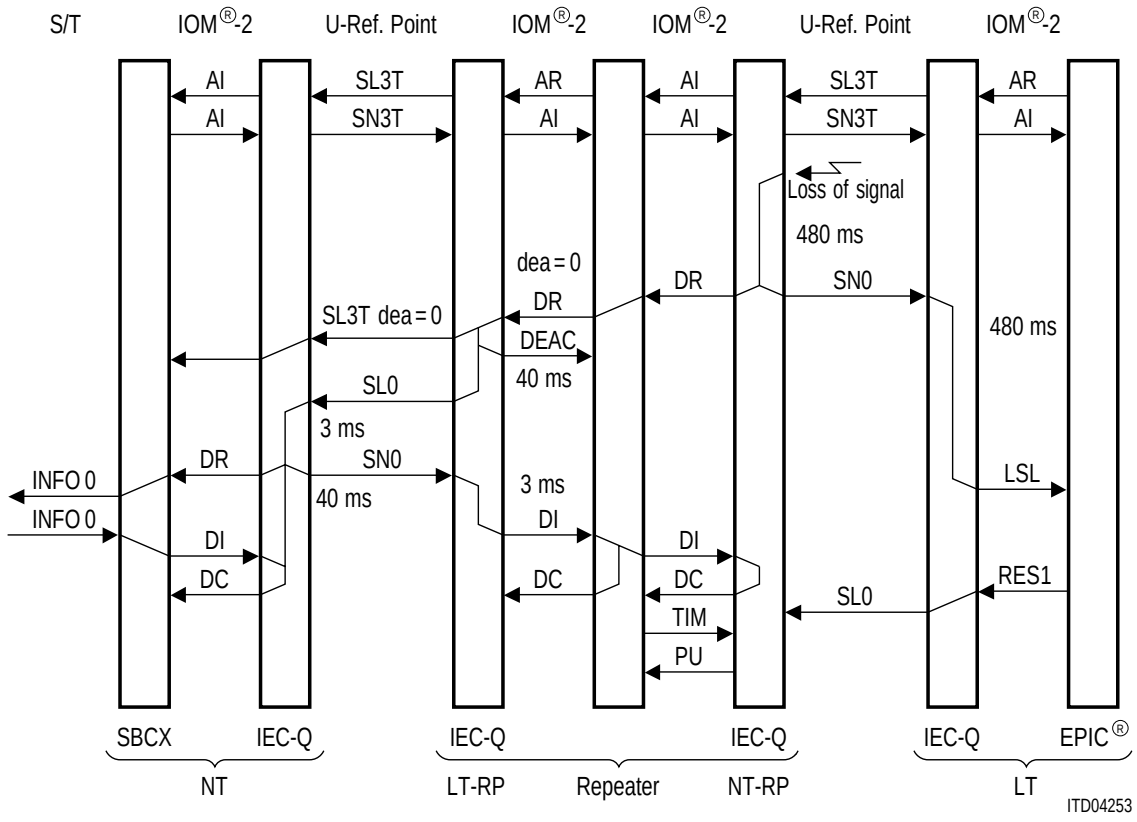


Figure 65 Loss of Signal at Repeater (LT Side)

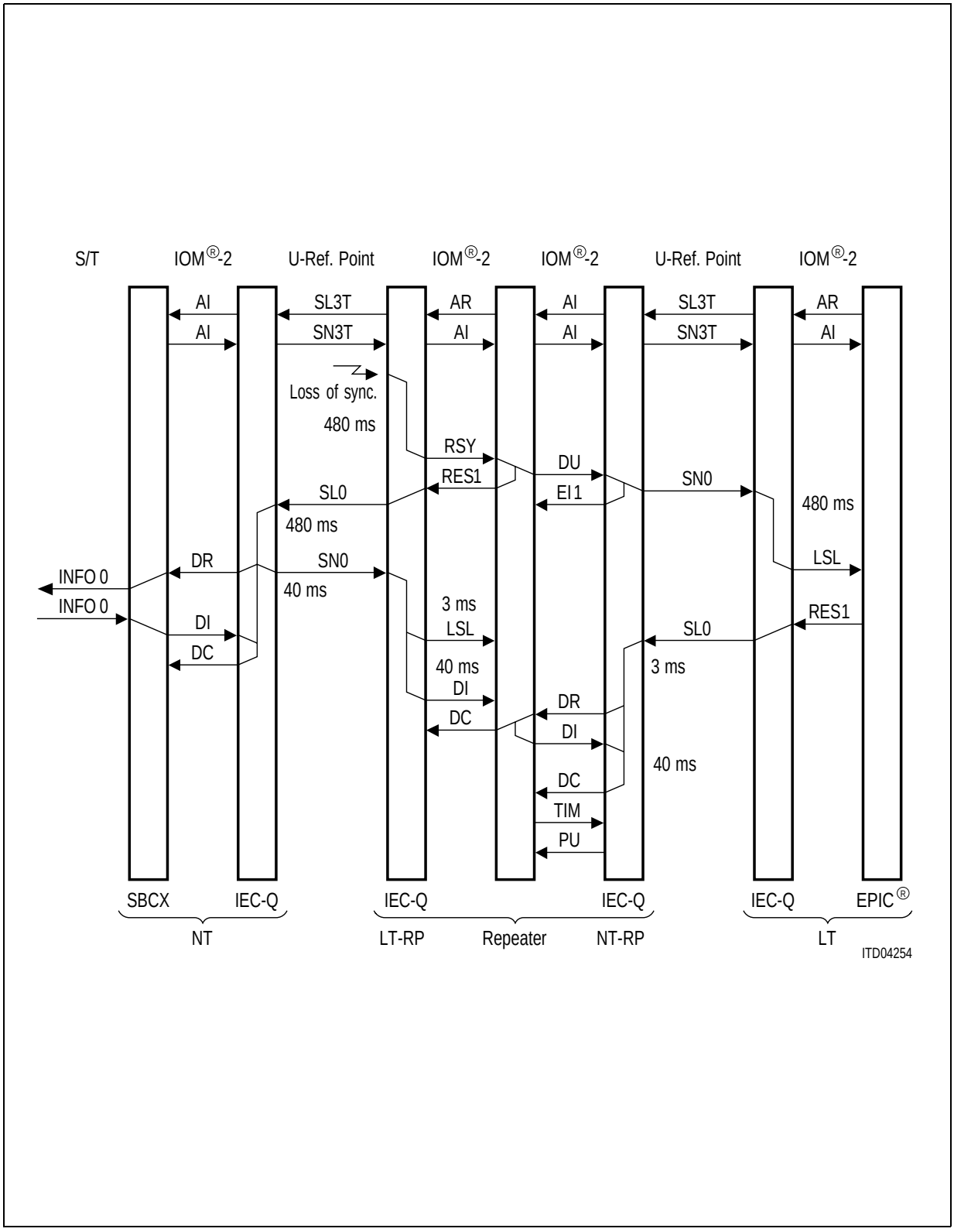


Figure 66 Loss of Synchronization at Repeater (NT side)

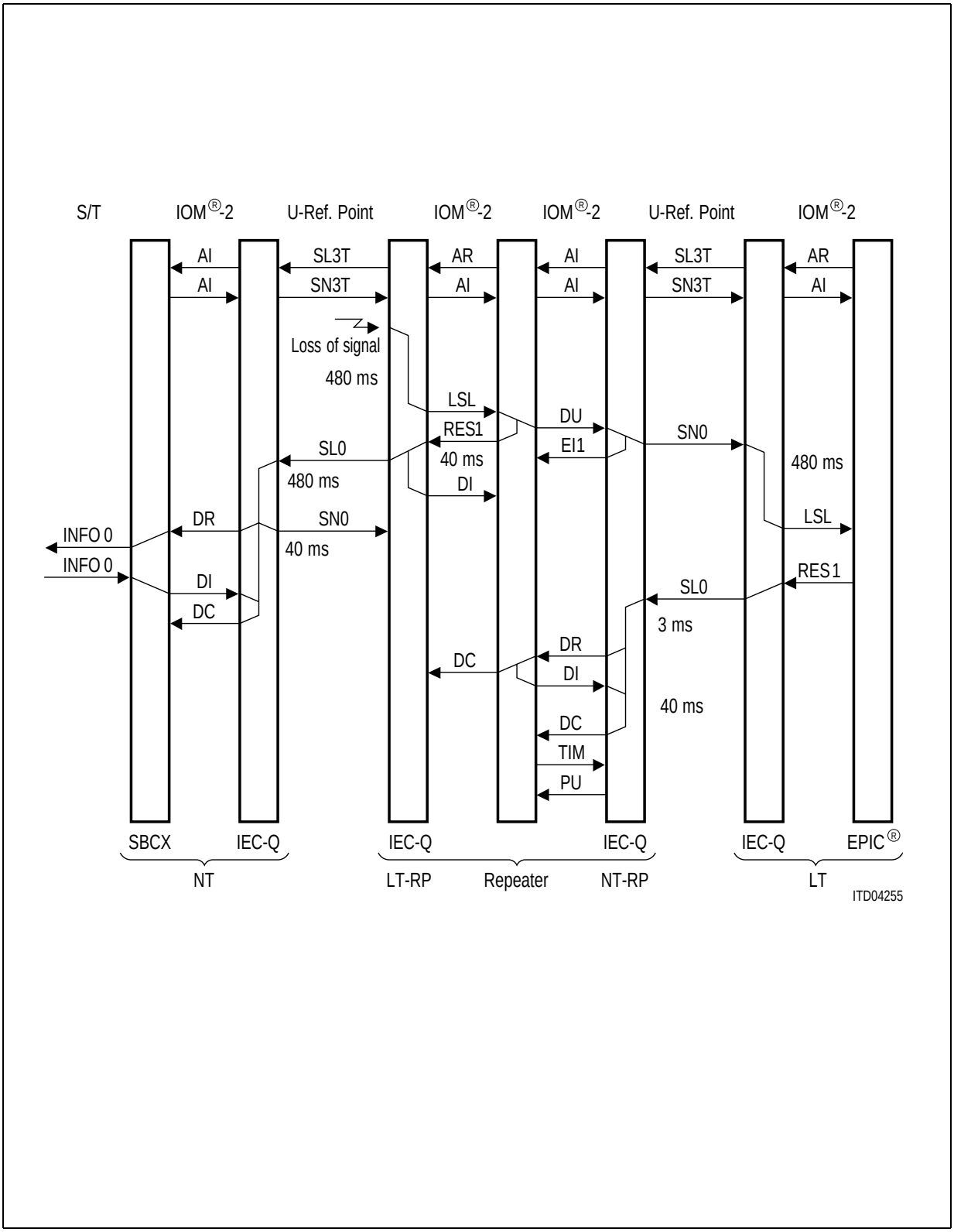


Figure 67 Loss of Signal at Repeater (NT side)

4.3.12 Deactivation with Repeater

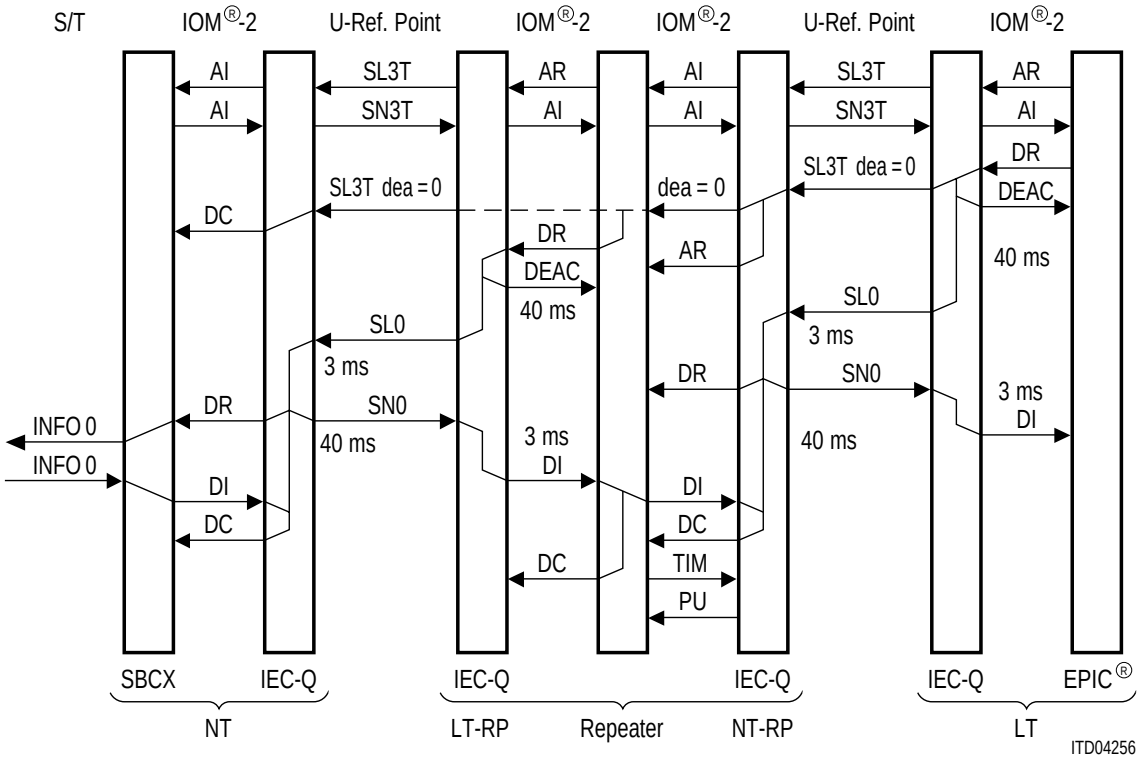


Figure 68 Deactivation with Repeater

4.3.13 Activation Attempt Initiated by NT in NT-Auto Activation Mode

Note 39: See "Basic Operating Mode", page 50, for setting this mode.

If the LT transceiver is available and ready for activation, e.g. if the LT is not in the reset or in any test state, the NT IEC-Q will start in this mode one single activation attempt after leaving the "TEST" state, i.e. after being reset. In this case activation proceeds as described in the previous sections.

However, If the LT is not ready for activation, the NT will periodically start a new activation attempt every 15 seconds, till the LT side will be available and ready for activations initiated by the NT side. See "State Transition Diagram in NT-Auto Activation Mode", page 162.

4.3.14 Activation in the µP-NT Mode

Note 40: This function is only available if the NT mode in conjunction with the microprocessor mode (PMODE = "1") are used. Note also that if the IOM®-2 clock disable mode is set (see "IOM®-2 Enable/Disable Mode", page 53) activation in µP NT mode without IOM®-2 will not be possible.

In some NT and TE applications in the µP mode, the IOM®-2 interface is functionally not needed (e.g. inband signaling, some PC card applications etc.). In such cases it is possible to control the internal state of the pin DIN via the MSB of the CIWU register (see "CIWU-Register", page 217). Setting the SPU (software power up) bit to "0" in the NT mode will cause the DIN signal to be set internally to "0", regardless of the value of the pin DIN. Setting the SPU bit to "1", which is the default value after reset, will set the pin DIN transparent to the internal circuit, see Figure 69 below.

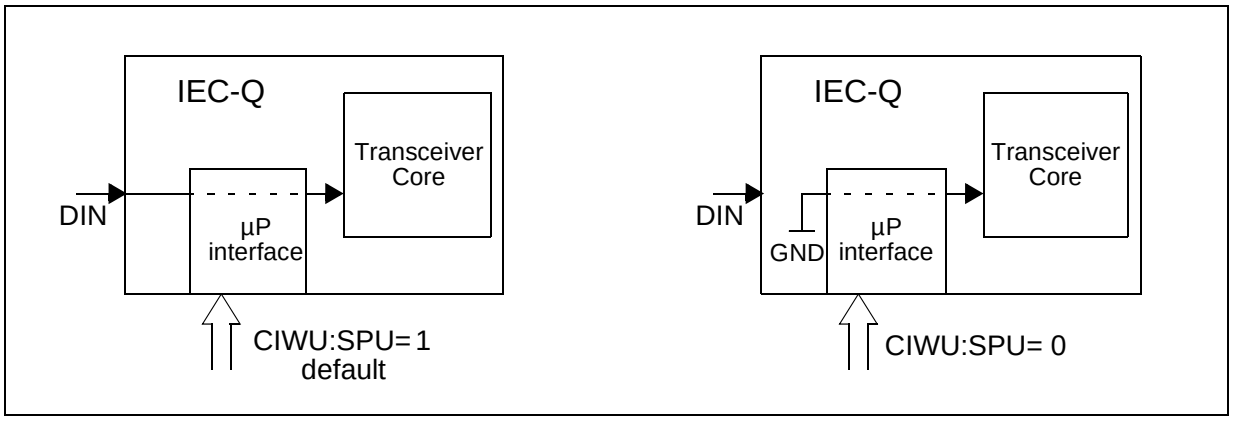


Figure 69 DIN Control via CIWU:SPU in NT µP Mode

Example for Activation with µP

Assumption: The C/I-Channel is being controlled via µP (i.e., SWST:CI=1, see "C/I Channel Access", page 100).

To activate the IEC-Q in NT mode from power down without external control of the pin DIN the following procedure has to be used:

- Set the SPU bit to "0" in the CIWU-register (see "CIWU-Register", page 217)
- Write C/I-command "TIM" (0_H)
- Read the CIRU register after receiving the ISTA:CICU interrupt and verify that the C/I code "PU" (7_H) has been indicated
- Write the C/I-command "AR" (8_H) in combination with setting the SPU bit to "1" in the CIWU register

4.3.15 Upstream Wake-Up Indication in the LT Repeater Mode

In repeater applications the IOM®-2 clocks are usually delivered by the NT repeater (see "Repeater Modes", page 87). In power down the IOM®-2 clock will be shut down. During power down the reception of a wake up tone from downstream will therefore not be indicated on C/I Channel in upstream direction.

The IEC-Q is equipped with an internal wake up detection function which doesn't depend on IOM®-2[1]. In the Deactivated state of the LT Repeater mode the pin DOUT will be clamped to "0" if a wake-up tone from down stream is detected and if no Monitor Channel command is active or pending (in both up and down stream directions)[2]. This allows connecting pin DOUT of the LT repeater directly to pin DIN of the NT repeater, and activation initiated by the TE will be carried out without restrictions, as Figure 70 below and the example thereafter show.

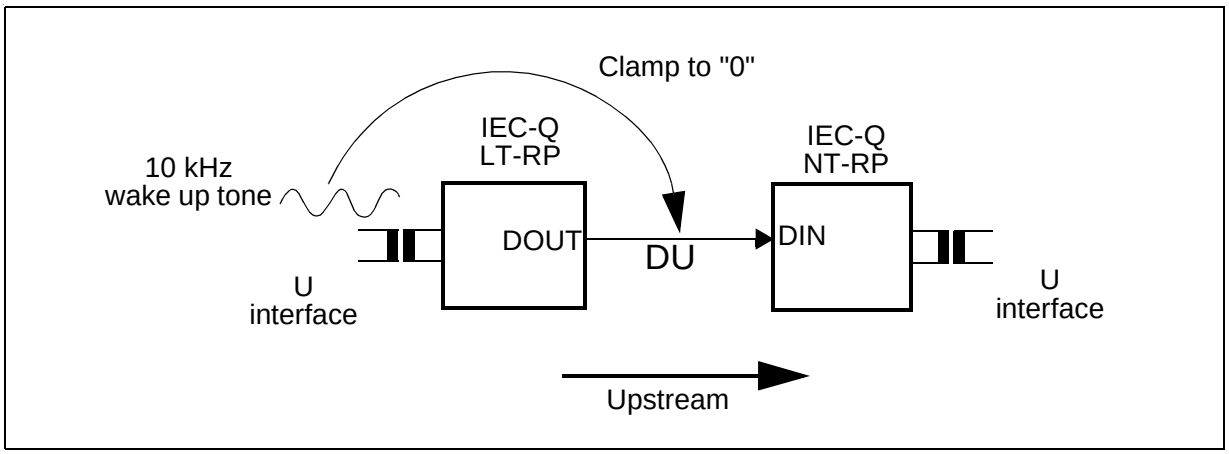


Figure 70 Wake Up Indication in Repeater Power Down

1) Note that the 15.36 MHz master clock will still be required. Version 5.3 provides such a clock on pin CLS in the NT repeater mode. Refer to "NT Repeater", page 88
2) To achieve this, all Monitor Channel commands and indications of the LT Repeater should be completed before the NT Repeater enters the power down state

Example: Repeater activation initiated by the terminal

- NT and LT repeater are in power down. No Monitor Channel command is active or pending.
- A wake-up tone is received from downstream.
- The LT repeater pulls DOUT low which is detected by the NT repeater on DIN.
- The NT repeater activates the IOM®-2 interface (see "State Transition Diagram NT-Repeater Mode", page 175).
- The LT repeater moves to the Awake state and DOUT will be released to indicate AR on the C/I Channel. Note that the C/I command DC must be given on DIN (see "State Transition Diagram LT-Repeater Mode", page 174).
- Activation takes now place as described in "Activation Initiated by TE with Repeater", page 136.

4.4 State Machines

4.4.1 State Machine Notation Rules

The state machine includes all information necessary for the user to understand and predict the activation/deactivation status of the IEC-Q. The information contained in a state bubble is:

– State name
– U-signal transmitted
– Overhead bits transmitted
– C/I-code transmitted
– Transition criteria
– Timers

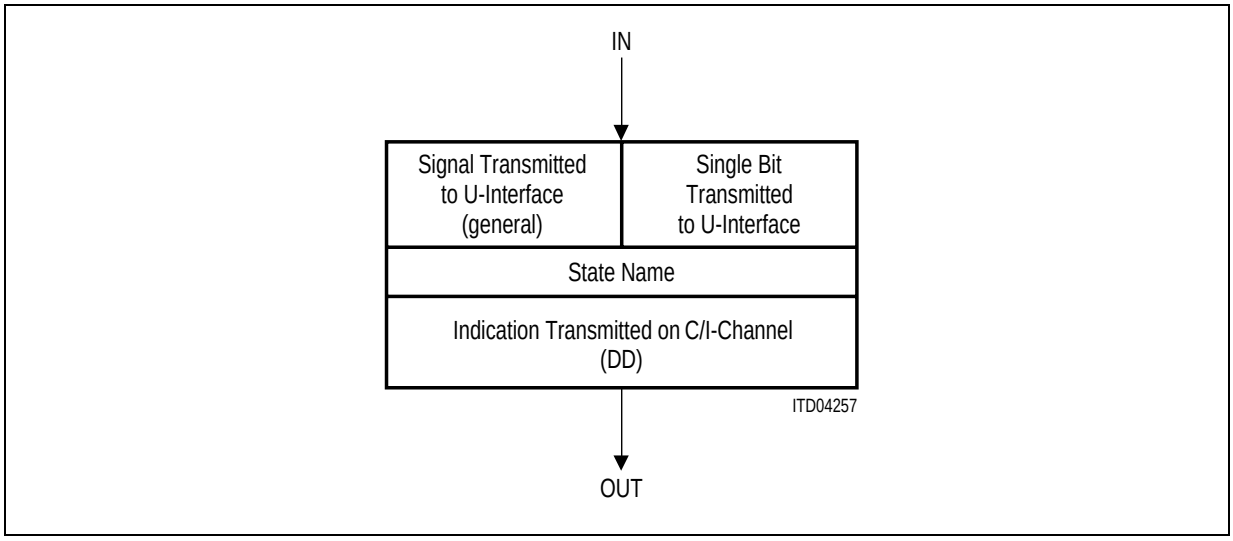


Figure 71 State Diagram Notation

The following example explains the use of a state diagram by an extract of the LT state diagram. The state explained is the "Deactivated" state in LT mode.

The state may be entered by either of three methods:

– From state "Receive Reset" after time T7 has expired (T7 E*xpired*)
– From state "Tear Down" after the internal transition criterion "LSU" is fulfilled
– From state "Test" after the C/I-command "DR" has been sent downstream

The following information is transmitted:

– SL0 is sent on the U-interface (no signal, see "U-Interface Signals", page 125)
– No overhead bits are sent
– C/I-message "DI" is issued on upstream

The state may be left by either of the following methods:

– Leave for state "Awake" after NT wake up tone (TN) was detected and the C/I-code DC is present in the downstream direction
– Leave for state "Alerting" after C/I-commands "AR", "ARX", "AR0" or "UAR" and not TN were received
– Leave for state "Reset for Loop" after C/I-command "ARL" was received

Combinations of transition criteria are possible. Logical "AND" is indicated by "&" (TN & DC), logical "OR" is written "or" and for a negation "/" is used. The start of a timer is indicated with "TxS" ("x" being equivalent to the timer number). Timers are always started when entering the new state. The action resulting after a timer has expired is indicated by the path labelled "TxE".

The sections following the state diagram contain detailed information about all states and signals used. These details are mode dependent and may differ for identically named signals/states. They are therefore listed for each mode.

Cold and Warm Starts

Two types of start-up procedures are supported by the IEC-Q: cold starts and warm starts.

Cold starts are performed after a reset and require all echo and equalizer coefficients to be recalculated. This procedure typically is completed after 1-7 seconds depending on the line characteristics. Cold starts are recommended for activations where the line characteristics have changed considerably since the last deactivation.

A warm start procedure uses the coefficient set saved during the last deactivation. It is therefore completed much faster (maximum 300 ms). Warm starts are however restricted to activations where the line characteristics do not change significantly between two activations.

Regarding the path in the transition diagram, cold starts have in particular that the IEC-Q has entered the state ’Test’ (e.g. due to a reset) prior to an activation. The activation procedure itself is then identical in both cases. Therefore, the following sections apply to both warm and cold starts.

4.4.2 State Machine in LT Modes

This section is applicable for the following LT modes:

– LT mode (512 kHz – 4096 kHz)
– COT 512 mode (512 kHz)
– COT 1536 mode (1536 kHz)

4.4.2.1 LT Modes State Diagram

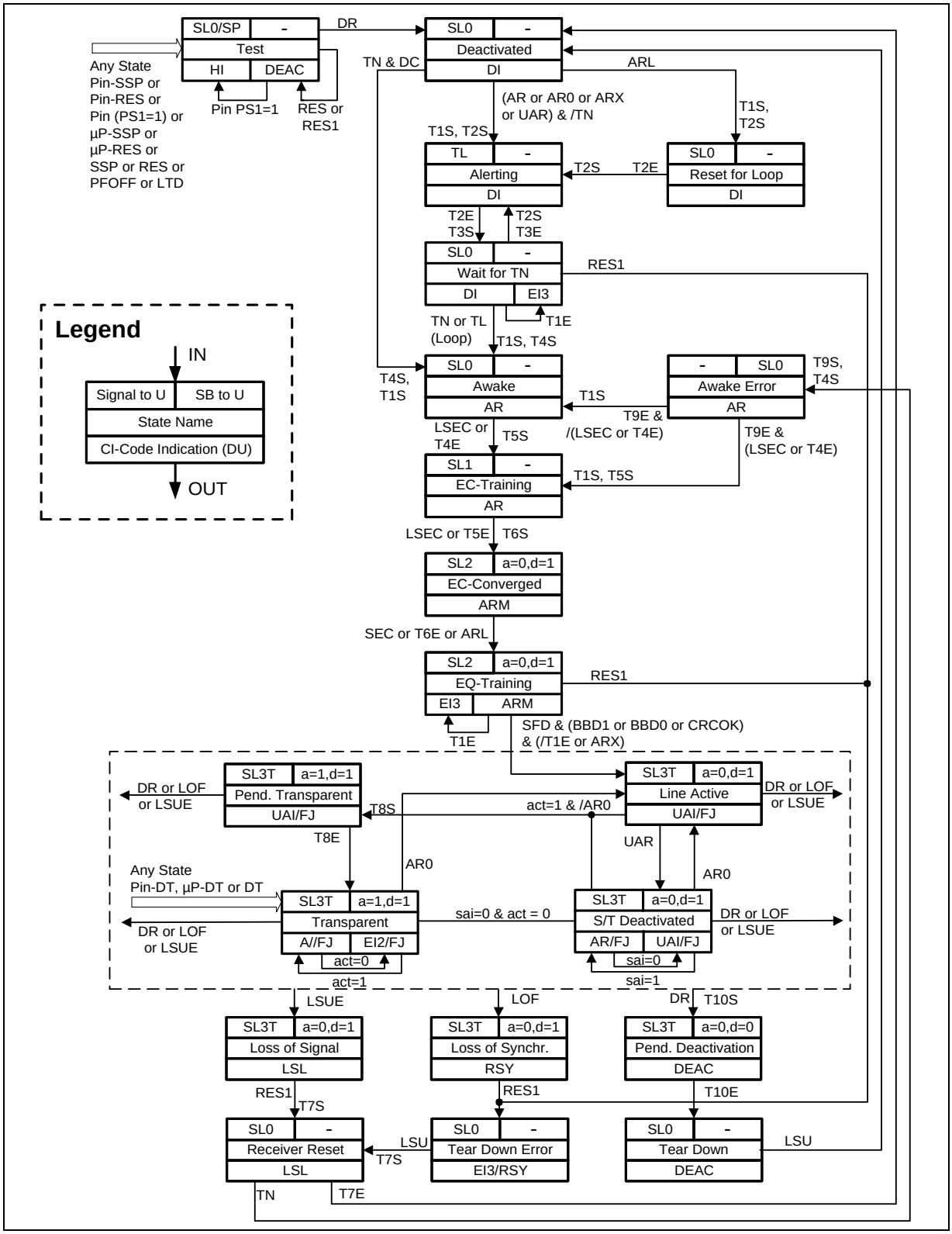


Figure 72 State Transition Diagram in LT Modes

4.4.2.2 Transition Criteria in LT Modes

The transition criteria used by the IEC-Q are described in the following sections. They are grouped into:

– C/I-commands
– Pin states
– Events related to the U-interface
– Timers

C/I-Commands

AR — Activation Request
The IEC-Q is requested to enter the power-up state and to start an activation procedure by sending the wake-up signal TL.

AR0 — Activation Request with "ACT" bit = (0)
The IEC-Q is requested to enter the power-up state and to start an activation procedure by sending the wake-up signal TL. After "EQ Training" the state "Line Active" will be entered independent of the "ACT" bit. Evaluation of the "ACT" bit is disabled when AR0 is received and enabled when AR is received.

ARX — Activation Request Extended
The IEC-Q is requested to enter the power-up state and to start an activation procedure by sending the wake-up signal TL. After "EQ Training" the state "Line Active" will be entered independently of the timer T1, i.e. if the signal SN3 has been received correctly by the LT the "Line Active" state will be entered, even if the T1 timer has expired. Note however that if the T1 timer expires in "EQ Training" the C/I code EI3 will still be issued and should be ignored by the control unit upstream.

ARL — Activation Request Local Loop-back
The IEC-Q is requested to operate an analog loop-back (close to the U-interface) and to start the start-up sequence by sending the wake-up tone TL. This command may be issued only after the IEC-Q has been set to the "Deactivated" state (C/I-channel code DI issued on DOUT) and has to be issued continuously as long as loop-back is requested.

DC — Deactivation Confirmation
This command enables transition from the Deactivated state to the Awake state, if an awake tone has been detected. If this command is not given in the transmission to the Awake state is disabled. However awake tones from downstream will still be recognized and latched. For more information refer also to Note 42, page 153.
In the U-Only activation mode the DC command can be used by the control unit on the LT side to achieve transmission transparency when the terminal

initiates an activation request. This can be done in the following manner
- Assumption: The IEC-Q on the LT side is in the "S/T Deactivated" state. It receives SAI=0 from the NT side, i.e. the terminal is deactivated. The control unit on the LT side issues the C/I command UAR. The IEC-Q on the LT side issues the C/I indication UAI.
- The terminal initiates an activation requests, i.e. it issues the C/I command "AR" on the NT side. This causes the IEC-Q on the NT side to transmit SAI=1 on U.
- Upon detection of SAI=1 the IEC-Q on the LT side issues the C/I indication AR.
- The control unit on the LT side can now issue the C/I command DC. This causes the IEC-Q on the LT side to reflect the polarity of the SAI bit on the UOA bit (see also "Signals on U-Interface", page 156). I.e., the IEC-Q on the LT side transmits UOA=1 on U.
- Upon reception of UOA=1 the IEC-Q on the NT side transmits ACT=1 to U if it is controlled as given in the NT state machine (see "NT Modes State Diagram", page 161 ff.). Transparency can now be achieved in the usual manner.

DR — Deactivation Request
This command requests the IEC-Q to start a deactivation procedure by setting the DEA bit to "0" and to cease transmission afterwards. The DR-code is a conditional command causing the IEC-Q only to react in the states "Test", "S/T Deactivated", "Line Active", "Pending Transparent" and "Transparent", i.e. when the C/I-channel codes DEAC, UAI, AR, AI, FJ or EI2 are issued on DOUT.

DT — Data Through
This unconditional command is used for test purposes only and forces the IEC-Q into the transparent state independent of the wake-up protocol. A far-end transceiver needs not to be connected; in case a far-end transceiver is present it is assumed to be in the same condition. Note however that the C/I indication (initiated by the IEC-Q) in this case depends on the state of the far-end transceiver and is not specified.

LTD — LT Disable
This is an unconditional command which requests the IEC-Q to switch-off the remote-power-feed circuit for the subscriber line by activating the pin DISS.
The IEC-Q is transferred to the "Test" state; the Receiver will not be reset.

RES Reset
Unconditional command which resets the transceiver core (see "Reset Behavior", page 94). For cold start the reset code should be applied for a period of at least 8 IOM®-2-frames (1 ms). In LT modes the DCL clock signal needs to be applied during reset.

RES1 Reset 1
The reset 1 command resets all Receiver functions; especially the EC- and EQ-coefficients and the AGC are set to zero. It resets also the awake signal detection. The RES1-code does not reset IOM®-2-functions (e.g. Monitor Channel procedure or power controller interface). The RES1-code should be used when the IEC-Q has entered a failure condition (expiry of timer T1, loss of framing or loss of signal level) indicated by the C/I-channel EI3, RSY or LSL on DOUT. Besides resetting the Receiver, this command stops transmission on the U-interface. The DEA bit is not set to "0" by RES1.

SSP Send Single Pulses
Unconditional command which requests the transmission of single pulses on the U-interface. The pulses are issued at 1.5 ms intervals and have a duration of 12.5 µs.
The chip is transferred to the "Test" state; the Receiver will not be reset.

UAR Partial Activation Request (U only)
The IEC-Q is requested to enter power-up state and to start an activation procedure of the U-interface only.

Pins

Pin-RES Pin-Reset
Corresponds to a low level at pin $\overline{\text{RES}}$. Resets the transceiver core and all registers except for register STCR in the microprocessor mode (see "Reset Behavior", page 94). The C/I-message DEAC will be issued. The duration of the reset pulse must be 30 ns minimum. The reset will be carried out only after the IOM®-2 clocks are issued.

Pin-SSP Pin-Send Single Pulses
Applies only in stand-alone mode. Corresponds to a high level at pin TSP. The function of this pin is the same as for the C/I-code SSP. The C/I-message DEAC will be issued. The high level needs to be applied continuously for the transmission of single pulses.

Pin-DT Pin-Data Through
Applies only in stand-alone mode. Entered when both $\overline{\text{RES}}$ and TSP are active ($\overline{\text{RES}}$ = "0" and TSP = "1"). The function is identical with the C/I-code DT.

Pin-PFOFF Power Feed OFF
Corresponds to pin PS1 being activated. This pin indicates that the remote-power-feed circuit for the subscriber line has been turned off. The IEC-Q is requested to forward this indication making use of the C/I-channel code HI.
The chip is transferred to the "Test" state; the Receiver will be reset.

Note 41: If one of the pin configurations Pin-Reset, Pin-SSP or Pin-DT is being used, C/I command (especially RES, SSP or DT) will not be executed, i.e. pin setting has higher priority than C/I Channel setting.

Microprocessor

µP-SSP µP-Send Single Pulses
Applies only in microprocessor mode. Corresponds to the setting: STCR:TM1 = ’1’ and STCR:TM2 = ’1’. The function of this pin is the same as of the C/I-code SSP. C/I-message DR will be issued. See "Test Modes", page 52.

µP-DT µP-Data Through
Applies only in microprocessor mode. This function is activated by setting: STCR:TM1 = ’0’ and STCR:TM2 = ’1’. The function of this pin is the same as of the C/I-code DT. See "Test Modes", page 52.

U-Interface Events

ACT = 0/1 "ACT" bit received from the NT side.

– ACT = 1 signals that the NT has detected INFO3 on the S/T-interface and indicates that the complete basic access system is synchronized in both directions of transmission. The LT side is requested to provide transparency of transmission in both directions and to respond with setting the ACT-bit to "1". In the case of loop-backs (loop-back 2 or single-channel loop-back in the NT), however, transparency is required even when the NT is not sending ACT = 1. Transparency is achieved in the following manner:

– The IEC-Q performs transparency in both directions of transmission after the Receiver has achieved synchronization (state EQ-training is left) independent of the status of the received ACT-bit.

– The status "ready for sending" is reached when the state transparent is entered i.e. when the C/I-channel indication AI is issued. This is valid in the case of a normal activation procedure for call control. In the case of loop-backs (loop-back 2 or single-channel loop-back in the NT and analog loop-back in the LT) however, the status "ready for sending" is reached when the state line active is entered i.e. when the C/I-channel

indication UAI is issued. Until the status "ready for sending" is reached, binary "0s" have to be passed in the B- and D-channels on DIN.

– ACT = 0 indicates the loss of transparency on the NT side (loss of framing or loss of signal level on the S/T-interface). The IEC-Q informs the LT side by issuing the C/I-channel indication EI2, but performs no state change or other actions.

CRCOK Cyclic Redundancy Check OK
This input is used as a criterion that the Receiver has acquired frame synchronization and both its EC and EQ coefficients have converged.

LOF Loss of Framing on the U-interface
This condition is fulfilled if framing is lost for 576 ms. 576 ms are the upper limit. If the correlation between synchronization word and input signal is not optimal, LOF can be issued earlier.

LSEC Loss of Signal Level behind the Echo Canceler
In the "Awake" state, this input is used as indication that the NT has ceased the transmission of signal SN1. In the EC-training state, this input is used as an internal signal indicating that the EC in the LT has converged.

LSU Loss of Signal Level on the U-interface
This signal indicates that a loss of signal level for the duration of 3 ms has been detected on the U-interface. This short response time is relevant in all cases where the LT waits for a response (no signal level) from the NT side, i.e. after a deactivation procedure has been started or after loss of framing in the LT occurred.

LSUE Loss of Signal Level on the U-interface (error condition)
After a loss of signal level has been noticed, a 492 ms timer is started. After this timer has elapsed, the LSUE-criterion is fulfilled. This long response time (see also LSU) is valid in all cases where the LT is not prepared to lose signal level. Note that 492 ms represent a minimum value; the actual loss of signal might have occurred earlier, e.g. when a long loop is cut at the LT side, the echo coefficients need to be readjusted to new parameters. Only after the adjusted coefficient cancel the echo completely, the loss of signal is detected and the timer can be started (if the long loop is cut at the remote end, the coefficients are still correct and a loss of signal will be detected immediately).

SEC Signal Level behind the echo canceler
This signal indicates that a signal level corresponding to SN2 from the NT has been detected on the U-interface.

SFD Superframe Detected

TN — Tone (wake-up signal) received from the NT.
When in the "Deactivated" state, the IEC-Q is requested to start an activation procedure and to inform the LT side making use of the C/I-channel code AR. When in the "Wait for TN" state, the signal TN sent by the NT acknowledges the receipt of a wake-up signal TL from the LT.
When an analog loop-back is operated, the wake-up signal TL sent by the LT-transmitter is detected by the LT receiver.
The TN-criteria is fulfilled when 12 consecutive periods of the 10 kHz wake-up tone were detected.

Note 42: Transition from state Deactivated to state Awake will only be done if the C/I command DC is issued in downstream direction, as indicated in the state diagram. However, the wake-up tone will still be detected and latched by the IEC-Q even if the C/I command DC is not present. In this case the IEC-Q will not react to the C/I commands AR, AR0, ARX and UAR. Furthermore, if the DC command is issued later on, the IEC-Q will activate immediately. If a previously received wake-up tones should be ignored, e.g. because it is "old" and no more valid, the user might want to reset the wake-up tone before further action. This can be done with any kind of reset (see "Reset Behavior", page 94). The wake-up tone can also be reset by the C/I command RES1, if it is applicable (state dependent).

BBD0/1 — Binary "0" or "1s" detected in the B- and D-channels
This internal signal indicates that for a period of time of 6–12 ms a continuous stream of binary "0s" or "1s" has been detected. It is used as a criterion that the Receiver has acquired frame synchronization and both its EC- and EQ-coefficients have converged. BBD1 corresponds to the signals SN2 or SN3 in the case of a normal activation and BBD0 corresponds to the internally received signal SL2 in the case of an analog loop-back or possibly a loop-back 2 in the NT.

Timers

The start of timers is indicated by TxS, the expiry by TxE. Table 29 below shows which timers are used in LT modes:

Table 29 Timers for LT State Machine

Timer	Duration (ms)	Function	State
T1	15000	Supervisor for start-up	
T2	3	TL-transmission Receiver reset	Alerting Reset for loop
T3	40	Re-transmission of TL	Wait for TN
T4	6000	Supervisor SN0 detect	Awake
T5	1000	Supervisor EC converge	EC training
T6	6000	Supervisor SN2 detect	EC converge
T7	40	Hold time	Receiver reset
T8	24	Delay time for AI detection	Pend. transparent
T9	40	Hold time	Awake error
T10	40	"DEA" = (0) transmission	Pend. Deactivation

4.4.2.3 Output Signals and Indications in LT Modes

Signals and indications are issued on the IOM®-2-interface (C/I-codes) and U-interface (predefined U-signals).

C/I-Indications

AI Activation Indication
This indication signals that "ACT" = 1 has been received and that timer T8 has elapsed. This indication is not issued in case AR0 is applied or an analog loop-back is operated.

AR Activation Request
The AR-code signals that a wake-up signal has been received and that a start-up procedure has commenced. Receiver synchronization has not yet been achieved.
When already partially active (U only activation), AR indicates that the "SAI" bit was set to (1), i.e. the S/T-interface has become active.

DEAC Deactivation
This indication is issued in response to a DR-code (Pend. Deactivation, Tear Down) and in the "Test" state (unless PFOFF is active, i.e. PS1 = (1)).

DI — Deactivation Indication
Idle code on the IOM®-2-interface. Normally the IEC-Q stays in the "Deactivated" state unless an activation procedure is started by the NT side.

EI2 — Error Indication 2
EI2 is issued if the received ACT-bit is (0). The NT receiver indicates a loss of signal or framing on the S/T-interface by setting the upstream ACT-bit to (0). The IEC-Q remains in the "Transparent" state. After a signal level or framing is detected again, the C/I-indication AI will be issued anew.

EI3 — Error Indication 3
This indication is issued when the IEC-Q has not been able to activate successfully (expiry of timer T1).

LSL — Loss of Signal Level
The IEC-Q has entered a failure condition after loss of signal level (LSUE).

RSY — Re-Synchronization indication after a loss of framing (LOF)
For EI3, LSL and RSY indication the LT side should react by applying the C/I-channel code RES1 to allow the IEC-Q to enter the "Receive reset" state and to reset the Receiver functions.

FJ — Frame Jump
This indication signals that either a data buffer overflow/underflow has been detected or a phase jump of one of the IOM®-2-timing signals DCL or FSC has occurred. The FJ-code is issued for a period of 1.5 ms.

HI — High Impedance
PFOFF is activated which means that the remote-power-feed circuit for the subscriber line is turned off.

UAI — U-Activation Indication
The UAI-code signals that the line system is synchronized in both directions of transmission (see also the input ACT = 1). Maintenance bits are transmitted normally.

ARM — Activation Request Maintenance
Transmission of maintenance bits is possible.

INT — Interrupt (Stand-alone mode only)
A level change on input pin INT triggers the transmission of this C/I code for four successive IOM®-2 frames. Please refer to "Interrupt", page 197 for details.

Signals on U-Interface

The signals SLx, TL and SP transmitted on the U-interface are defined in Table 28, page 125. The polarity of the overhead bits ACT and DEA is indicated as follows:

a = 0/1 corresponds to ACT bit set to binary "0/1".
d = 0/1 corresponds to DEA bit set to binary "0/1".

The polarity of the transmitted UOA-bit depends on the received C/I-channel code:

– UAR sets UOA-bit to binary 0.
– AR sets UOA-bit to binary 1.
– Any other C/I-codes sets the UOA to the same value as the received SAI bit. After deactivation the UOA-bit is set to binary 0 until a valid SAI-bit is received.

4.4.2.4 LT States

This section describes the functions of all states defined in LT modes.

Alerting

The wake-up signal TL is transmitted for 3 ms (T2) in response to an activation request from the LT side (AR, AR0, UAR or ARL). In the case of an analog loop-back, the signal TL is forwarded internally to the wake-up signal detector and stored.

Awake

If the C/I command is issued in the Deactivated state the Awake state is entered upon the receipt of a wake-up or an acknowledge signal TN from the NT. In the case of an activation started by the LT side, timer T1 is restarted when the "Awake" state is entered.

Awake Error

The "Awake Error" state is equivalent to the "Awake" state, but is entered only when a wake-up signal is received while being in the "Receive reset" state. As the "Receive reset" state was entered upon the application of the C/I-channel code RES1, the "Awake error" state assures that a minimum amount of time elapses between the application of the RES1-code and the IEC-Q entering a state (EQ training) in which it again reacts on the RES1-code. The LT side is requested to stop issuing the command RES1 within T9 after the receipt of the C/I-channel code AR on DOUT and to replace it by another command such as the idle code DC for instance.

Deactivated (Full Reset)

In the "Deactivated" state the device may enter the low power consumption condition. The power-down mode is entered if no monitor messages are active or pending. In power-down the Receiver and parts of the interface are deactivated while functions related to the IOM®-2-interface and the wake-up detector are still active.
No signal is sent on the U-interface, the differential outputs AOUT and BOUT are set to 0 V. The IEC-Q waits for a wake-up signal TN from the NT side or an activation request (AR, ARX, AR0, UAR or ARL) from the LT side to start an activation procedure.

For the recognition of the wake-up signal TN the following procedure applies:

– TN detected for 4 periods –> transfer within the "Deactivated" state into power-up
– In power-up both differential outputs are set to 3.2 V
– TN detected for a total of 12 consecutive periods –> transition criterion TN fulfilled, change to next state, if in addition the C/I-command DC is issued in the downstream direction.
– TN detected for more than 4 but less than 12 periods –> return to power-down

The input sensitivity stated "Analog Characteristics", page 266, presents the minimum level required to meet the TN transition criterion. The power-up condition may thus already be entered at a lower level.

Note 43: Refer also to Note 42, page 153, for more information about device behavior when a wake-up tone TN is detected in the deactivated state.

EC Converged

Upon the EC-coefficients having converged, the IEC-Q starts the transmission of signal SL2 and waits for the receipt of signal SN2 from the NT (SEC). If this condition is not met within T6, the start-up procedure will be continued. In the case of an analog loop-back, this state is left immediately because the EC compensates for the looped back transmit signal.

EC-Training

The signal SL1 is transmitted on the U-interface to allow the LT Receiver to update its EC-coefficients. The "EC-training" state is left when the EC has converged (LSEC) or when timer T5 has elapsed. Timer T5 allows the start-up procedure to proceed even if LSEC could not be detected, e.g. due to a high noise level on the U-interface.

EQ-Training

The "EQ-Training" is left after the Receiver has achieved synchronization and the superframe indication has been detected (SFD). Upon expiry of timer T1 the C/I-channel indication EI3 is issued.

Line Active

In the "Line Active" state, the IEC-Q transmits transparently in both directions. The U-Interface is synchronized and the maintenance channel is operational. The IEC-Q stays in the line-active state

– during a normal activation procedure while the "ACT" bit = (0) is received
– when an analog loop-back is established
– while C/I-command AR0 is applied downstream

In the case of normal activation with call control, binary "0s" have to be applied to the B and D channels in downstream direction. After the C/I-channel indication UAI has been issued, the layer-2 receiver should be fully operational to prevent the first layer-2 message issued by the NT side upon the receipt of the ALI-code in the TE, to be lost.

Loss of Signal

The "Loss of Signal" state is entered upon the detection of a failure condition i.e. loss of receive signal (LSUE). The ACT bit is set to "0" and the C/I-channel indication LSL is issued. The IEC-Q waits for the C/I-channel command RES1 to enter the "Receive Reset" state.

Loss of Synchronization

The "Loss of Synchronization" state is entered upon the detection of a failure condition i.e. loss of framing by the LT Receiver (LOF). The ACT-bit is set to "0" and the C/I-channel indication RSY is issued. The IEC-Q waits for the C/I-channel command RES1 to enter the "Tear Down Error" state and subsequently the "Receive Reset" state.

Pending Deactivation

"Pending Deactivation" is a transient state entered after the receipt of a DR-code. The DEA-bit is set to "0". Timer T10 assures that the DEA-bit is set to "0" in at least three consecutive superframes before the transmit level is turned off.

Pending Transparent

"Pending Transparent" is a transient state entered upon the detection of ACT = 1 and left by T8. The ACT-bit is set to "1". The purpose of this state is to issue the C/I-channel indication AI (corresponding to "ready for sending") 24 ms after the ACT-bit has been set to "1" by the LT-transceiver. This assures that under normal operating conditions the AI-indication is issued first on the TE side and only afterwards on the LT side. Thus the layer-2 receiver in the TE is already operational when the first layer-2 message is issued by the LT side.

Reset for Loop

"Reset for Loop" resets the Receiver in order to guarantee a correct adaption of the echo- and equalizer coefficients.

Receive Reset

The "Receive Reset" state assures that for a period of T7 no signal, especially no wake-up signal TL, is sent on the U-interface, i.e. no activation procedure is started from the LT side. A wake-up signal TN, however, from the NT side is acknowledged.

S/T Deactivated

The state "S/T Deactivated" will be entered if the received ACT- and SAI-bits are set to (0). In this state the signal SL3T, ACT = (0), DEA = (1) and UOA = (0) are transmitted downstream. The C/I-code UAI is issued upstream while the received SAI = (0).
In order to initiate a complete activation from the S/T deactivation state, the LT needs to set the UOA-bit to (1). This will occur if either of the following three conditions are met:

– C/I = AR (LT activation)
– SAI = (1) & AR (TE activation with exchange control [C/I UAR downstream])
– SAI = (1) (TE activation without exchange control [C/I DC downstream])

"S/T deactivated" will be left if the received ACT bit is (1), or the C/I code AR0 is applied.

Tear Down

In "Tear Down" state, transmission ceases in order to deactivate the basic access, and the IEC-Q waits for a response (no signal level, LSU) from the NT side.

Tear Down Error

"Tear Down Error" state is entered after loss of framing has been detected. Transmission ceases in order to deactivate the basic access and the IEC-Q waits for a response (no signal level, LSU) from the NT side. EI3-indication is transmitted after a transition forced by RES1 from the Wait-For-TN or EQ-Training states. In the case of transition from the "Loss of Synchronization" state RSY is sent.

Test

This "Test" mode is entered when the unconditional commands RES, SSP, LTD, Pin-RES, Pin-SSP or PFOFF are used. It is left when the pins RESQ, TSP and PS1 are inactive and the C/I-channel code DR is received. The output signals are as follows:

– When the C/I-channel code RES or RES1 is applied or when the pin RESQ is activated:
  SL0 and DEAC
– When the C/I-channel code SSP is applied or when the pin TSP is activated:
  single pulses (SP) and DEAC
– When the C/I-channel code LTD is applied:
  SL0 and DEAC; furthermore, the pin DISS is activated
– When the pin PS1 is activated:
  SL0 and HI

In this state the IEC-Q does not react to the receipt of a wake-up signal TN.

Transparent

This "Transparent" state corresponds to the fully active state in the case of a normal activation for call control. It may also be entered in the case of a loop-back 2 if the NT issues ACT = 1 or in case of a single-channel loop-back in the NT. The LT side is informed that the status "ready for sending" is reached (indication AI). If the NT side loses transparency (receipt of ACT = 0), the LT side is informed by making use of the C/I-channel indication EI2, but no state change is performed. If the S/T-interface is deactivated (SAI = (0) & ACT = (0)), the device is transferred to the S/T deactivated state.

Wait for TN

In "Wait for TN" the IEC-Q waits for a response (tone TN from the NT or tone TL in case of an analog loop-back) to the transmission of the wake-up signal TL. If no response is received within T3, the state is left for re-transmission of a wake-up tone TL. This procedure is repeated until the detection of tone TN or until expiry of timer T1. In this case the C/I-channel indication EI3 is issued, but no state change is performed.

4.4.3 State Machine in NT Modes

This chapter describes the behavior of the IEC-Q device if operated in either of the following NT modes:

– NT mode (512 kHz)
– NT-PBX mode (512 – 4096 kHz)
– TE mode (1536 kHz)
– NT-Auto Activation mode (512 kHz)

Figure 73 describes the behavior of the first three modes, and Figure 74 describes the behavior of the last one.

4.4.3.1 NT Modes State Diagram

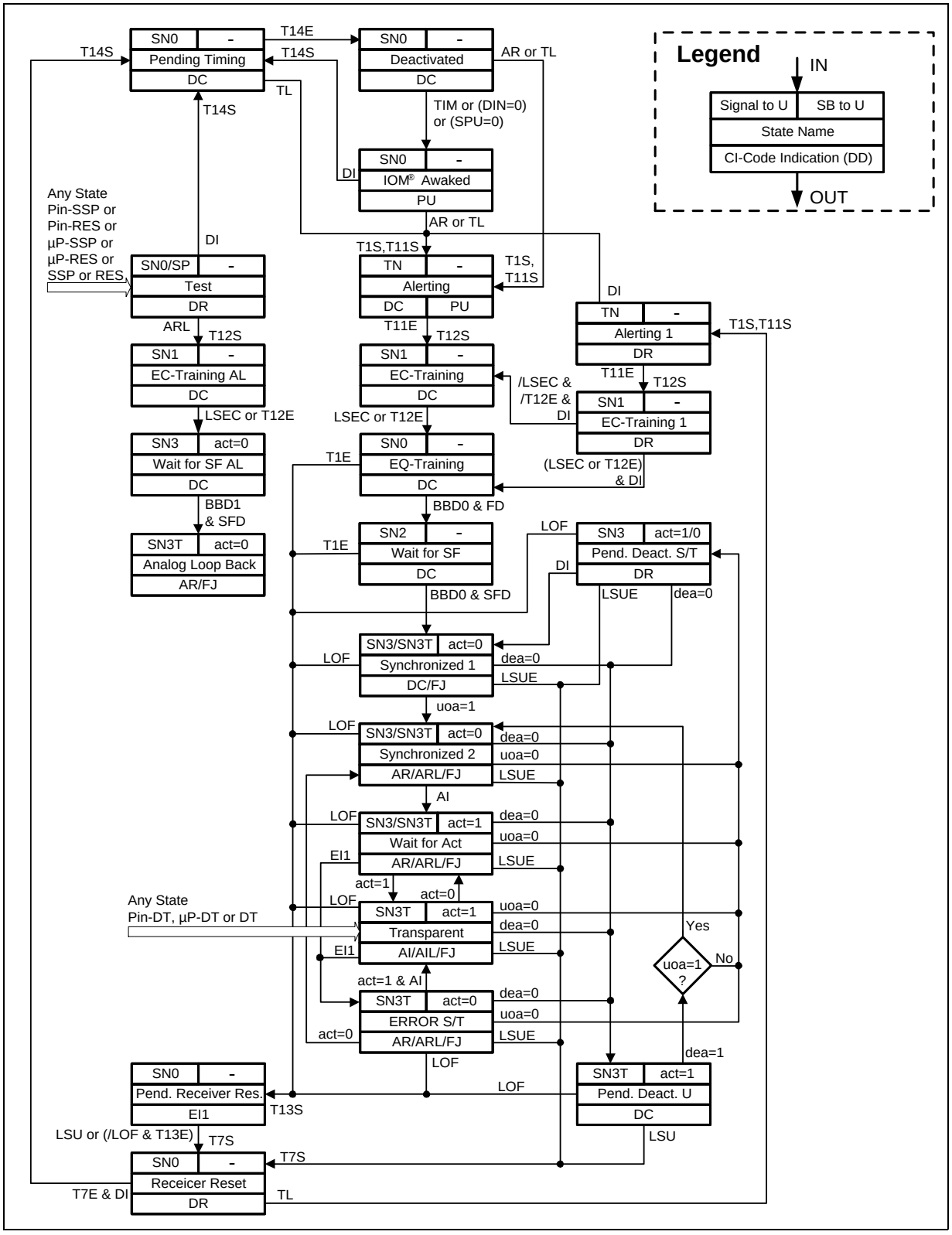


Figure 73 State Transition Diagram in NT, TE and NT-PBX Modes

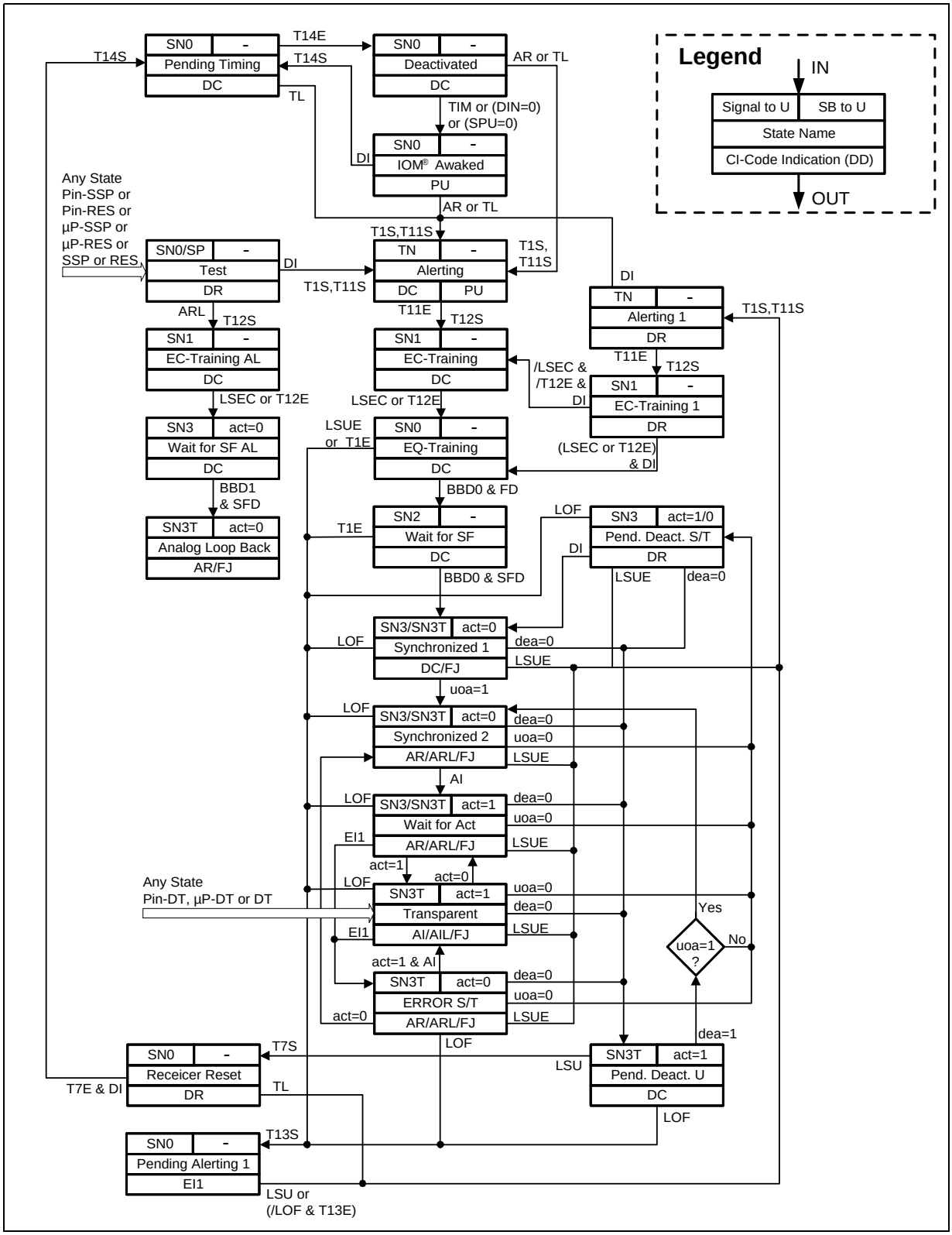


Figure 74 State Transition Diagram in NT-Auto Activation Mode

4.4.3.2 Transition Criteria in NT Modes

C/I-Commands

AI — Activation Indication
The S-transceiver issues this indication to announce that the S-receiver is synchronized. The IEC-Q informs the LT side by setting the "ACT" bit to "1".

AR — Activation Request
INFO1 has been received by the S-transceiver or the Intelligent NT wants to activate the U-interface. The IEC-Q is requested to start the activation process by sending the wake-up signal TN.

ARL — Activation Request Local Loop-back
The IEC-Q is requested to operate an analog loop-back (close to the U-interface) and to begin the start-up sequence by sending SN1 (without starting timer T1). This command may be issued only after the IEC-Q has been reset by making use of the C/I-channel code RES or a hardware reset. This assures that the EC- and EQ-coefficients updating algorithms converge correctly. The ARL-command has to be issued continuously as long as the loop-back is required.

DI — Deactivation Indication
This indication is used during a deactivation procedure to inform the IEC-Q that timing signals are needed no longer and that the IEC-Q may enter the deactivated (power-down) state. The DI-indication has to be issued until the IEC-Q has answered with the DC-code.

DIN = 0 — Binary "0" polarity on DIN
This asynchronous signal requests the IEC-Q to provide IOM®-2 clocks. Hereafter, binary "0s" in the C/I-channel (code TIM "0000" or any other code different from DI "1111") keep the IOM®-2 interface active.

DT — Data Through
This unconditional command is used for test purposes only and forces the IEC-Q into a state equivalent to the "Transparent" state. The far-end transceiver is assumed to be in the same condition. Note however that in this case the C/I indication (initiated by the IEC-Q) depends on the state of the far-end transceiver and is not specified.

EI1 — Error Indication 1
The S-transceiver indicates an error condition on its receiver side (loss of frame alignment or loss of incoming signal). The IEC-Q informs the LT side by setting the ACT-bit to "0" thus indicating that transparency has been lost.

RES Reset
Unconditional command which resets the transceiver core (see "Reset Behavior", page 94). Especially the EC- and EQ-coefficients are set to zero.

SSP Send Single Pulses
Unconditional command which requests the transmission of single pulses on the U-interface. The pulses are issued at 1.5 ms intervals and have a duration of 12.5 µs.
The chip is in the "Test" state, the Receiver will not be reset.

TIM Timing
In the NT mode the IEC-Q is requested to continue providing timing signals and not to leave the "Power-up" state.

Pins

Pin-Res Pin-Reset
Corresponds to a low level at pin $\overline{\text{RES}}$. Resets the transceiver core and all registers except for register STCR in the microprocessor mode (see "Reset Behavior", page 94). C/I-message DEAC will be issued. The duration of the reset pulse must be 30 ns minimum.

Pin-SSP Pin-Send Single Pulses
Applies only in stand-alone mode. Corresponds to a high-level at pin TSP in stand-alone mode. The function of this pin is the same as of the C/I-code SSP. C/I-message DR will be issued. The high-level must be applied continuously for single pulses.

Pin-DT Pin-Data Through
Applies only in stand-alone mode. This function is activated when both pins $\overline{\text{RES}}$ and TSP are active ($\overline{\text{RES}}$ = ’0’ and TSP = ’1’). The function of this pin is the same as of the C/I-code DT.

Note 44: If one of the pin configurations Pin-Reset, Pin-SSP or Pin-DT is being used, C/I command (especially RES, SSP or DT) will not be executed, i.e. pin setting has higher priority than C/I Channel setting.

Microprocessor

SPU=0 This condition applies only in the microprocessor mode. Setting the CIWU:SPU (Software Power Up) bit to "0" in the NT mode will cause the DIN signal to be set internally to "0", regardless of the value of the pin DIN. See "Activation in the µP-NT Mode", page 142.

µP-SSP µP-Send Single Pulses
Applies only in microprocessor mode. Corresponds to the setting: STCR:TM1 = ’1’ and STCR:TM2 = ’1’. The function of this setting is the same as of the C/I-code SSP. C/I-message DR will be issued. See "Test Modes", page 52.

µP-DT µP-Data Through
Applies only in microprocessor mode. This function is activated by setting: STCR:TM1 = ’0’ and STCR:TM2 = ’1’. The function of this setting is the same as of the C/I-code DT. See "Test Modes", page 52.

U-Interface Events

The signals SLx and TL received on the U-interface are defined in Table 28, page 125.

ACT ACT-bit received from LT side.

– ACT = 1 requests the IEC-Q to transmit transparently in both directions. As transparency in receive direction (U-interface to IOM®-2) is already performed when the Receiver is synchronized, the receipt of ACT = 1 establishes transparency in transmit direction (IOM®-2 to U-interface), too. In the case of loop-backs, however, transparency in both directions of transmission is established when the Receiver is synchronized.

– ACT = 0 indicates that the LT side has lost transparency.

DEA DEA-bit received from the LT side

– DEA = 0 informs the IEC-Q that a deactivation procedure has been started by the LT side.

– DEA = 1 reflects the case when DEA = 0 was detected by faults due to e.g. transmission errors and allows the IEC-Q to recover from this situation (see state ’Pend. Deact. U’).

UOA UOA-bit received from network side

– UOA = 0 informs the IEC-Q that only the U-interface is to be activated. The S/T-interface must remain deactivated.

– UOA = 1 enables the S/T-interface to activate.

LOF Loss of Framing on the U-interface

This condition is fulfilled if framing is lost for 576 ms. 576 ms are the upper limit. If the correlation between synchronization word and the input signal is not optimal, LOF may be issued earlier.

LSEC Loss of Signal level behind the Echo Canceler
Internal signal which indicates that the echo canceler has converged.

LSU — Loss of Signal level on the U-interface
This signal indicates that a loss of signal level for a duration of 3 ms has been detected on the U-interface. This short response time is relevant in all cases where the NT waits for a response (no signal level) from the LT side, i.e. after a deactivation has been announced (receipt of DEA = 0), after the NT has lost framing, and after timer T1 has elapsed.

LSUE — Loss of Signal level on the U-interface (error condition)
After a loss of signal has been noticed, a 588 ms timer is started. When it has elapsed, the LSUE-criterion is fulfilled. This long response time (see also LSU) is valid in all cases where the NT is not prepared to lose signal level i.e. the LT has stopped transmission because of loss of framing, an unsuccessful activation, or the transmission line is interrupted.
Note that 588 ms represent a minimum value; the actual loss of signal might have occurred earlier, e.g. when a long loop is cut at the NT side and the echo coefficients need to be readjusted to the new parameters. Only after the adjusted coefficients cancel the echo completely, the loss of signal is detected and the timer can be started (if the long loop is cut at the remote end, the coefficients are still correct and loss of signal will be detected immediately).

SFD — Superframe (ISW) Detected on U-interface

FD — Frame (SW) Detected on U-interface

TL — Wake-up signal received from the LT
The IEC-Q is requested to start an activation procedure. The TL-criterion is fulfilled when 12 consecutive periods of the 10-kHz wake-up tone were detected.
When in the "Pending Timing" state and automatic activation after reset is selected (NT-Auto Activation mode), a recognition of TL is assumed every time the "Pending Timing" state has been entered from the "Test" state (caused by C/I code DI). This behavior allows the IEC-Q to initiate activation attempts after having been reset (see "Activation Attempt Initiated by NT in NT-Auto Activation Mode", page 142).

BBD0/1 — Binary "0s" or "1s" detected in the B- and D-channels
This internal signal indicates that for 6-12 ms, a continuous stream of binary "0s" or "1s" has been detected. It is used as a criterion that the Receiver has acquired frame synchronization and both its EC- and EQ-coefficients have converged. BBD0 corresponds to the signal SL2 in the case of normal activation and BBD1 corresponds to the internally received signal SN3 in case of an analog loop back in the NT mode.

Timers

The start of timers is indicated by TxS, the expiry by TxE. The Table 30 shows which timers are used by the IEC-Q in NT mode:

Table 30 Timers for NT State Machine

Timer	Duration (ms)	Function	State
T1	15000	Supervisor for start-up	
T7	40	Hold time	Receive reset
T11	9	TN-transmission	Alerting
T12	5500	Supervisor EC-converge	EC-training
T13	15000	Frame synchronization	Pend. receive reset
T14	0.5	Hold time	Pend. timing

4.4.3.3 Output Signals and Indications in NT Modes

Signals and indications are issued on the C/I Channel and on the U-interface (predefined U-signals).

C/I Indications

AI Activation Indication
The IEC-Q has established transparency of transmission in the direction IOM®-2 to U-interface. In an NT1, the S-transceiver is requested to send INFO4 and to achieve transparency of transmission in the direction IOM®-2 to S/T-interface.

AIL Activation Indication Loop-back
The IEC-Q has detected ACT = 1 while loop-back 2 is still established. In an NT1, the S-transceiver is requested to send INFO4 (if a transparent loop-back 2 is to be implemented) and to keep loop-back 2 active.

AR Activation Request
The IEC-Q has synchronized on the incoming signal. In an NT1, the S-transceiver is requested to start the activation procedure on the S/T-interface by sending INFO2.

ARL Activation Request Loop-back
The IEC-Q has detected a loop-back 2 command in the EOC-channel and has established transparency of transmission in the direction IOM®-2 to U-interface. In an NT1, the S-transceiver is requested to send INFO2 (if a transparent loop-back 2 is to be implemented) and to operate loop-back 2.

DC Deactivation Confirmation
Idle code on the C/I Channel. The IEC-Q stays in the power-down mode unless an activation procedure has been started from the LT side. The U-interface may be activated but the S/T-interface has to remain deactivated.

DR Deactivation Request
The IEC-Q has detected a deactivation request command from the LT side for a complete deactivation or a S/T only deactivation. In an NT1, the S-transceiver is requested to start the deactivation procedure on the S/T-interface by sending INFO0.

EI1 Error Indication 1
The IEC-Q has entered a failure condition caused by loss of framing on the U-interface or expiry of timer T1.

INT Interrupt (Stand-alone mode only)
A level change on input pin INT triggers the transmission of this C/I code for four successive IOM®-2 frames. Please refer to "Interrupt", page 197 for details.

PU Power Up
The IEC-Q provides IOM®-2 clocks.

Signals on U-Interface

The signals SNx, TN and SP transmitted on the U-interface are defined in Table 28, page 125.
The polarity of the transmitted ACT-bit is as follows:

a = 0/1 corresponds to ACT-bit set to binary "0/1"

The polarity of the issued SAI-bit depends on the received C/I-channel code: DI and TIM leads to SAI = 0, any other C/I-code sets the SAI-bit to 1 indicating activity on the S/T-interface.

4.4.3.4 NT States

This section describes the functions of all states defined in NT modes:

Alerting

The wake-up signal TN is transmitted for a period of T11 either in response to a received wake-up signal TL or to start an activation procedure on the LT side.

Alerting 1

"Alerting 1" state is entered when a wake-up tone was received in the "Receive Reset" state and the deactivation procedure on the NT side was not yet finished. The transmission of wake-up tone TN is started.

Analog Loop-Back

Upon detection of binary "1s" for a period of 6–12 ms and of the superframe indication, the "Analog loop-back" state is entered and transparency is achieved in both directions of transmission. This state can be left by making use of any unconditional command. Only the C/I-channel code RES should be used, however. This assures that the EC- and EQ-coefficients are set to zero and that for a subsequent normal activation procedure the Receiver updating algorithms converge correctly.

Deactivated

The ’Deactivated’ state is a power-down state. If there are no pending Monitor Channel messages from the IEC-Q, i.e. all Monitor Channel messages have been acknowledged, the IOM®-2-clocks are turned off. No signal is sent on the U-interface.
The IEC-Q waits for a wake-up signal TL from the LT side to start an activation procedure. To enter state ’IOM®-2 Awake’ a wake-up signal (DIN = 0 or SPU=0 in µP mode) is required if the IOM®-2-clocks are disabled. The wake-up signal is provided via the IOM®-2 interface (pin DIN = 0 or bit SPU=0 in µP mode). If the IOM®-2-clocks were active in state ’Deactivated’ C/I-code TIM is sufficient for a transition to state ’IOM®-2 Awake’.

EC Training

The signal SN1 is transmitted on the U-interface to allow the NT Receiver to update the EC-coefficients. The automatic gain control (AGC), the timing recovery and the EQ updating algorithm are disabled. The "EC-training" state is left when the EC has converged (LSEC) or when timer T12 has elapsed.

EC-Training 1

The "EC-Training 1" state is entered if transmission of signal SN1 has to be started and the deactivation procedure on the NT side is not yet finished.

EC-Training AL

This state is entered in the case of an analog loop-back. The signal SN1 is transmitted on the U-interface to allow the NT Receiver to update the EC-coefficients. The automatic gain control (AGC), the timing recovery and the EQ updating algorithm are disabled. The "EC-training" state is left when the EC has converged (LSEC) or when timer T12 has elapsed.

EQ-Training

The Receiver waits for signal SL1 or SL2 to be able to update the AGC, to recover the timing phase, to detect the synch-word (SW), and to update the EQ-coefficients. The "EQ-training" state is left upon detection of binary "0s" in the B- and D-channels for a period of 6–12 ms corresponding to the detection of SL2.

Error S/T

Loss of framing or loss of incoming signal has been detected on the S/T-interface (EI1). The LT side is informed by setting the ACT-bit to "0" (loss of transparency on the NT side). The following codes are issued on the C/I-channel:

– Normal activation or single-channel loop-back: AR
– Loop-back 2: ARL

IOM®-2 Awaked

Timing signals are delivered on the IOM®-2 interface. The IEC-Q enters the "Deactivated" state again upon detection of the C/I-channel code DI (idle code).

Pending Deactivation of S/T

The IEC-Q has received the UOA-bit at zero after a complete activation of the S/T-interface. The IEC-Q deactivates the S/T-interface by issuing DR in the C/I-channel. The value of the ACT-bit depends on its value in the previous state.

Pending Deactivation of U-Interface

The IEC-Q waits for the receive signal level to be turned off (LSU) to enter the "Receiver Reset" state and start the deactivation procedure.

Pending Receive Reset

Note 45: This state doesn't exist in NT-Auto Activation mode.

The "Pending Receive Reset" state is entered upon detection of loss of framing on the U-interface or expiry of timer T1. This failure condition is signalled to the LT side by turning off the transmit level (SN0). The IEC-Q then waits for a response (no signal level LSU) from the LT side to enter the "Receive Reset" state.

Pending Alerting 1

Note 46: This state only exists in NT-Auto Activation mode.

The "Pending Alerting" state is entered upon detection of loss of framing on the U-interface or expiry of timer T1. This failure condition is signalled to the LT side by turning off the transmit level (SN0). The IEC-Q then waits for a response (no signal level LSU) from the LT side to enter the "Alerting 1" state.

Pending Timing

The pending timing state assures that the C/I-channel code DC is issued four times before the timing signals on the IOM®-2 interface are turned off.
In case the NT-Auto Activation mode is selected the recognition of the LT wake-up tone TL is assumed every time the "Pending Timing" state has been entered from the "Test" state. This function guarantees that the NT (in NT-Auto Activation mode) starts one activation attempts after having been reset, see "Activation Attempt Initiated by NT in NT-Auto Activation Mode", page 142.

Receive Reset

The "Receive Reset" state is entered upon detection of a deactivation request from the LT side, after a failure condition on the U-interface (loss of signal level LSUE), or following the "Pending Reset" state upon expiry of timer T1 or loss of framing. No signal is transmitted on the U-interface, especially no wake-up signal TN, and the S-transceiver or microcontroller is requested to start the deactivation procedure on the NT side (DR). Timer T7 assures that no activation procedure is started from the NT side for a minimum period of T7. This gives the LT a chance to activate the NT.
The state is left only after completion of the deactivation procedure on the NT side (receipt of the C/I-channel code DI), unless a wake-up tone is received from the LT side.

Synchronized 1

When reaching this state the IEC-Q informs the LT side by sending the superframe indication (inverted synchronization word). The loop-back commands decoded by the EOC-processor control the output of the transmit signals:

– Normal activation and UOA = 0: SN3
– Any loop-back and UOA = 0 (no loop-back): SN3T

The value of the issued SAI-bit depends on the received C/I-channel code: DI and TIM lead to SAI = 0, any other C/I-code sets the SAI-bit to 1 indicating activity on the S/T-interface. The IEC-Q waits for the receipt of UOA = 1 to enter the "Synchronized 2" state.

Synchronized 2

In this state the IEC-Q has received UOA = 1. This is a request to activate the S/T-reference point. The loop-back commands detected by the EOC-processor control the output of indications and transmit signals:

- Normal activation and UOA = (1): SN3 and AR
- Single channel loop-back and UOA = (1): SN3T and AR
- Loop-back 2 (LBBD): SN3T and ARL
- The value of the issued SAI-bit depends on the received C/I-channel code: DI and TIM lead to SAI = 0, any other C/I-code sets the SAI-bit to 1 indicating activity on the S/T-interface. The IEC-Q waits for the receipt of the C/I-channel code AI to enter the "Wait for ACT" state.

Test

The "Test" mode is entered when the unconditional commands RES, SSP, Pin-RES, Pin-SSP or µP-SSP are used. It is left when normal IEC-Q operation is selected, i.e. reset and test modes are not active, and the C/I-channel codes DI or ARL are received.

The following signals are transmitted on the U-interface:

- No signal level (SN0) when the C/I-channel code RES is applied or a hardware reset is activated.
- Single pulses (SP) when one of the SSP commands is applied.

Transparent

This state is entered upon the detection of ACT = 1 received from the LT side and corresponds to the fully active state. In the case of a normal activation in both directions of transmission the following codes are output:

- Normal activation or single-channel loop-back: AI
- Loop-back 2: AIL

Wait for ACT

Upon the receipt of AI, the ACT-bit is set to "1" and the NT waits for a response (ACT = 1) from the LT side. The output of indications and transmit signals is as defined for the "Synchronized" state.

Wait for SF

Upon detection of SL2, the signal SN2 is sent on the U-interface and the Receiver waits for detection of the superframe indication. Timer T1 is then stopped and the "Synchronized" state is entered.

Wait for SF AL

This state is entered in the case of an analog loop-back and allows the Receiver to update the AGC, to recover the timing phase, and to update the EQ-coefficients. Signal SN3 is sent instead of signal SN2 in the "Wait-for-SF" state.

4.4.4 State Machine in Repeater Modes

State Diagram

The LT-RP- and NT-RP-state diagrams are subsets of the related diagrams of LT and NT modes so the meaning of events and states are mostly identical. All differences caused by special requirements of the implementation of the repeater modes are listed below.

– ACT-, UOA-, SAI- and DEA-bits are completely controlled via the MON-2-messages, so they are not referenced as outputs in the state diagrams.
– To enable the deactivation of the first section in case of an erroneous situation in the second section of the U-interface, a new C/I-channel code is introduced. DU (0011) leads to the deactivation of the NT-RP passing to "Receive Reset".
– The MON-2-message is accepted and stored at any time except during reset (pin or C/I-channel command).

Note 47: In repeater applications it is recommended to use the EOC Transparent mode. This implies that the C/I indications ARL and AIL are not issued upon reception of the EOC command LBBD from upstream in the states 'Synchronized', Transparent and 'ERROR S/T' of the NT-RP state diagram (see "State Transition Diagram NT-Repeater Mode", page 175). For handling EOC commands in repeater mode, see "EOC Addressing Management", page 257.
In non standard applications of the NT repeater mode the C/I indications ARL and AIL will be issued if the EOC Auto mode is being used and if the EOC command LBBD has been received from upstream.

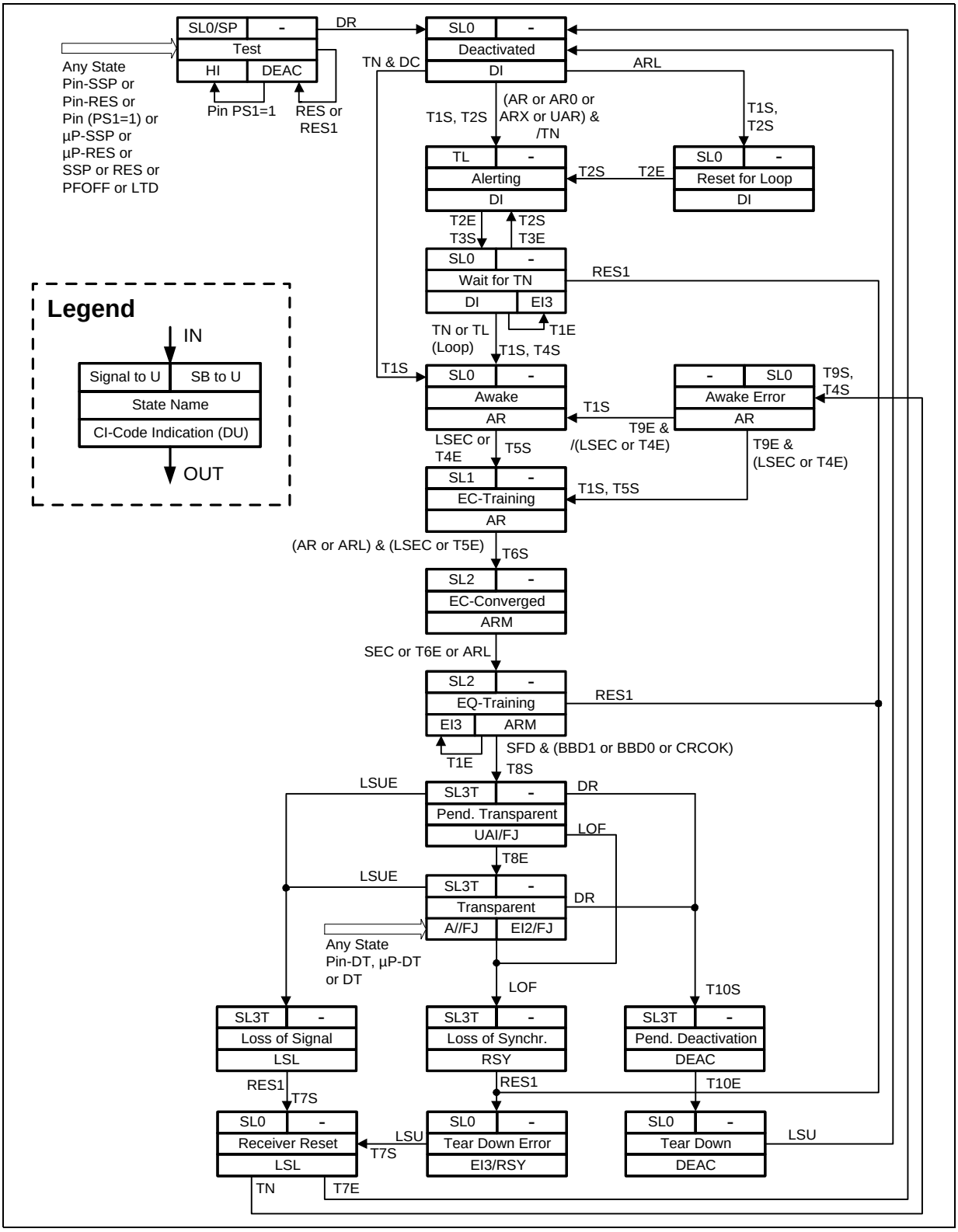
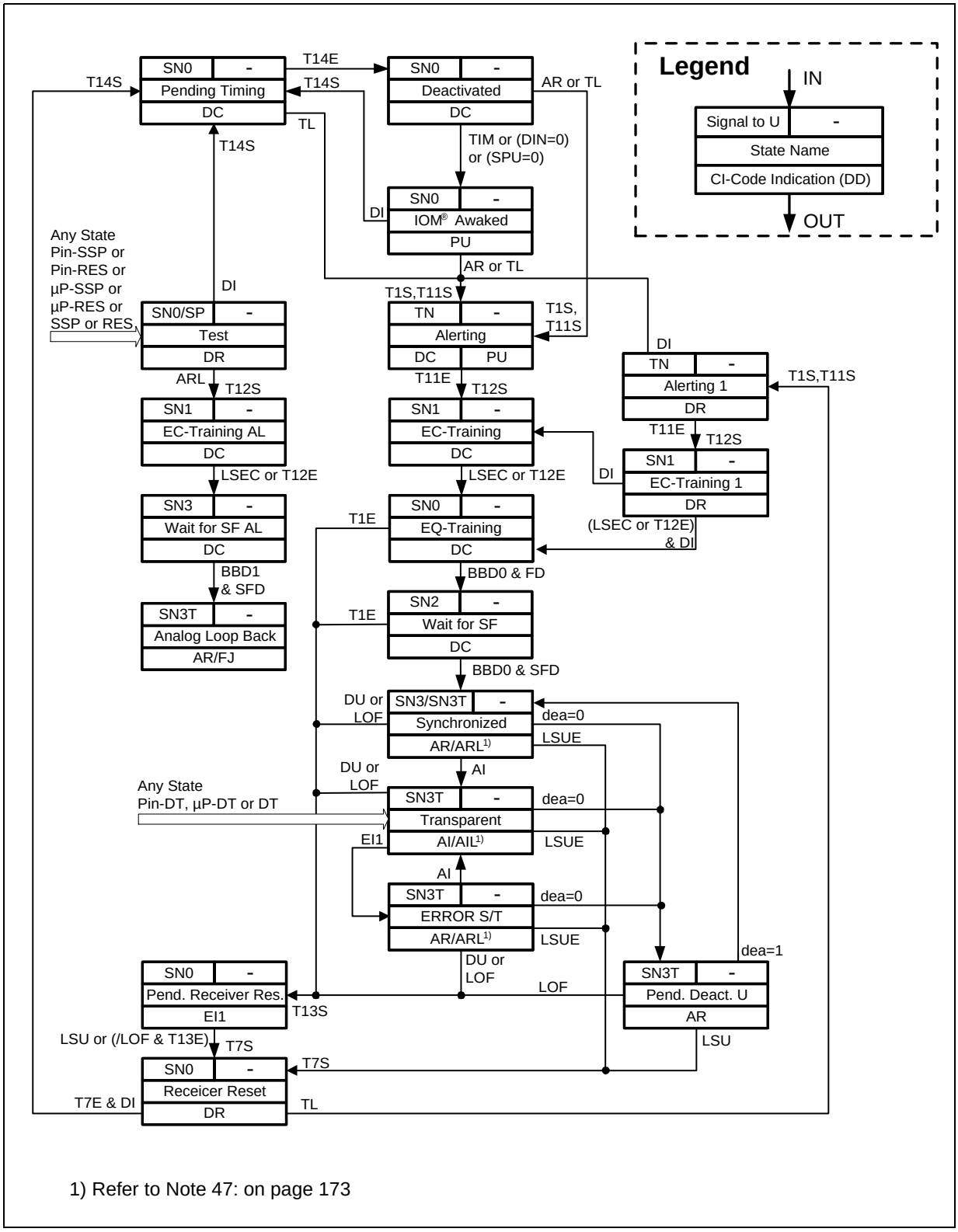


Figure 75 State Transition Diagram LT-Repeater Mode



1) Refer to Note 47: on page 173

Figure 76 State Transition Diagram NT-Repeater Mode

4.5 Monitoring Transmission Quality

The basic tool for monitoring transmission quality is the cyclic redundancy check procedure (see "Cyclic Redundancy Check (CRC)", page 64). Calculation verification and insertion of the CRC bits are performed automatically by the IEC-Q and there is no possibility to directly control this procedure, or access the CRC bits. Nevertheless, the IEC-Q provides several methods for monitoring CRC failures and CRC procedure function. This will be discussed in this chapter. For an overview of CRC violation indications on both LT and NT sides, see Figure "CRC Violation Indications", page 184.

Definitions

NEBE: For the 2B+D and M4 bits received from the U-interface the check sum will be calculated by the CRC processor and compared with the CRC bits received in the successive superframe (see "U-Frame Structure", page 68, for definition of data position in the U-interface). A "Near End Block Error" (NEBE) occurs If these two values are not identical. In other words

– NEBE (LT side) error during transmission from NT to LT
– NEBE (NT side) error during transmission from LT to NT

If a NEBE has been detected the bit FEBE of the next U superframe available for transmission is set to ’0’.

FEBE: A "Far End Block Error" (FEBE) is detected if the FEBE bit of the received from the U-interface is set to ’0’. In other words

– FEBE (LT side) error during transmission from LT to NT
– FEBE (NT side) error during transmission from NT to LT

Note 48: Near-end block errors and far end block errors correspond to bit errors occurred in the superframe preceding the last completed one. This is due to the fact that the CRC sum of a superframe, say SF(1), is transmitted in the next superframe SF(2), i.e. a comparison between the calculated sum and the received sum can only be performed if the superframe containing the check sum, SF(2), has been completely received. Figure 77 shows this relationship for the CRC and the FEBE bits.

LT --> NT Superframe					
Frame Number	...Z	A	B	C	D
Current CRC Bits Related to Frame Number		Z	A	B	C
Current FEBE Bit Related to Frame Number			0	1	2

NT --> LT Superframe					
Frame Number	...0	1	2	3	4
Current CRC Bits Related to Frame Number		0	1	2	3
Current FEBE Bit Related to Frame Number			Z	A	B

Figure 77 Relationship between CRC and FEBE Bits and Superframe Number

NEBE Indications

In NT and LT-RP modes each NEBE will be indicated in the following way

– The MON-1 message NEBE is issued via IOM®-2 and µP interface if only a NEBE occurred
– The MON-1 message FNBE is issued via IOM®-2 and µP interface if NEBE and a FEBE occurred simultaneously

For informations about MON-1 structure and codes, see "MON-1 Codes", page 227.

Note 49: In LT and COT modes a NEBE will not be actively indicated by the IEC-Q. To monitor NEBE violations the NEBE counter should be read out, see "Block Error Counters", page 178.

FEBE Indications

In NT and LT-RP modes each FEBE will be indicated in the following way

– The MON-1 message FEBE is issued via IOM®-2 and µP interface if only a FEBE have occurred
– The MON-1 message FNBE is issued via IOM®-2 and µP interface if NEBE and a FEBE have occurred simultaneously

For informations about MON-1 structure and codes, see "MON-1 Codes", page 227.

Note 50: In LT and COT modes a FEBE will not be actively indicated by the IEC-Q. To monitor NEBE violations the NEBE counter should be read out, see "Block Error Counters", page 178.
Note also that although the FEBE bit is part of the MON-2 indication, a change of the Single bit FEBE alone (i.e. if all other Single Bits didn't change) will not initiate a MON-2 indication in any filtering method setting of Single Bits indications, see "Single Bits Reception from U", page 120 for more information.

4.5.1 Block Error Counters

The IEC-Q provides internal counters for far-end and near-end block errors. This allows a comfortable surveillance of the transmission quality at the U-interface. One block error thus indicates that one U-superframe has not been transmitted correctly. No conclusion about the number of bit errors is therefore possible.

4.5.1.1 NEBE Counter

Each detected NEBE will cause the NEBE counter to be incremented. The maximum count is FF_H. No further incrementation will be done after maximum count is reached.

Read Out and Reset

Issuing the MON-8 command RBEN will cause the IEC-Q to respond with the MON-8 indication ABEC consisting of the NEBE counter value in the second byte of the two byte Monitor Channel indication. For more information about MON-8 codes, refer to "MON-8 Codes", page 228.

MON-8 RBEN

1	0	0	0	0	0	0	0

Read Block Errors Near-end

1	1	1	1	1	0	1	1

MON-8 ABEC

1	0	0	0	0	0	0	0

Answer Block Error Counter

C7	C6	C5	C4	C3	C2	C1	C0

C0 … C7: 8-bit counter value

Each read operation resets the NEBE counter to 00_H. The counter is also reset in all except the following states:

LT modes	NT modes
Line Active	Synchronized
Pend. Transparent	Wait for ACT
Transparent	Transparent
S/T Deactivated	Error S/T

4.5.1.2 FEBE Counter

Each detected FEBE will cause the FEBE counter to be incremented. The maximum count is FF_H. No further incrementation will be done after maximum count is reached.

Read Out and Reset

Issuing the MON-8 command RBEF will cause the IEC-Q to respond with the MON-8 indication ABEN consisting of the NEBE counter value in the second byte of the two byte Monitor Channel indication. For more information about MON-8 codes, refer to "MON-8 Codes", page 228.

MON-8 RBEF

1	0	0	0	0	0	0	0

Read Block Errors Near-end

1	1	1	1	1	0	1	0

MON-8 ABEC

1	0	0	0	0	0	0	0

Answer Block Error Counter

C7	C6	C5	C4	C3	C2	C1	C0

C0 … C7: 8-bit counter value

Each read operation resets the FEBE counter to 00_H. The counter is also reset in all except the following states:

LT modes	NT modes
Line Active	Synchronized
Pend. Transparent	Wait for ACT
Transparent	Transparent
S/T Deactivated	Error S/T

4.5.1.3 Testing Block Error Counters

The block error counter is tested by simulating transmission errors on the line. To simulate transmission errors artificially corrupted CRC bits (as a matter of fact, inverted CRC bits) are send from the LT to the NT side and vice versa. The device detecting corrupted CRC bits will start incrementing the corresponding block error counter which can in turn be read out by a MON-8 command, as described above in this chapter. Figure 78, page 183, gives a complete overview of the test procedures. Describing the commands needed to perform these tests and the corresponding device behavior is the scope of this section.

MON-8 CCRC causes the IEC-Q to permanently transmit inverted CRCs. This command may be used on LT side with the LT in Transparent or Auto mode. On the terminal side CCRC is only required when the device is operated in transparent mode.

In NT-Auto Activation mode corrupted CRCs can be requested directly by the LT side with the EOC command RCC. Again the CRC will be permanently inverted.

With the MON-8 command SFB it is possible on LT and NT side to invert single FEBE-bits. Because this command does not provoke permanent FEBE-bit inversion but sets only one FEBE-bit to (0) per SFB command, it is possible to predict the exact FEBE-counter reading. For more information about MON-8 codes, refer to "MON-8 Codes", page 228.

Note 51: The main application for setting single FEBE-bits are repeater stations not operating in the LT-RP- or NT-RP mode).

Request Corrupt CRCs (RCC)

If the EOC Auto mode is used on the NT side (see "EOC Auto/Transparent Mode", page 55) this command requests the NT side to transmit corrupted (i.e. inverted) CRCs upstream to test the LT NEBE-counter. Simultaneously the FEBE-counter and MON-1-messages of the NT are disabled.

If the EOC Transparent mode is used on the NT side the CRC will not be corrupted, the FEBE-counter is enabled and MON-1 FEBE-messages will be issued, i.e. the IEC-Q will not react to this command.

This command is a predefined EOC command which can be controlled by the MON-0 message issued on the LT side downstream (see "Access to EOC of U-Interface", page 110).

Initialization (LT side)

MON-0							RCC
0	0	0	0	0	0	0	1

Request of Corrupt CRC

0	1	0	1	0	0	1	1

Acknowledgment (NT and LT side)

MON-0							RCC
0	0	0	0	0	0	0	1

Request of Corrupt CRC

0	1	0	1	0	0	1	1

Notify of Corrupt CRC (NCC)

If the EOC Auto mode is used on the NT side (see "EOC Auto/Transparent Mode", page 55) this command requests the NT to disable the NEBE-counter and MON-1 NEBE indications.

In the EOC Transparent mode the IEC-Q will not react to this command.

This command is a predefined EOC command which can be controlled by the MON-0 message issued on the LT side downstream (see "Access to EOC of U-Interface", page 110).

Initialization (LT side)

MON-0							NCC
0	0	0	0	0	0	0	1

Notify of Corrupt CRC

0	1	0	1	0	1	0	0

Acknowledgment (NT and LT side)

MON-0							NCC
0	0	0	0	0	0	0	1

Notify of Corrupt CRC

0	1	0	1	0	1	0	0

Return to Normal (RTN)

If the EOC Auto mode is used on the NT side (see "EOC Auto/Transparent Mode", page 55) this command requests the NT to disable all previously received EOC commands.

In the EOC Transparent mode the IEC-Q will not react to this command.

This command is a predefined EOC command which can be controlled by the MON-0 message issued on the LT side downstream (see "Access to EOC of U-Interface", page 110).

Initialization (LT side)

MON-0						RTN	
0	0	0	0	0	0	0	1

Return to Normal							
1	1	1	1	1	1	1	1

Acknowledgment (NT and LT side)

MON-0						RTN	
0	0	0	0	0	0	0	1

Return to Normal							
1	1	1	1	1	1	1	1

Corrupt CRCs (CCRC)

If the EOC Transparent mode is used on the NT side, or if one of the LT modes is used (see "EOC Auto/Transparent Mode", page 55) this command requests the IEC-Q to transmit corrupted (i.e. inverted) CRCs. It will be executed immediately.

If the EOC Auto mode is used on the NT side the IEC-Q will not react to this command.

This command is delivered by the MON-8 message (see also "MON-8 Codes", page 228).

Initialization (NT [transparent only], LT [auto/transparent])

MON-8						CCRC	
1	0	0	0	0	0	0	0

Corrupt CRC							
1	1	1	1	0	0	0	0

No acknowledgment will be issued.

Normal (NORM)

Disables all previously sent MON-8 latching commands. The command may be used in Auto and Transparent mode in LT modes and in Transparent mode in NT modes.

If the EOC Auto mode is used on the NT side the IEC-Q will not react to this command.

Initialization (NT [Transparent only], LT [Auto/Transparent]):

MON-8						NORM	
1	0	0	0	0	0	0	0

Normal							
1	1	1	1	1	1	1	1

No acknowledgment will be issued.

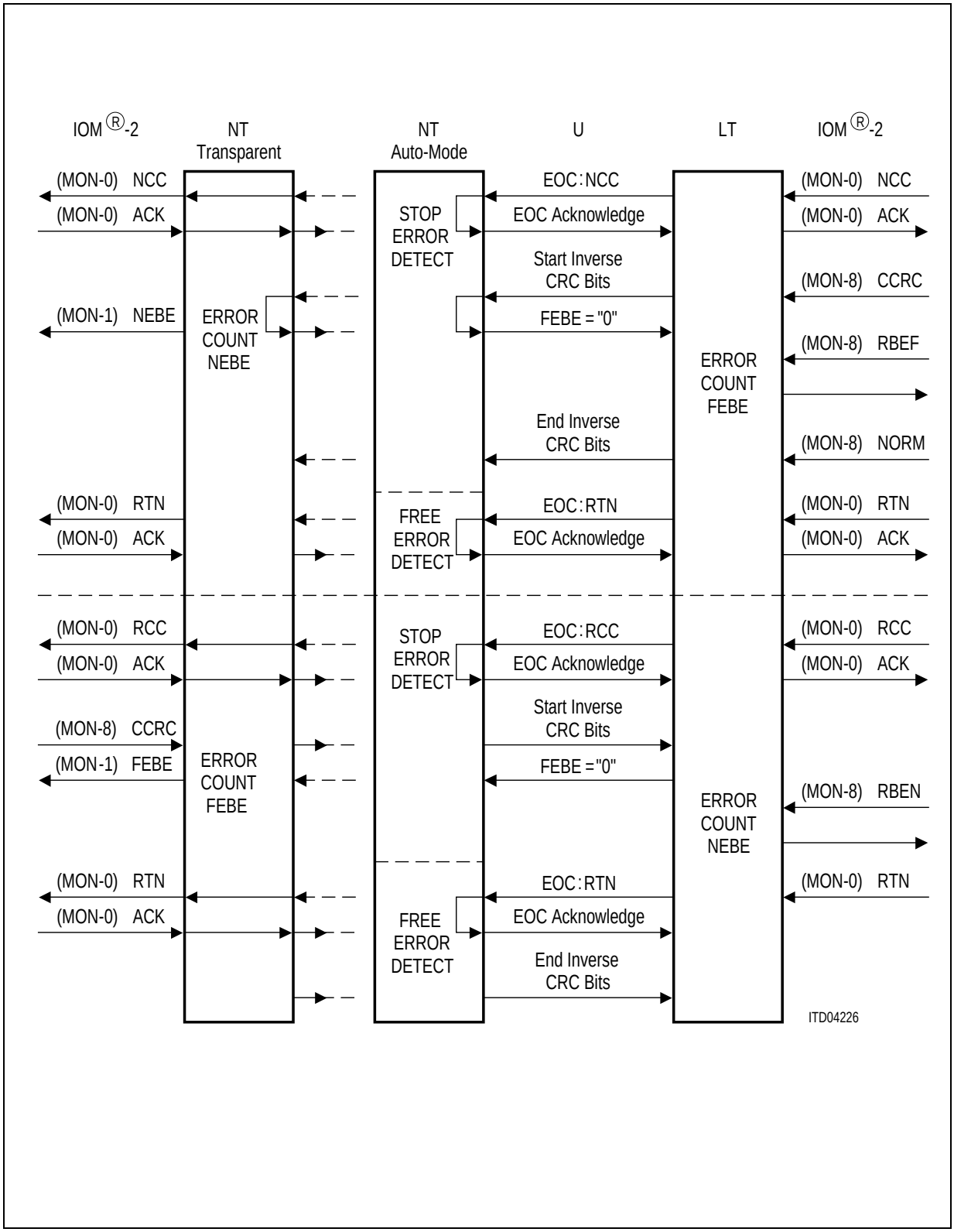


Figure 78 Block Error Counter Test

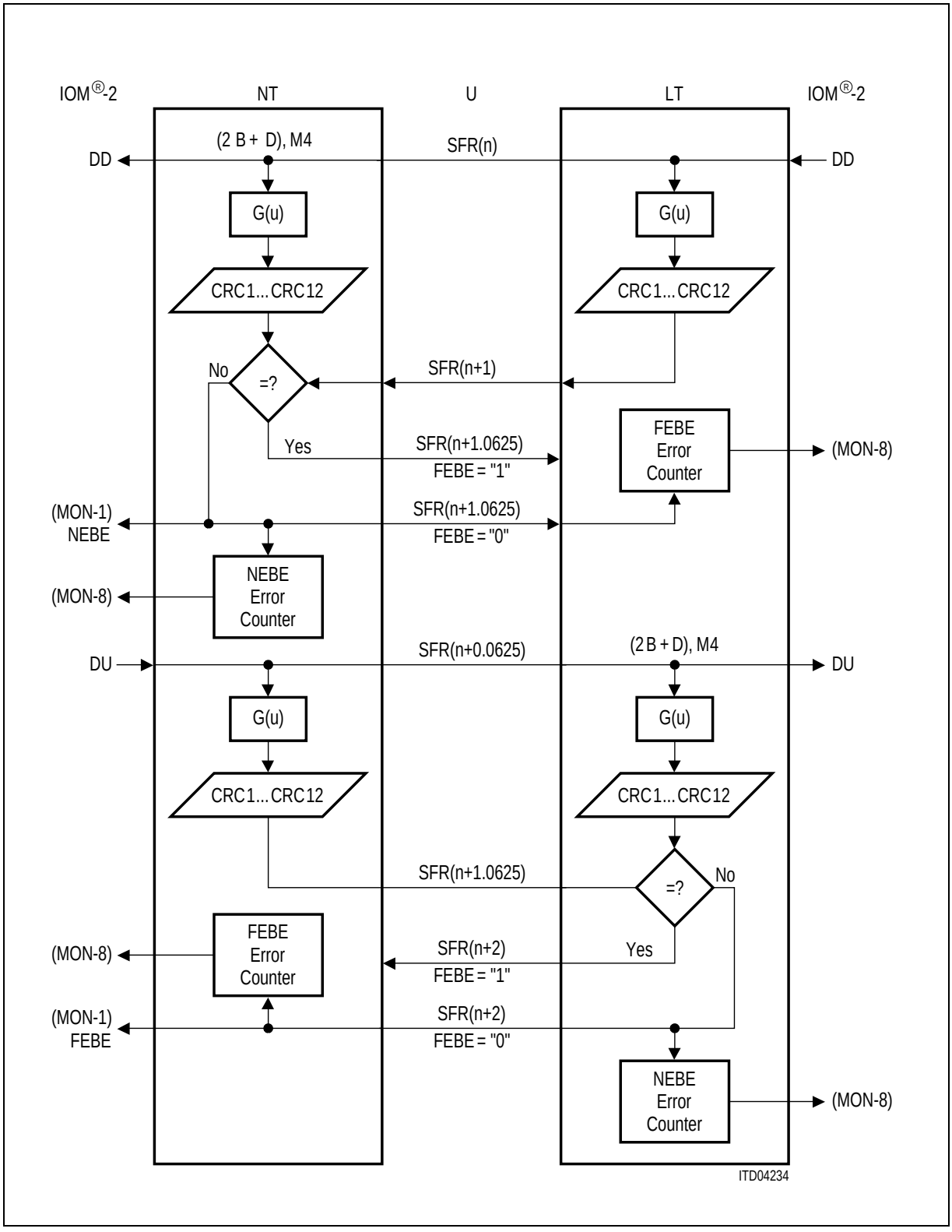


Figure 79 CRC Violation Indications

4.6 Chip Internal Test Options

The IEC-Q permits limited access to internal test procedures and internal data. This chapter explains how these tests can be performed.

4.6.1 Self-Test

Note 52: This section applies only in the NT, NT-PBX and TE modes.

This test can be requested by the terminal in order to verify correct performance. The self-test is started with the MON-1-command ST. No tests are performed within the IEC-Q. If the ST-message has been received correctly, the device returns the MON-1-message STP (self-test passed) to the terminal. With this function the terminal has a possibility to verify the existence of a layer-1 device.

Initialization (NT side)

MON-1							ST
0	0	0	1	0	0	0	0

Self Test							
0	0	0	1	x	x	x	x

Acknowledgment (NT side)

MON-1							STP
0	0	0	1	0	0	0	0

Self Test Pass							
0	0	1	0	x	x	x	x

x: Do not care

For more information about MON-1 commands and codes, see "MON-1 Codes", page 227.

4.6.2 Receiver Coefficient Values

Some of the internal chip registers can be read via MON-8-messages.

Of interest to the user are the values of the coefficients for equalizer and echo canceller. This information will however only proof useful if a detailed, theoretical chip knowledge exists.

Registers are read by sending a two-byte MON-8 message RCOEF. The first byte identifies the command as an internal register access, the second addresses the register.

The 16-bit register value is returned in two MON-8 messages DCOEF of two bytes each.

Table 31 shows the address range for equalizer (26 coefficients) and echo canceller coefficients (36 coefficients).

Initialization

Read request

MON-8	(1. Byte)	1 0 0 0	1 0 0 0	; Select register access
	(2. Byte)	a a a a	a a a a	; Coefficient address

For each requested coefficient 16 bit are returned in the following manner

MON-8	(1. Byte)	1 0 0 0	1 0 0 0	
	(2. Byte)	d d d d	d d d d	; Data bits D0 – D7[1)]
	(3. Byte)	1 0 0 0	1 1 0 0	
	(4. Byte)	d d d d	d d d d	; Data bits D8 – D15[1)]

Table 31 Internal Coefficient Addresses

Register	Address Range (decimal)	1. Filter Coefficient
Echo Canceller	6 … 41	41
Equalizer	44 … 69	69

For more information about MON-8 commands and codes, see "MON-8 Codes", page 228.

4.7 Test Loop-Backs

Test loop-backs are specified by the national PTTs in order to facilitate the location of defect systems. Four different loop-backs are defined. The position of each loop-back is illustrated in Figure 80.

1) Binary complement format ($FFFF_H$ = –1d)

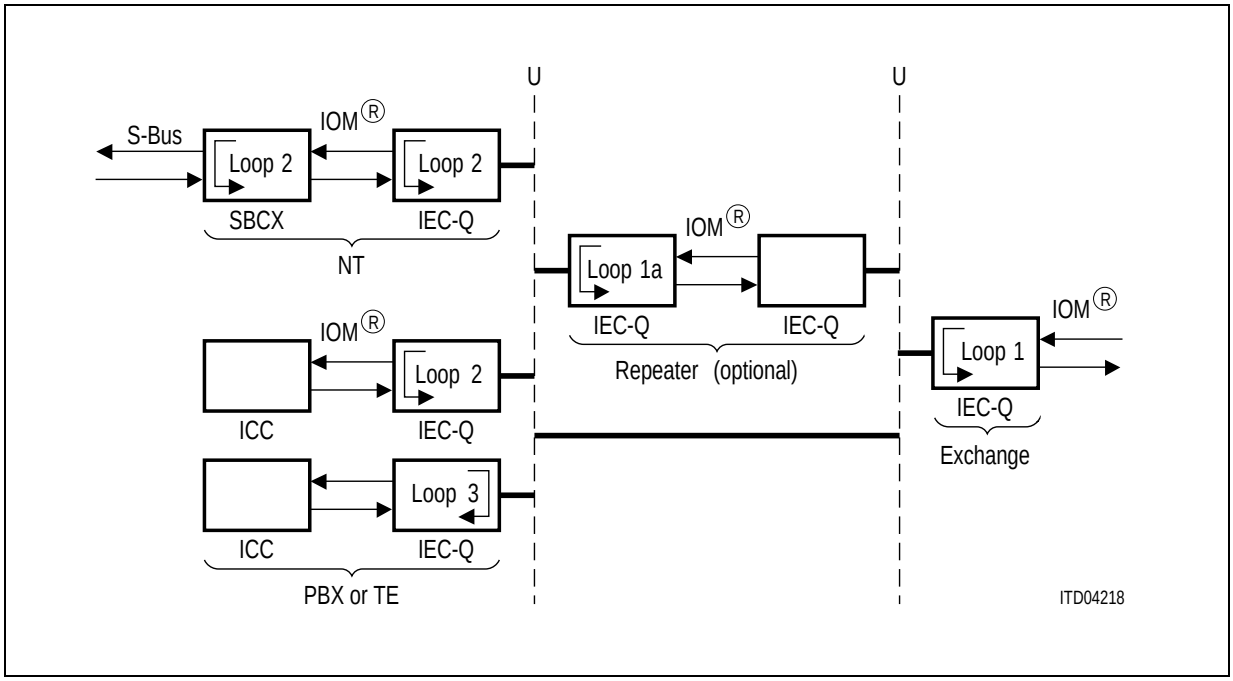


Figure 80 Test Loop-Backs Supported by the IEC-Q

Loop-backs #1, #1A and #2 are controlled by the exchange. Loop-back #3 is controlled by the terminal. All four loop-back types are transparent. This means all bits that are looped back will also be passed onwards in the normal manner.

The next sections describe how these loop-backs are closed and opened using the C/I- and MON-commands available to the IEC-Q.

4.7.1 Analog Loop-Back (No. 1/No. 3)

Both loop-back #1 and loop-back #3 are closed by the IEC-Q as near to the U-interface as possible. For this reason they are also called analog loop-backs. Data transmitted to the U-interface are looped back as well. Only this internal loop-back signal is processed; signals received from the U-interface are ignored. Because all analog signals will still be passed on to the U-interface the opposite station (NT in case of #1, LT in case of #3) will be activated as well, if available.

States

Because signals received from the metallic line are ignored, the IEC-Q stays in LT modes in the "Line Active" state for loops No.1 and No.1a (upstream ACT-bit cannot be received, see "LT Modes State Diagram", page 147).

In LT-RP mode the device stays in the "Transparent" state (see "State Machine in Repeater Modes", page 173).
In NT modes (No.3) the device stays in "Analog Loop-Back" (see "NT Modes State Diagram", page 161).

Analog Loop-Back Control

Before an analog loop-back is closed with the C/I-command ARL (activation request loop-back, see "C/I Channel Codes", page 224), the device should have been reset.

In order to open an analog loop-back correctly, reset the device into the TEST state with the C/I-command RES (or by pin reset). This ensures that the echo coefficients and equalizer coefficients will converge correctly when activating the following time.

Although loop-back #1 and loop-back #3 are closed with the same command and perform the same function, they cannot be started from the same state: Loop-back #1 is closed when in the state "Deactivated" (LT side); loop-back #3 can only be closed in the state "Test" (NT side).

For examples of programming these loops, refer to "Examples for Analog Loop-Back Control", page 236.

4.7.2 Partial and Complete Loop-Back (No. 2)

For loop-back #2 several alternatives exist. Both the type of loop-back and the location may vary. Three loop-back types belong to the loop-back-#2 category:

– Complete loop-back
– B1-channel loop-back
– B2-channel loop-back

The complete loop-back comprises both B-channels and the D-channel. It may be closed either in the IEC-Q itself or in a downstream device. Single-channel loop-backs are always performed within the IEC-Q. In this case the digital data of DOUT will be directly fed back into DIN. This also applies if the complete loop-back is closed in the IEC-Q.

Normally loop-back #2 is controlled from the exchange. The EOC commands LBBD, LB1 and LB2 are used. They will be recognized and executed automatically in the NT IEC-Q if the EOC Auto mode is selected (see "EOC Auto/Transparent Mode", page 55). Due to the automatic acknowledgment in EOC Auto mode, the EOC-message will be mirrored back immediately by the NT as a confirmation[1)]. EOC commands are accessed via MON-0 messages. For more details, see "Access to EOC of U-Interface", page 110.

If the EOC Transparent mode is used in the NT the MON-8-commands LBBD, LB1 and LB2 are available (see "EOC Auto/Transparent Mode", page 55).

All loop-back functions are latched. This allows channel B1 and channel B2 to be looped back simultaneously. All loop-backs are opened when the EOC command RTN or the MON-8 command NORM is sent.

A detailed operational description will be give in the subsequent sections.

1) Note however that this confirmation is issued before the loop-back function is initialized. Therefore it cannot be regarded as an acknowledgment that the loop-back function was started correctly

4.7.2.1 Complete Loop-Back

When receiving the EOC-command LBBD in Auto mode, the NT IEC-Q does not close the loop-back immediately. Because the intention of this loop-back is to test the complete NT, the IEC-Q passes the complete loop-back request on to the next downstream device. This is achieved by issuing the C/I-code AIL in the "Transparent" state or C/I = ARL in states different than "Transparent" (see "State Machine in NT Modes", page 160). If the downstream device is not able to close the complete loop-back, a MON-8-message LBBD may be returned to the NT IEC-Q. This then will close the complete loop-back within the IEC-Q itself (B1 + B2 + D-channels). All remaining IOM®-2-information (monitor, C/I-channel as well as the bits MR and MX) are still read from the IOM®-2 or the µP interface (if used). For this reason it is still possible for a layer-2 device to deactivate the NT despite the fact that the loop-backs are controlled by the exchange.

Note 53: ***If operated in EOC Auto mode, the complete loop-back can only be closed in the IEC-Q if previously the EOC-command LBBD was received. Without this EOC-message the MON-8-command LBBD will be ignored.***
If operated in EOC Transparent mode, a complete loop-back may be closed at any time with MON-8 LBBD.

In EOC Auto mode the complete loop-back is reset after RTN has been received in the EOC-channel. In the EOC Transparent mode MON-8 NORM is used for this purpose. No reset as for loop-backs #1 or #3 is required for loop-back #2. The line is active and ready for data transmission.

As an example Figure 81 illustrates these two options if the IEC-Q is used together with the SBC-X and the ICC.

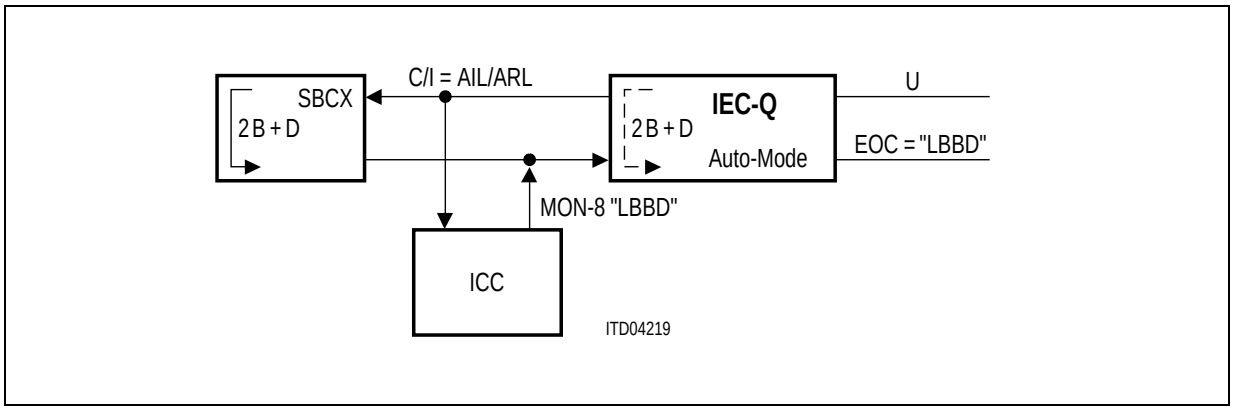


Figure 81 Complete Loop-Back Options in NT modes

4.7.2.2 Single-Channel Loop-Backs

Single-channel loop-backs are always performed directly in the IEC-Q. No difference between the B1-channel and the B2-channel loop-back control procedure exists. They are therefore discussed together.

In EOC Auto mode the B1-channel is closed with the EOC-command LB1. LB2 causes the channel B2 to be looped back. Because these functions are latched, both channels may be looped back simultaneously by sending first the command to close one channel followed by the command for the second one.

In the EOC Transparent mode, single channels are closed with the corresponding MON-8-commands.

Single-channel loop-backs are resolved in the same manner as described for the complete loop-back. The NT may be deactivated with layer 2 while single loop-backs are closed.

4.7.2.3 Repeater Loop-Back (No. 1A)

Loop-back #1A is always closed in the repeater. Functionally it corresponds to loop-backs #1 and #3 on the exchange and on the network side. If a line contains more than one repeater unit, it is possible to address each unit individually in order to close loop-back #1A in the specified unit only.

For loop-back #1A everything described in section "Analog Loop-Back (No. 1/No. 3)", page 187 applies: The loop-back is opened with the C/I-command RES, closed with the C/I-command ARL, and it is closed as near to the U-interface as possible. The difference results from the fact that the command ARL needs to be generated by the repeater control unit (µP or ASIC) according to national repeater specifications.

This specification defines an EOC-command which will activate loop-back #1A if received in conjunction with the repeater address (001_B). The NT-RP is operating in transparent mode. The repeater control unit watches for MON-0-commands with address (001_B). If the predefined loop-back #1A command is received, the repeater control unit sends the C/I-code ARL to the LT-RP and loop-back #1A will be closed.

For more information, see "EOC Addressing Management", page 257.

Figure 82 illustrates this in a system with two repeater units where the second unit is requested to close loop-back #1A.

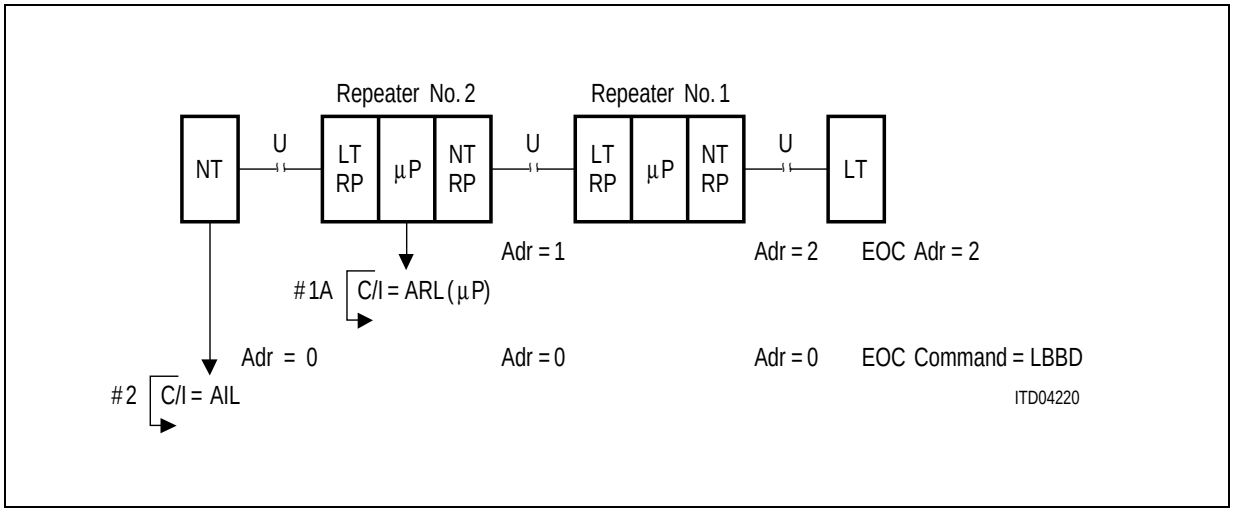


Figure 82 Closing Loop-Back #1A in a Multi-Repeater System

4.7.2.4 Codes

This section gives the Monitor Channel messages used to control test loop-back #2. For more information about Monitor messages and codes in general, see also "Monitor Channel Codes", page 226.

Codes Used in EOC Auto Modes for Partial Loop-Backs

Initialization from LT

MON-0						LB1		Close loop-back in B1-channel							
0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	1

Acknowledgment (issued on LT and NT side)

MON-0						LB1		Close loop-back in B1-channel							
0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	1

Initialization from LT

MON-0						LB2		Close loop-back in B2-channel							
0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	0

Acknowledgment (issued on LT and NT side)

MON-0						LB2		Close loop-back in B2-channel							
0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	0

Codes Used in EOC Auto Modes for Complete Loop-Backs

If the complete loop should be closed outside the IEC-Q, the following code is applied.

Initialization (LT side)

MON-0							LBBD	Close loop-back 2B + D							
0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0

Acknowledgment (issued on LT and NT side)

MON-0							LBBD	Close loop-back 2B + D							
0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0

If the complete loop should be closed inside the IEC-Q, the following code is applied.

Initialization (LT side)

MON-0							LBBD	Close loop-back 2B + D							
0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0

Acknowledgment (issued on LT and NT side)

MON-0							LBBD	Close loop-back 2B + D							
0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0

Close loop in IEC-Q (NT side)

MON-8							LBBD	Close loop-back 2B + D							
1	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1

Codes Used in EOC Transparent Modes for Partial Loop-Backs

Single-channel and complete loop-backs are closed from the NT side with the MON-8-commands.

Initialization (NT side)

MON-8 LB1

1	0	0	0	0	0	0	0

Close loop-back in B1-channel

1	1	1	1	0	1	0	0

No acknowledgment issued.

Initialization (NT side)

MON-8 LB2

1	0	0	0	0	0	0	0

Close loop-back in B2-channel

1	1	1	1	0	0	1	0

No acknowledgment issued.

Initialization (NT side)

MON-8 LBBD

1	0	0	0	0	0	0	0

Close loop-back in 2B + D

1	1	1	1	0	0	0	1

No acknowledgment issued.

4.8 Chip Identification

The chip identification of IEC-Q Version 5.3 is "03_H". It is the same chip identification as Versions 5.1 and 5.2. If the MON-8 command RID is issued the IEC-Q will respond by indicating this identification via the MON-8 command AID (see also "MON-8 Codes", page 228).

Codes

Identification demand

MON-8 **RID**

1	0	0	0	0	0	0	0

Read Identification

0	1	0	–	–	–	A0	A1

Response

MON-8 **AID**

1	0	0	0	0	0	0	0

Answer Identification

0	0	0	0	0	0	1	1

4.9 Access to Power Status Pins

This chapter deals with the operational aspects of accessing the power controller maintenance features provided by the IEC-Q. Pins PS1 and PS2 are available to support these features. Furthermore, in stand-alone mode pin DISS is also available.

4.9.1 Monitoring Primary and Secondary NT Power Supply

Note 54: This section applies only in NT and TE modes.

Power status bits 1 and 2 (PS1/2) are used to monitor both primary and secondary NT power supply. This information is transferred via the Single Bits channel to the exchange side. For information about the Single Bits, see "Single Bits Channel", page 69.

PS1

The primary power supply status bit (bit M42 of the U-frame) is level sensitive. With pin PS1 set to (1) the overhead bit is set to (1). With pin PS1 set to (0) overhead bit M42 is set to (0).

PS2

The secondary power supply status bit (bit M43 of the U-frame) is level sensitive. With pin PS2 set to (1) the overhead bit is set to (1). With pin PS2 set to (0) overhead bit M43 is set to (0).

4.9.2 Monitoring Remote Power Feed Circuit in LT Modes

Note 55: This section applies only in LT modes.

The first power status pin PS1 is used to monitor the remote power feed circuit of the subscriber line. A high level ’1’ indicates that the remote power has been turned off. In order to indicate this to the processing unit, the C/I-code "HI" (0011_B) will be issued and the device is reset into the "TEST" state. An existing communication link will break down.

4.9.3 Monitoring Power Feed Current in LT Modes

Note 56: This section applies only in LT modes.

The pin PS2 provides a serial interface in order to read in the value of the current fed to the subscriber line by the power controller. This feature is available only in combination with a power controller which supports this feature (the IEPC does not). The power controller is to send eight-bit data which are read synchronous to the IOM®-2-clock signals. Timing of the serial data stream forwarded to pin PS2 must be synchronous to the signals of pin DIN (see Figure 83 for details).

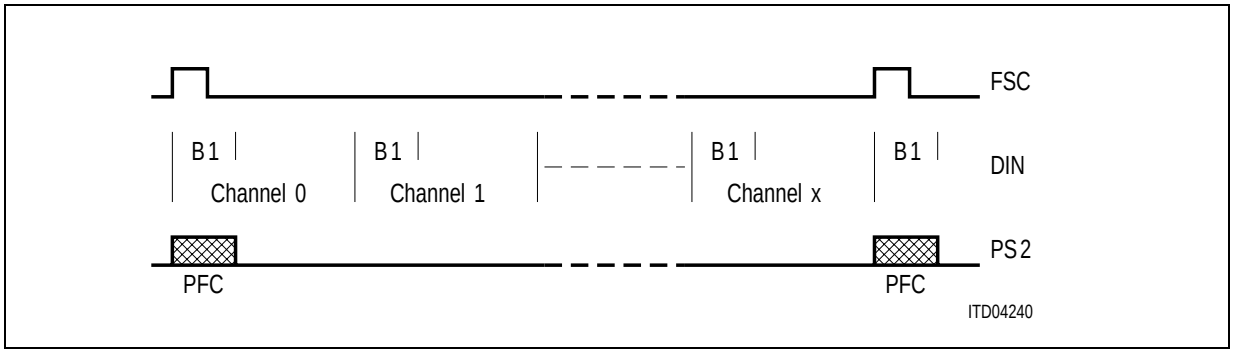


Figure 83 Serial Data Port of Pin PS2 in LT Modes

This value can be read out through MON8-Channel. The MON-8 command RPFC (Read Power Feed Current) requests the IEC-Q to return the current feed value which has been read from pin PS2. The IEC-Q will then respond by issuing the MON-8 indication "APFC" (Answer Power Feed Current) in the next IOM®-2 frame available. The codes of these commands are given below.

Refer to "IOM®-2 Monitor Channel", page 76[1)] for informations about the structure and function of the Monitor Channel. See also "MON-8 Codes", page 228, for a summary of all available MON-8 command.

MON-8 **RPFC** **Read Power Feed Current**

1	0	0	0	0	0	0	0

1	1	1	1	1	0	0	0

MON-8 **APFC** **Answer Power Feed Current**

1	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0

4.9.4 Access to Pin DISS

Note 57: This section applies only in stand-alone mode.

NT and TE Modes

Note 58: This feature is only available in EOC Auto mode (see "EOC Auto/Transparent Mode", page 55).

In these modes the output pin DISS (disable) is set to (1) if the EOC-command "close complete loop" (LBBD) has been detected by the NT (see "Predefined EOC Codes", page 231). It may be used to test a secondary power source (e.g. battery check). The DISS-pin is set back to (0) with the EOC-command "RTN" or a reset.

1) If the microprocessor mode is being used refer to "Monitor Channel Access", page 101

LT Modes

The pin DISS is used for switching off the remote power supply of the subscriber line. It is set to ’1’ by the C/I-command "LTD" (0011_B). A software reset with C/I = "RES" does not affect the DISS-pin. While the DISS-pin is set to (1), the device is in the "TEST" state "State Machine in LT Modes", page 146.

4.10 Access to Power Controller Interface

Note 59: This chapter applies only in stand-alone mode.

The interface consists of three data bits PCD0 ... 2, two address bits PCA0,1, read and write signals $\overline{\text{PCRD}}$ and $\overline{\text{PCWR}}$ respectively as well as an interrupt facility INT.

For dynamical characteristics, see "Power Controller Interface Timing", page 277.

For an example for programming code, see "Example for Programming Power Controller Interface", page 235.

4.10.1 Data Port

Communication with the data port (PCD0 ... 2, PCA0,1, $\overline{\text{PCRD}}$ and $\overline{\text{PCWR}}$) of the power controller interface is established with local Monitor messages (MON-8) of the IOM®-2 interface. Table 32 lists all MON-8 commands that are relevant to the power controller interface.

Table 32 MON-8 and C/I-Commands

Channel	Code	Function
MON-8	WCI	Write to interface. Address and data is contained in the MON-command. The address is latched, data is not latched.
MON-8	RCI	Read from interface at specified address. Address is latched and the current value of the data port is read. The result is returned to the user with MON-8 "ACI".
MON-8	ACI	Answer from interface. After a RCI-request the value of three data bits at the specified address is returned.

The codes of these commands are given below. For more information about programming MON-8 commands see "MON-8 Codes", page 228

MON-8 **WCI** **Write Controller Interface**

1	0	0	0	0	0	0	0

0	1	1	D0	D1	D2	A0	A1

MON-8 **RCI** **Read Controller Interface**

1	0	0	0	0	0	0	0

0	1	0	–	–	–	A0	A1

MON-8 **ACI** **Answer Controller Interface**

1	0	0	0	0	0	0	0

D0	D1	D2	–	–	–	–	–

After the receipt of a MON-8-command the IEC-Q will set the address/data bits and generate a read or write pulse.

The address bits are latched, and the output is stable until a new dedicated MON-8 command is issued.

The initial value on the address lines after a software, hardware or power-on reset is (11_B).

4.10.2 Interrupt

For every change at the input pin INT, the IEC-Q will transmit a C/I-channel code (0110_B), INT, in 4 successive IOM®-2-frames.

Note 60: Interpretation of the interrupt cause and resulting actions need to be performed by the control unit.

The input condition of the pin INT is sampled every 4 IOM®-2-frames. An interrupt indication must therefore be applied to pin "INT" for at least 4 IOM®-2-frames.

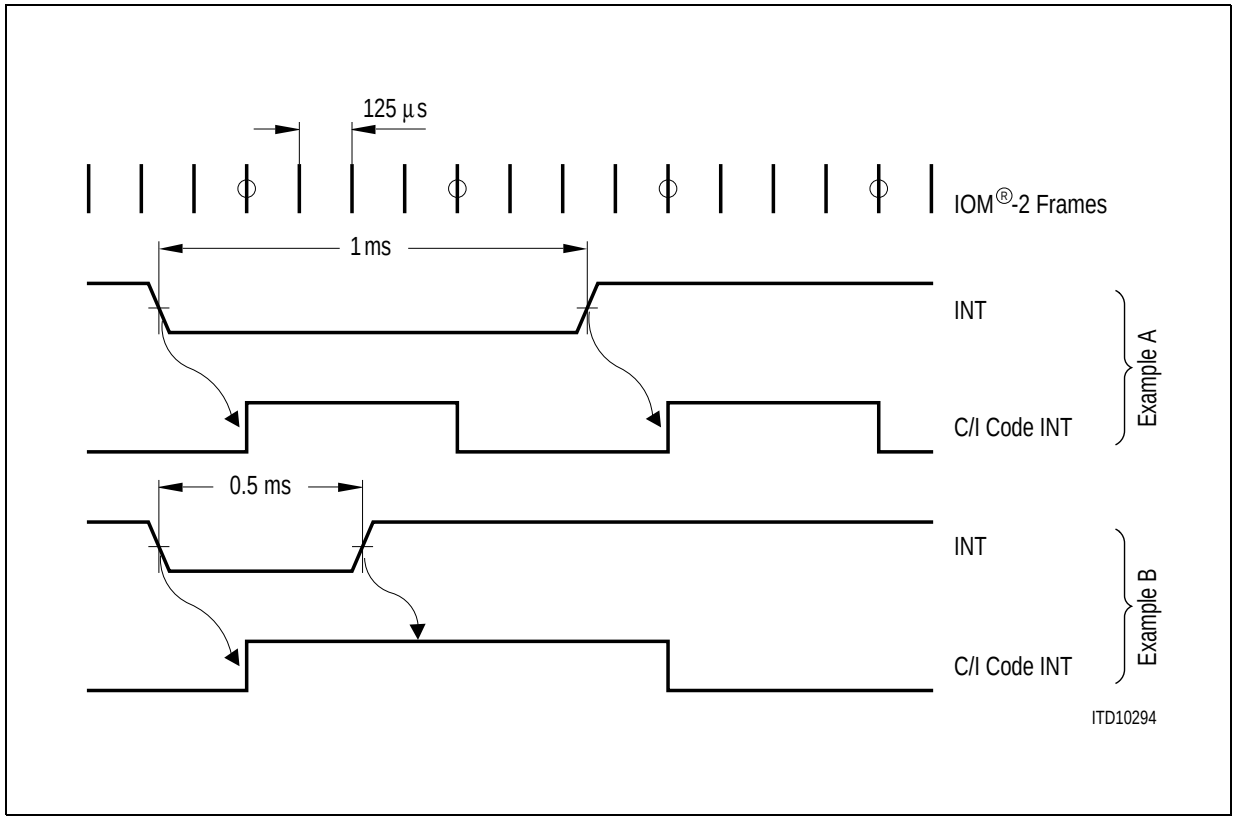


Figure 84 Sampling of Interrupts

4.11 S/G Bit and BAC Bit Operations

Note 61: This chapter applies only in the µP-TE mode (see "Setting Operating Modes", page 50).

If DCL = 1.536 MHz the IOM®-2 interface consists of three IOM®-2 channels (see "Terminal Timing Mode", page 73). The last octet of an IOM®-2 frame includes the S/G and the BAC bit. The S/G bit is always written and never read by the IEC-Q. Its value depends on the last received EOC-command and on the status of the BAC bit. The processing mode for the S/G bit is selected via bits SWST:BS, SWST:SGL and ADF:CBAC (see "ADF-Register", page 219). The following table and state machine give the detailed behavior of the complete S/G bit control function.

Table 33 S/G Bit Control Overview

SWST: BS	SWST: SGL	ADF: CBAC	Description	Application
0	0	x[1)]	S/G bit always "0"	(default)
0	1	0	S/G bit always "1"	S/G and BAC are handled by other devices than the IEC-Q
0	1	1	S/G bit set to "1" continuously with EOC 25_H received, reset to "0" with EOC 27_H received BAC bit controls S/G-bit, upstream D-channel not affected	ELIC® on linecard, Interframe fill of terminals contains zeroes (e.g. ’01111110’)
1	0	0	S/G bit set to "1" for 4 IOM®-2-frames with EOC 25_H received, automatically reset to "0" after that. This is the default setting of ADF:CBAC after reset	Synchronization of base station, e.g. IBMC or MBMC
1	0	1	S/G bit set to "0" for 4 IOM®-2-frames with EOC 25_H received, automatically reset to "1" after that	Synchronization of base station, e.g. IBMC or MBMC. Inverse polarity to the setting 1,0,0 (last row)
1	1	0	S/G bit set to "1" continuously with EOC 25_H received, reset to "0" with EOC 27_H received BAC bit not read by IEC-Q V 5.3	
1	1	1	S/G bit set to "1" continuously with EOC 25_H received, reset to "0" with EOC 27_H received BAC bit controls upstream D-channel and S/G-bit	ELIC® on linecard, Interframe fill of terminals are ’ones’

1) ’x’ is don’t care

4.11.1 State Machine

The exact S/G Bit Control function is given in the following state diagrams.

The values in the state diagrams are to be interpreted as follows

:

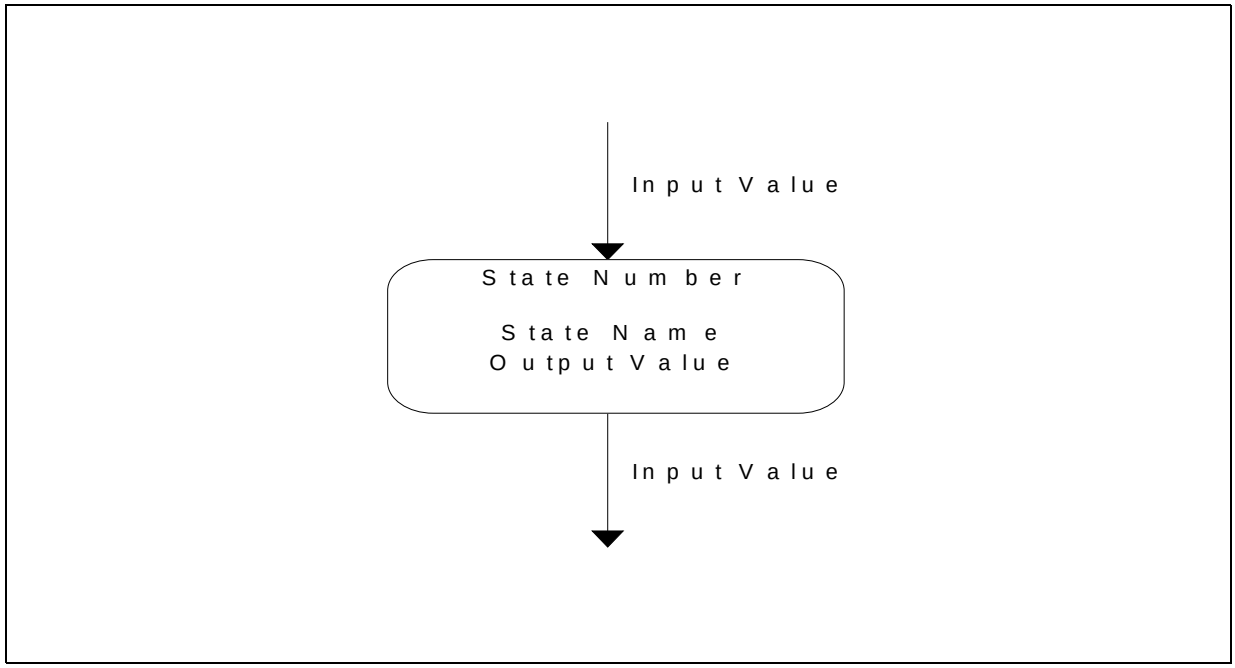


Figure 85 State Machine Notation for S/G Bit Control

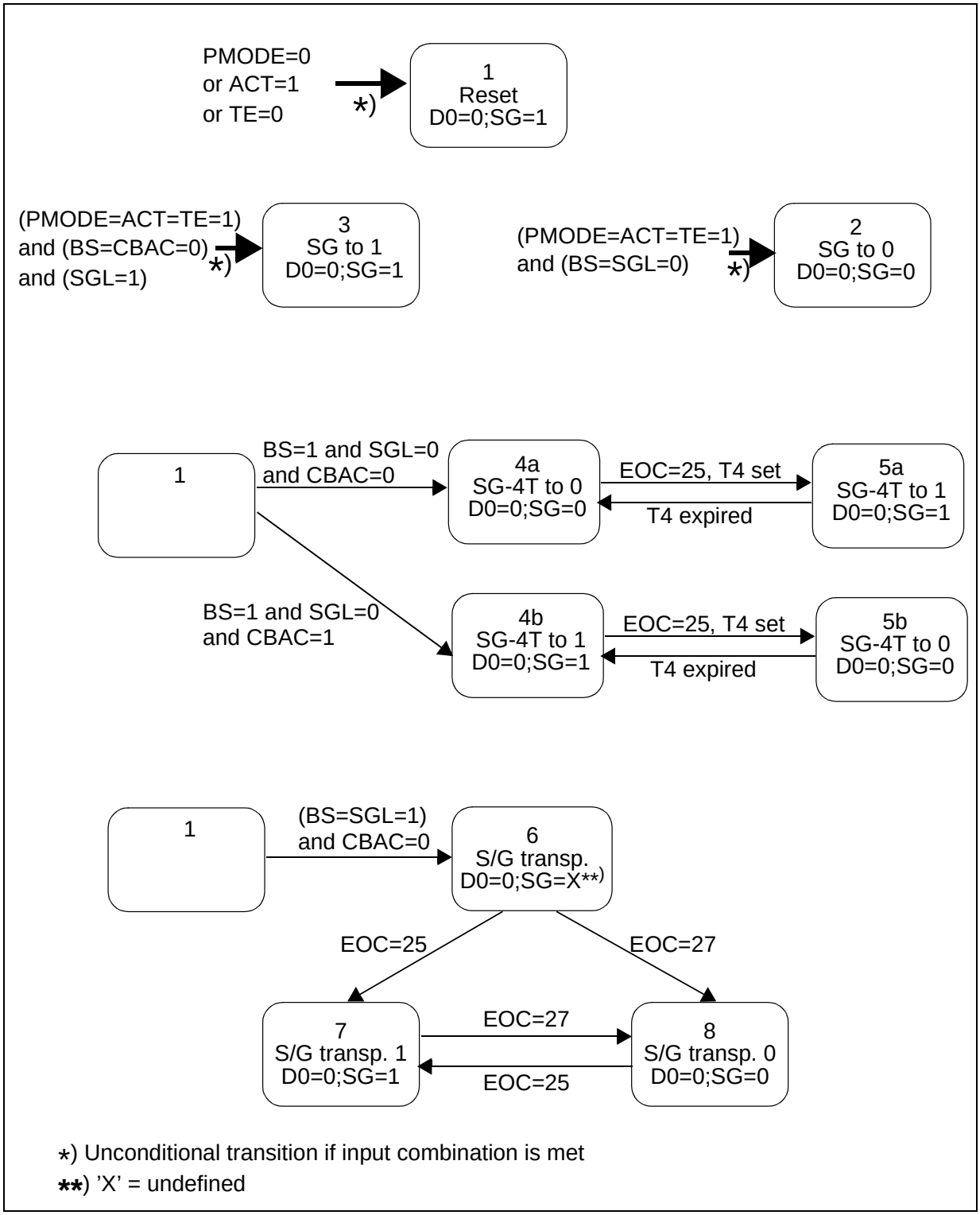


Figure 86 State Machine for S/G Bit Control (part 1)

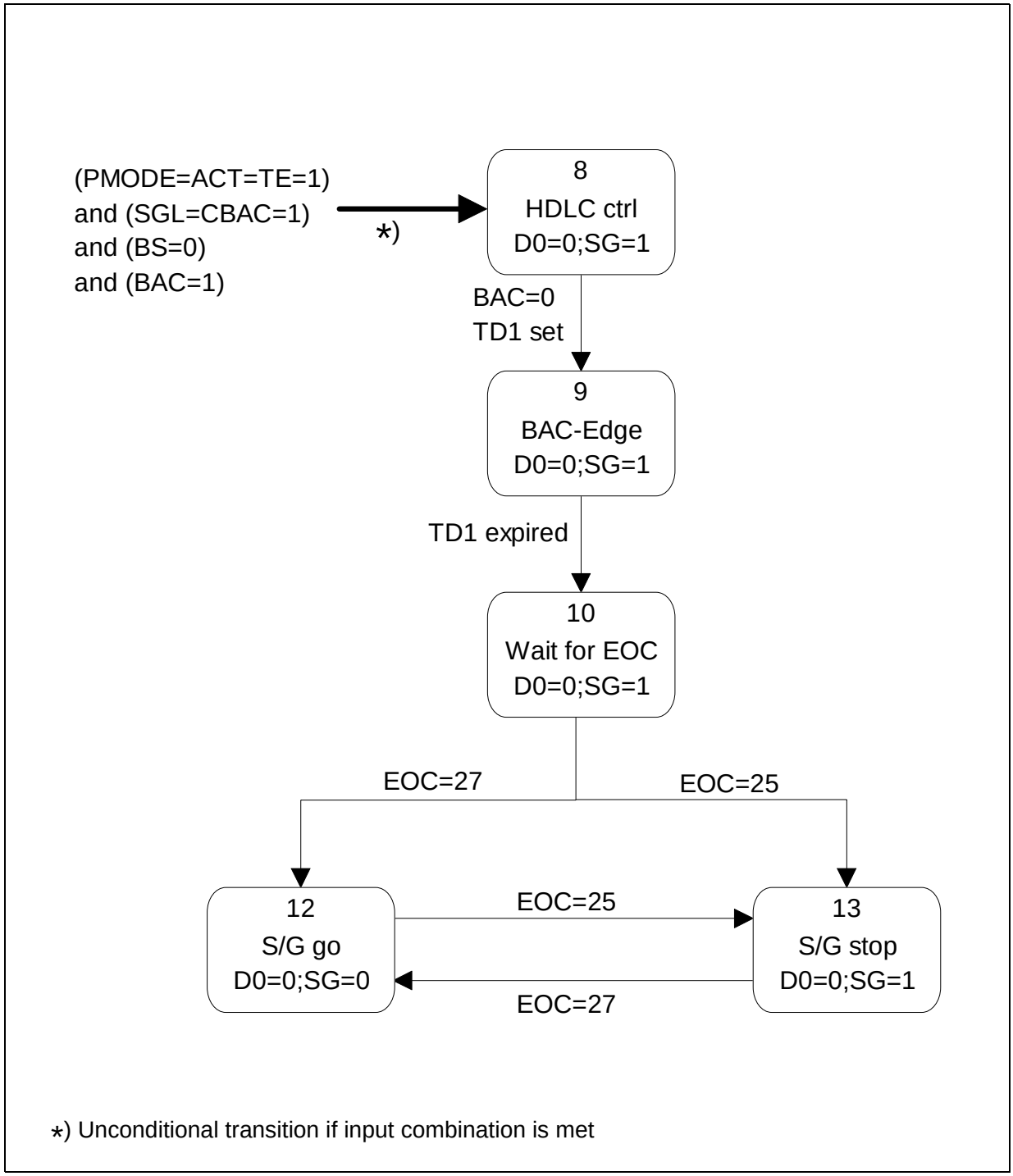


Figure 87 State Machine for S/G Bit Control (part 2)

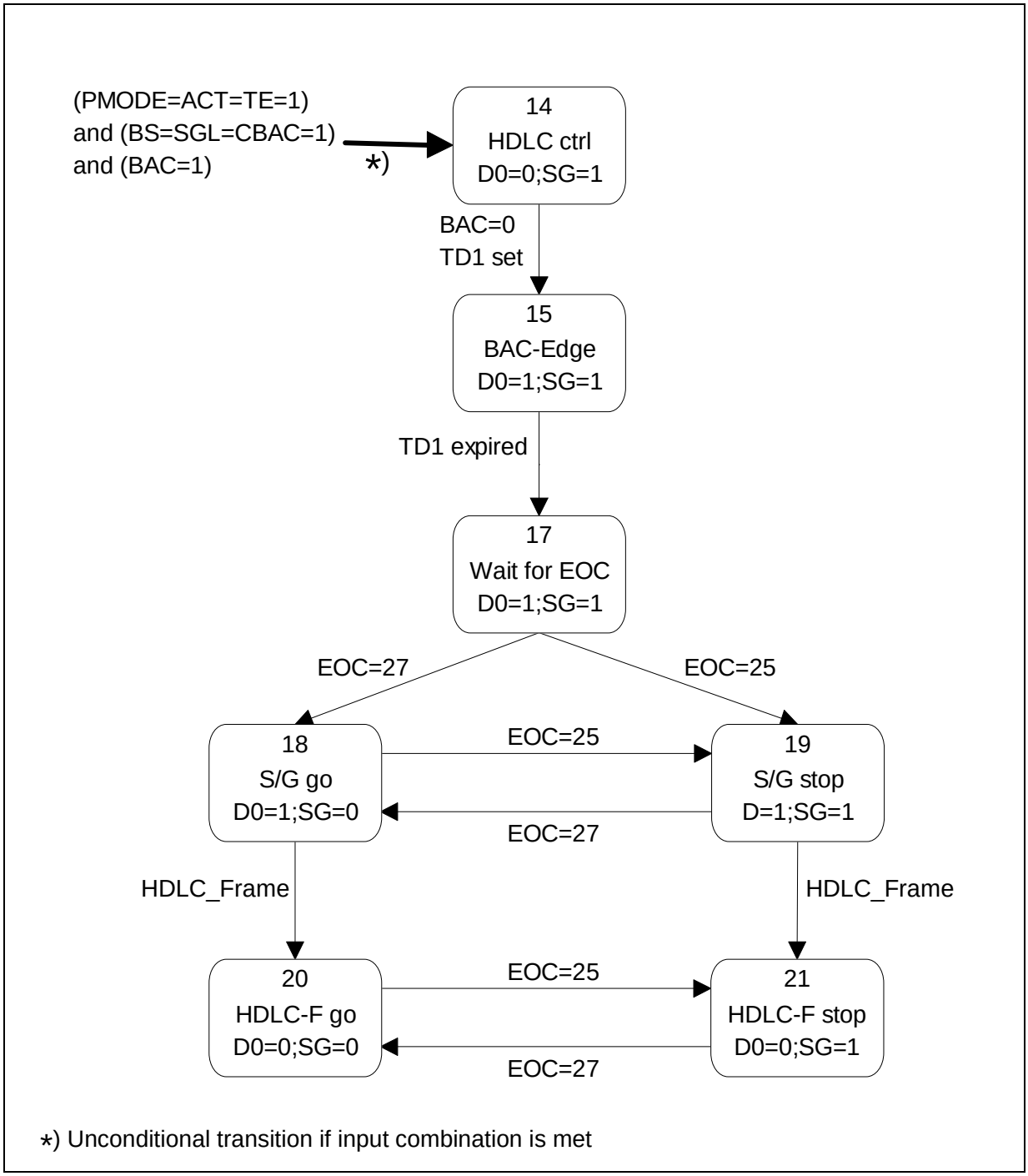


Figure 88 State Machine for S/G Bit Control (Part 3)

Table 34 State Machine Input Signals for S/G Control

No.	Signal name	Description
1	PMODE	Corresponds to the PMODE pin. Set to "1" (only) in the microprocessor mode
2	TE	This input is set to "1" (only) in the TE mode
3	ACT	"1" on this input indicates receive synchronization (e.g. in the Transparent state, see User's Manual 02.95 of the PEB 2091-Version 4.3, page 175).
4	BS	SWST:BS bit.
5	SGL	SWST:SGL bit.
6	CBAC	ADF:CBAC bit.
7	EOC=25	This input indicates that the EOC code 25h (stop) was received from the U-interface.
8	EOC=27	This input indicates that the EOC code 27h (go) was received from the U-interface.
9	T1 set	An internal 500 micro seconds timer is enabled.
10	T1 expired	The 500 micro seconds timer (see 9) has expired.
11	TD1 set	An internal timer TD1 is enabled. The length of this timer depends on the position of the EOC frame in the currently received U data. It varies between 7.5 and 15 ms.
12	TD1 expired	The timer TD1 has expired, (see 11).
13	BAC	BAC bit on DIN. This is bit no. 27 positioned in the third IOM®-2 slot

Table 35 State Machine Output Signals for S/G Control

No.	Signal name	Description
1	SG	Value of the S/G bit on DOUT. The S/G bit is bit no. 27 in the third slot on DOUT.
2	D0	Sets the D channel upstream to "0" if active ("1")

4.11.2 Indication of S/G Bit Status on Pin SG

Note 62: This feature is only available if one of the packages T-QFP-64 or M-QFP-64 is being used. This function is not available in the P-LCC-44 package.

The S/G bit status information will be additionally provided on pin SG (see "Miscellaneous Function Pins", page 46).

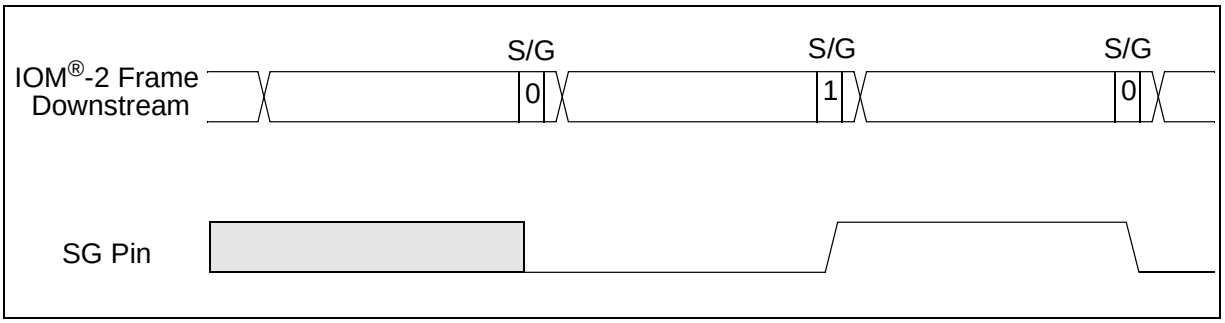


Figure 89 S/G Bit Status on Pin S/G

Note that in state number 6 of the S/G bit control state machine (see Figure 86, page 201) the S/G bit is not defined. In this case the polarity of pin SG may differ from the polarity of the S/G bit on IOM®-2.

For timing properties see "Timing Properties of Pin SG in TE Mode", page 286.

5 Register Description

Note 63: This chapter applies only in µP mode.

The setting of the IEC-Q in µP mode and the transfer of data are programmed with registers. The address map and a register summary are given in Table 36 and in Table 37, respectively.

Table 36 Register Overview

Reg Name	Access	Address (hex)	Reset Value	Comment	Page No.
ISTA	Read	0	00_H	Interrupt Status Register	**210**
MASK	Write	0	FF_H	Interrupt Mask register	**211**
STCR	Write	1	04_H	Status Control Register	**212**
MOR	Read	2	FF_H	Read Monitor data	**222**
MOX	Write	2	FF_H	Write Monitor data	**222**
DRU	Read	3	FF_H	Read D from U	**221**
DWU	Write	3	FF_H	Write D to U	**221**
ADF2	Write	4	18_H	Additional Features Reg. 2	**214**
	Read	5	Reserved for the test mode (must not be used in normal operation)		
	Write	5			
RB1U	Read	6	00_H	Read B1 from U	**221**
WB1U	Write	6	00_H	Write B1 to U	**221**
RB2U	Read	7	00_H	Read B2 from U	**221**
WB2U	Write	7	00_H	Write B2 to U	**221**
RB1I	Read	8	00_H	Read B1 from IOM®-2	**221**
WB1I	Write	8	00_H	Write B1 to IOM®-2	**221**
RB2I	Read	9	00_H	Read B2 from IOM®-2	**221**
WB2I	Write	9	00_H	Write B2 to IOM®-2	**221**
MOSR	Read	A	00_H	Monitor Status Register	**215**
MOCR	Write	A	00_H	Monitor Control Register	**216**
DRI	Read	B	FF_H	Read D from IOM®-2	**221**
DWI	Write	B	FF_H	Write D to IOM®-2	**221**
CIRU	Read	C	03_H	Read C/I-code from U	**217**
CIWU	Write	C	$C3_H$	Write C/I-code to U	**217**
CIRI	Read	D	03_H	Read C/I-code from IOM®-2	**218**
CIWI	Write	D	$C7_H$	Write C/I-code to IOM®-2	**218**
ADF	Write	E	14_H	Additional Features Reg.	**219**
SWST	Write	F	00_H	Switch Status Register	**220**

Table 37 Register Summary

Address	7	6	5	4	3	2	1	0	Name	
0_H	D	CICI	CICU	SF	MDR	B1	B2	MDA	ISTA	R
0_H	D	CICI	CICU	SF	MDR	B1	B2	MDA	MASK	W
1_H	TEST1	TEST2	MS2	MS1	MS0	TM1	TM2	AUTO	STCR	W
2_H									MOR	R
2_H									MOX	W
3_H									DRU	R
3_H									DWU	W
4_H	TE1	MTO	DOD	SFEN	MIN	1	ICEC	1	ADF2	W
6_H									RB1U	R
6_H									WB1U	W
7_H									RB2U	R
7_H									WB2U	W
8_H									RB1I	R
8_H									WB1I	W
9_H									RB2I	R
9_H									WB2I	W
A_H	MDR	MER	MDA	MAB	MAC				MOSR	R
A_H	MRE	MRC	MXE	MXC	1	1	1	1	MOCR	W
B_H									DRI	R
B_H									DWI	W
C_H	0	0	C/I	C/I	C/I	C/I			CIRU	R
C_H	SPU	1	C/I	C/I	C/I	C/I	1	1	CIWU	W
D_H	C/I	C/I	C/I	C/I	C/I	C/I			CIRI	R
D_H	C/I	C/I	C/I	C/I	C/I	C/I	1	1	CIWI	W
E_H	WTC2	WTC1	PCL1	PCL0	1	UVD	BCL	CBAC	ADF	W
F_H	WT	B1	B2	D	CI	MON	BS	SGL	SWST	W

5.1 Interrupt Structure

The cause of an interrupt is determined by reading the Interrupt Status Register (ISTA). In this register, 7 interrupt sources can be directly read. Interrupt bits are cleared by reading the corresponding registers. ISTA:D is cleared after DRI and DRU have been read. ISTA:B1 is cleared after RB1I and RB1U have been read. ISTA:B2 is cleared after RB2I and RB2U have been read etc. ISTA:CICI is cleared after CIRI is read, ISTA:CICU is cleared after CIRU is read. ISTA:SF indicates a superframe marker received from the transceiver core. It is cleared when the ISTA register has been read. Pin $\overline{INT}$ is set to "0" if one bit of ISTA changes from "0" to "1", except for the bit masked in the MASK register. The MASK register allows to prevent an interrupt to influence the $\overline{INT}$ pin. Setting the bits of MASK that correspond to the bits of ISTA to "1" masks the bits, i.e. the bits are still set in ISTA, but they do not contribute to the input of the NOR-function on the interrupt bits which sets the $\overline{INT}$ pin. The interrupt structure is illustrated in Figure 90:

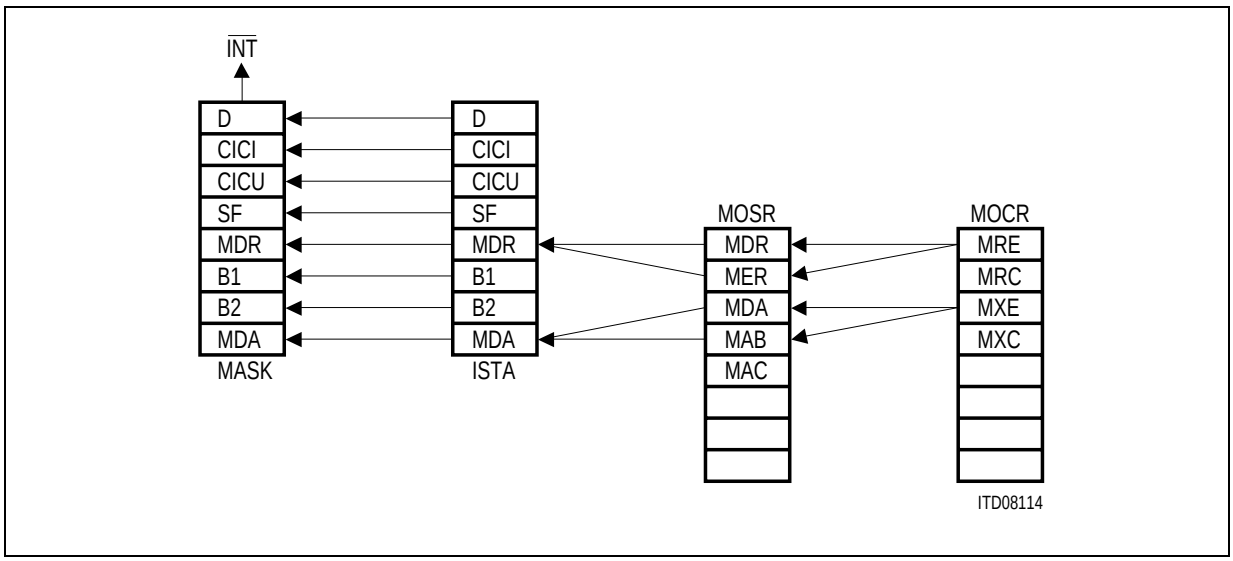


Figure 90 Interrupt Structure

5.1.1 Monitor-Channel Interrupt Logic

The Monitor Data Receive (MDR) and the Monitor End of Reception (MER) interrupt status bits have two enable bits, Monitor Receive Interrupt Enable (MRE) and MR-bit Control (MRC). The Monitor channel Data Acknowledged (MDA) and Monitor channel Data Abort (MAB) interrupt status bits have a common enable bit Monitor Interrupt Enable (MXE).

MRE prevents the occurrence of the MDR status, including when the first byte of a packet is received. When MRE is active ("1") but MRC is inactive, the MDR interrupt status is generated only for the first byte of a receive packet. When both MRE and MRC are active, MDR is generated and all received Monitor bytes - marked by a low edge in

MX bit - are stored. Additionally, an active MRC enables the control of the MR handshake bit according to the Monitor channel protocol.

5.2 Detailed Register Description

5.2.1 ISTA-Register

Read Address 0_H

The Interrupt Status Register (ISTA) generates an interrupt for the selected channel. Interrupt bits are cleared by reading the corresponding register.

Reset value: 00_H

7	6	5	4	3	2	1	0
D	CICI	CICU	SF	MDR	B1	B2	MDA

D D-channel Interrupt

1= Indicates an interrupt that 8 bits D-channel data have been updated

0= Occurs after DRI and DRU have been read

CICI C/I-channel Interrupt IOM®-2

1= Indicates a change in the C/I-channel on IOM®-2

0= Occurs after CIRI is read

CICU C/I-channel Interrupt U

1= Indicates a change in the C/I-channel coming from the transceiver core

0= Occurs after CIRU is read

SF Superframe Marker

1= Indicates a superframe marker received from the transceiver core

0= Occurs when the ISTA-Register has been read

MDR Monitor Data Receive Interrupt

1= Indicates an interrupt after the MOSR:MDR or the MOSR:MER bits have been activated

0= Indicates the inactive interrupt status

B1 B1-channel Interrupt

1= Indicates an interrupt every time B1-channel bytes arrive

0= Occurs after RB1I and RB1U have been read

B2 B2-channel Interrupt

1= Indicates an interrupt every time B2-channel bytes arrive

0= Occurs after RB2I and RB2U have been read

MDA Monitor Data Transmit Interrupt

1= Indicates an interrupt after the MOSR:MDA or the MOSR:MAB bits have been activated

0= Indicates the inactive interrupt status

5.2.2 MASK-Register

Write Address 0_H

The Interrupt Mask Register (MASK) can selectively mask each interrupt source in the ISTA register by setting to "1" the corresponding bit.

Reset value: FF_H

7	6	5	4	3	2	1	0
D	CICI	CICU	SF	MDR	B1	B2	MDA

D D-channel mask

1= Prevents an interrupt ISTA:D to influence the $\overline{INT}$ pin

0= Disables the function described above

CICI CICI-channel mask IOM®-2

1= Prevents an interrupt ISTA:CICI to influence the $\overline{INT}$ pin

0= Disables the function described above

CICU CICU-channel mask U

1= Prevents an interrupt ISTA:CICU to influence the $\overline{INT}$ pin

0= Disables the function described above

SF Superframe marker mask

1= Prevents an interrupt ISTA:SF to influence the $\overline{INT}$ pin

0= Disables the function described above

MDR Monitor data receive mask

1= Prevents an interrupt ISTA:MDR to influence the $\overline{\text{INT}}$ pin

0= Disables the function described above

B1 B1-channel mask

1= Prevents an interrupt ISTA:B1 to influence the $\overline{\text{INT}}$ pin

0= Disables the function described above

B2 B2-channel mask

1= Prevents an interrupt ISTA:B2 to influence the $\overline{\text{INT}}$ pin

0= Disables the function described above

MDA Monitor data transmit mask

1= Prevents an interrupt ISTA:MDA to influence the $\overline{\text{INT}}$ pin

0= Disables the function described above

5.2.3 STCR-Register

Write Address 1_H

The Status Control Register (STCR) selects the operating modes of the IEC-Q as given in Table 2, "Setting Modes of Operation (Stand-Alone and µP Mode)", on page 51.

Note 64: The STCR-register is only reset after a power-on. Please refer also to "Reset Behavior", page 94.

Reset value: 04_H

7	6	5	4	3	2	1	0
BURST	LT	TS2	TS1	TS0	TM1	TM2	AUTO

BURST Selection of burst modes

1= Selects the burst modes (LT, NT-PBX)

0= Selects the non-burst modes (NT, TE, COT-512/1536, LT/NT-RP)

LT Selection of LT modes

1= Selects the LT modes (LT,COT-512/1536, LT-RP)

0= Selects the non LT modes (NT, TE, NT-PBX, NT-RP)

TS2 Mode Selection 2
Selects operation mode according to Table 2, page 51

TS1 Mode Selection 1
Selects operation mode according to Table 2, page 51

TS0 Mode Selection 0
Selects operation mode according to Table 2, page 51

TM1 Test-Mode-Bit 1
This bit determines, in combination with STCR:TM2, the operation modes.
See table below

TM2 Test-Mode-Bit 2
This bit determines, in combination with STCR:TM1, the operation modes.
See table below

Test-Mode	TM1	TM2
Normal Mode	1	0
Send Single-Pulses	1	1
Data-Through	0	1

AUTO Selection between EOC Auto and Transparent mode

1= Sets the Auto mode for EOC channel processing

0= Sets the Transparent mode for EOC channel processing

5.2.4 ADF2-Register

Write Address 4_H

Additional Features Register 2 (ADF2).Write Address 4_H.

Reset value: 18H

7	6	5	4	3	2	1	0
TE1	MTO	DOD	SFEN	MIN	1	ICEC	1

TE1 Terminal Equipment Channel 1

1= Enables the IEC-Q to write Monitor data on DOUT to the MON1 channel instead of the MON0 channel and to write 6-bit C/I indications on DOUT into the C/I-channel 1

0= Enables the normal operations where the IEC-Q addresses only IOM®-2 channel 0

MTO Monitor Procedure Time-out

1= Disables the internal 6ms Monitor time-out

0= Enables the internal 6ms Monitor time-out

DOD Dout Open Drain

1= Selects pin DOUT to be open drain

0= Selects pin DOUT to be tristate

SFEN Superframe Enable

1= Enables the superframe marker function

0= Disables the superframe marker function

MIN Monitor-In-Bit

1= Combined with the SWST:MON = "1" and ADF2:TE1 = "0" bits, enables the controller to access the core of the IEC-Q

0= Combined with the SWST:MON = "1" and ADF2:TE1 = "0" bits, enables the controller to access the IOM®-2 interface directed out of the IEC-Q

ICEC IOM®-2 Clocks Enable Control

1= Inverts meaning of pin ICE.
Clocks are enabled if pin ICE=0. Clocks are disabled if pin ICE=1

0= The status of pin ICE is valid (Reset value)

5.2.5 MOSR-Register

Read Address A_H

The Monitor Status Register (MOSR) indicates the status of the Monitor channel.

Reset value: 00_H

7	6	5	4	3	2	1	0
MDR	MER	MDA	MAB	MAC			

MDR Monitor Channel Data Received Interrupt

1= Generates an interrupt status after the receiving device has stored the contents of the MOX register in the MOR register

0= Inactive interrupt status

MER Monitor Channel End of Reception Interrupt

1= Is generated after two consecutive inactive MX bits (end of message) or as a result of a handshake procedure error

0= Indicates that the transmission is running

MDA Monitor Channel Data Acknowledged

1= Results after a Monitor byte is acknowledged by the receiving device

0= Occurs when the receiver waits for an acknowledge of the Monitor bit

MAB Monitor Channel Data Abort

1= Indicates that during a transmission the receiver aborted the process by sending an inactive ("1") MR bit value in two consecutive frames

0= Indicates that the transmission is running properly and that no abort request has been activated

MAC Monitor Channel Active

1= Indicates a transmission on the Monitor channel

0= Indicates that the transmitter is inactive, i.e. ready for a transmission

5.2.6 MOCR-Register

Write Address A_H

The Monitor Control Register (MOCR) allows to program and control the Monitor channel as described in the section 5.1.1.

Reset value: 00_H

7	6	5	4	3	2	1	0
MRE	MRC	MXE	MXC	1	1	1	1

MRE Monitor Receive Interrupt Enable

1= Enables the Monitor data receive (MDR) interrupt status bit; MRE = 1 enables the Monitor data receive (MDR) and the Monitor end of reception (MER) interrupt status bits

0= Masks the MDR and the MER bits

MRC Monitor Channel Receive Control

1= Enables the control of the MR bit internally by the IEC-Q according to the Monitor channel protocol

0= Enforces a "1" (inactive state) in the Monitor channel receive (MR) bit

MXE Monitor Transmit Interrupt Enable

1= Combined with the MXC bit tied to "1" enable the Monitor channel data acknowledged (MDA) and the Monitor channel data abort (MAB) interrupt status bits

0= Masks the MDA and the MAB bits

MXC Monitor Channel Transmit Control

1= Enables the control of the MX bit internally by the IEC-Q according to the Monitor channel protocol

0= Enforces a "1" (inactive state) in the Monitor channel transmit (MX) bit

5.2.7 CIRU-Register

Read Address C_H

The Read C/I-code from U Register (CIRU) reads the C/I-code from the transceiver core.

Reset value: 03_H

7	6	5	4	3	2	1	0
		C/I	C/I	C/I	C/I		

7., 6. bits Set to "0".

5.-2. bits Contain the C/I-indication coming from the transceiver core.

1., 0. bits Set to "1".

5.2.8 CIWU-Register

Write Address C_H

The Write C/I-code to U Register (CIWU) writes the C/I-code to the transceiver core.

Reset value: $C3_H$

7	6	5	4	3	2	1	0
SPU	1	C/I	C/I	C/I	C/I	1	1

SPU Software Power-Up Bit
Valid only in the NT mode.

1= Data on DIN will be transparently transmitted to the transceiver core (default)

0= Data on DIN will be ignored and binary "0" will be continuously transmitted to the transceiver core if the NT mode is selected (pin LT="0")

6. bits Set to "1"

5.-2. bits Contain the C/I-code going to the transceiver core

1., 0. bits Set to "1"

5.2.9 CIRI-Register

Read Address D_H

The Read C/I-code from IOM®-2 Register (CIRI) reads the C/I-code from the IOM®-2 interface.

Reset value: 03_H

7	6	5	4	3	2	1	0
C/I	C/I	C/I	C/I	C/I	C/I		

7., 6. bits ADF2:TE1 = 1 indicates that the C/I-channel 1 in the TE mode can be accessed and that the C/I-channel on IOM®-2-channel 0 is passed transparently from the transceiver core to the IOM®-2. The two bits contain C/I-code
ADF2:TE1 = 0 sets the normal mode. The two bits are set to "0"

5.-2. bits Contain the C/I-command coming from the IOM®-2

1., 0. bits Set to "1"

5.2.10 CIWI-Register

Write Address D_H

The Write C/I-code to IOM®-2 Register (CIWI) writes the C/I-code to the IOM®-2 interface.

Reset value: $C7_H$

7	6	5	4	3	2	1	0
C/I	C/I	C/I	C/I	C/I	C/I	1	1

7., 6. bits These bits are the MSBs of the 6-bit wide C/I code in IOM®-2 channel 1 if ADF2:TE1 = 1.
If ADF2:TE1 = 0 these two bits have no effect. They should however be set to 1 for future compatibility

5.-2. bits Contain the C/I-code going to the IOM®-2

1., 0. bits Set to "1"

5.2.11 ADF-Register

Write Address E_H

Additional Features Register (ADF).

Reset value: 14_H

7	6	5	4	3	2	1	0
WTC2	WTC1	PCL1	PCL0	1	UVD	BCL	CBAC

WTC2, WTC1 Watchdog Controller
The bit patterns "10" and "01" has to be written in WTC1 and WTC2 by the enabled watchdog timer within 132ms. If it fails to do so, a reset signal of 5ms at pin $\overline{RST}$ is generated

PCL1, PCL0 Prescaler
The clock frequency on MCLK is selected by setting the bits according to the table below:

PCL1	PCL0	Frequency at MCLK (MHz)
0	0	7.68
0	I	3.84
I	0	1.92
I	I	0.96

UVD Undervoltage Detector

1= Enables the undervoltage detector. For details see "Undervoltage Detection", page 92

0= Disables the undervoltage detector

BCL Bit Clock

1= Changes the DCL-output into the bit-clock mode

0= Gives the doubled bit clock on the DCL-output

CBAC Control BAC
Operates in combination with SWST:SGL and SWST:BS bits to control the S/G bit and the BAC bit. For the operational description see "S/G Bit and BAC Bit Operations", page 198

5.2.12 SWST-Register

Write Address F_H

The Switch Status Register (SWST) selects the switching directions of the processor interface (PI).

Reset value: 00_H

7	6	5	4	3	2	1	0
WT	B1	B2	D	CI	MON	BS	SGL

WT Watchdog Timer

1= Enables the watchdog timer (see "Watchdog Timer", page 93)

0= Disables the watchdog timer

B1 B1-channel Processing

1= Enables the microprocessor to access B1-channel data between IOM®-2 and the transceiver core

0= Disables the function described above

B2 B2-channel Processing

1= Enables the microprocessor to access B2-channel data between IOM®-2 and the transceiver core

0= Disables the function described above

D D-channel Processing

1= Enables the microprocessor to access D-channel data between IOM®-2 and transceiver core

0= Disables the function described above

CI C/I-channel Processing

1= Enables the microprocessor to access C/I-commands and indications between IOM®-2 and transceiver core

0= Disables the function described above

MON Monitor-channel Processing

1= Enables the microprocessor to access Monitor-channel messages at IOM®-2 and at the transceiver core

0= Disables the function described above

BS BS Bit
Operates in combination with SWST:SGL and ADF:CBAC bits to control the S/G bit and the BAC bit. For the functional description see "Indication of S/G Bit Status on Pin SG", page 205

SGL Stop/Go
Operates in combination with SWST:BS and ADF:CBAC bits to control the S/G bit and the BAC bit. For the functional description see "Indication of S/G Bit Status on Pin SG", page 205

5.2.13 B-Channel Access Registers

Register	Value after reset (hex)	Function	Address (hex)
WB1U	00	write B1-channel data to transceiver core	6
RB1U	00	read B1-channel data from transceiver core	6
WB1I	00	write B1-channel data to IOM®-2	8
RB1I	00	read B1-channel data from IOM®-2	8
WB2U	00	write B2-channel data to transceiver core	7
RB2U	00	read B2-channel data from transceiver core	7
WB2I	00	write B2-channel data to IOM®-2	9
RB2I	00	read B2-channel data from IOM®-2	9

5.2.14 D-Channel Access Registers

Register	Value after Reset (hex)	Function	Address (hex)
DWU	FF	write D-channel data to transceiver core	3
DRU	FF	read D-channel data from transceiver core	3
DWI	FF	write D-channel data to IOM®-2	B
DRI	FF	read D-channel data from IOM®-2	B

5.2.15 Monitor-Channel Access Registers

Register	Value after reset (hex)	Function	Address (hex)
MOX	FF	Monitor data transmit register	2
MOR	FF	Monitor data receive register	2

6 Programming

This chapter contains a summery of commands and indications used to program the IEC-Q. An overview of the following codes is given

- C/I channel commands and indications
- Predefined Monitor channel messages
- Predefined EOC messages

Furthermore, several examples for programming codes are given. This includes

- programming code for the C/I and the Monitor channel in the microprocessor mode (sections 6.4 and 6.5)
- Programming code for the power controller interface, which applies only in stand-alone mode (section 6.6)
- Programming code for test loop-backs (section 6.7)
- Programming code for activation and deactivation control for all important configurations (section 6.8)

Note 65: Programming the C/I channel and the Monitor channel can be performed using either the IOM®-2 interface, which is available in every mode, or the µP interface if the µP mode is used. A combination of both is also possible in the µP mode.
For information about the IOM®-2 interface characteristics, see "IOM®-2 Interface", page 70. See also "Microprocessor Access to IOM®-2 Channels", page 97, for the µP mode.

6.1 C/I Channel Codes

Both commands and indications depend on the IEC-Q mode and the data direction. Table 38 gives all defined C/I-codes.

Table 38 Command / Indicate Codes

Code	NT Mode		LT Mode	
	IN	OUT	IN	OUT
0000	TIM	DR	DR	–
0001	RES	–	RES	DEAC
0010	–	FJ[1)]	–	FJ
0011	DU[2)]	–	LTD	HI
0100	EI1	EI1	RES1	RSY
0101	SSP	–	SSP	EI2
0110	DT	INT	DT	INT
0111	–	PU	UAR	UAI
1000	AR	AR	AR	AR
1001	–	–	ARX	ARM
1010	ARL	ARL	ARL	–
1011	–	–	–	EI3
1100	AI	AI	–	AI
1101	–	–	AR0	LSL
1110	–	AIL	–	–
1111	DI	DC	DC	DI

1) in NT-PBX mode only

2) DU is only used in the repeater

Table 39 shows the abbreviations used for C/I-commands and indications.

Table 39 C/I-Abbreviation

Code	Description
AI	Activation Indication
AR	Activation Request
AR0	Activation Request with act bit = 0
ARL	Activation Request Local Loop
ARM	Activation Request Maintenance bits
ARX	Activation Request with timer T1 [15 sec.] ignored
DC	Deactivation Confirmation
DR	Deactivation Request
DEAC	Deactivation Accepted
DI	Deactivation Indication
DT	Data-Through Test Mode
DU	Deactivation Request Upstream
EI1	Error Indication1 (error on U)
EI2	Error Indication2 (error on S/T)
EI3	Error Indication3 (time-out T1 [15sec] error on U)
FJ	Frame Jump
HI	High Impedance (set by pin "PS1")
INT	Interrupt (set by pin "INT")
LTD	LT Disable (control of pin "DISS")
LSL	Loss of Signal Level on U
UAI	U-Activation Indication
UAR	U-Activation Request
RES	Reset
RES1	Reset Receiver
RSY	Loss of Synchronization
PU	Power-Up
SSP	Send-Single-Pulses Test Mode
TIM	Timing Request

6.2 Monitor Channel Codes

4 categories of Monitor messages are supported by the IEC-Q:

– MON-0 (EOC Programming)
– MON-1 (Maintenance Bits, S/Q-Channel)
– MON-2 (Overhead Bits)
– MON-8 (Local Functions)

6.2.1 MON-0 Codes

Table 40 Format of MON-0-Commands

1. Byte		2. Byte	
0 0 0 0	A A A | 1	E E E E	E E E E
MON-0	Addr. | d/m	EOC Code	

Addr: Address
– 0 = NT
– 1 … 6 = Repeater
– 7 = Broadcast

d/m: Data/Message
– 0 = Data
– 1 = Message

E: EOC Code
– 00 … FF_H = coded EOC command/indication

Table 41 Predefined MON-0 Commands and Indications

MON-0-Functions					
Code Hex.	NT		LT		Function
	D	U	D	U	
00			H	H	Hold
50	LBBD		LBBD		Close complete loop
51	LB1		LB1		Close loop B1
52	LB2		LB2		Close loop B2
53	RCC		RCC		Request corrupt CRC
54	NCC		NCC		Notify of corrupt CRC
AA				UTC	Unable to comply
FF	RTN		RTN		Return to normal
XX				ACK	Acknowledge

6.2.2 MON-1 Codes

Table 42 Format of MON-1 Messages

1. Byte		2. Byte	
0 0 0 1	0 0 0 0	S S S S	M M M M
MON-1		S/Q-Code	M-bits

S/Q: S/Q-channel – 00 … FF_H = coded S/Q-command indication
M: Maintenance bits – 00 … FF_H = set/reset maintenance bits

The following indications and maintenance bits are defined in MON-1-messages.

Table 43 MON-1 S/Q-Channel Commands and Indications

MON-1-Functions					
S/Q (Bin)	**NT**		**LT-RP**		**Function**
	D	**U**	**D**	**U**	**S/Q-Channel**
0 0 0 1		ST[1)]			Self-test request
0 0 1 0	STP[1)]				Self-test pass.
0 1 0 0	FEBE			FEBE	Far-end block error.
1 0 0 0	NEBE			NEBE	Near-end block error.
1 1 0 0	FNBE			FNBE	Far and near-end block error.
1 1 1 1		NORM [1)]			

Table 44 MON-1 M-Bit Commands

MON-1-Functions					
M-Bit (Hex)	**NT**		**LT**		**Function**
	D	**U**	**D**	**U**	**M-Bit-Channel**
1 x x 0		NTM[1)]			NT test mode
1 1 1 1		NORM[1)]			Normal

1) These messages are used in NT , NT-PBX, and TE modes only

6.2.3 MON-2 Codes

Table 45 Format of MON-2-Messages

1. Byte		2. Byte
0 0 1 0	D11 D10 D9 D8	D7 D6 D5 D4 D3 D2 D1 D0
MON-2	Overhead Bits	Overhead Bits

D0 … 11: Overhead bits.

6.2.4 MON-8 Codes

Table 46 Format of MON-8-Messages

1. Byte		2. Byte
1 0 0 0	r | 0 0 0	D7 D6 D5 D4 D3 D2 D1 D0
MON-8	Register | Addr.	Local Command (Message/Data)

r: Register address
- 0 = local function register
- 1 = internal register

D0…7 Local command
- 00 … FF_H = local function code
- 00 … FF_H = internal register address

The following local commands are defined.

Table 47 MON-8-Local Function Commands

MON-8-Functions						
r	Code (Bin)	NT		LT		Function
		D	U	D	U	
0	1000 1110		TLL[1)]	TLL[1)]		A change in at least one of the M4 Bits will be passed via MON-2 only after valid triple last look
0	1000 1101		CRC[2)]	CRC[2)]		A change in at least one of the M4 Bits will be passed via MON-2 only if the CRC is valid for the last two superframes, not including the current one.
0	1000 1111		TLL, CRC	TLL, CRC		A change in at least one of the M4 Bits will be passed via MON-2 only after valid triple last look, and if the CRC is valid for the last two superframes, not including the current one
0	1000 1100		On Change	On Change		Every change in at least one of the M4 Bits will be passed via MON-2
0	1000 1010		TLL[1)]	TLL[1)]		A change in at least one of the Additional Overhead Bits will be passed via MON-2 only after valid triple last look.
0	1000 1001		CRC[2)]	CRC[2)]		A change in at least one of the Additional Overhead Bits will be passed via MON-2 only if the CRC is valid for the last two superframes, not including the current one.
0	1000 1011		TLL, CRC	TLL, CRC		A change in at least one of the Additional Overhead Bits will be passed via MON-2 only after valid triple last look, and if the CRC is valid for the last two superframes, not including the current one
0	1000 1000		On Change	On Change		Every change in at least one of the Additional Overhead Bits will be passed via MON-2
0	1011 1110		PACE	PACE		Partial Activation Control External
0	1011 1111		PACA	PACA		Partial Activation Control Automatic
0	1111 0000		CCRC[3)]	CCRC		Corrupt CRC
0	1111 0100		LB1[3)]			Loop B1

Table 47 MON-8-Local Function Commands

		MON-8-Functions				
0	1111 0010		LB2[3]			Loop B2
0	1111 0001		LBBD[4]			Loop B1 + B2 + D
0	1111 1111		NORM[3]	NORM		Return to Normal
0	1111 1011		RBEN	RBEN		Read Near-end Block Error Counter
0	1111 1010		RBEF	RBEF		Read Far-end Block Error Counter
0	r r r r r r r	ABEC			ABEC	Answer Block Error Counter
0	1111 1000			RPFC		Read Power Feed Current
0	vvvv vvvv				APFC	Answer Power Feed Current
0	011d ddaa		WCI[5]	WCI[5]		Write Controller Interface
0	010* * * *		RCI[5]	RCI[5]		Read Controller Interface
0	ddd* ****	ACI[5]			ACI[5]	Answer Controller Interface
0	0000 0000		RID	RID		Read Identification
0	**** ****	AID			AID	Answer Identification. The IEC-Q Version 5.3 will reply with the ID 8003_H
0	1111 1001		SFB	SFB		Set FEBE-Bit to (0)
1	cccc cccc		RCOEF	RCOEF		Read Coefficient
1 1	bbbb bbbb bbbb bbbb	DCOEF			DCOEF	Data Coefficients, 2 bytes. Data bits D0 … D 7, 1. byte Data bits D8 … D15, 2. byte[6]

1) Default setting after reset in non repeater modes

2) default setting after reset in repeater modes

3) Used in EOC Transparent mode only

4) This code is used in EOC Transparent mode or in EOC Auto mode after the receipt of "LBBD" in the EOC-channel

5) See power controller interface description

6) The first byte of the corresponding MON-8 message will be "10001100"

Definitions:

a … a	power controller address to pins PCA
b … b	internal coefficient value
c … c	internal coefficient address
d … d	power controller data to/from pins PCD
r … r	result from block error counter
v … v	power feed current value

6.3 Predefined EOC Codes

The EOC contains an address field, a data/message indicator and an eight-bit information field, see "U -Frame Structure", page 67 for details.

The data/message indicator needs to be set to (1) to indicate that the information field contains a message. If set to (0), numerical data is transferred to the NT. Currently no numerical data transfer to or from the NT is required.

From the 256 codes possible in the information field 64 are reserved for non-standard applications, 64 are reserved for internal network use and eight are defined by ANSI for diagnostic and loop-back functions. All remaining 120 free codes are available for future standardization.

Table 48 Supported EOC-Commands

EOC					
Address Field	**Data/ Message Indicator**	**Information**	**O (rigin) D (estination)**		**Message**
a1a2a3	**d/m**	**i1 i2 i3 i4 i5 i6 i7 i8**	**LT**	**NT**	
000	x				NT
111	x				Broadcast
0 01 1 10	x				Repeater stations No. 1 – No. 6
	0				Data
	1				Message
	1	0 1 0 1 0 0 0 0	O	D	LBBD
	1	0 1 0 1 0 0 0 1	O	D	LB1
	1	0 1 0 1 0 0 1 0	O	D	LB2
	1	0 1 0 1 0 0 1 1	O	D	RCC
	1	0 1 0 1 0 1 0 0	O	D	NCC
	1	1 1 1 1 1 1 1 1	O	D	RTN
	1	0 0 0 0 0 0 0 0	D/O	O/D	H
	1	1 0 1 0 1 0 1 0	D	O	ACK

6.4 Example for C/I Channel Programming

Note 66: This example applies only in µP-NT mode.

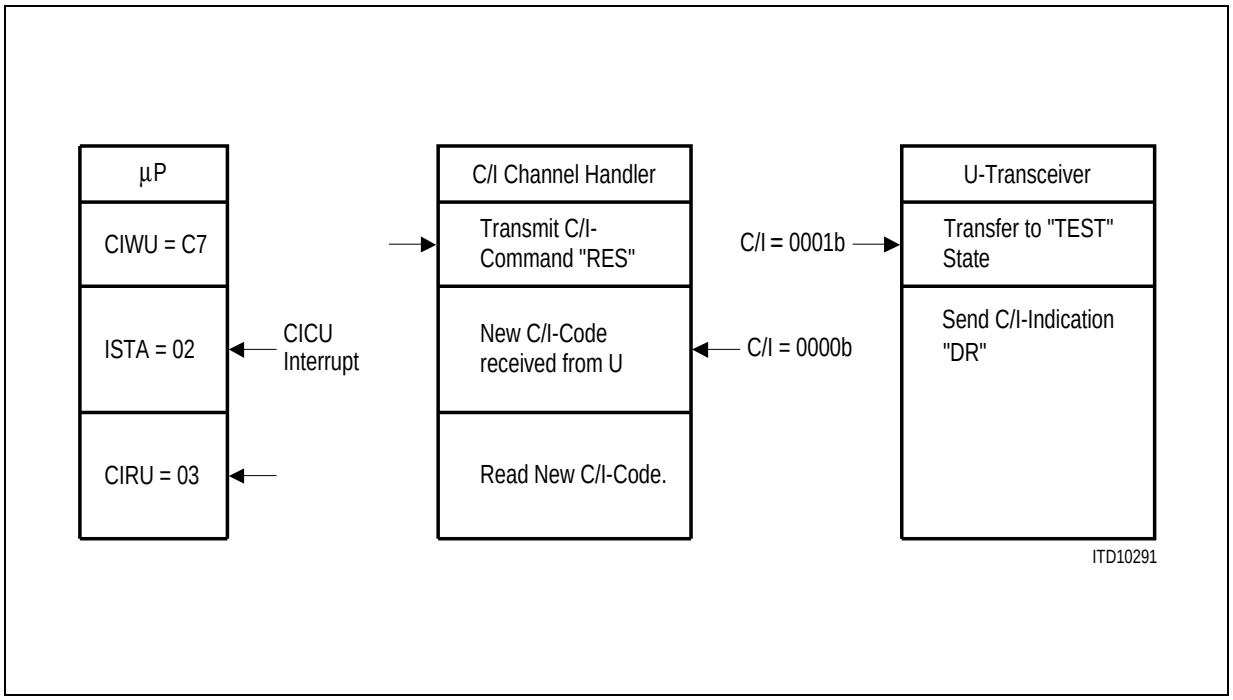


Figure 91 Example: C/I-Channel Use (all data values hexadecimal)

6.5 Example for Monitor Channel Programming

Note 67: This chapter applies only in µP mode.

The example on page 234 illustrates the read-out of the transceiver's identification number (ID). It consists of the transmission of a two-byte message from the control unit to the transceiver in IOM®-2 channel 0. The transceiver acknowledges the receipt by returning a two-byte long message in the Monitor channel. The procedure is absolutely identical for Monitor channel 1.

The µP starts the transfer procedure after having confirmed that the Monitor channel is inactive. The first byte of Monitor data is loaded into the transmit register MOX. Via the Monitor Control Register MOCR Monitor interrupts are enabled and control of the MX-bit is handed over to the IEC-Q. Then transmission of the first byte begins. The transceiver core reacts to a low level of the MX-bit by reading and acknowledging the Monitor channel byte automatically. On detection of the confirmation, the IEC-Q issues a Monitor interrupt to inform the µP that the next byte may be sent. Loading the second byte into the transmit register results in an immediate transmission (timing is controlled by the IEC-Q). The transceiver core receives the second byte in the same manner as before. When transmission is completed, the transceiver core sends "End of Message" (MX-bit high).

It is assumed that a Monitor command was sent that needs to be answered by the transceiver core (e.g. read-out of a register). Therefore, the transceiver core commences to issue a two-byte confirmation after an End-of-Message indication from the IEC-Q has been detected. The IEC-Q notifies the µP via interrupt when new Monitor data has been received. The processor may then read and acknowledge the byte at a convenient instant. When confirmation has been completed, the transceiver core sends "EOM". This generates a corresponding interrupt in the IEC-Q. By setting the MR-bit to high, the Monitor channel is inactive, the transmission is finished.

Example: Monitor Channel Transmission and Reception

Basic Configuration, IOM®-2 Clocks must be active

```
w   STCR  =  0x15      // TE Mode, EOC Auto Mode
w   SWST  =  0x0C      // Access to C/I and Monitor channel
w   ADF2  =  0x48      // Monitor access to transceiver core
```

Transmission

```
r   MOSR  =  0x00      // Transmission inactive (MAC = 0)
w   MOX   =  0x80      // Mon-8 Command
w   MOCR  =  0x30      // Transmit Command
r   ISTA  =  0x11      // Monitor MDA Interrupt
r   MOSR  =  0x28      // Ackn. Indication
w   MOX   =  0x00      // Access to Register 0
r   ISTA  =  0x11      // Monitor MDA Interrupt
r   MOSR  =  0x28      // Ackn. Indication
```

Reception

```
w   MOCR  =  0x80      // Enable Receive of Monitor Message
r   ISTA  =  0x08      // Monitor MDR Interrupt
r   MOSR  =  0x80      // Data Received
r   MOR   =  0x80      // Value read Monitor 8 Command Ind.
w   MOCR  =  0xC0      // Acknowledge Reading
r   ISTA  =  0x08      // Monitor MDR Interrupt
r   MOSR  =  0x80      // Data Received
r   MOR   =  0x03      // Data from Register 0 (Identification)
r   ISTA  =  0x08      // Monitor MDR Interrupt
r   MOSR  =  0x40      // EOM received
w   MOCR  =  0x80      // Enable Interrupts.
```

6.6 Example for Programming Power Controller Interface

Note 68: This chapter applies only in stand-alone mode.

Assumption: The address lines are not connected, the data lines are clamped to the values given in the application.

1. Write to controller interface:

IOM®-2	IEC-Q	
a) MON-8 WCI (80 7C) ——>	Pin PCA0 = (0)	; Write data 7_H to address
	Pin PCA1 = (0)	; 0_H
	Pin PCD0 … 2 = (1)	; Data not latched
b) MON-8 WCI (80 62) ——>	Pin PCA0 = (0)	; Write data 0_H to address
	Pin PCA1 = (1); 1_H	
	Pin PCD0 … 2 = (0)	; Data not latched

2. Read from controller interface:

IOM®-2	IEC-Q	
a)	Pin PCD0 = (0)	; Values stable on data port
	Pin PCD1 = (0)	
	Pin PCD2 = (0)	
MON-8 RCI (80 40) ——>	Pin PCA0 = (0)	; Read from address 0_H
	Pin PCA1 = (0)	; Address is latched
MON-8 ACI (80 00) <——		; PCD0 … 2 = (0)
b)	Pin PCD0 = (0)	; Values stable on data port
	Pin PCD1 = (0)	
	Pin PCD2 = (0)	
MON-8 RCI (80 42) ——>	Pin PCA0 = (1)	; Read from address 1_H
	Pin PCA1 = (0)	; Address is latched
MON-8 ACI (80 00) <——		; PCD0 … 2 = (0)
c)	Pin PCD0 = (1)	; Values stable on data port
	Pin PCD1 = (0)	
	Pin PCD2 = (1)	
MON-8 RCI (80 41) ——>	Pin PCA0 = (0)	; Read from address 2_H
	Pin PCA1 = (1)	; Address is latched
MON-8 ACI (80 A0) <——		; PCD0 … 2 = (101)

3. Interrupt

IOM®-2	IEC-Q	
C/I AI (1100) <——		; Initial C/I-code
	Pin INT (0) <-> (1)	; Level change on INT pin
C/I INT (0110) <——		; C/I-code INT issued for
C/I AI (1100) <——		; 4 IOM®-2-frames

6.7 Examples for Activating Test Loop-Backs

6.7.1 Examples for Analog Loop-Back Control

The examples below demonstrate the use of loop-backs #1 and #3.

Loop-back #1 (LT side)

	NT		LT			
<———	C/I DC	(1111_B)	C/I DI	(1111_B)	———>	
			C/I ARL	(1010_B)	**<–––––**	; Close loop-back #1
<———	C/I AR	(1000_B)	C/I AR	(1000_B)	———>	; Activation proceeds in NT
			C/I ARM	(1001_B)	———>	; and LT
			C/I UAI	(0111_B)	———>	; Activation complete, ; #1 closed
			C/I RES	(0001_B)	**<–––––**	; Open loop-back #1, ; reset the IEC-Q

Loop-back #3 (NT side)

For correct operation of this example it is assumed that the IEC-Q is not in the power-down mode, i.e. FSC and DCL are present.

	NT		LT			
–––––>	C/I RES	(0001_B)	C/I DI	(1111_B)	———>	; NT in "Test" state
<———	C/I DR	(0000_B)				
–––––>	C/I ARL	(1010_B)				; Close loop-back #3
<———	C/I DC	(1111_B)				
<———	C/I AR	(1000_B)				; NT act. complete, #3 closed
–––––>	C/I RES	(0001_B)				; Open #3 and reset NT

6.7.2 Examples for Complete Loop-Back #2 Control

The typical procedure for closing and opening a complete loop-back is demonstrated in the examples below.

Complete Loop-Back in EOC Auto Mode

	NT		LT			
			C/I AR	(1000_B)	<———	; U-interface is activated
<———	C/I AR	(1000_B)	C/I UAI	(0111_B)	———>	; without terminal confirmation
(———>	C/I AI	(1100_B)				; or with
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; terminal confirmation)
			MON-0 LBBD	**(50_H)**	**<–––––**	; Close complete loop (EOC)
<———	C/I AIL	(1110_B)				; Request for downstream
<———	MON-0 LBBD	(50_H)				; device to close complete loop-back
			MON-0 LBBD	(50_H)	———>	; Receive acknowledgment
–––––>	**MON-8 LBBD**	**($F1_H$)**				; If downstream device can't close, loop is closed in IEC
			MON-0 RTN	**(FF_H)**	**<–––––**	; Open all loop-backs
<———	MON-0 RTN	(FF_H)				; All loop-backs opened
			MON-0 RTN	(FF_H)	———>	; Receive acknowledgment

In the above example the LT is operated in EOC Auto mode.

Complete Loop-Back in EOC Transparent Mode

	NT		LT			
———>	C/I AI	(1100_B)	C/I AR	(1000_B)	<———	; U-interface is activated
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	
			MON-0 LBBD	**(50_H)**	<———	; Close complete loop (EOC)
<———	MON-0 LBBD	(50_H)				; Request passes IEC-Q ; transparent
–––––>	**MON-0 LBBD**	**(50_H)**	MON-0 LBBD	(50_H)	———>	; Transmit acknowledgment
–––––>	**MON-8 LBBD**	**($F1_H$)**				; Close complete loop in IEC
			MON-0 RTN	**(FF_H)**	<———	; Request to open all loops
–––––>	**MON-0 RTN**	**(FF_H)**	MON-0 RTN	(FF_H)	———>	; Receive acknowledgment
–––––>	**MON-8 NORM**	**(FF_H)**				; Open all loop-backs

In the above example the LT is operated in EOC Auto mode.

6.7.3 Examples for Single Channel Loop-Back #2 Control

The typical procedure for closing and opening a single channel loop-back is demonstrated in the examples below.

Single-Channel Loop-Back in EOC Auto Mode

	NT		LT			
———>	C/I AI	(1100_B)	C/I AR	(1000_B)	<———	; U-interface is activated
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	
			MON-0 LB1	**(51_H)**	<———	; Close B1 loop (EOC)
<———	MON-0 LB1	(51_H)				; Loop B1 closed
			MON-0 LB1	(51_H)	———>	; Receive acknowledgment
			MON-0 LB2	**(52_H)**	<———	; Close B2 loop-back (EOC)
<———	MON-0 LB2	(52_H)				; Loop-back B1 and B2 closed
			MON-0 LB2	(52_H)	———>	; Receive acknowledgment
			MON-0 RTN	**(FF_H)**	<———	; Open all loop-backs
<———	MON-0 RTN	(FF_H)				; All loop-backs opened
			MON-0 RTN	(FF_H)	———>	; Receive acknowledgment

In the above example the LT is operated in EOC Auto mode.

Single-Channel Loop-Back in EOC Transparent Mode

	NT		LT			
———>	C/I AI	(1100_B)	C/I AR	(1000_B)	<———	; U-interface is activated
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	
			MON-0 LBBD	**(51_H)**	<———	; Close B1 loop (EOC)
<———	MON-0 LB1	(51_H)				; Request passes IEC ; transparent
–––––>	**MON-0 LB1**	**(51_H)**	MON-0 LBBD	(51_H)	———>	; Transmit acknowledgment
–––––>	**MON-8 LB1**	**($F4_H$)**				; Close B1 loop in IEC
			MON-0 LBBD	**(52_H)**	<———	; Close B2 loop (EOC)
<———	MON-0 LB2	(52_H)				; Request passes IEC ; transparent
–––––>	**MON-0 LB2**	**(52_H)**	MON-0 LB2	(52_H)	———>	; Transmit acknowledgment
–––––>	**MON-8 LB2**	**($F2_H$)**				; Close B2 loop in IEC ; B1 and B2 closed
			MON-0 RTN	**(FF_H)**	<———	; Request to open all loops
–––––>	**MON-0 RTN**	**(FF_H)**	MON-0 RTN	(FF_H)	———>	; Receive acknowledgment
–––––>	**MON-8 NORM**	**(FF_H)**				; Open all loop-backs

In the above example the LT is operated in EOC Auto mode.

6.8 Examples for Activation and Deactivation Control Codes

6.8.1 Complete Activation Initiated by LT

Activation initiated by AR

	NT		**LT**			
<———	C/I DC	(1111_B)	CI/DC	(1111_B)	<———	; Initial state is "Deactivated"
———>	C/I DI	(1111_B)	C/IDI	(1111_B)	———>	;
<———	C/I PU	(0111_B)	**C/I AR**	**(1000_B)**	**<–––––**	; Start activation
<———	C/I DC	(1111_B)	C/I AR	(1000_B)	———>	; Activation proceeds
			C/I ARM	(1001_B)	———>	; :
<———	C/I AR	(1000_B)	C/I UAI	(0111_B)	———>	; :
–––––>	C/I AI	(1100_B)				; Confirm that terminal is ; active
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Activation complete

Activation initiated by ARX

	NT		**LT**			
<———	C/I DC	(1111_B)	CI/DC	(1111_B)	<———	; Initial state is "Deactivated"
———>	C/I DI	(1111_B)	C/IDI	(1111_B)	———>	;
<———	C/I PU	(0111_B)	**C/I ARX**	**(1001_B)**	**<–––––**	; Start activation
<———	C/I DC	(1111_B)	C/I AR	(1000_B)	———>	; Activation proceeds
			C/I ARM	(1001_B)	———>	; :
[			C/I EI3	(1011_B)	———>	; :only if T1 expires **]**
<———	C/I AR	(1000_B)	C/I UAI	(0111_B)	———>	; :
–––––>	C/I AI	(1100_B)				; Confirm that terminal is ; active
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Activation complete

6.8.2 Complete Activation Initiated by TE

When initiating an activation from the terminal side, the LT must be in the "DEACTIVATED" state. For a TE initiated activation to be successful the downstream LT C/I-code must be DC. This is not the case if the "DEACTIVATED" state has been entered from the "TEST" state (the last code is DR in this case).

	NT		**LT**			
<———	C/I DC	(1111_B)	C/I DC	(1111_B)	<———	; Initial state is "Deactivated"
———>	C/I DI	(1111_B)	C/I DI	(1111_B)	———>	
–––––>	**C/I TIM**	**(0000_B)**				; Start IOM®-2-clocks
<———	C/I PU	(0111_B)				; IEC-Q is in power-up
–––––>	**C/I AR**	**(1000_B)**				
———>	TIM release					; Start activation
<———	C/I DC	(1111_B)	C/I AR	(1000_B)	———>	; Activation proceeds
			C/I ARM	(1001_B)	———>	; :
<———	C/I AR	(1000_B)	C/I UAI	(0111_B)	———>	; :
———>	C/I AI	(1100_B)				; Confirm that terminal is active
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Activation complete

6.8.3 Activation with ACT-Bit Status Ignored by Exchange Side

The LT ignores the ACT-bit transmitted upstream from the NT if the LT activation has been initiated with AR0 instead of AR. Because the activation with AR0 is performed with the UOA-bit set to "0", initially only a partial activation is started. By setting UOA = 1 via a MON2 message the S-interface is activated as well.

	NT		LT			
<———	C/I DC	(1111_B)	C/I DC	(1111_B)	<———	; Initial state is "Deactivated"
———>	C/I DI	(1111_B)	C/I DI	(1111_B)	———>	;
			C/I AR0	**(1101_B)**	<———	; Start activation
<———	C/I PU	(0111_B)	C/I AR	(1000_B)	———>	;
<———	C/I DC	(1111_B)	C/I ARM	(1001_B)	———>	;
			C/I UAI	(0111_B)	———>	;
			MON8 PACE	(80 BE_H)	<———	; Enable control of UOA-bit
			MON2 UOA	(2F FF_H)	<———	; and set UOA = 1
<———	C/I AR	(1000_B)				
———>	C/I AI	(1100_B)				: Confirm that terminal is ; active
<———	C/I AR	(1000_B)	C/I UAI	(1100_B)	———>	; ACT-bit status ignored
			C/I AR	(1000_B)	<———	; Enable ACT-bit evaluation
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Activation complete
			C/I AR0	(1101_B)	<———	: Disable ACT-bit evaluation
<———	C/I AR	(1000_B)	C/I UAI	(0111_B)	———>	: ACT-bit status ignored

6.8.4 Complete Deactivation

Deactivating the U-interface can be initiated only by the exchange. A deactivation can be started when the device is in the states "LINE ACTIVE", "PEND. TRANSPARENT" , "TRANSPARENT" or "S/T DEACTIVATED"

	NT		LT			
			C/I DR	**(0000_B)**	**<–––––**	; Start deactivation
<———	C/I DR	(0000_B)	C/I DEAC	(0001_B)	———>	; Deactivation proceeds
			C/I DI	(1111_B)	———>	; Deactivation complete on ; LT
———>	C/I DI	(1111_B)				; Power down NT
<———	C/I DC	(1111_B)				; Deactivation complete on ; NT

6.8.5 Partial Activation (U Only)

Activating the U-interface only partially is a requirement specified by the CNET. The S-interface remains deactivated.

When activating partially from the LT side, the exchange has two options:

First, in case the C/I-command DC is not issued after the partial activation is complete, the exchange has to issue AR before a terminal initiated complete activation request is accepted (see 6.8.7, case 1). This allows the exchange to retain full control, even in case of terminal initiated activation requests.

Secondly the exchange can issue DC after UAI has been received. This allows the terminal to activate the S-interface independently of the exchange (see 6.8.7, case 2). In this case the exchange has no control of the S-interface activation procedure.

	NT		**LT**			
<———	C/I DC	(1111_B)	C/I DC	(1111_B)	<———	; Initial state is "Deactivated"
———>	C/I DI	(1111_B)	C/I DI	(1111_B)	———>	
			C/I UAR	**(0111_B)**	**<–––––**	; Start partial activation
<———	C/I PU	(0111_B)	C/I AR	(1000_B)	———>	; Activation proceeds
<———	C/I DC	(1111_B)	C/I ARM	(1001_B)	———>	; :
			C/I UAI	(0111_B)	———>	; Partial activation complete
			[C/I DC	(1111_B)]	<———	; Exchange retains no control of S-interface activation

6.8.6 Complete Activation Initiated by LT with U Active

When U is already active, the S-interface can be activated either by the exchange or the terminal. The first case is described here, the second in the next section.

	NT		**LT**			
<———	C/I DC	(1111_B)	C/I UAR [DC]		<———	; U only is activated
———>	C/I DI	(1111_B)	C/I UAI	(0111_B)	———>	; [exchange retains no control]
			C/I AR	**(1000_B)**	**<––––**	; Start complete activation
<———	C/I AR	(1000_B)				
———>	C/I AR	(1100_B)				
			C/I AR	(1000_B)	———>	; Activation proceeds
———>	C/I AI	(1100_B)				; Confirm that terminal is active
			C/I UAI	(0111_B)	———>	
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Activation complete

6.8.7 Complete Activation Initiated by TE with U Active

When the terminal requests to activate the S-interface (U-interface already active) two cases can occur:

In the first case the exchange has retained control over the S-interface activation. Then S-activation can proceed only after the explicit permission by the exchange with AR. This situation is discussed in this section under "case 1". In the second case the exchange is not requested to send AR in order to continue activation. This situation is described in "case 2" of this section.

The terminal recognizes no difference between the two types, the procedure on NT side consequently is identical in both cases.

Case 1 (controlled by exchange)

	NT		LT			
<———	C/I DC	(1111_B)	C/I UAR	(0111_B)	<———	; U only is activated
———>	C/I DI	(1111_B)	C/I UAI	(0111_B)	———>	
–––––>	**C/I AR**	**(1000_B)**				; Terminal requests activation
			C/I AR	(1000_B)	———>	; Exchange is notified of request
			C/I AR	(1000_B)	**<–––––**	; Exchange permits S-activation
<———	C/I AR	(1000_B)				
–––––>	C/I AI	(1100_B)				; Confirm that terminal is active
			C/I UAI	(0111_B)	———>	
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Activation complete

Case 2 (no control by exchange)

	NT		LT			
<———	C/I DC	(1111_B)	C/I DC		<———	; U only is activated
———>	C/I DI	(0011_B)	C/I UAI	(0111_B)	———>	
–––––>	**C/I AR**	**(1000_B)**				; Terminal requests activation
			C/I AR	(1000_B)	———>	; Exchange is notified of
<———	C/I AR	(1000_B)				; proceeding S-activation
–––––>	C/I AI	(1100_B)				; Confirm that terminal is active
			C/I UAI	(0111_B)	———>	
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Activation complete

6.8.8 Deactivating S/T-Interface Only

The following example shows the procedure for deactivating the S-interface only while leaving the U-interface active.

	NT		LT			
<———	C/I AI	(1100_B)	C/I AI	(1100_B)	———>	; Initial state: layer 1 activated
———>	C/I AI	(1100_B)	C/I AR	(1000_B)	<———	
<———	C/I DR	(0000_B)	**C/I UAR**	**(0111_B)**	**<–––––**	; Deactivate S-interface only
–––––>	C/I DI	(1111_B)	C/I UAI	(0111_B)	———>	; S-interface is deactivated
<———	C/I DC	(1111_B)	[C/I DC	(1111_B)]	<———	; Exchange retains no control

6.8.9 Activation Initiated by LT with Repeater

For LT and NT the activation procedure with a repeater between exchange and network is identical to that described at the beginning of this chapter. The repeater transforms the received U-signals into C/I-codes and monitor messages. These codes and messages pass the repeater control unit (e.g. µP). In this control unit a number of adaptations are made to comply with a specific national specification.

In this section only C/I-codes are considered which need to be transformed by the control unit such that the repeater counterpart will operate correctly. In addition overhead bits and the specified 2B+D data needs to be transferred for a correct repeater activation/deactivation.

In order to recognize the dependence of LT-RP and NT-RP-signals more easily, the arrows point towards the middle.
When activating the repeater unit from the exchange side, the UAI-code issued by the LT-RP needs to be converted into AI for the NT-RP.

LT-RP				**NT-RP**		
C/I DC	(1111_B)	<———	<———	C/I PU	(0111_B)	; Initial state "Power Up" to provide timing
C/I DI	(1111_B)	———>	———>	C/I TIM	(0000_B)	
C/I AR	(1000_B)	<———	<———	C/I DC	(1111_B)	; Activation started by LT
C/I AR	(1000_B)	———>	<———	C/I AR	(1000B)	
C/I ARM	(1001_B)	———>				; Activation proceeds
C/I UAI	(0111_B)	———>	———>	C/I AI	(1100_B)	
C/I AI	(1100_B)	———>	<———	C/I AI	(1100_B)	; Activation complete

6.8.10 Activation Initiated by TE with Repeater

In order to recognize a terminal initiated activation successfully the NT-RP must be in "Power Up" condition to provide clocks for the LT-RP. During the activation procedure the LT-RP-signal "UAI" needs to be changed into "AI" by the control unit.

LT-RP				NT-RP		
C/I DC	(1111_B)	<———	<——— C/I PU	(0111_B)	;	Initial state "Power Up" to provide timing
C/I DI	(1111_B)	———>	———> C/I TIM	(0000_B)		
C/I AR	(1000_B)	———>	———> C/I AR	(1000_B)	;	Terminal requests activation
C/I AR	(1000_B)	<———	<——— C/I AR	(1000_B)	;	Activation proceeds
C/I ARM	(1001_B)	———>				
C/I UAI	(0111_B)	———>	———> C/I AI	(1100_B)		
C/I AI	(1100_B)	———>	<——— C/I AI	(1100_B)	;	Activation complete

6.8.11 Deactivation by Repeater

The start of a deactivation procedure is passed from the LT to the NT side via Single bits in the U-frame. These are interpreted by the LT-RP. Thereafter the deactivation process in LT-RP and NT-RP is running mostly independent of each other as illustrated below. No C/I-codes need to be converted by the control unit.

LT-RP				NT-RP		
C/I AR	(1000_B)	<———	<——— C/I AI	(1100_B)	;	Layer 1 is activated
C/I AI	(1100_B)	———>	———> C/I AI	(1100_B)		
C/I DR	(0000_B)	<———	<——— C/I AR	(1000_B)	;	Deactivation started by LT
C/I DEAC	(0001_B)	———>	<——— C/I DR	(0000_B)	;	Deactivation proceeds
C/I DI	(1111_B)	———>	———> C/I DI	(1111_B)		
C/I DC	(1111_B)	<———	<——— C/I DC	(1111_B)	;	Deactivation complete
			———> C/I TIM	(0000_B)	;	Stay in "Power Up" to keep clocks
			<——— C/I PU	(0111_B)	;	turned on.

7 Application Hints

One of the most important conditions for maximizing device, board and system performance is the way the IEC-Q is connected to external circuitry on the board. Section 7.1 gives some recommendations concerning external circuitry and layout. It also defines the characteristics of the crystal if it is needed for the mode being used.

Section 7.2 gives an example for using the S/G and BAC bit feature of the IEC-Q to design PBX systems with D-channel arbitration.

Some application hits for repeater systems are given in section 7.3.

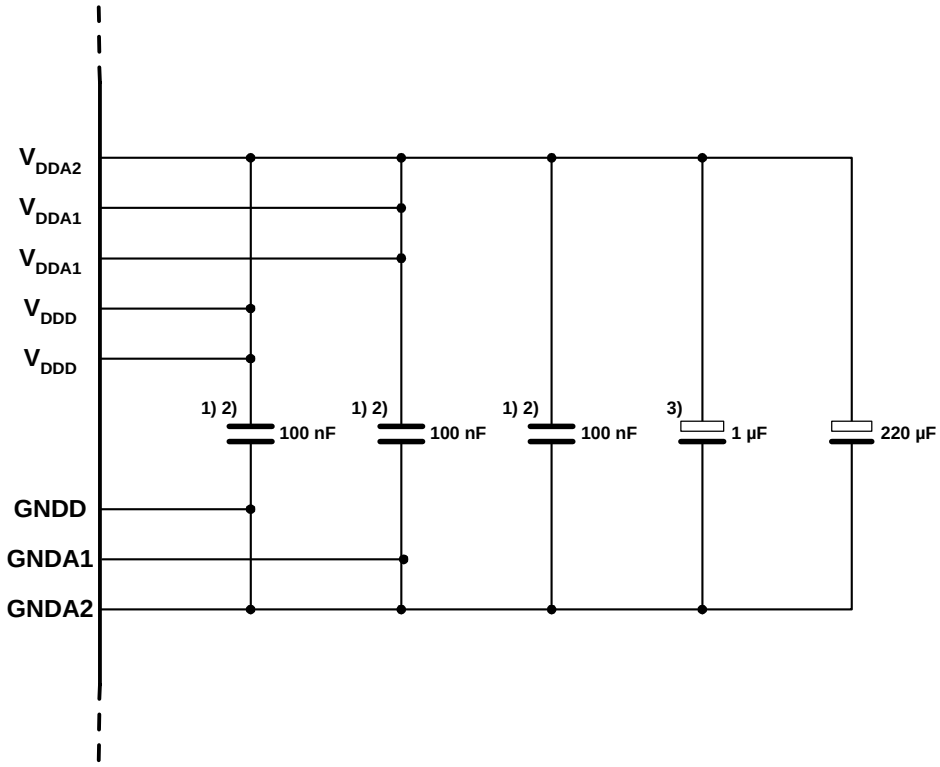
The IEC-Q provides special modes to allow performance of system measurements defined by ITU, ANSI and ETSI. Section 7.4 shows which system set-ups are needed for performing these measurement.

Note 69: This chapter covers only a small part of the applications which can be served by the IEC-Q. For more information, refer to the various application notes published on this subject.

7.1 External Circuitry

7.1.1 Power Supply Blocking Recommendation

The following blocking circuitry is suggested.



1) These capacitors should be located as near as possible to the pins
2) MKT-stack film capacitors
3) Tantanum electrolytic capacitor

Figure 92 Power Supply Blocking

7.1.2 U-Interface

Note 70: ***The requirements for the power spectral density of the transmitted 2B1Q signal on the U-interface has been changed by ETSI. This change aims to reduce interference between basic rate 2B1Q signals on the one hand and ADSL and VDSL signals on the other. All of these signals will be transmitted on the same kind of lines in the future. For more information, refer to the ETSI document "Technical Specification 101080" (1999).***
To meet the new specification some modifications of the hybrid recommended in previous IEC-Q versions are required. Figure 93 below illustrates the hybrid circuit needed to meet these new ETSI requirements.

Note 71: ***This change will be in force from January, 2000 onward. After this date systems with the old hybrid will not comply to ETSI standards at this point.***

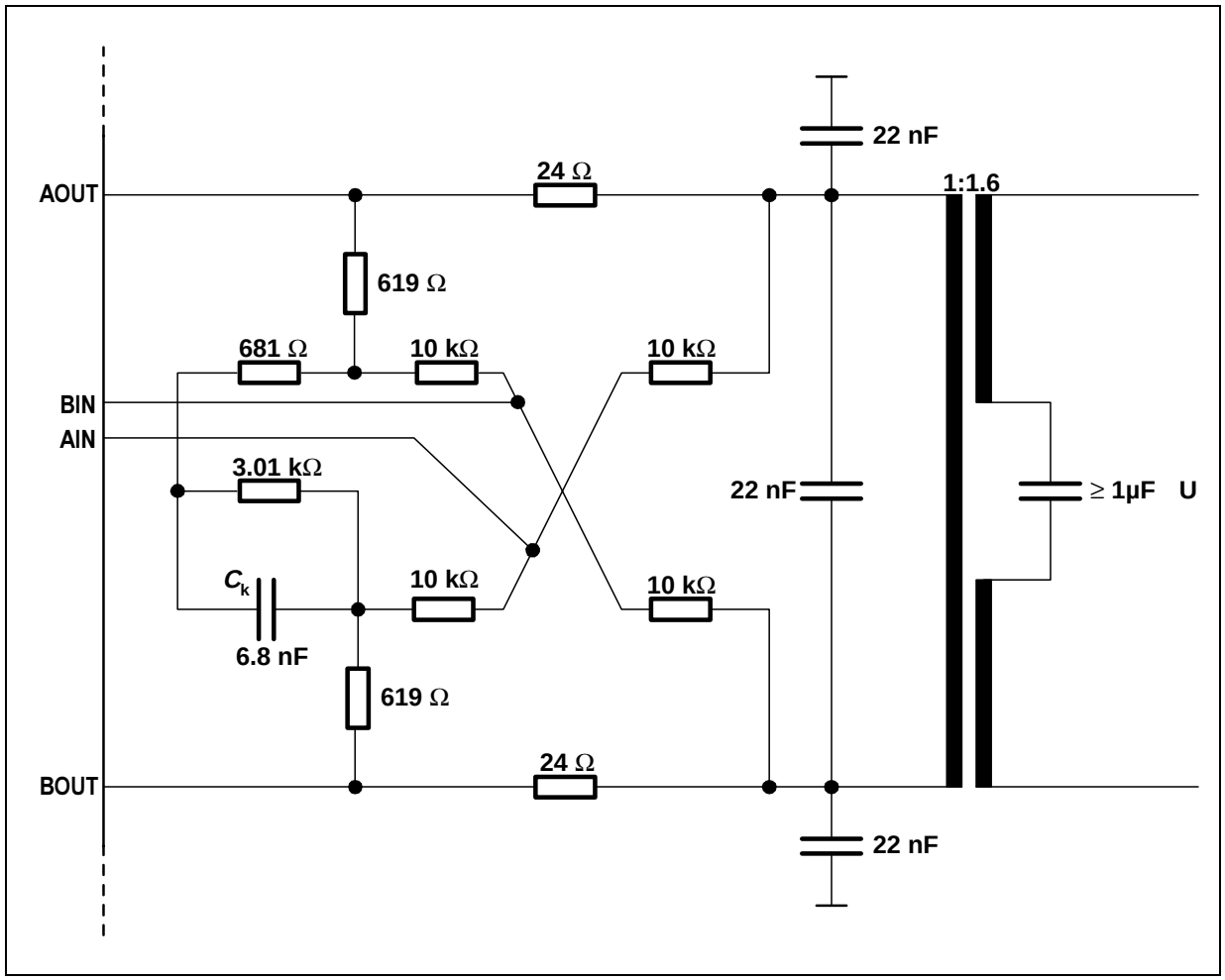


Figure 93 U-Interface Hybrid Circuit

Note 72: The three 22 nF capacitors can be replaced by one 33 nF capacitor in the middle. However, the solution with the three capacitors can absorb longitudinal disturbances in a better way.

To improve transmission performance the following recommendations should be considered in circuit design:

- All capacitors of the hybrid should be MKT. Ceramic capacitors are not recommended
- Do not cross hybrid or XTAL with clock lines
- Analog lines between transformer and chip should be symmetric and close together so that noise is inducted symmetrically
- Hybrid layout should be symmetric
- If possible there should be a ground plane underneath the IEC-Q
- Blocking of VDD according to recommendation and as close as possible to device (see also "Power Supply Blocking Recommendation", page 249).
- Tolerances

  Resistors: 1%
  6.8 nF: 5%
  22 nF: 5%

7.1.3 Oscillator Circuit and Crystal

Figure 94 illustrates the recommended oscillator circuit. A crystal or an oscillator signal may be used.

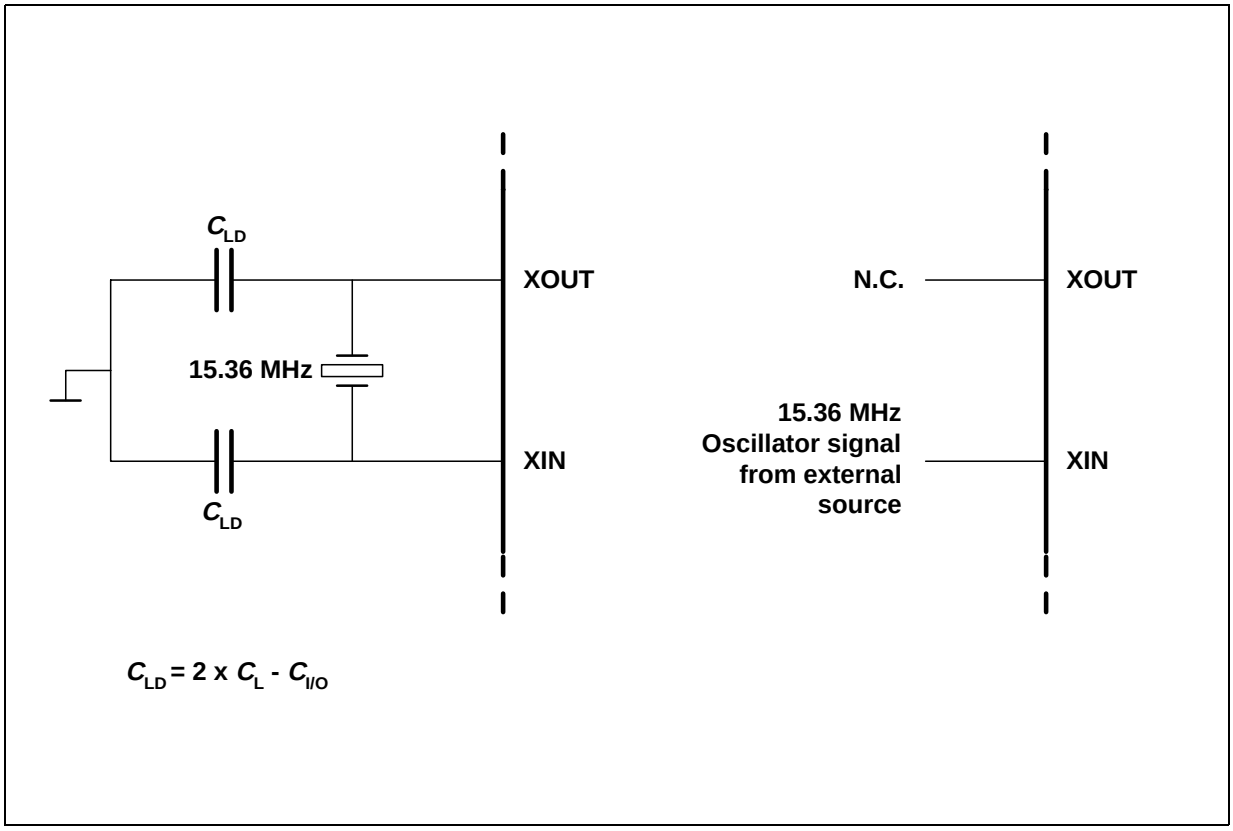


Figure 94 Crystal Oscillator or External Clock Source

Crystal Parameters

Frequency:	15.36 MHz
Load Capacitance C_L:	20 pF ± 0.3 pF
Frequency Tolerance:	60 ppm
Resonance Resistance:	20 Ω
Max. Shunt Capacitance:	7 pF
Drive Current I_Q	1 mA
Maximum Drive Current I_{Qmax}	2 mA
Motional Capacitance	20 fF ± 20%
Motional Inductance	≈ 9.4 mH
Oscillator Mode:	fundamental

Note 73: Typical values for capacitances connected to the crystal are 22 ... 33 pF, depending on board layout.

Note 74: These Parameter shall apply to the complete temperature range and life time. The temperature range depends on the version used. For PEB 2091 it is between 0°C and 70°C, for the PEF 2091 it is between -40°C and 85°C.

External Oscillator

Frequency:	15.36 MHz
Frequency tolerance:	80 ppm

In this case the requirements for the master clock are the same as the requirements in the LT case. See "Master Clock", page 281 for details.

7.2 Applications with EPIC® on the Line Card (PBX)

This section gives an example for using the S/G bit and BAC bit control feature (see section 3.9, page 90) for D-channel arbitration in PBX applications with the PEB 20550 (ELIC®) used in the Line card.

The S/G bit on DOUT (downstream) and the BAC bit on DIN (upstream) can be used to allow D-channel arbitration similar to the operation of the Upn interface realized with the OCTAT-P and the ISAC®-P TE. The basic function is as follows:

The PBX line card using the ELIC® assigns one HDLC controller to a number of terminals. As soon as one terminal *T* requests the D-channel, e.g. for signalization, all other terminals receive a message indicating the D-channel to be blocked for them. The request is done with the BAC bit. At terminal *T* the BAC bit is set and the IEC-Q transfers the need for the D-channel to the LT side. There, the HDLC-controller is assigned to the appropriate IOM®-2-channel. Once this is done and indicated to the terminal by means of the S/G bit, the terminal begins to send D-channel messages.

Note that this procedure is somewhat different from the operation of the OCTAT-P used with the ISAC®-P TE. There, the begin of the upstream D-channel data transfer itself indicates the need for the HDLC-controller. This implies that any other terminal, that incidentally sent a HDLC-message the same time, can be stopped before the message is lost in case the HDLC-controller is not available. The U-interface featured by the IEC-Q is not able to transfer the available/blocked information often enough to ensure this. Hence, it is necessary to indicate a D-channel access by the terminal in advance. "In advance" actually means about 14 ms.

Giving MON-0 25_H at the LT during Transparent operation will cause the D-channel access at the NT side to be on "STOP". As one EOC-message is transmitted via the EOC-channel once every 6 ms, the S/G bit on IOM®-2 can be set in 6 ms intervals.

If the 4 channel PEB 24911 (DFE-Q) is used in the LT, a PEB 20550 (ELIC®) can arbitrate the D-channel via the C/I command as known from the OCTAT-P and QUAT-S devices. Please refer to the PEB 24911 Data Sheet for detailed information on this.

The BAC bit together with the EOC-messages received from the LT control the S/G bit and the upstream D-channel according to Table 49.

.

Table 49 Control Structure of the S/G Bit and of the D-Channel

BAC bit of last IOM®-2-frame	S/G bit 1 = stop 0 = go	D-channel upstream
0	reflects last received EOC message after falling edge after delay TD1 (1.5 ms and two EOC-frames)	tied to "0"
1	1	set transparent with first "0" in D-channel

D-Channel Request by the Terminal

Figure 95, page 256, illustrates the request for the HDLC-controller by the terminal. The start state is BAC = 1 at DIN after TD1 has expired. That causes the S/G bit to be set to the stop position.

BAC = 1 received on DIN sets the S/G bit on DOUT to the stop position (’1’) at the next IOM®-2-frame. When the terminal requests access to the HDLC-controller in the ELIC® it sets the BAC-bit at DIN of it’s IEC-Q to "0". That causes the D-channel data upstream to be tied to "0" and the S/G-bit to be set to "1". The ELIC® receives the zeros and reacts by assigning the HDLC-controller to this very terminal. This is indicated via the change of C/I code downstream at the LT side resulting in the S/G bit to be set to "0" (’go’) after delay TD1 (see below for the explanation of TD1 and TD2).

The IEC-Q will continue to send "0" upstream in the D-channel until the HDLC data arrives at DIN. The HDLC-frame itself, marked by the first "0" in the D-channel will reset the D-channel back to transparent. This allows to have arbitrary delays between the S/G bit going to "0" and the D-channel being used without the risk of loosing the HDLC-controller by sending an abort request consisting of all "1".

At the end of the HDLC-frame the BAC bit is reset to "1" again by the layer-2 controller (e.g. SMARTLINK; ICC). This causes the S/G bit to be set to "1" in the next IOM®-2 frame which stops a possible second HDLC-frame that could not be processed in the ELIC® anymore.

TD1 and TD2

The delays TD1 and TD2 (see Figure 95, page 256) have the following reasons: TD2 is caused by the 6ms interval in which an EOC message can be transmitted on the

U-interface. As an EOC-message can start once every 6 ms and will take 6 ms to be transmitted, TD2 will be 12 ms in the worst case.

TD1 is at minimum 7.5 ms depending on the location of the superframe at the time the HDLC-controller is requested by the terminal. This delay is necessary because instead of receiving an EOC-message "go" as requested, the terminal could as well receive the EOC message "stop" because the HDLC-controller was assigned to an other subscriber just before .

Flags as Interframe Fill

The influence to the upstream D-channel can be disabled while the control of the S/G-bit via EOC-messages and via the BAC bit is still given as described above by setting SWST:BS to "0", SWST:SGL to "1" and ADF:CBAC to "1". This is useful when having a controlling device in the terminal, that is able to send the interframe timefill "flags".

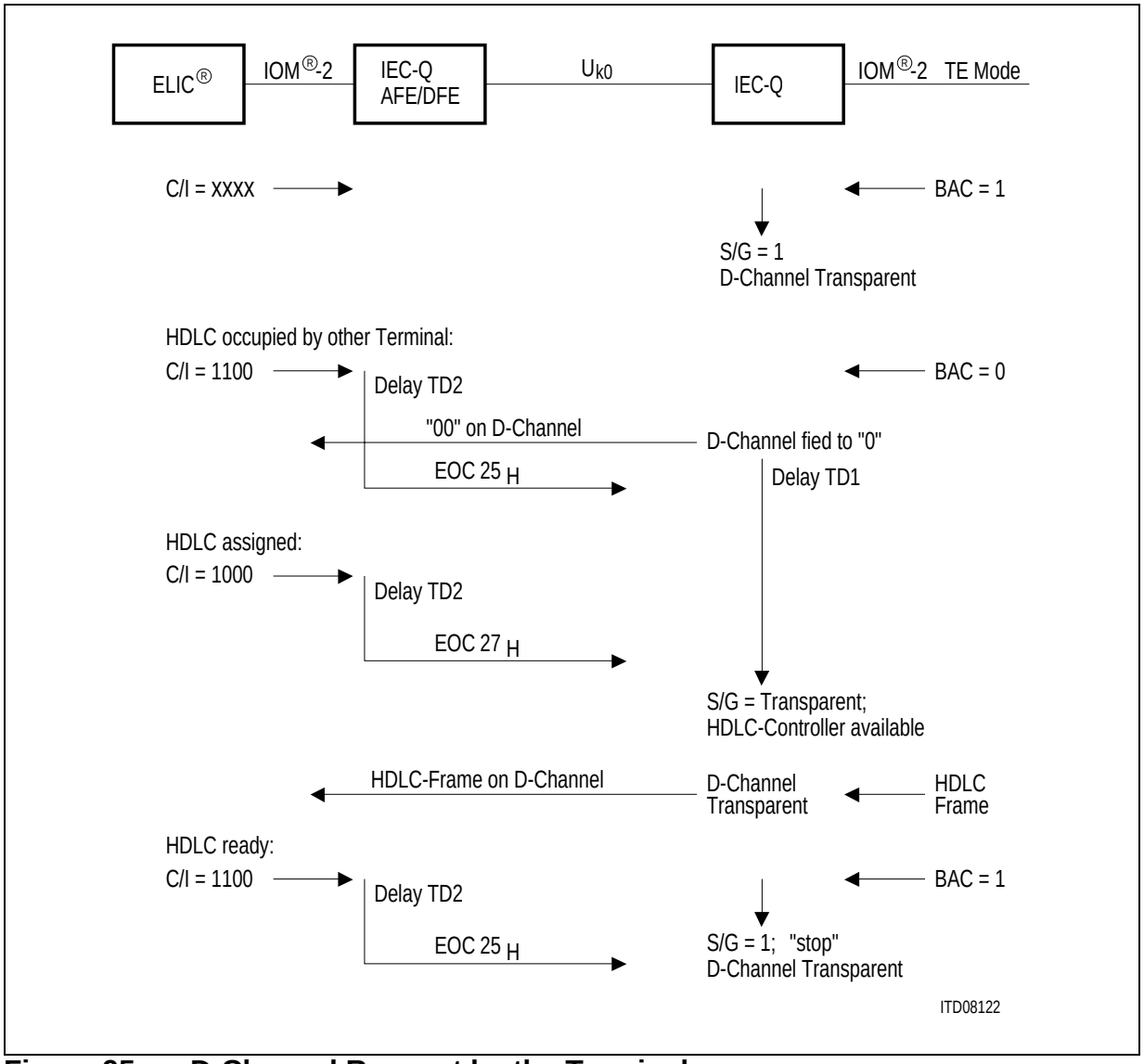


Figure 95 D-Channel Request by the Terminal

7.3 Hints for Repeater Applications

7.3.1 EOC Addressing Management

Note 75: Access to EOC is described in detail in "Access to EOC of U-Interface", page 110.

This application hint describes a way of addressing a certain repeater if one or more repeater are used in one transmission line.

The LT-RP and NT-RP should be operated in EOC Transparent mode (see "EOC Auto/Transparent Mode", page 55). In order to address each repeater individually, the EOC-addresses (001_B) to (110_B) are used. This allows a maximum of 6 repeater stations to be addressed.

The repeater address is 001_B. If a repeater control unit detects an EOC-message with this address, the EOC-command will be executed according to the national repeater specification. In case an EOC-message with the NT (000_B) or broadcast (111_B) address is received by the repeater, the message needs to be passed on without modifications. If any other address is received (i.e. (010_B) to (110_B)) the repeater control unit (µP or ASIC) decrements the address before passing the EOC-message downstream. Figure 96 illustrates this procedure with a repeater and a NT EOC-address.

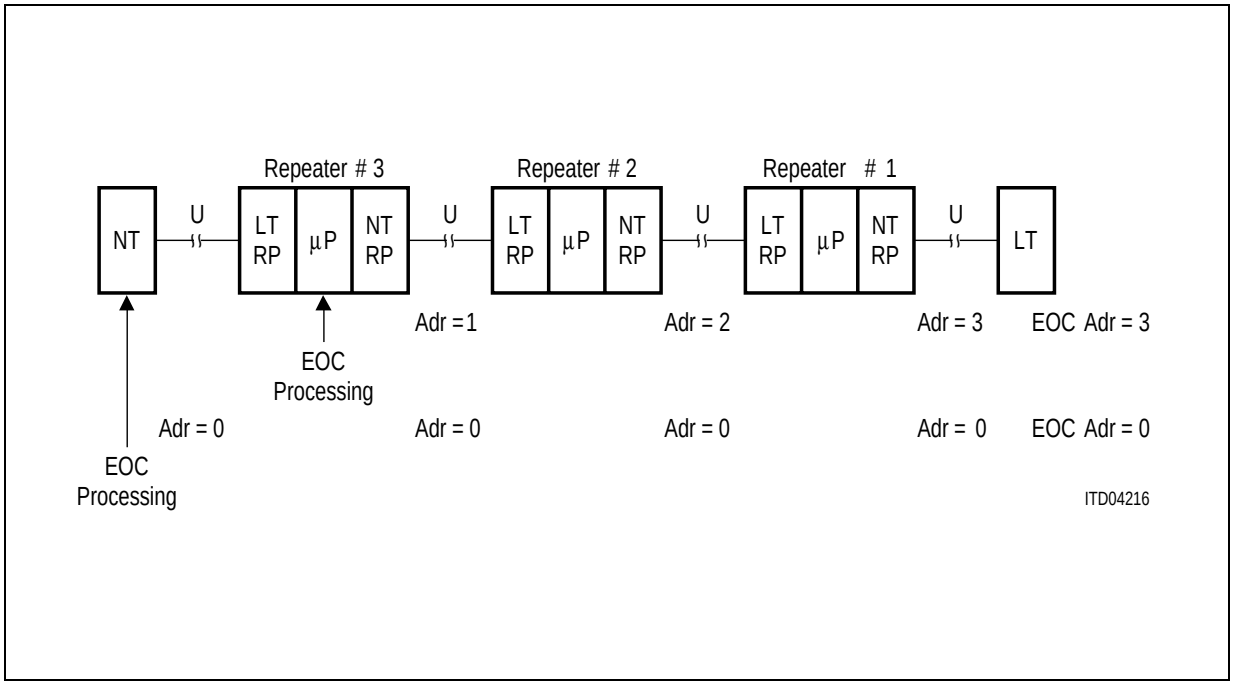


Figure 96 EOC-Handling in Repeater Applications

7.3.2 Single Bits Handling

Figure 97 shows an example for typical maintenance bit handling in repeater applications via MON-2. In this example a microprocessor can be used as a control unit and the microprocessor interface can be used instead of the IOM®-2 interface.

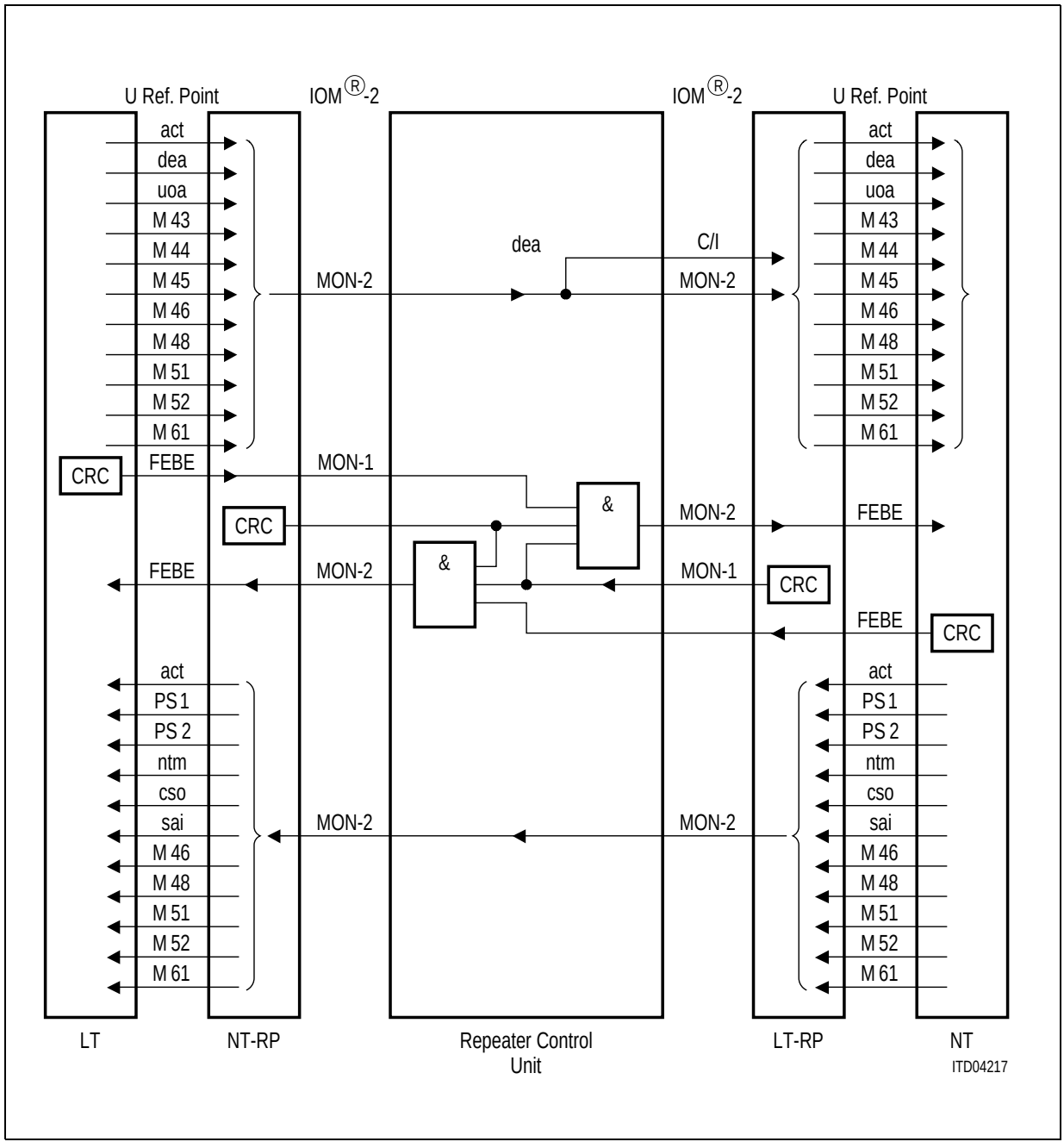


Figure 97 Maintenance Bit Handling in Repeaters (Example)

7.4 Set-ups for Test Modes and System Measurements

With a number of operational modes the IEC-Q supports system measurements. These modes along with the most frequently needed system measurements are described in the following sections.

7.4.1 Tests in Send Single Pulses Mode

The SSP-test mode is required for pulse mask measurements.

In this test mode, the IEC-Q transmits on the U-interface alternating ± 3 pulses spaced by 1.5 ms. This test mode is used in LT and NT like modes. Three options exist for selecting the “Send-Single-Pulses" (SSP) mode:

– hardware selection: RESQ = 1 & TSP = 1
– software selection: C/I = SSP (0101_B)
– microprocessor selection Bits (STCR:TM1 = 1) and (STCR:TM2 = 1)

All methods are fully equivalent. In the SSP mode the C/I-code transmitted by the IEC-Q is DEAC in LT modes and DR in the NT modes.

Pulse Mask Measurement

– Pulse mask is defined in ANSI T1.601 and ETSI TS 101080
– U-interface has to be terminated with 135 Ω
– IEC-Q is in “Single-Pulses" mode
– Measurements are done using an oscilloscope

7.4.2 Tests in Data-Through Mode

The DT mode is required for power spectral density and total power measurements.

When selecting the data-through mode, the IEC-Q is forced directly into the “Transparent" state. This is possible from any state in the state diagram.

The Data-Through option (DT) provides the possibility to transmit a standard scrambled U-signal even if no U-interface wake-up protocol is possible. This feature is of interest when no counter station can be connected to supply the wake-up protocol signals. The DT-test mode may be used in LT and NT like applications.

As with the SSP mode, three options are available.

– hardware selection: RESQ = 0 & TSP = 1
– software selection: C/I = DT (0110_B)
– microprocessor selection Bits (STCR:TM1 = 0) and (STCR:TM2 = 1)

Power Spectral-Density Measurement

– PSD is defined in ANSI T1.601 and ETSI TS 101080
– U-interface has to be terminated with 135 Ω
– IEC-Q is in “Data-Through" mode
– For measurements a spectrum analyzer is employed

Total Power Measurement

– Total power is defined in ANSI T1.601 and ETSI TS 101080
– Total power must be between 13 dBm and 14 dBm
– U-interface has to be terminated with 135 Ω
– IEC-Q is in “Data-Through" mode
– Measurements are done using an 80 kHz high-impedance low-pass filter and true RMS-voltmeter

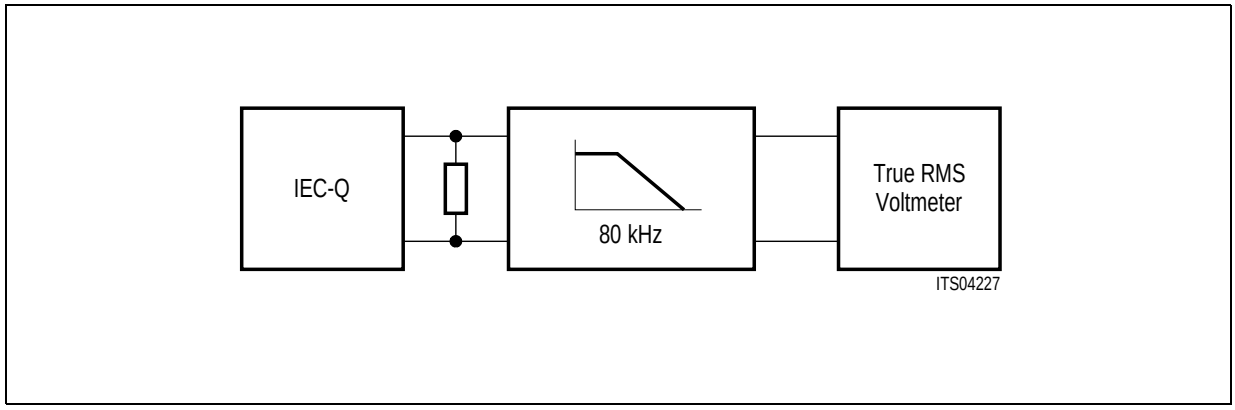


Figure 98 Total Power Measurement Set-Up

Insertion Loss Measurement

– Insertion loss is defined in ANSI T1.601
– IEC-Q is in Data-Through mode
– Trigger and exit criteria have to be realized externally

7.4.3 Tests in Master-Reset Mode

The master-reset test mode is used for the return-loss measurements.

The master-reset mode characterizes the mode where the IEC-Q does not transmit any signals. The chip is in the “Test" state. All echo canceller and equalizer coefficients are reset. As can be seen from the state diagram, no activation is possible in LT or NT modes when the device is in the “Test" state.

For measurements two methods are recommended in order to transfer the IEC-Q into the master-reset mode:

– hardware selection: RESQ = 0 & TSP = 0
– software selection: C/I = RES (0001_B)

The C/I-code transmitted by the IEC-Q in the “Test" state is DEAC in LT modes and DR in all NT modes.

Return-Loss Measurement

– Return loss is defined in ANSI T1.601 and ETSI TS 101080
– IEC-Q is in Test state
– Measure complex impedance “Z" from 14 kHz – 200 kHz
– Calculate return loss with formula:

RL(dB) = 20log (abs((Z + 135) / (Z –135)))

Quiet Mode Measurement

– Quite mode is defined in ANSI T1.601
– IEC-Q is in the Test state
– Trigger and exit criteria have to be realized externally

8 Electrical Characteristics

This chapter specifies on the one hand the electrical characteristics of device inputs and power needed to guarantee proper operation of the IEC-Q. On the other hand it specifies the electrical characteristics of the IEC-Q outputs, power consumption and analog functions.

Note 76: All electrical characteristics of the IEC-Q apply only in the specified operational range and under the stated test conditions.

Sections 8.1 and 8.2 describe the maximum ratings allowed and the power supply needed.

Section 8.3 specifies the maximal overload which can be imposed directly on the IEC-Q line interface, without causing device damage.

Sections 8.4 and 8.5 specify the power consumption and the analog functions (e.g. ADC and DAC performance).

Section 8.6 describes the DC characteristics of the IEC-Q.

The dynamic characteristics of the microprocessor interface, the IOM®-2 interface, the power controller interface, the undervoltage detection block and device clock are given in section 8.7.

8.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_{DD}	$-0.3 < V_{DD} < 7.0$	V
Input voltage	V_I	$-0.3 < V_I < V_{DD} + 0.3$ (max. 7)	V
Output voltage	V_O	$-0.3 < V_O < V_{DD} + 0.3$ (max 7)	V
Max. voltage applied at U-Interface	V_S	$-0.3 < V_S < V_{DD} + 0.3$ (max. 7)	V
Max. voltage between GNDA1 (GNDA2) and GNDD	V_S	$\pm$ 250	mV
Storage temperature	T_{stg}	– 65 to 125	°C
Ambient temperature PEB 2091 PEF 2091	 T_A T_A	 0 to 70 – 40 to 85	 °C °C
Thermal resistance (system-air) (system-case)	 $R_{th\ SA}$ $R_{th\ SC}$	 40 9	 K/W K/W

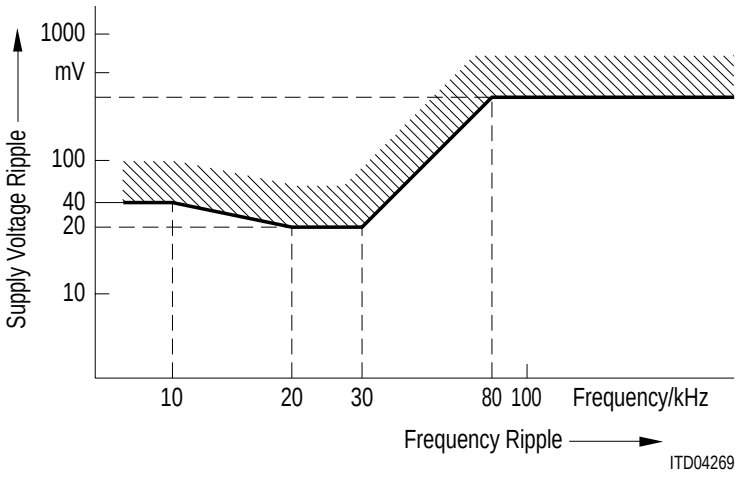
Note 77: ***Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.***
Exposure to conditions beyond those indicated in the recommended operational conditions of this specification may affect device reliability.
This is a stress rating only and functional operation of the device under those conditions or at any other condition beyond those indicated in the operational conditions of this specification is not implied.
It is not implied, that more than one of those conditions can be applied simultaneously.

8.2 Power Supply

Supply voltages

V_{DDD} = + 5 V ± 0.25 V
V_{DDA1} = + 5 V ± 0.25 V
V_{DDA2} = + 5 V ± 0.25 V

The maximum sinusoidal ripple on V_{DDA1} and V_{DDA2} is specified in the following figure:



Note: The supply voltage ripple in measured peak to peak

Figure 99 Maximum Sinusoidal Ripple on Supply Voltage

8.3 Line Overload Protection

The maximum input current (under overvoltage conditions) is given as a function of the width of a rectangular input current pulse as outlined in the following figure.

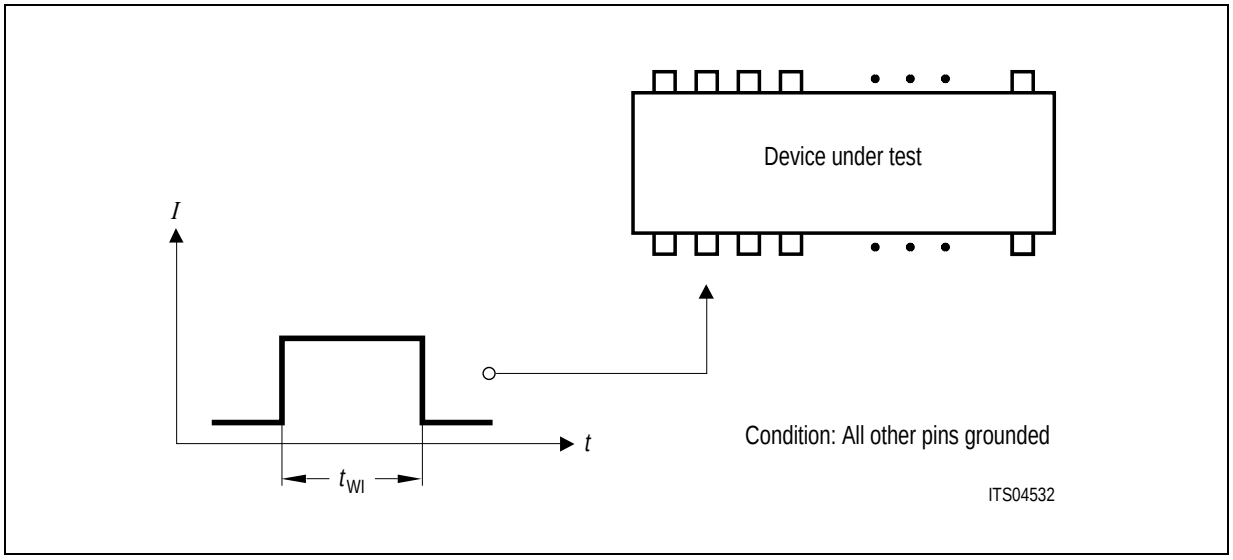


Figure 100 Test Condition for Maximum Input Current

Line Input Current

The destruction limits for AOUT, BOUT, AIN and BIN are given in Figure 101.

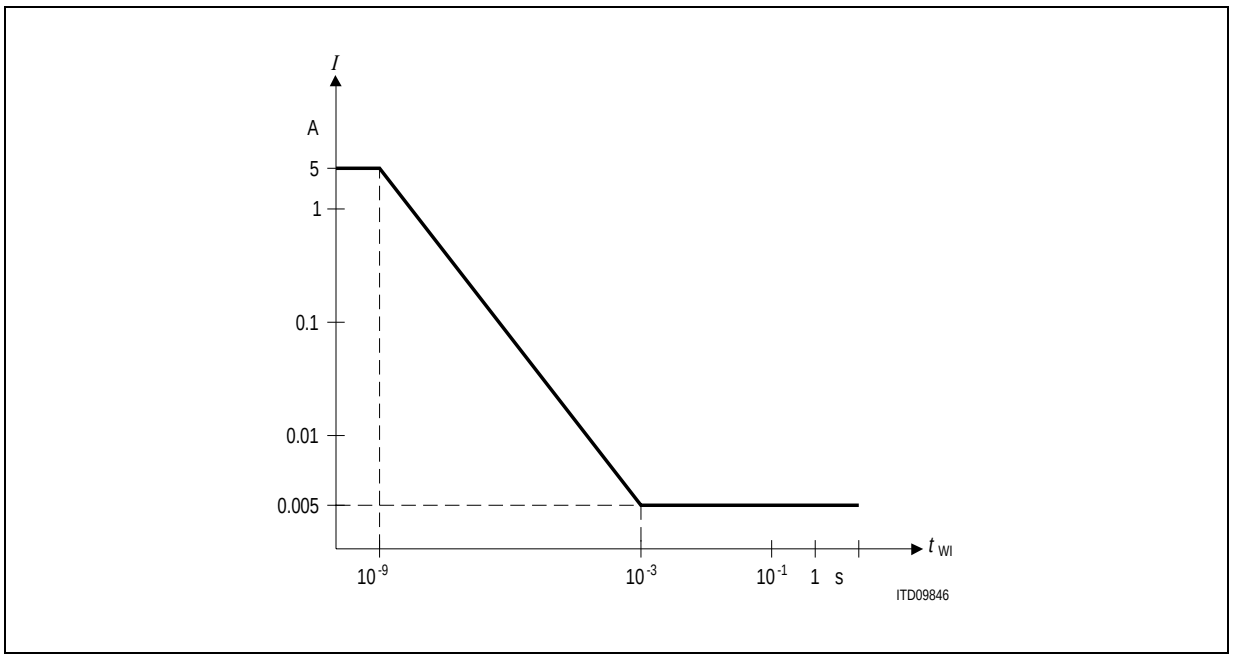


Figure 101 U transceiver Input Current

8.4 Power Consumption

The power consumption of version 5.3 has been reduced, compared with version 5.1. Version 5.3 will have the same power consumption values as version 5.2.

All measurements with random 2B + D data in active states.

Mode	Test Conditions	Limit Values		Unit
		typ.	max.	
Power up	5.00 V, open outputs 98 Ω load at AOUT/BOUT Inputs at VDD/GND	53.0	59.0	mA
LT-Power down	5.00 V, open outputs 98 Ω load at AOUT/BOUT Temperature ≥ 0°C Inputs at VDD/GND	6.7	11.0	mA
	5.00 V, open outputs 98 Ω load at AOUT/BOUT Temperature < 0°C Inputs at VDD/GND	8.0	13.0	mA
NT-Power down	5.00 V, open outputs 98 Ω load at AOUT/BOUT Temperature ≥ 0°C Inputs at VDD/GND	4.7	9.0	mA
	5.00 V, open outputs 98 Ω load at AOUT/BOUT Temperature < 0°C Inputs at VDD/GND	6.5	11.0	mA

Note 78: The power consumption specified above includes the power dissipation in the load resistance. The power dissipation in the IEC-Q itself is 7.5 mA less in the active state, i.e. the maximum internal power dissipation of the IEC-Q in the active state is less than 52 mA, under the stated conditions.

8.5 Analog Characteristics

	Limit Values			Unit
	min.	typ.	max.	
Receive Path				
Signal / N+D (noise + total harmonic distortion)[1)]	60	65		dB
DC-level at AD-output	45	50	55	%[2)]
Threshold of level detect	4	20	28	mV
Input impedance AIN/BIN	50			kΩ
Transmit Path				
Signal / N+D (noise + total harmonic distortion)[3)]	65	70		dB
Output DC-level	2.05	2.375	2.6	dB
Offset between AOUT and BOUT			35.5	mV
Signal amplitude[4)]	3.10	3.20	3.30	V
Output impedance AOUT/BOUT: Power-up Power-down		 2 6	 4 12	 Ω Ω

1) Test conditions: 1.3 Vpp antisemetric sine wave as input on AIN/BIN with long range (low, critical range)

2) The percentage of the "1"-values in the PDM-signal

3) Interpretation and test conditions: The sum of noise and total harmonic distortion, weighted with a low pass filter 0 to 80 kHz, is at least 65 dB below the signal for an evenly distributed but otherwise random sequence of + 3, + 1, – 1, – 3

4) The signal amplitude measured over a period of 1 min. varies less than 1%

Pulse Shape

The pulse mask for a single positive pulse measured between AOUT and BOUT at a load of 98 Ω is given in the following figure.

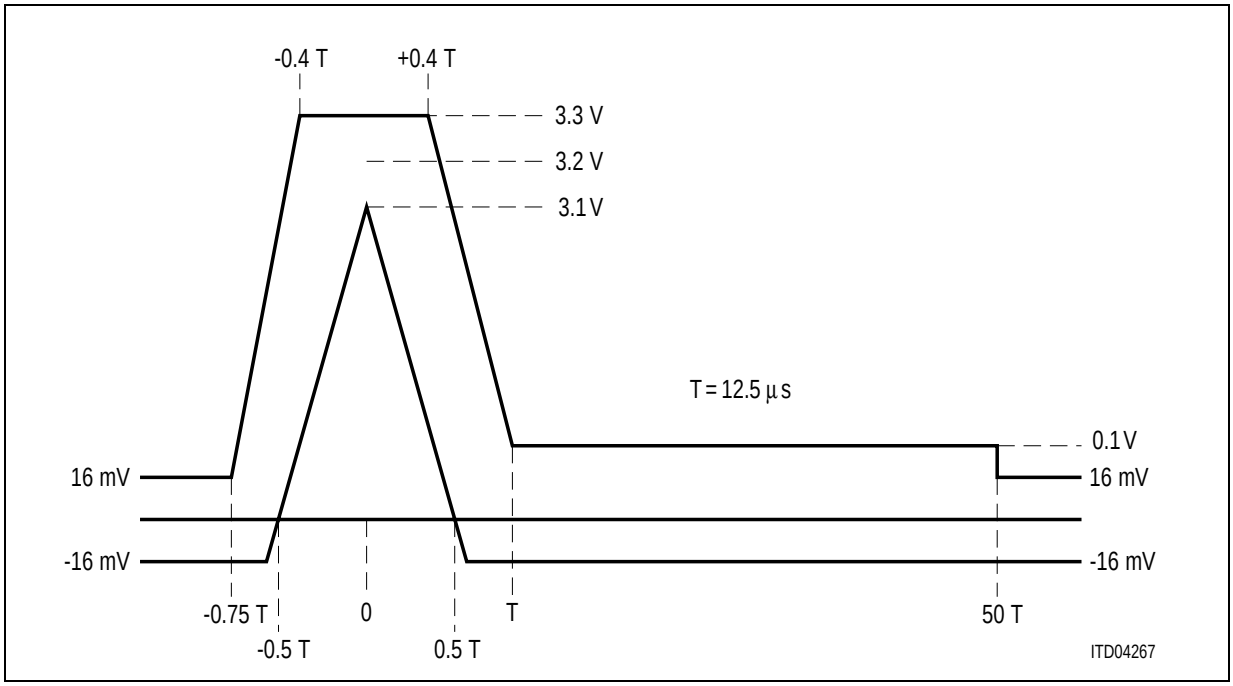


Figure 102 Pulse Mask for a Single Positive Pulse

8.6 DC Characteristics

V_{DD} = 4.75 to 5.25 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
H-level input voltage	V_{IH}	2.0	V_{DD} + 0.3	V	
L-level input voltage	V_{IL}		0.8	V	
L-level input leakage current for all pins except for PIN #11, #14, #15	I_{IL}	– 10		µA	V_I = DGND[1)]
H-level input leakage current for all pins except for PIN #11, #14, #15	I_{IH}		10	µA	V_I = DVDD[1)]
L-level input leakage current of PIN #11 (XIN)	I_{IL}	– 40		µA	V_I = DGND[1)]
H-level input leakage current of PIN #11 (XIN)	I_{IH}		40	µA	V_I = DVDD[1)]
L-level input leakage current of PIN #14, #15 (AIN, BIN)	I_{IL}	– 70		µA	V_I = DGND[1)]
H-level input leakage current of PIN #14, #15 (AIN, BIN)	I_{IH}		70	µA	V_I = DVDD[1)]
L-level input leakage current for pins with pull-up resistors	I_{ILPU}	– 100	100	µA	V_I = DGND[1)]
H-level input leakage current for pins with pull-up resistors	I_{IHPU}	– 10	10	µA	V_I = DVDD[1)]
L-level input leakage current for pins with pull-down resistors	I_{ILPD}	– 30	30	µA	V_I = DGND[1)]
H-level input leakage current for pins with pull-down resistors	I_{IHPD}		500	µA	V_I = DVDD[1)]
H-level output voltage for all outputs except DOUT	V_{OH1}	2.4		V	I_{OH1} = 0.4 mA[1)]
H-level output voltage for DOUT[2)]	V_{OH2}	3.5		V	I_{OH2} = 6 mA[1)]
L-level output voltage for all outputs except DOUT	V_{OL1}		0.4	V	I_{OL1} = 2 mA[1)]
L-level output voltage for DOUT	V_{OL2}		0.5	V	I_{OL1} = 7 mA[1)]

1) Inputs at DVDD/DGND

2) Applies only to the active channel in the tristate mode of DOUT (see "DOUT Driver Modes", page 53)

Pin Capacitances

T_A = 25 °C; V_{DD} = 5 V ± 5 %; V_{SS} = 0 V; f_C = 1 MHz

Pin	Symbol	Limit Values		Unit
		min.	max.	
DIN, PS1, PS2, DCL (input), FSC (input), DOUT (open)	C_{IO}		10	pF
XIN, XOUT	C_{IO}		5	pF
All other pins	C_{IO}		7	pF

8.7 AC Characteristics

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and 0.8 V for a logical "0". The AC testing input/output wave forms are shown in Figure 103 below.

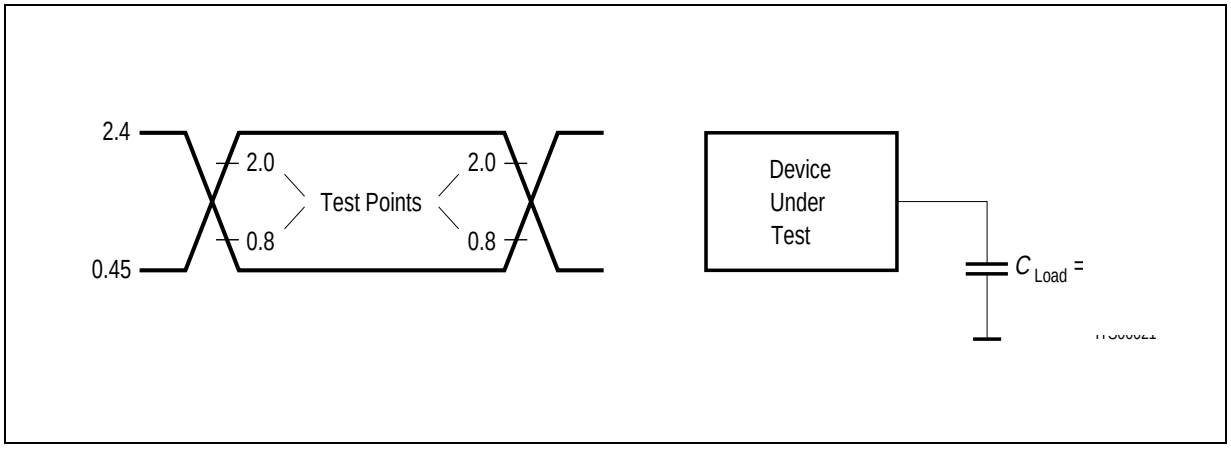


Figure 103 Input/Output Wave form for AC Tests

8.7.1 Microprocessor Interface Timing in Parallel Mode

The microprocessor interface timing in the parallel mode has been accelerated. This allows using the IEC-Q in applications which demand high data transmission rates, e.g. PCM-4, 8, or in applications with high speed microcontroller.

8.7.1.1 Siemens/Intel Bus Mode

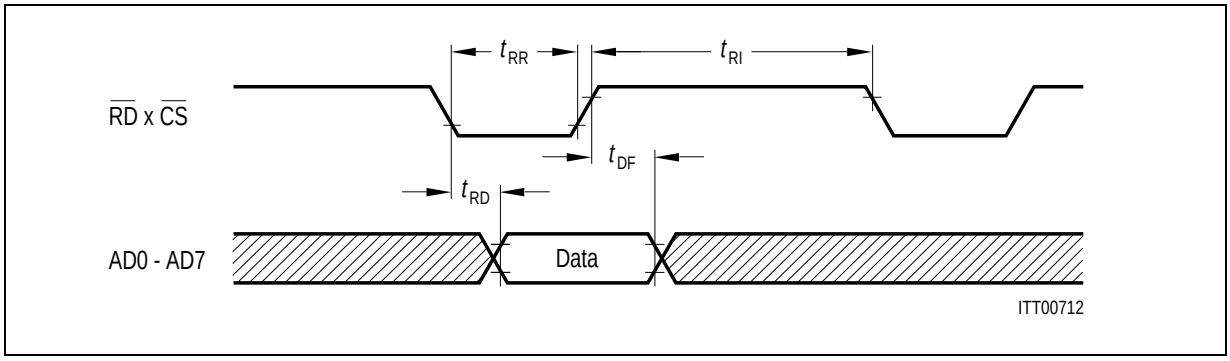


Figure 104 Siemens/Intel Read Cycle

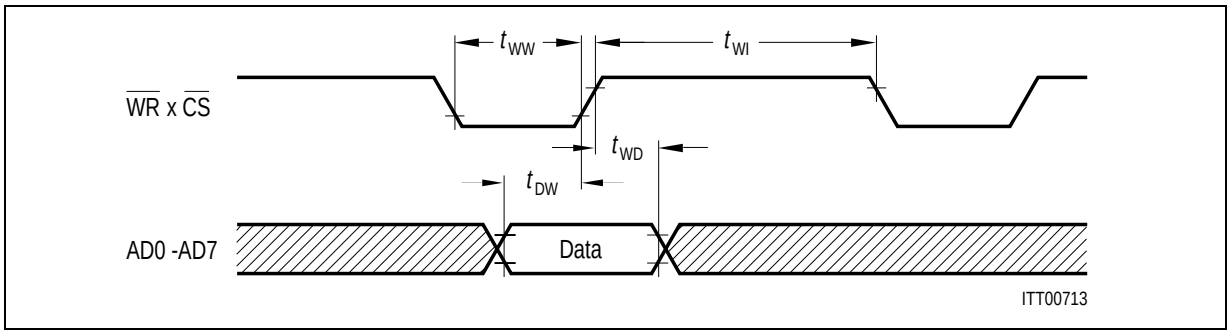


Figure 105 Siemens/Intel Write Cycle

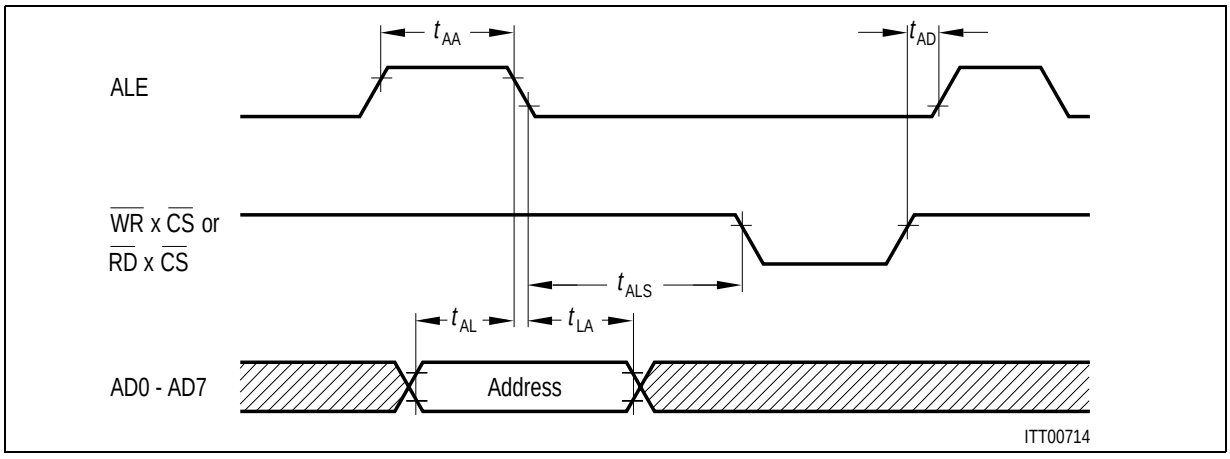


Figure 106 Siemens/Intel Multiplexed Address Timing

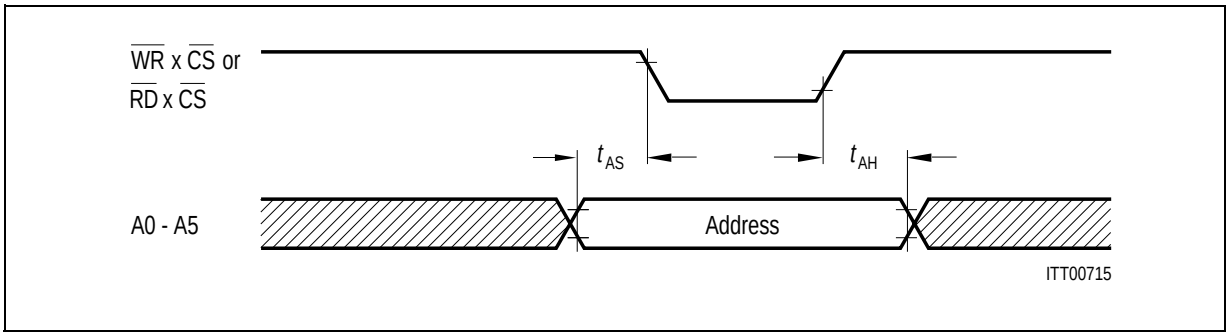


Figure 107 Siemens/Intel Non-Multiplexed Address Timing

8.7.1.2 Motorola Bus Mode

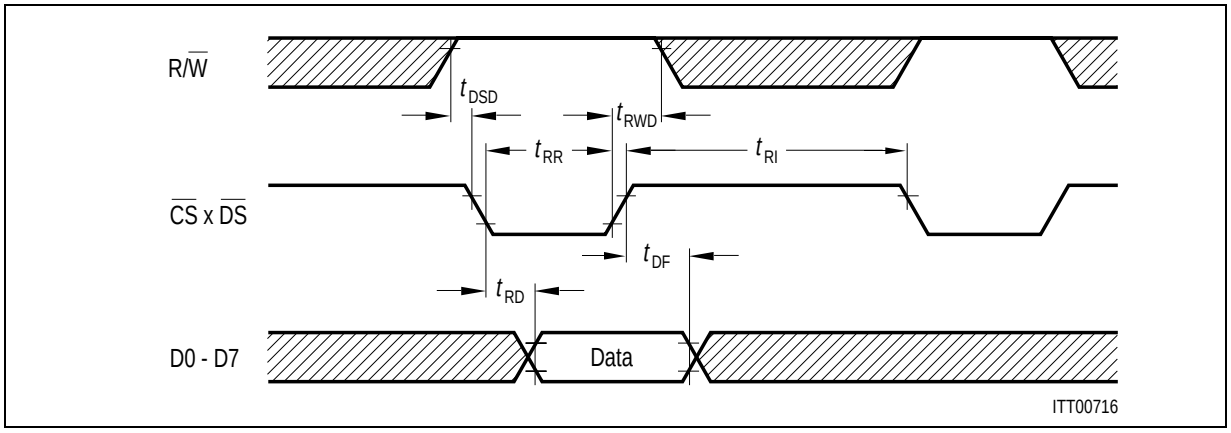


Figure 108 Motorola Read Timing

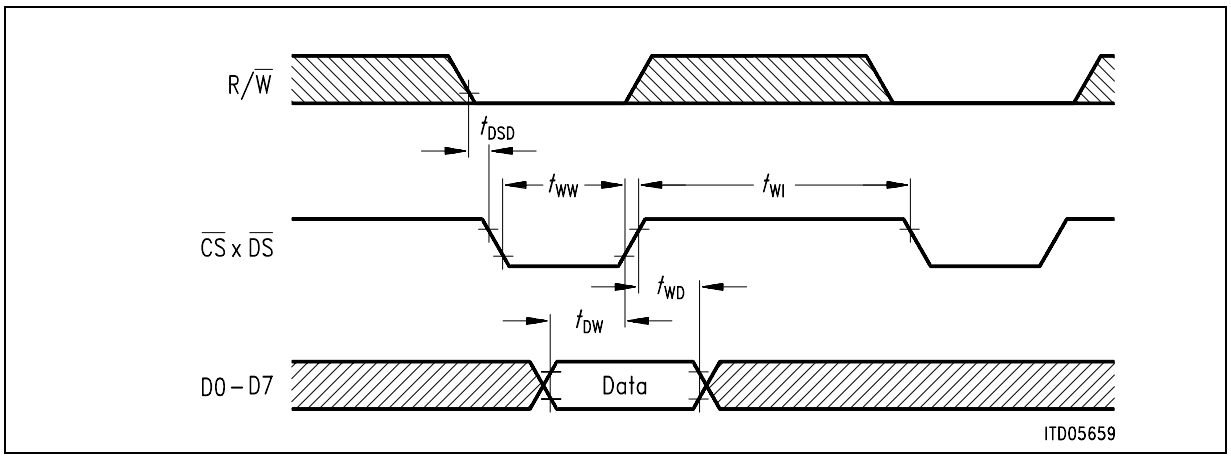


Figure 109 Motorola Write Cycle

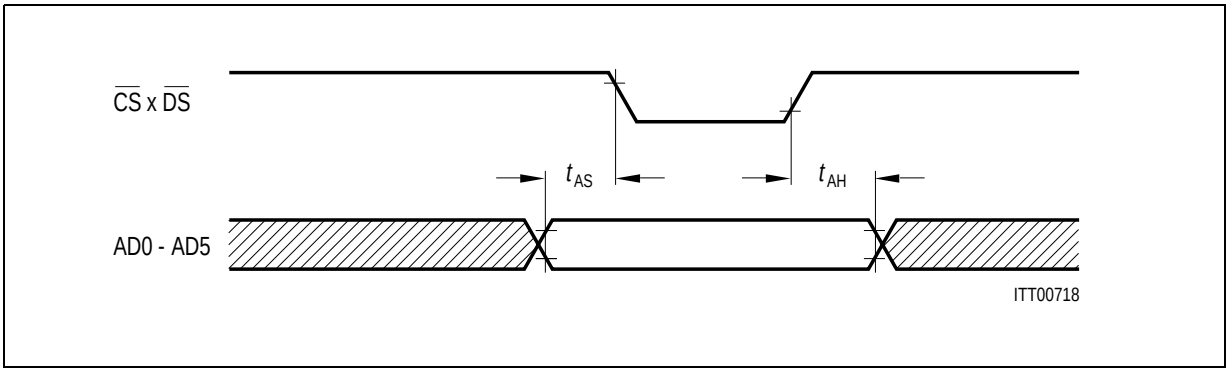


Figure 110 Motorola Non-Multiplexed Address Timing

8.7.1.3 Timing Values of the µP interface in Parallel Mode

C_{Load} = 50pF

Parameter	Symbol	min.	max.	unit
ALE pulse width	t_{AA}	50		ns
Address setup time to ALE	t_{AL}	15		ns
Address hold time from ALE	t_{LA}	10		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0		ns
Address setup time to $\overline{WR}$, $\overline{RD}$	t_{AS}	25		ns
Address hold time from $\overline{WR}$, $\overline{RD}$	t_{AH}	0		ns
ALE pulse delay	t_{AD}	10		ns
$\overline{DS}$ delay after R/$\overline{W}$ setup	t_{DSD}	0		ns
R/$\overline{W}$ hold time after $\overline{DS}$	t_{RWD}	0		ns
$\overline{RD}$ pulse width	t_{RR}	110		ns
Data output delay from $\overline{RD}$	t_{RD}		110	ns
Data float from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	70		ns
$\overline{WR}$ pulse width	t_{WW}	60		ns
Data setup time to $\overline{WR}$ x $\overline{CS}$	t_{DW}	35		ns
Data hold time from $\overline{WR}$ x $\overline{CS}$	t_{WD}	10		ns
$\overline{WR}$ control interval	t_{WI}	70		ns

8.7.2 Serial Microprocessor Interface Timing

The following 2 figures describe the read/write cycles and the corresponding address timing for the serial microprocessor interface:

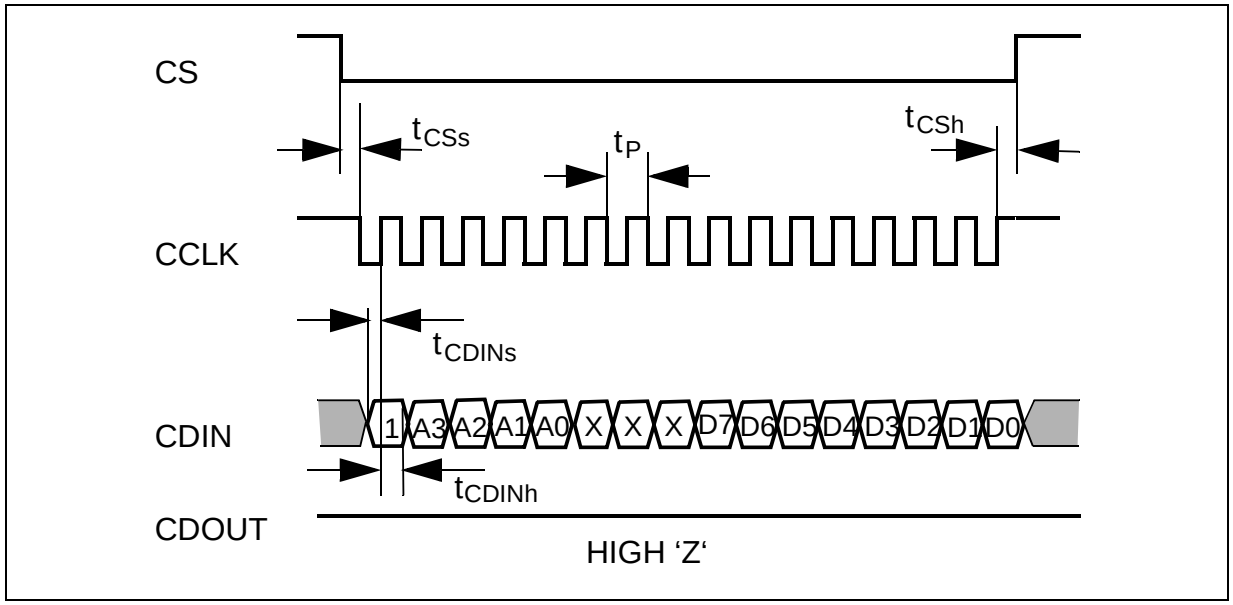


Figure 111 Serial µP Interface Mode Write

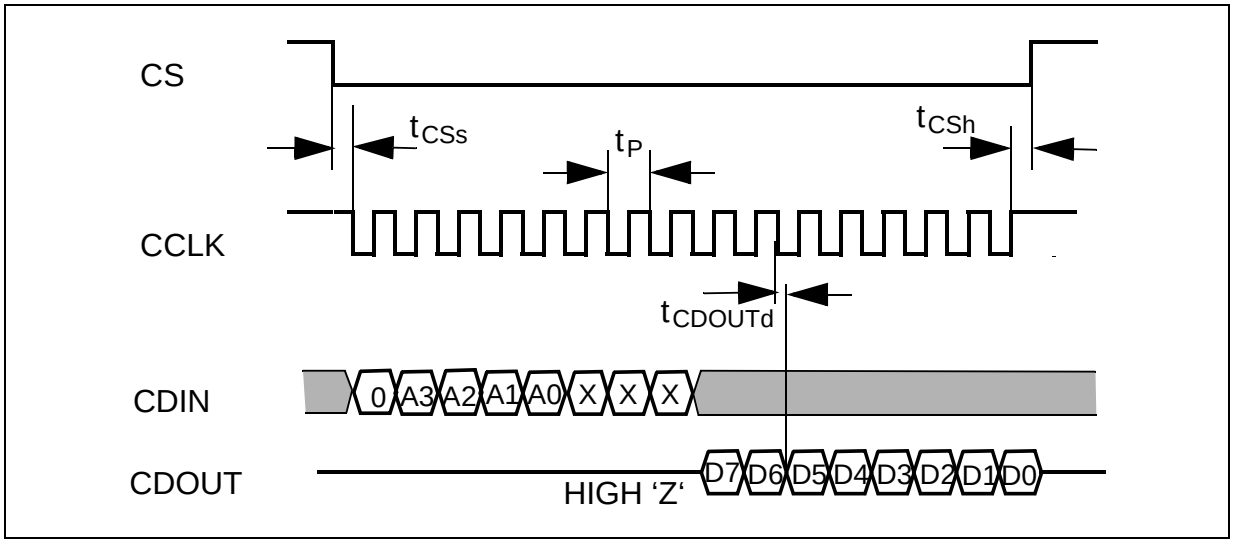


Figure 112 Serial µP Interface Mode Read

Table 50 Timing Characteristics (serial µP interface mode)

C_{Load} = 50pF

Parameter	Symbol	min.	max.	unit
Clock period	t_P	130		ns
Chip Select setup time	t_{CSs}	0		ns
Chip Select hold time	t_{CSh}	20		ns
CDIN setup time	t_{CDINs}	40		ns
CDIN hold time	t_{CDINh}	40		ns
CDOUT data out delay	t_{CDOUTd}		30	ns

8.7.3 IOM®-2 Interface Timing

Note 79: In case the period of signals is stated the time reference will be at 1.4 V; in all other cases 0.8 V (low) and 2.0 V (high) thresholds are used as reference.

Via the IOM®-2-interface data is transmitted in both directions (DU and DD) at half the data clock rate. The data clock (DCL) is a square wave signal with a duty cycle ratio of typically 1:1. Incoming data is sampled on the falling edge of the DCL-clock.

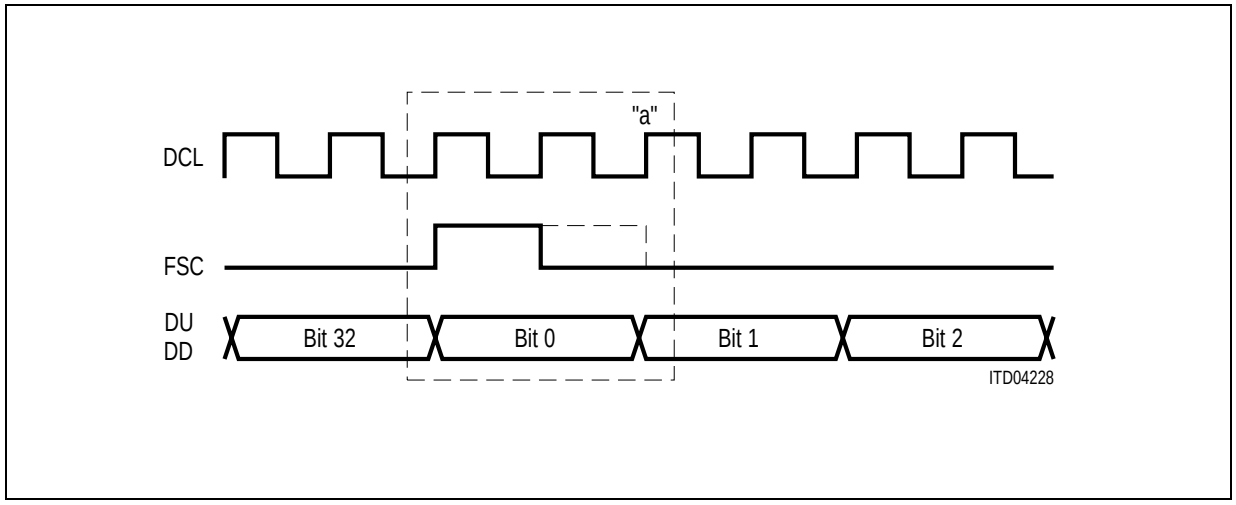


Figure 113 IOM®-2 Interface Timing

The dynamic characteristics of the IOM®-2-interface is given in the following Figure 114 where Detail "a" of Figure 113 is shown in more detail.

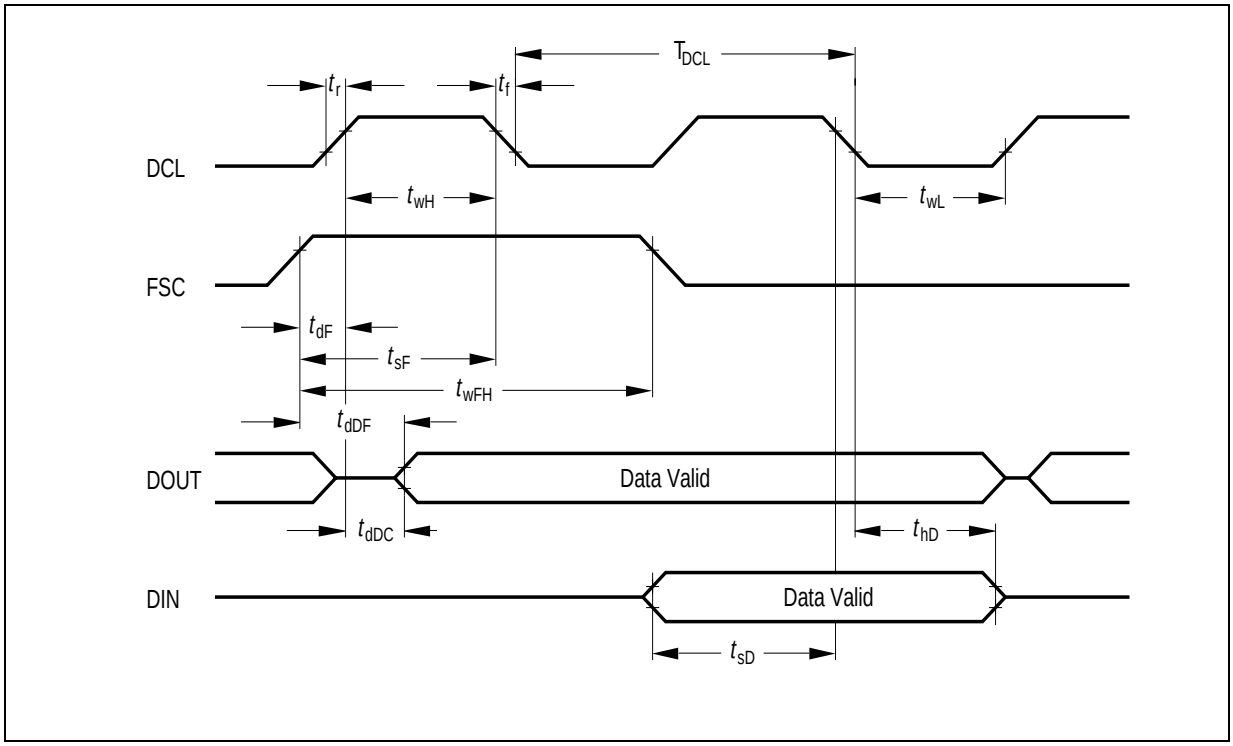


Figure 114 IOM®-2 Timing of IOM®-2 Interface (Detail)

Table 51 IOM®-2 Dynamic Input Characteristics

Parameter	Signal	Symbol	Limit Values		Unit
			min.	max.	
Data clock rise/fall	DCL	t_R, t_F		60	ns
Clock period		T_{DCL}	200		ns
Pulse width high/low		t_{wH} t_{wL}	53 53		ns ns
Frame synch. rise/fall	FSC	t_R, t_F		60	ns
Frame setup		t_{sF}	30		ns
Frame hold		t_{dF}		t_{wL} – 30	ns
Frame width high/low[1)]		t_{wFH} t_{wFL}	100 $2 \times T_{DCL}$		ns
Data sample delay	DIN	t_{sD}	t_{wH} + 20		ns
Data hold		t_{hD}	50		ns

1) This is in according to the IOM®-2-timing specification. For correct functional operation the high period must be $1 \times T_{DCL}$ for superframe markers and at least $2 \times T_{DCL}$ for non-superframe markers

Table 52 IOM®-2 Dynamic Output Characteristics

Parameter	Signal	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Data clock rise/fall	DCL	t_R, t_F			30	ns	C_L = 25 pF
Clock period[1]		T_{DCL}	1875	1953	2035	ns	C_L = 25 pF
Pulse width[1] high/low		t_{wH} t_{wL}	850	960	1105	ns	
Clock period[2]		T_{DCL}	565	651	735	ns	C_L = 25 pF
Pulse width[2] high/low		t_{wH} t_{wL}	200	310	420	ns	
Frame width high[3]	FSC	t_{wFH}		T_{DCL}			C_L = 25 pF
Frame width high[4]	FSC	t_{wFH}		$2 \times T_{DCL}$			C_L = 25 pF
Frame synch. rise/fall		t_R, t_F			30	ns	C_L = 25 pF
Frame advance		t_{dF}	0	65	130	ns	C_L = 25 pF
Data out	DOUT	t_F			200	ns	C_L = 150 pF (R = 1 kΩ to V_{DD}, DOD pin high) or RESQ pin low
Data out		t_R, t_F			150	ns	C_L = 150 pF DOD pin low RESQ pin high
Data delay clock[5]		t_{dDC}			100	ns	C_L = 150 pF
Data delay frame[5]		t_{dDF}			150	ns	C_L = 150 pF

1) 256 kbit/s

2) 768 kbit/s

3) FSC marking superframe

4) FSC marking non-superframe

5) The point of time at which the output data will be valid is referred to the rising edges of either FSC (t_{dDF}) or DCL (t_{dDC}). The rising edge of the signal appearing last (normally DCL) shall be the reference

8.7.4 Power Controller Interface Timing

Note 80: This section is only applicable to the stand-alone mode.

Note 81: In case the period of signals is stated the time reference will be at 1.4 V; in all other cases 0.8 V (low) and 2.0 V (high) thresholds are used as reference.

For pin definition, see "Power Controller Pins", page 36.

8.7.4.1 Data Port

Figures 115 and 116 depict the timing for read and write operations.

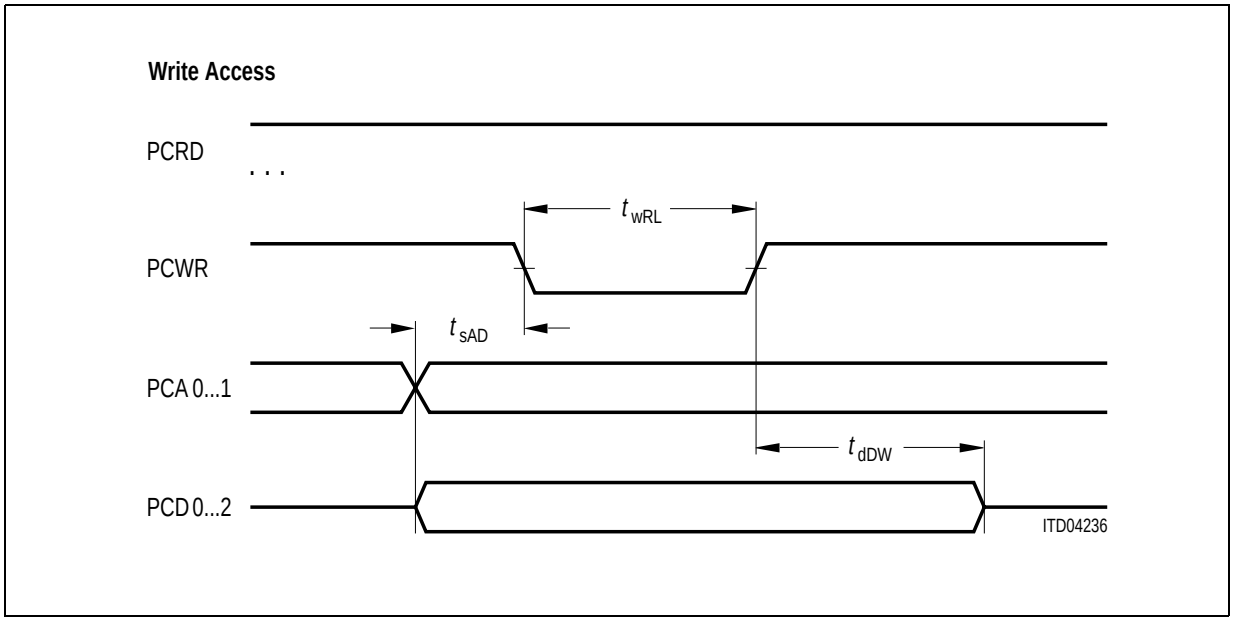


Figure 115 Dynamic Characteristics of Power Controller Write Access

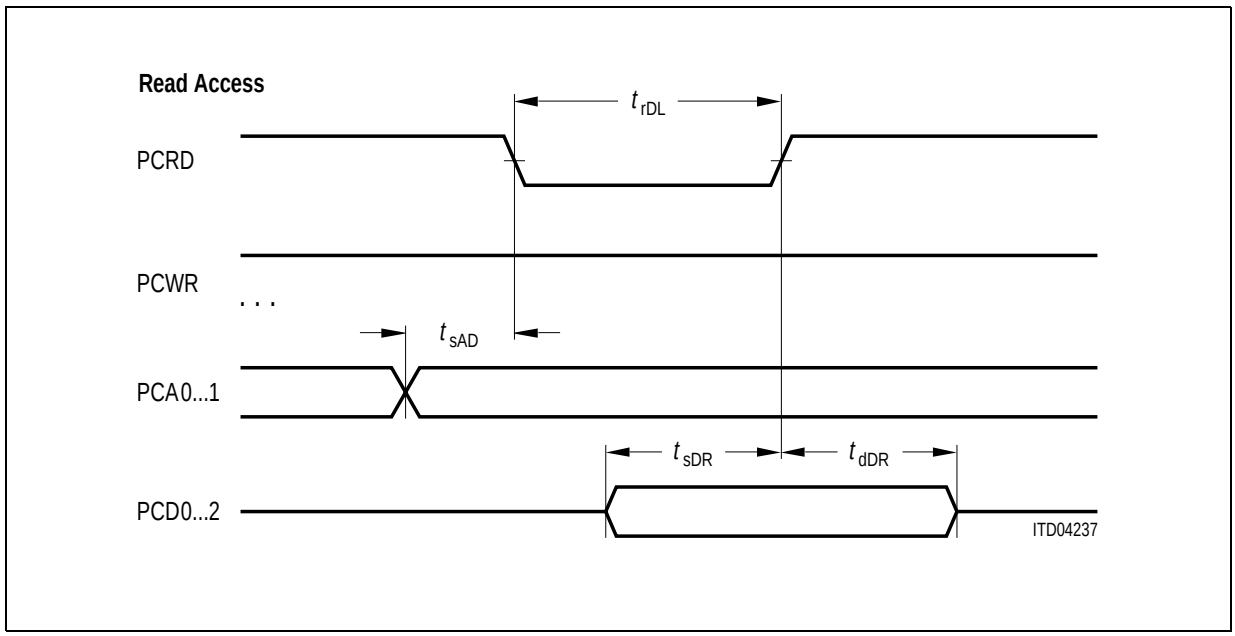


Figure 116 Dynamic Characteristics of Power Controller Read Access

Table 53 Power Controller Interface Dynamic Characteristics

C_{Load} = 25pF

Parameter	Signal	Symbol	Limit Values			Unit
			min.	typ.	max.	
Write clock rise/fall	PCWR	t_R, t_F			30	ns
Write with low		t_{wRL}		$4 \times T_{DCL}$		ns
Address set-up	PCA0 … 1	t_{sAD}		$2 \times T_{DCL}$		ns
Data delay write	PCD0 … 2	t_{dDW}		$2 \times T_{DCL}$		ns
Data delay read		t_{dDR}	130			ns
Set-up data read		t_{sDR}	130			ns
Read clock rise/fall	PCRD	t_R, t_F			30	ns
Read width		t_{rDL}		$4 \times T_{DCL}$		ns

8.7.4.2 Interrupt

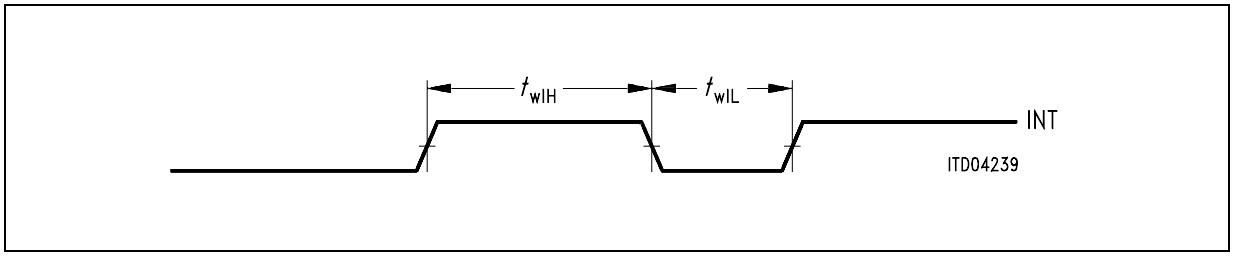


Figure 117 Dynamic Characteristics of Interrupt

Table 54 Dynamic Characteristics of Interrupt

Parameter	Signal	Symbol	Limit Values			Unit
			min.	typ.	max.	
Interrupt length	INT	t_{rDL}	$4 \times t_{FSC}$			
Interrupt width high		t_{wIH}	0.5			ms
Interrupt width low		t_{wIL}	0.5			ms

8.7.5 Undervoltage Detection Timing

The timing of the undervoltage detection function is given below.

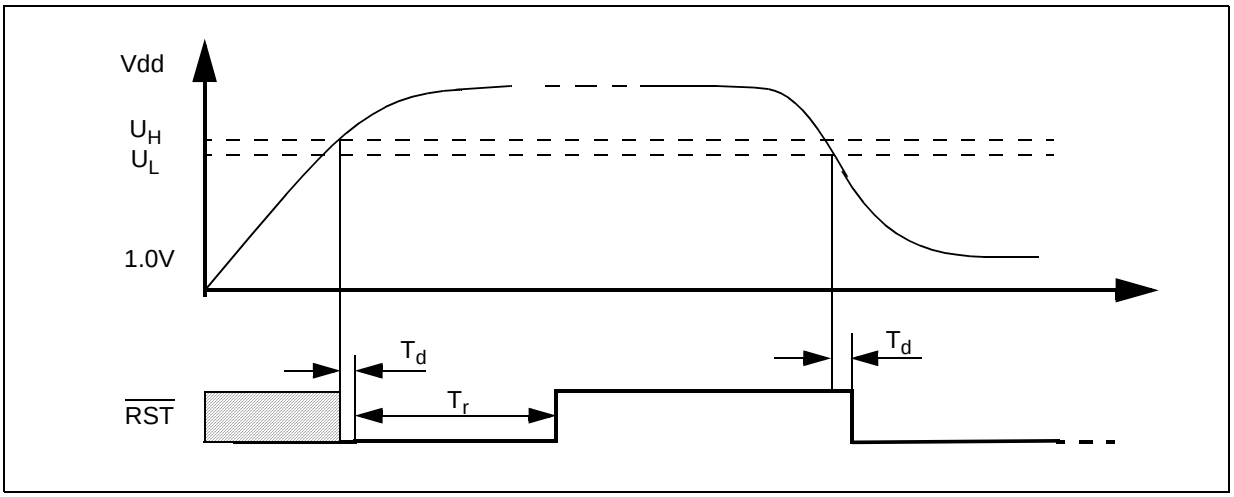


Figure 118 UVD Timing Characteristics

Table 55 Timing Parameters of UVD Function

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Upper threshold voltage	U_H	4.1	4.3	4.5	V
Lower threshold voltage	U_L	U_H -0.11	U_H -0.085	U_H -0.05	V
Length of reset pulse	T_r [1)]	67			ms
Delay of the reset generation after the threshold voltage has been passed	T_d	0	10	20	µs
Slope of the rise and fall time of VDD at every point of time	dV/dt	0		10^4	V/s

1) Note that this specification holds only if stability of the 15.36 MHz clock is guaranteed. During power-up, the reset pulse may therefor vary slightly from the value mentioned above due to instability of the oscillator during start up

8.7.6 Master Clock

8.7.6.1 LT Modes

In LT modes (except COT-512/1536 mode) all timing signals are derived from a system clock via an external phase locked loop. The clock specifications for these modes are described below.

For the LT modes COT-512 and COT-1536 the requirements as specified in section “NT Modes” on page 283 (NT modes) apply.

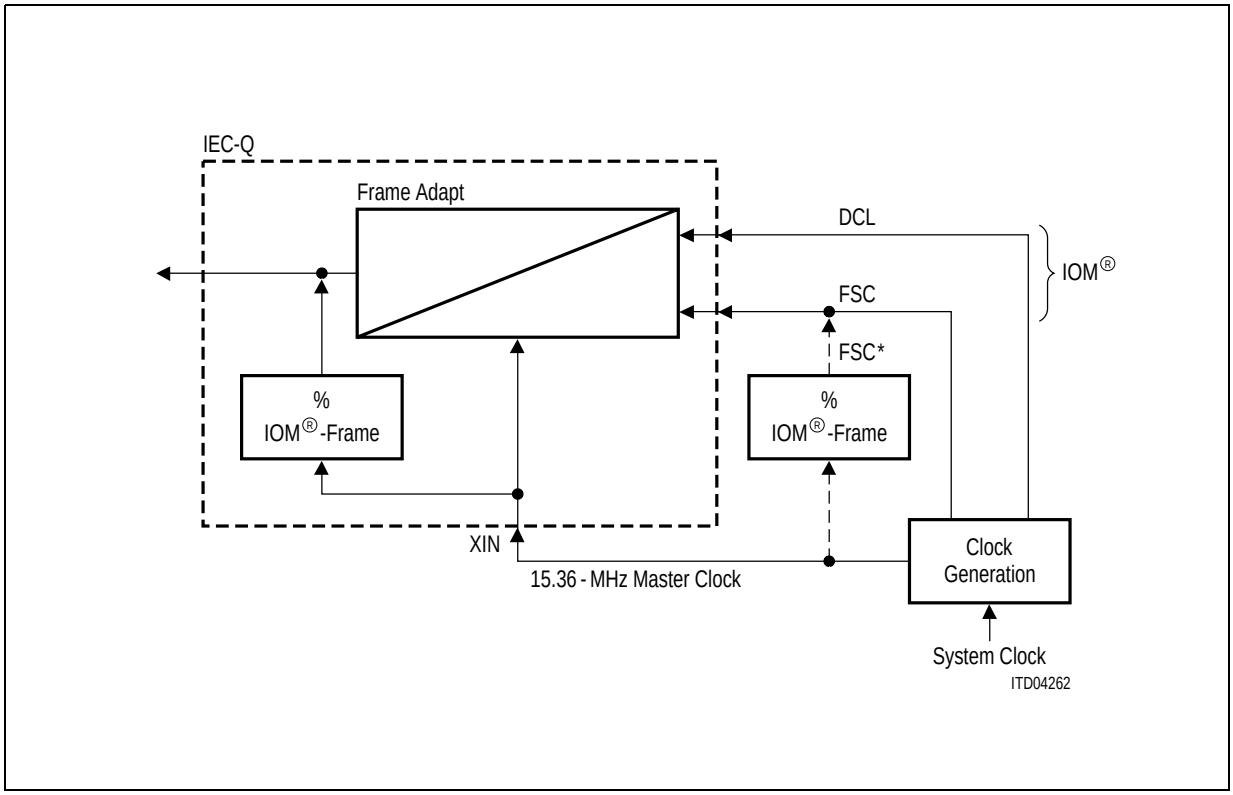


Figure 119 Clock Requirements in LT Modes

*Note 82: FSC*Fictitious FSC indicates ideal FSC-clock (existing master clock divided by 1920 without delay).*
FSCReal FSC (contains phase shift resulting from propagation delays in divider).

Master Clock

– Nominal Frequency15.36 MHz
– Jitter (peak-to-peak) see Figure 121, page 282
– Max. phase deviation between FSC and fictitious FSC*± 18 µs
– Duty ratio see Figure 120, page 282

Table 56 Duty Ratio

Parameter	Limit Values		Unit
	min.	max.	
t_H	26	39	ns
t_L	26	39	ns
t_R, t_F	0	13	ns

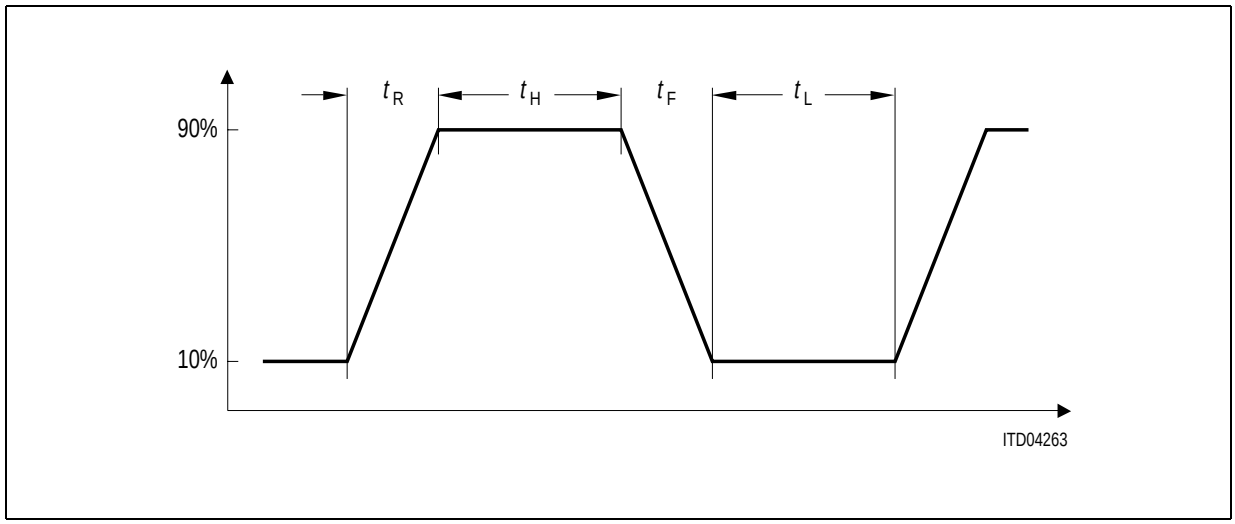


Figure 120 Dynamic Characteristics of the Duty Cycle

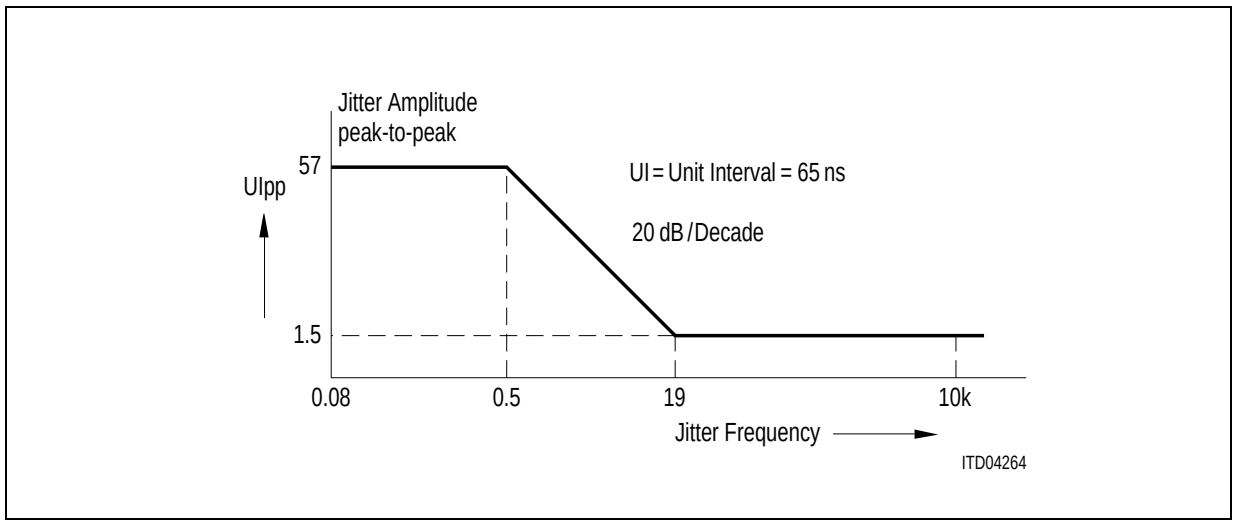


Figure 121 Maximum Sinusoidal Input Jitter of Master Clock 15.36 MHz

8.7.6.2 NT Modes

This section specifies the requirements of the master clock in all NT and TE modes as well as in COT-512/1536 modes. The master clock is derived from a built-in crystal oscillator. The crystal is connected to the pins XIN and XOUT. The maximum capacitive load at XIN is 40 pF each.

For information about the crystal refer to "Oscillator Circuit and Crystal", page 252.

Master Clock

Nominal frequency15.36 MHz
Overall tolerance between LT master clock and NT master clock± 100 ppm

Max. phase deviation between FSC and fictitious FSC* (NT-PBX mode only) : ± 18 µs

NT-PBX Mode

In NT-PBX mode the IEC-Q uses an internal data buffer to compensate for phase deviations between IOM®-2-interface and U-interface clocks. This becomes necessary because in NT-PBX mode the device is slave with respect to both interfaces.

A phase deviation of up to ± 18 µs can be compensated by the IEC-Q. To achieve this a 64 bit wide buffer for user data is implemented in each direction (IOM®-2 → U and U → IOM®-2).

If the phase deviation becomes too large for the buffer to compensate, the phase relation will be redetermined. This involves the loss of data because a frame jump occurs. Each frame jump will be indicated in the C/I Channel of the IOM®-2-interface with the indication "FJ" (0010_B).

Note 83: The "FJ" indication will only be issued after a frame jump occurred (independently of the actual phase deviation which led to the frame jump). This indication can therefore not be used as a warning which will be issued when ± 18 µs phase deviation is reached.

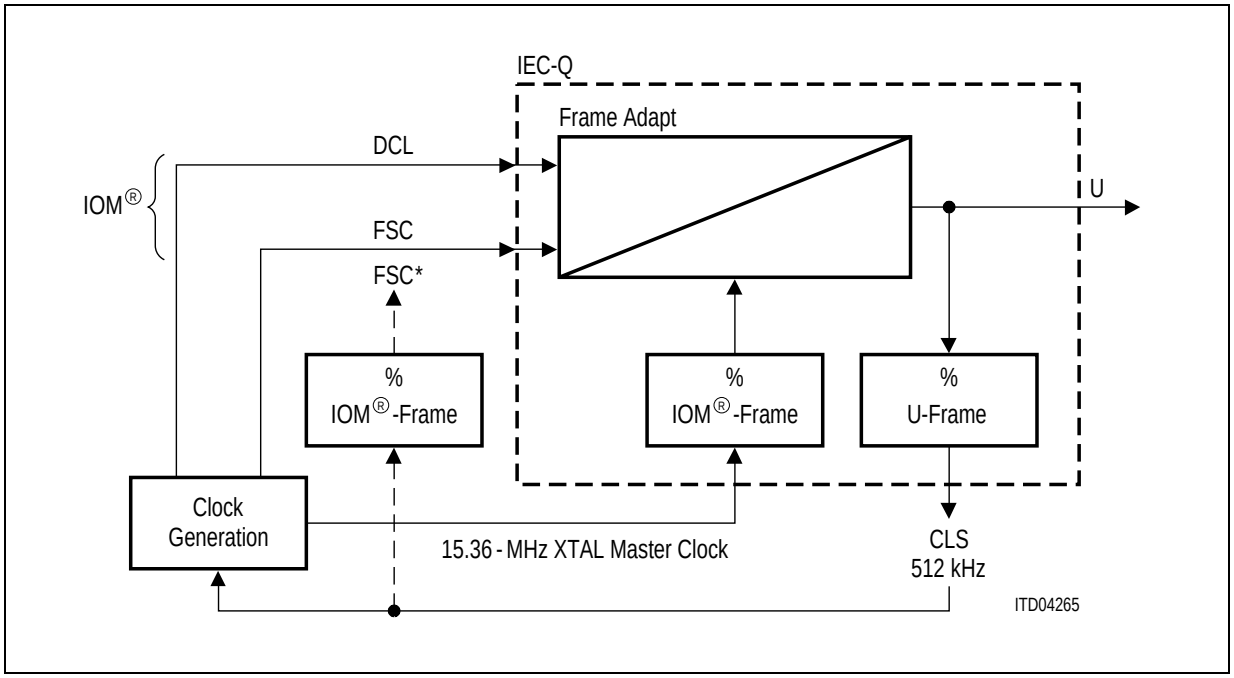


Figure 122 Clock Requirements in NT-PBX

8.7.7 Timing Properties of CLS

Note 84: In case the period of signals is stated the time reference will be at 1.4 V; in all other cases 0.8 V (low) and 2.0 V (high) thresholds are used as reference.

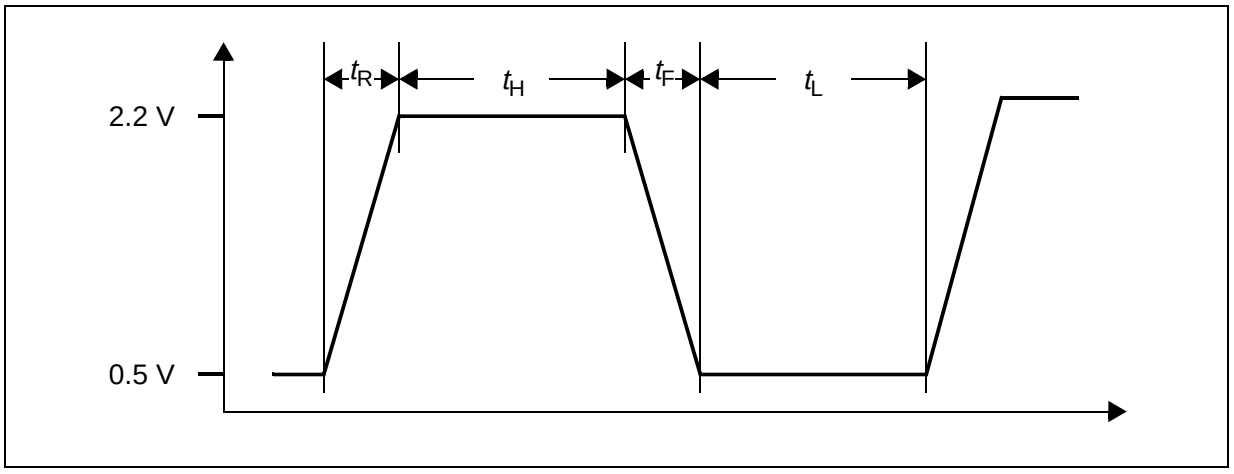


Figure 123 Dynamic Characteristics of CLS[1)]

1) Applies only with a crystal which has the properties given in "Oscillator Circuit and Crystal", page 252

Table 57 Output Characteristics of CLS in NT-RP Mode

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Pulse width high, low	t_H, t_L	26	39	ns	C_{Load} = 20pF
Rise time, fall time	t_R, t_F	0	13	ns	C_{Load} = 20pF

Table 58 Output Characteristics of CLS in NT-PBX and LT-RP Modes

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Pulse width high, low	t_H, t_L	850	960	ns	C_{Load} = 10pF
Rise time, fall time	t_R, t_F	0	30	ns	C_{Load} = 10pF

Table 59 Output Characteristics of CLS in all other Modes[1)]

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Pulse width high, low	t_H, t_L	40	90	ns	C_{Load} = 10pF
Rise time, fall time	t_R, t_F	0	25	ns	C_{Load} = 10pF

1) Except LT mode. Note that CLS is not defined in LT mode

8.7.8 Timing Properties of Pin SG in TE Mode

C_{Load} = 25pF

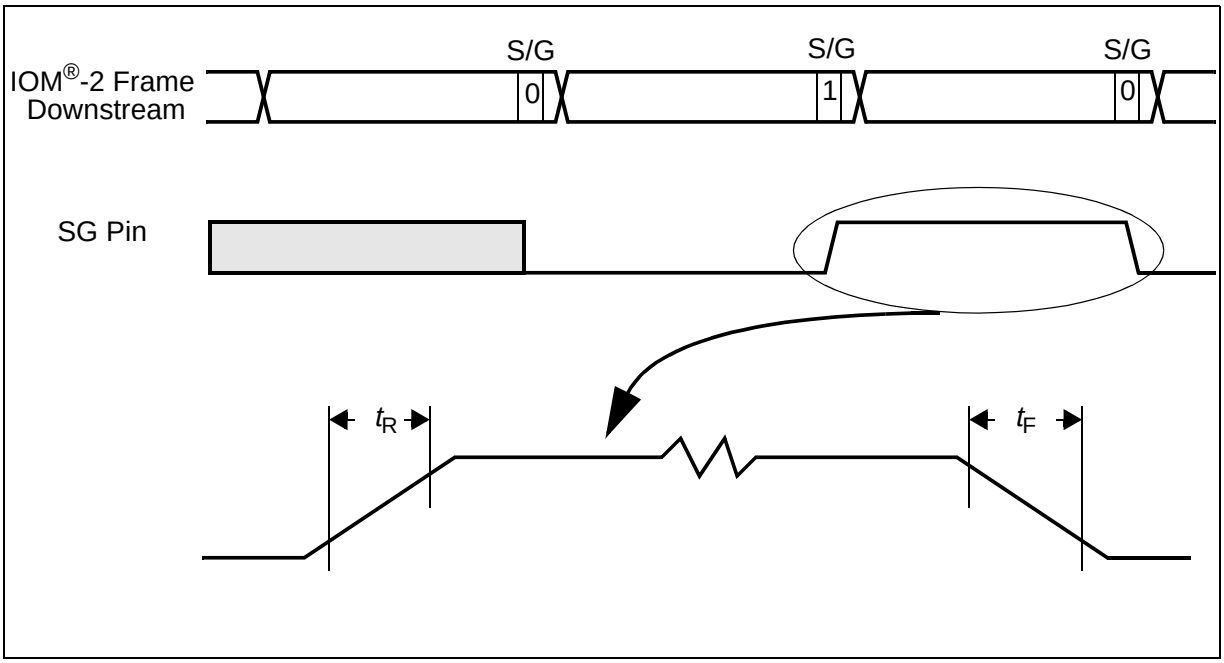


Figure 124 Dynamic Characteristics of Pin SG

Table 60 Output Characteristics of Pin S/G

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Rise time, fall time	$t_{R,}t_F$	0	30	ns

9 Package Outlines

Plastic Package, P-LCC-44
(Metric Quad Flat Package)

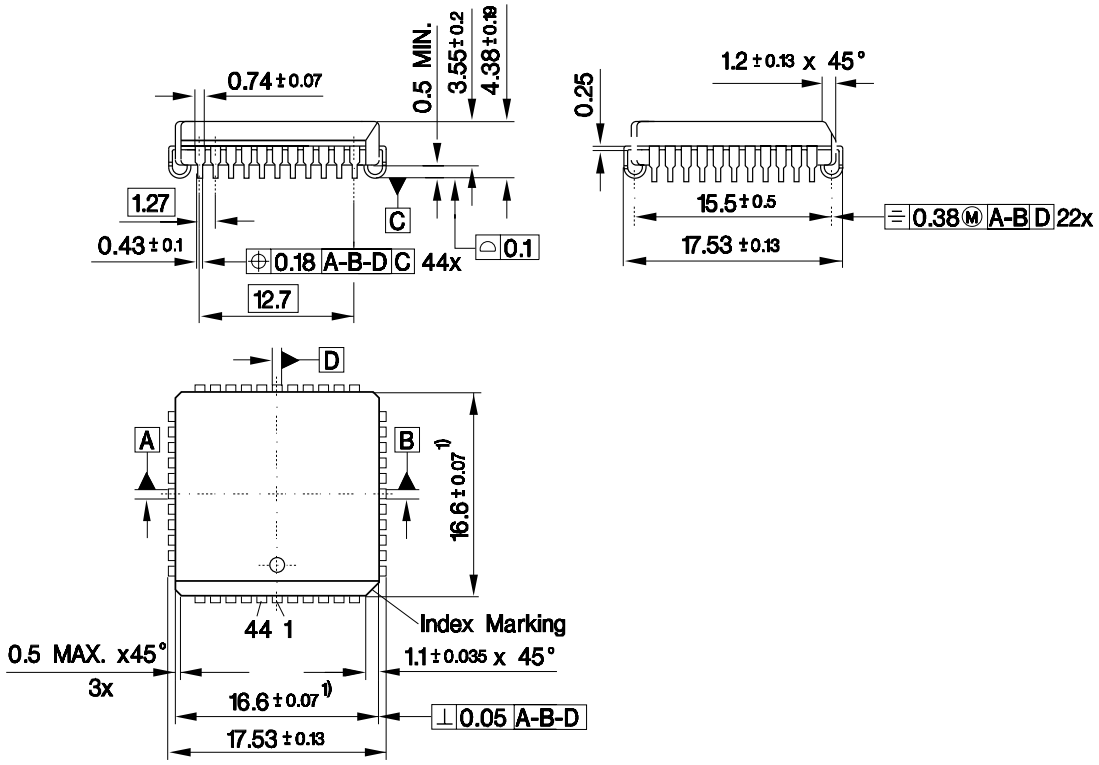


Figure 125 Package Outline for P-LCC-44

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book 'Package Information'.

SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, M-QFP-64
(Metric Quad Flat Package)

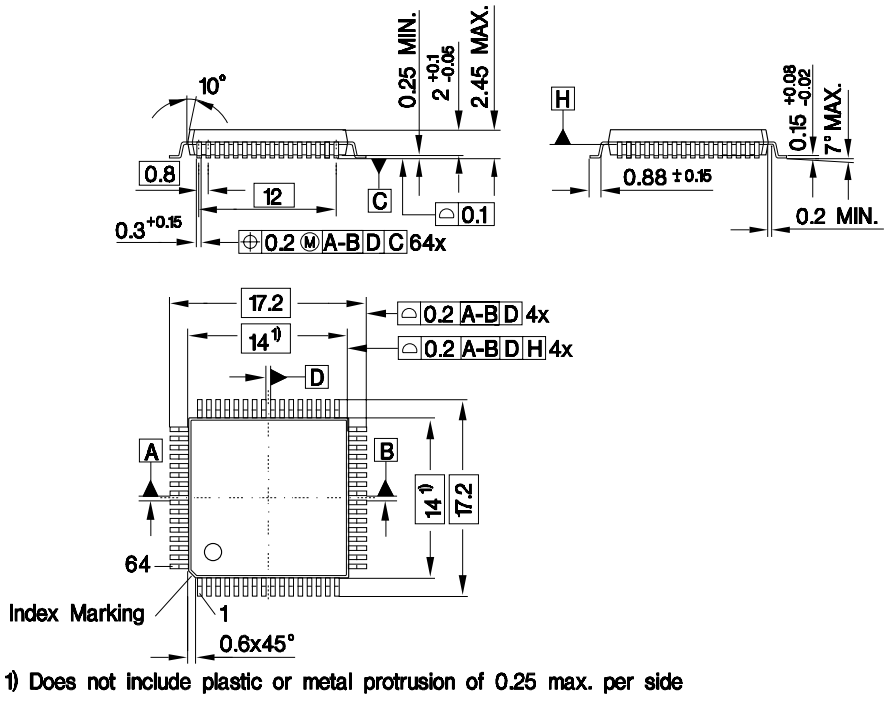


Figure 126 Package Outline for M-QFP-64

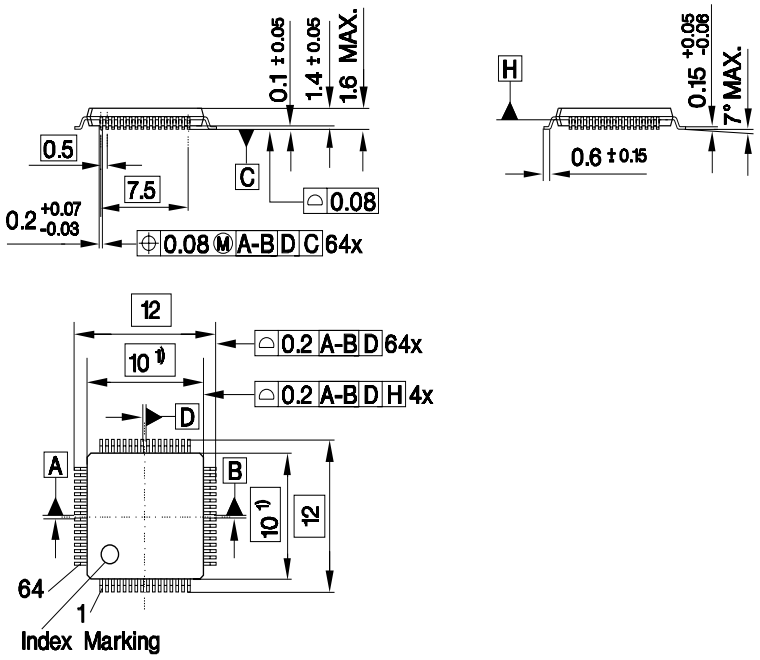
Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book 'Package Information'.

SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, T-QFP-64
(Thin Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Figure 127 Package Outline for T-QFP-64

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book 'Package Information'.

SMD = Surface Mounted Device

Dimensions in mm

10 Glossary

A/D	Analog-to digital
ADC	Analog-to digital converter
AGC	Automatic gain control
AIN	Differential U-interface input
ANSI	American National Standardization Institute
ARCOFI	Audio ringing codec filter
AOUT	Differential U-interface output
B	64-kbit/s voice and data transmission channel
BCL	Bit clock
BIN	Differential U-interface input
BOUT	Differential U-interface output
C/I	Command/Indicate (channel)
CCRC	Corrupted CRC
CRC	Cyclic redundancy check
D	16-kbit/s data and control transmission channel
D/A	Digital-to-analog
DAC	Digital-to-analog converter
DCL	Data clock
DD	Data downstream
DT	Data through test mode
DU	Data upstream
EC	Echo canceller
EOC	Embedded operations channel
EOM	End of message
ETSI	European Telephone Standards Institute
FEBE	Far-end block error
FIFO	First-in first-out (memory)
FSC	Frame synchronizing clock
GND	Ground
HDLC	High-level data link control
ICC	ISDN-communications controller
IEC-Q	ISDN-echo cancellation circuit conforming to 2B1Q-transmission code
IOM®-2	ISDN-oriented modular 2nd generation
INFO	U- and S-interface signal as specified by ANSI/ETSI
ISDN	Integrated services digital network
ISW	Inverted synchronization word
LB	Loop back
LBBD	Loop-back of B- and D-channels
LSB	Least significant bit
LT	Line termination
MON	Monitor channel command

MSB	Most significant bit
MR	Monitor read bit
MTO	Monitor procedure time-out
MX	Monitor transmit bit
NCC	Notify of corrupt CRC
NEBE	Near-end block error
NT	Network termination
OSI	Open systems interconnection
PLL	Phase locked loop
POR	Power-On Reset
PS	Power supply status bit
PSD	Power spectral density
PTT	Post, telephone, and telegraph administration
PU	Power-up
RCC	Request corrupt CRC
RCI	Read Power Controller Interface
RMS	Root mean square
RP	Repeater
S/T	Two-wire pair interface
SBCX	S/T-bus interface circuit extended
SICOFI	Signal processing codec filter
SLIC	Subscriber line interface circuit
SSP	Send single pulses (test mode)
ST	Self test
SW	Synchronization word
TE	Terminal equipment
TL	Wake-up tone, LT side
TN	Wake-up tone, NT side
TP	Test pin
U	Single wire pair interface
UTC	Unable to comply
UVD	Undervoltage Detection
2B1Q	Transmission code requiring 80-kHz bandwidth

11 Index

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Appendix A Basic Standards

The following table gives a list of the most important standards related to the IEC-Q.

Organization		Valid for	Document	
ITU	International Telecommunication Union	World-wide	ITU-T G.961	Digital Transmission System on Metallic Line for ISDN Basic Rate Access
ETSI	European Telecommunications Standards Institute	EU	"ETSI Technical Report 080" (ETR080), Nov. 1996 **New name (1999)** "Technical Specification 101080" (TS 101080)	Transmission and Multiplexing; ISDN Basic Rate Access; Digital Transmission Systems on Metallic Local Lines
ANSI	American National Standards Institute, Inc.	USA	T1E1 4/92-004 - T1.601-1992	Basic Access Interface for Use on Metallic Loops for Application on the Network Side of the NT (Layer 1 Specification)
Bellcore		USA	TR-NWT-000393, Issue 2, December 1992	Generic Requirements for ISDN Basic Access Digital Subscriber Lines
			TR-NWT-000397, Issue 3, December 1993	ISDN Basic Access Transport System Requirements
			TR-NWT-000829, Issue 1, November 1989	OTGR: Generic Operations Interface, Embedded Operations Channel
			SR-NWT-002397, Issue 1, June 1993	Layer 1 Test Plan for ISDN Basic Access Digital Subscriber Line Transceivers
BT	British Telecommunications plc.	GB	Specification RC7355E, Issue E, 03/97	2B1Q Generic Physical Layer Specification

Appendix B Comment on Activation in µP-NT Modes

Erroneous Signals on U-Interface after Power-Up in NT Mode with Enabled Microprocessor Interface Mode

This point applies only if the IEC-Q is used in NT mode and if the microprocessor interface mode is enabled by pin PMODE set to "1". The stand-alone mode is not affected.

After applying V_{DD} (power-on) the device enters the LT mode according to the default value $C4_H$ in the STCR register (see "STCR-Register", page 212). In applications where no IOM®-2 clocks are provided to the PEB/F 2091 Version 5.1 this results in an undefined state of the IEC-Q. The undefined state may cause unwanted signals on the U-interface. It is left once the device is brought into the NT or TE mode by programming the STCR register. Thus, for the time between applying V_{DD} and programming the STCR register, unwanted signals may be sent on the U-interface.

In the PSB/F 21911 IEC-Q TE the default value of the STCR register has been changed to "04H". Thus "unwanted" signals won't be sent on the U-interface any longer.