

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

65,536-WORD BY 16-BIT CMOS STATIC RAM

DESCRIPTION

The TC551664BJ/BFT is a 1,048,576-bit high-speed static random access memory (SRAM) organized as 65,536 words by 16 bits. Fabricated using CMOS technology and advanced circuit techniques to provide high speed, it operates from a single 5 V power supply. Chip enable (\overline{CE}) can be used to place the device in a low-power mode, and output enable (\overline{OE}) provides fast memory access. Data byte control signals (\overline{LB} , \overline{UB}) provide lower and upper byte access. This device is well suited to cache memory applications where high-speed access and high-speed storage are required. All inputs and outputs are directly TTL compatible. The TC551664BJ/BFT is available in a plastic 44-pin SOJ (400 mil width) and TSOP packages for high density surface assembly.

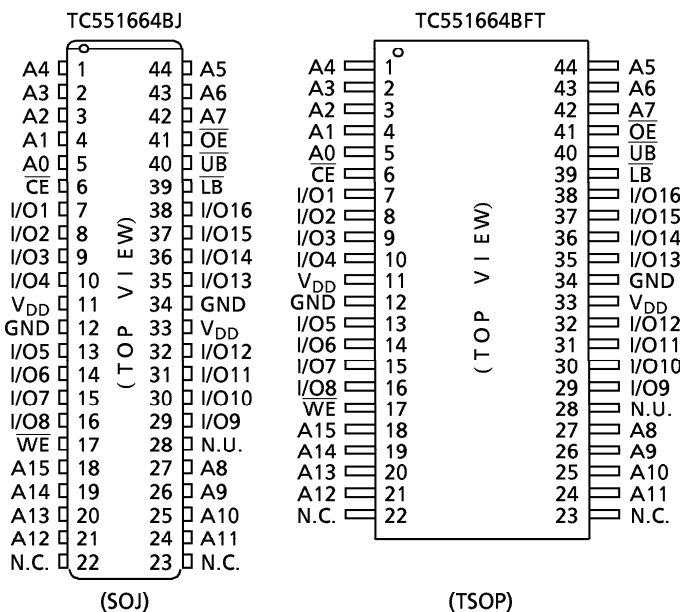
FEATURES

- Fast access time (the following are maximum values)
 - TC551664AJ-12: 12 ns
 - TC551664AJ-15: 15 ns
- Low-power dissipation (the following are maximum values)
- Single power supply voltage of 5 V \pm 10%
- Fully static operation
- All inputs and outputs are TTL compatible
- Output buffer control using \overline{OE}
- Data byte control using \overline{LB} (IO1 to IO8) and \overline{UB} (IO9 to IO16)
- Package:
 - SOJ44-P-400-1.27 (BJ) (Weight: 1.64 g typ)
 - TSOP II 44-P-400-0.80 (BFT) (Weight: 0.45 g typ)

Cycle Time	12	15	20	25	30	ns
Operation (max)	290	260	220	200	180	mA

Standby: 1 mA (both devices)

PIN ASSIGNMENT



PIN NAMES

A0 to A15	Address Inputs
I/O1 to I/O16	Data Inputs/Outputs
\overline{CE}	Chip Enable
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable
\overline{LB} , \overline{UB}	Data Byte Control Input
V_{DD}	Power (+ 5 V)
GND	Ground
NC	No Connection
NU	Not Used (Input)

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DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	-	V _{DD} + 0.5	V
V _{IL}	Input Low Voltage	- 0.5 *	-	0.8	V

*: - 3 V with a pulse width of 10 ns

DC CHARACTERISTICS (Ta = 0° to 70°C, V_{DD} = 5 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
I _{IL}	Input Leakage Current (Except NU Pin)	V _{IN} = 0 V to V _{DD}	-	-	± 10	μA	
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ V _{OUT} = 0 V to V _{DD}	-	-	± 10	μA	
I _{I(NU)}	Input Current (NU Pin)	V _{IN} = 0 to 0.8 V	- 1	-	20	μA	
I _{OH}	Output High Current	V _{OH} = 2.4 V	- 4	-	-	mA	
I _{OL}	Output Low Current	V _{OL} = 0.4 V	8	-	-	mA	
I _{DDO}	Operating Current	$\overline{CE} = V_{IL}$, I _{out} = 0 mA Other Inputs = V _{IH} or V _{IL}	tcycle = 12 ns	-	-	290	mA
			tcycle = 15 ns	-	-	260	
			tcycle = 20 ns	-	-	220	
			tcycle = 25 ns	-	-	200	
			tcycle = 30 ns	-	-	180	
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$, Other Inputs = V _{IH} or V _{IL}	-	-	30	mA	
I _{DDS2}		$\overline{CE} = V_{DD} - 0.2 V$ Other Inputs = V _{DD} - 0.2 V or 0.2 V	-	-	1		

CAPACITANCE (Ta = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	6	pF
C _{I/O}	Input/Output Capacitance	V _{I/O} = GND	8	pF

Note: This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

MODE	\overline{CE}	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O1 to I/O8	I/O9 to I/O16	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	x	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Outputs Disable	L	H	H	x	x	High Impedance	High Impedance	I_{DDO}
	L	x	x	H	H			
Standby	H	x	x	x	x	High Impedance	High Impedance	I_{DDS}

X: Don't care

Note: The NU pin must be left unconnected or tied to GND or a voltage level of less than 0.8 V.
 You must not apply a voltage of more than 0.8 V to the NU.

AC CHARACTERISTICS ($T_a = 0^\circ$ to 70°C (Note 1), $V_{DD} = 5\text{ V} \pm 10\%$)

READ CYCLE

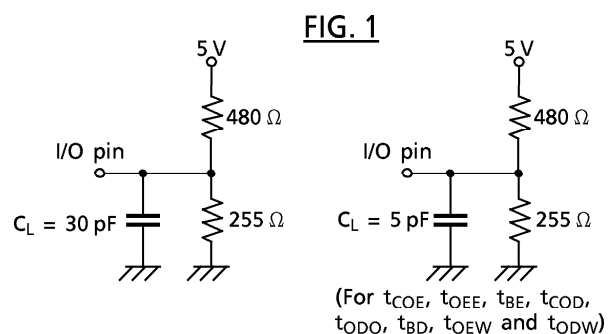
SYMBOL	PARAMETER	TC551664BJ/BFT-12		TC551664BJ/BFT-15		UNIT
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	12	–	15	–	ns
t_{ACC}	Address Access Time	–	12	–	15	
t_{CO}	Chip Enable Access Time	–	12	–	15	
t_{OE}	Output Enable Access Time	–	6	–	8	
t_{BA}	Upper Byte, Lower Byte Access Time	–	6	–	8	
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	
t_{COE}	Output Enable Time from Chip Enable	5	–	5	–	
t_{OEE}	Output Enable Time from Output Enable	1	–	1	–	
t_{BE}	Output Enable Time from Upper Byte, Lower Byte	1	–	1	–	
t_{COD}	Output Disable Time from Chip Enable	–	8	–	8	
t_{ODO}	Output Disable Time from Output Enable	–	8	–	8	
t_{BD}	Output Disable Time from Upper Byte, Lower Byte	–	8	–	8	

WRITE CYCLE

SYMBOL	PARAMETER	TC551664BJ/BFT-12		TC551664BJ/BFT-15		UNIT
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	12	–	15	–	ns
t_{WP}	Write Pulse Width	8	–	9	–	
t_{CW}	Chip Enable to End of Write	10	–	12	–	
t_{BW}	Upper Byte, Lower Byte Enable to End of Write	10	–	12	–	
t_{AW}	Address Valid to End of Write	10	–	12	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{DS}	Data Setup Time	6	–	8	–	
t_{DH}	Data Hold Time	0	–	0	–	
t_{OEW}	Output Enable Time from Write Enable	1	–	1	–	
t_{ODW}	Output Disable Time from Write Enable	–	8	–	8	

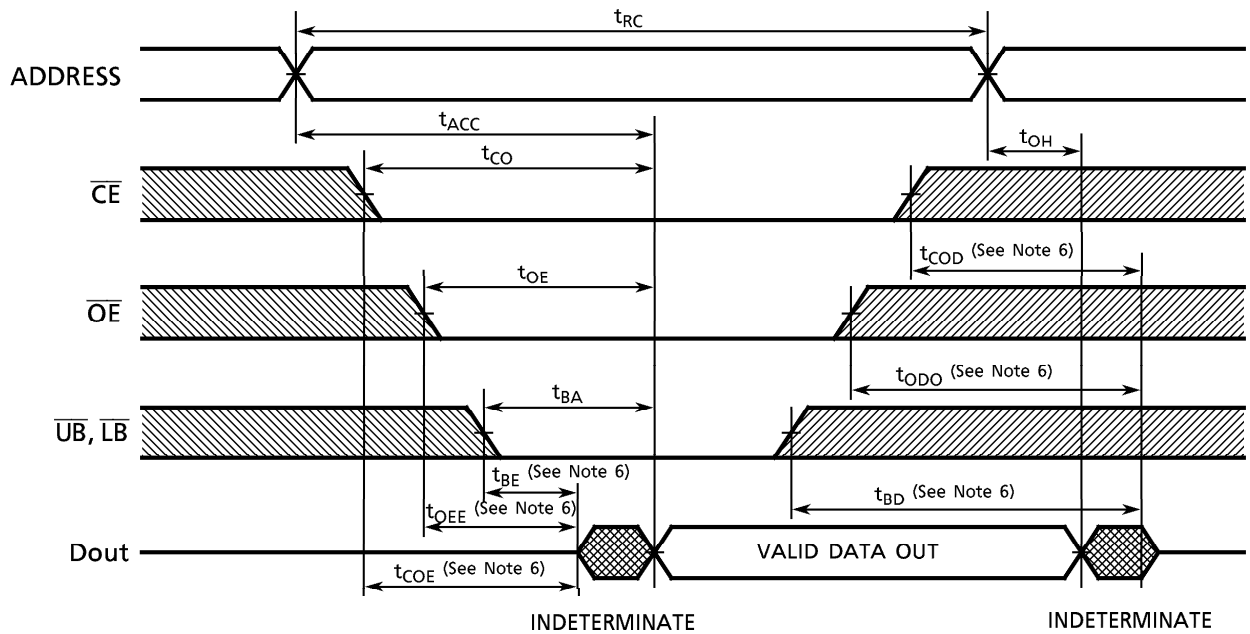
AC TEST CONDITIONS

Input Pulse Level	3.0 V, 0.0 V
Input Pulse Rise and Fall Time	3 ns
Input Timing Measurement Reference Level	1.5 V
Output Timing Measurement Reference Level	1.5 V
Output Load	Fig. 1

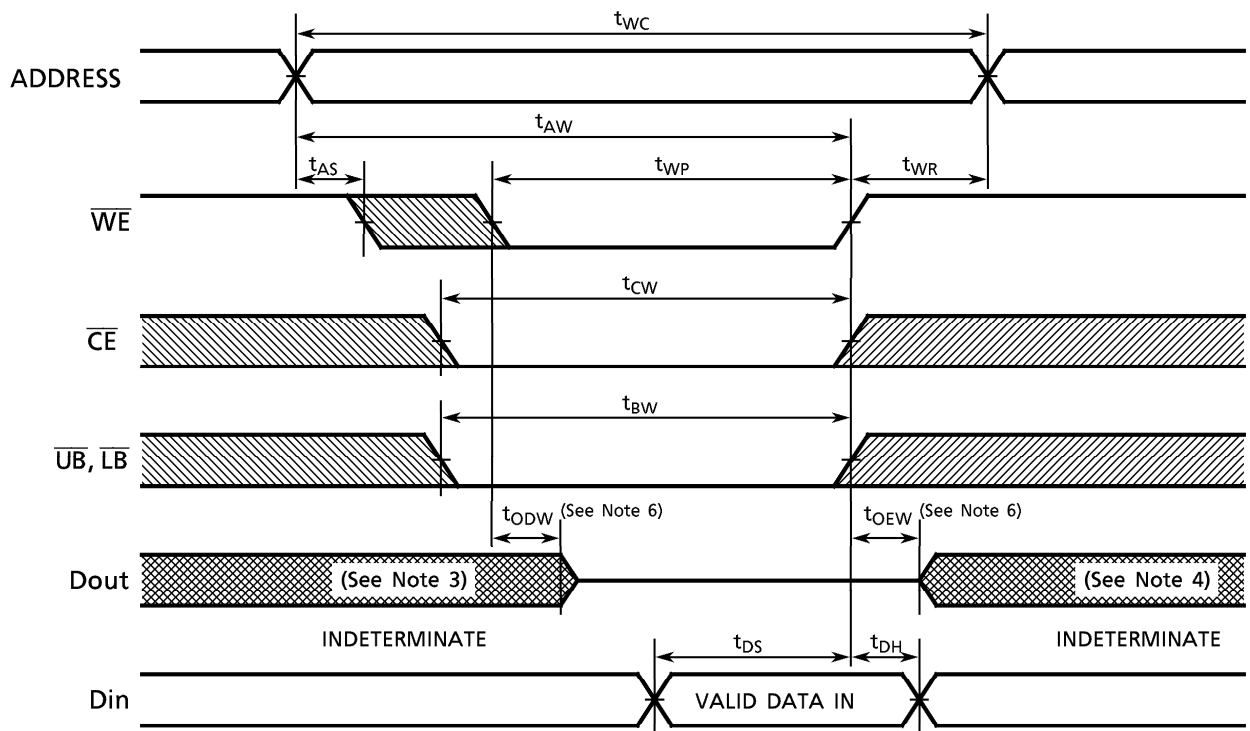


TIMING DIAGRAMS

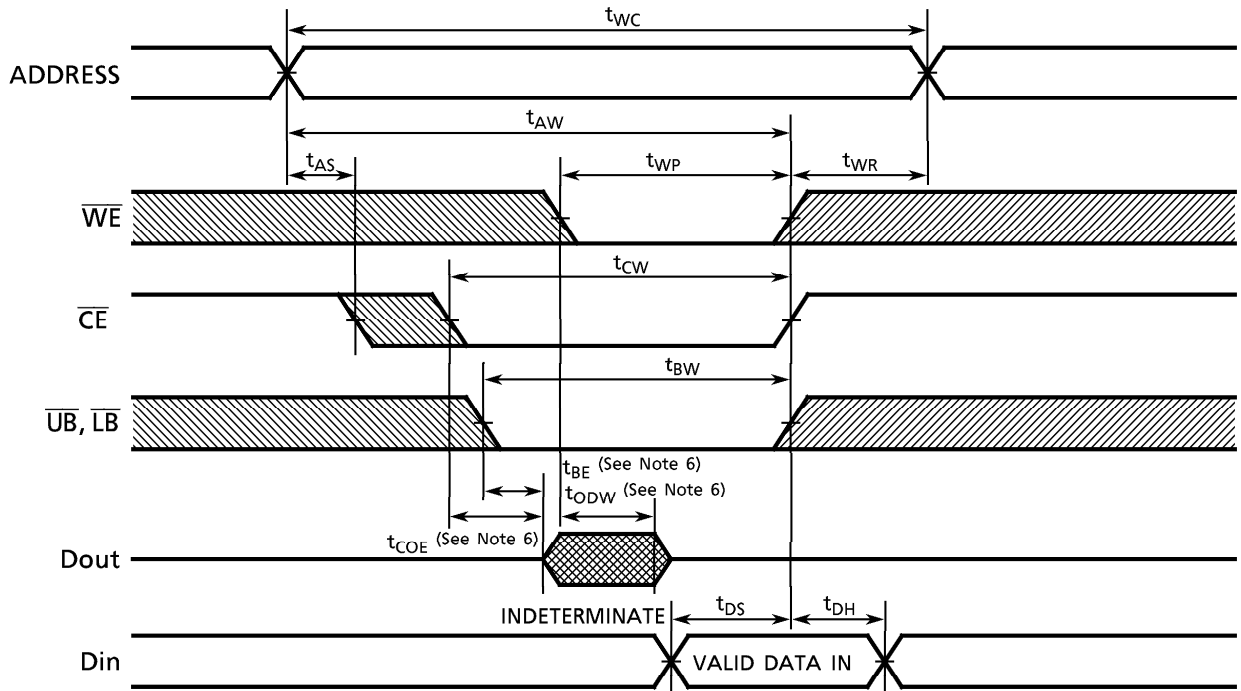
READ CYCLE (See Note 2)



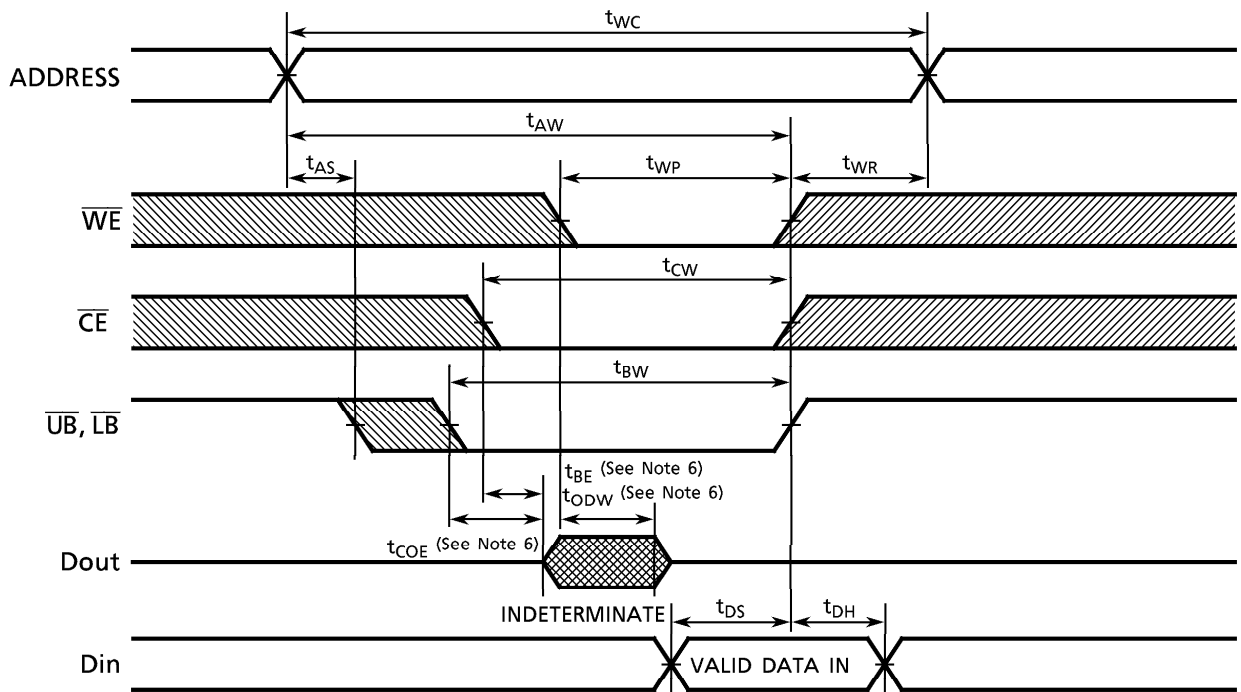
WRITE CYCLE 1 (\overline{WE} CONTROLLED) (See Note 5)



WRITE CYCLE 2 (\overline{CE} CONTROLLED) (See Note 5)



WRITE CYCLE 3 ($\overline{UB}, \overline{LB}$ CONTROLLED) (See Note 5)



Note: (1) Operating temperature (Ta) is guaranteed for transverse air flow exceeding 400 linear feet per minute.

(2) \overline{WE} remains HIGH for the Read Cycle.

(3) If \overline{CE} goes LOW coincident with or after \overline{WE} goes LOW, the outputs will remain at high impedance.

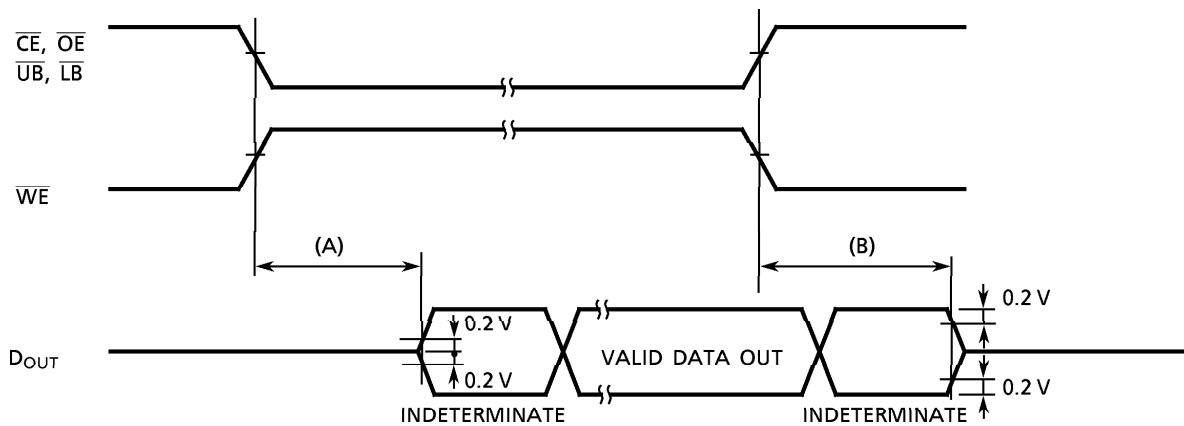
(4) If \overline{CE} goes HIGH coincident with or before \overline{WE} goes HIGH, the outputs will remain at high impedance.

(5) If \overline{OE} is HIGH during the write cycle, the outputs will remain at high impedance.

(6) The parameters specified below are measured using the load shown in Fig. 1.

(A) $t_{COE}, t_{OEE}, t_{BE}, t_{OEW}$ Output Enable Time

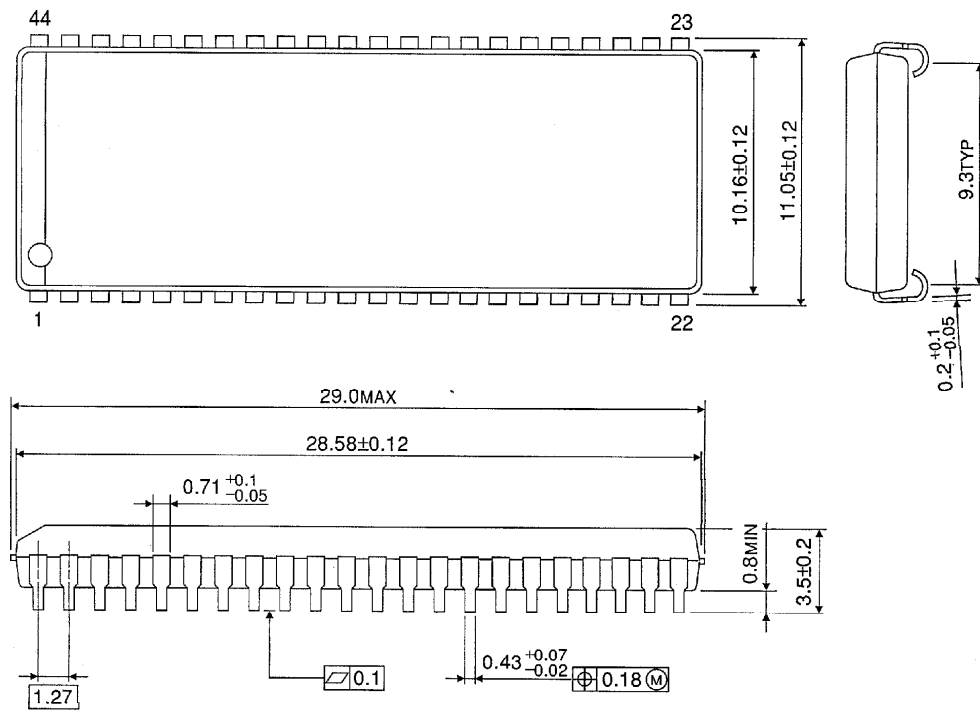
(B) $t_{COD}, t_{ODO}, t_{BD}, t_{ODW}$ Output Disable Time



PACKAGE DIMENSIONS

Plastic SOJ (SOJ44-P-400-1.27)

Units in mm

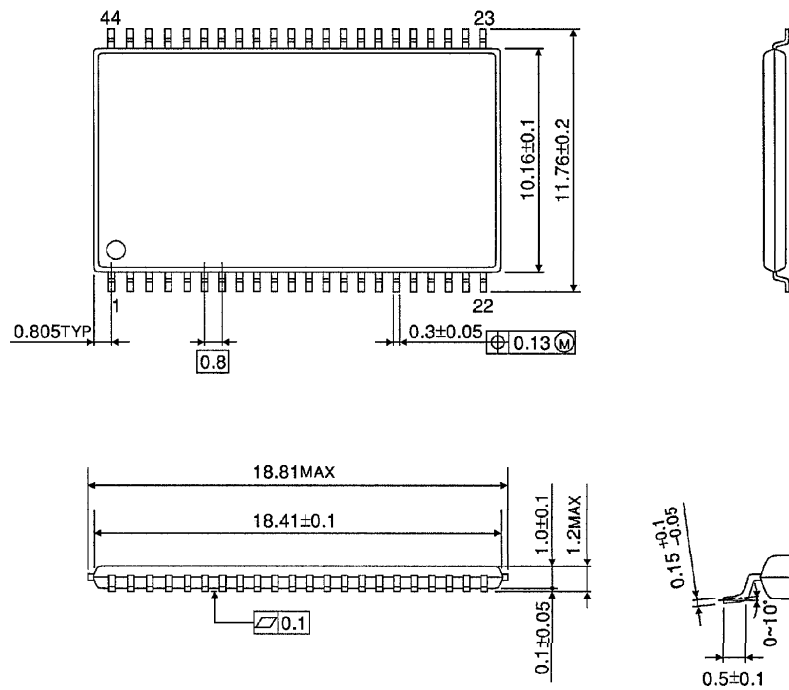


Weight: 1.64 g (typ)

PACKAGE DIMENSIONS

Plastic TSOP (TSOPII 44-P-400-0.80)

Units in mm



Weight: 0.45 g (typ)

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