

C161S

16-Bit Single-Chip Microcontroller

16bit

Microcontrollers



Never stop thinking.

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C161S**Revision History:** **2003-11**

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Previous Version: none

Page	Subjects (major changes since last revision)

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C161S

1 Summary of Features

- High Performance 16-bit CPU with 4-Stage Pipeline
 - 80 ns Instruction Cycle Time at 25 MHz CPU Clock
 - 400 ns Multiplication (16 × 16 bit), 800 ns Division (32 / 16 bit)
 - Enhanced Boolean Bit Manipulation Facilities
 - Additional Instructions to Support HLL and Operating Systems
 - Register-Based Design with Multiple Variable Register Banks
 - Single-Cycle Context Switching Support
 - 16 Mbytes Total Linear Address Space for Code and Data
 - 1024 Bytes On-Chip Special Function Register Area
- 16-Priority-Level Interrupt System with 30 Sources, Sample-Rate down to 40 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- Clock Generation via on-chip PLL (factors 1:1.5/2/2.5/3/4/5), via prescaler or via direct clock input
- On-Chip Memory Modules: 2 Kbytes On-Chip Internal RAM (IRAM)
- On-Chip Peripheral Modules
 - Two Multi-Functional General Purpose Timer Units with 5 Timers
 - Two Serial Channels (Sync./Asynchronous and High-Speed-Synchronous)
 - On-Chip Real Time Clock
- External Address Space for Code and Data
 - Programmable External Bus Characteristics for Different Address Ranges
 - Multiplexed or Demultiplexed External Address/Data Buses with 8-bit or 16-bit Data Bus Width
 - Four Programmable Chip-Select Signals
 - 4 Mbytes maximum address window size, results in a total external address space of 16 Mbytes, when all chip-select signal (address windows) are active
- Idle and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog
- Up to 63 General Purpose I/O Lines, partly with Selectable Input Thresholds and Hysteresis
- Power Supply: the C161S can operate from a 5 V or a 3 V power supply (see [Table 1](#))
- Supported by a Large Range of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader
- 80-Pin MQFP Package

Summary of Features

This document describes several derivatives of the C161 group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

Table 1 C161S Derivative Synopsis

Derivative	Max. Operating Frequency	Operating Voltage	Ambient Temperature
SAB-C161S-L25M	25 MHz	4.5 to 5.5 V (Standard)	0 to 70 °C
SAF-C161S-L25M	25 MHz	4.5 to 5.5 V (Standard)	-40 to 85 °C
SAB-C161S-LM3V	20 MHz	3.0 to 3.6 V (Reduced)	0 to 70 °C
SAF-C161S-LM3V	20 MHz	3.0 to 3.6 V (Reduced)	-40 to 85 °C

For simplicity all versions are referred to by the term **C161S** throughout this document.

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the C161S please refer to the “**Product Catalog Microcontrollers**”, which summarizes all available microcontroller variants.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

2 General Device Information

2.1 Introduction

The C161S is a derivative of the Infineon C166 Family of full featured single-chip CMOS microcontrollers. It combines high CPU performance (up to 12.5 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. It also provides clock generation via PLL and power management features. The C161S is especially suited for cost sensitive applications.

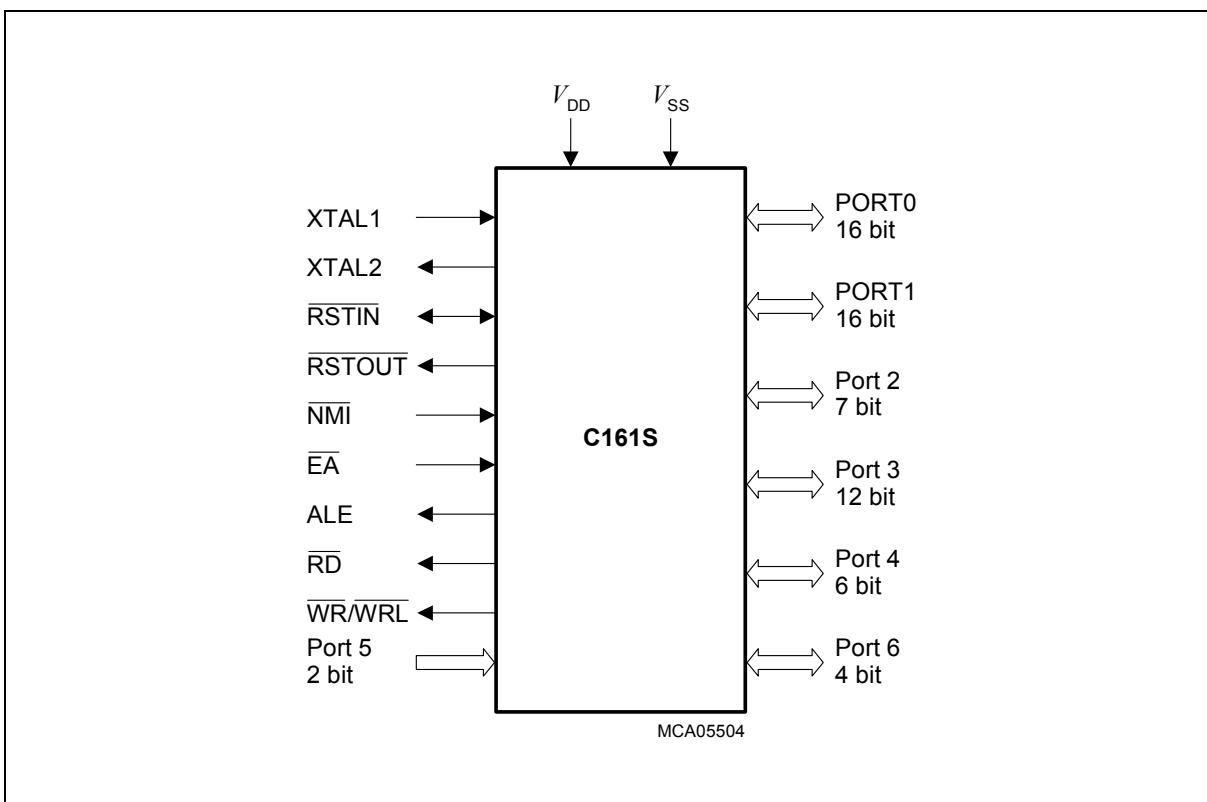


Figure 1 Logic Symbol

2.2 Pin Configuration and Definition

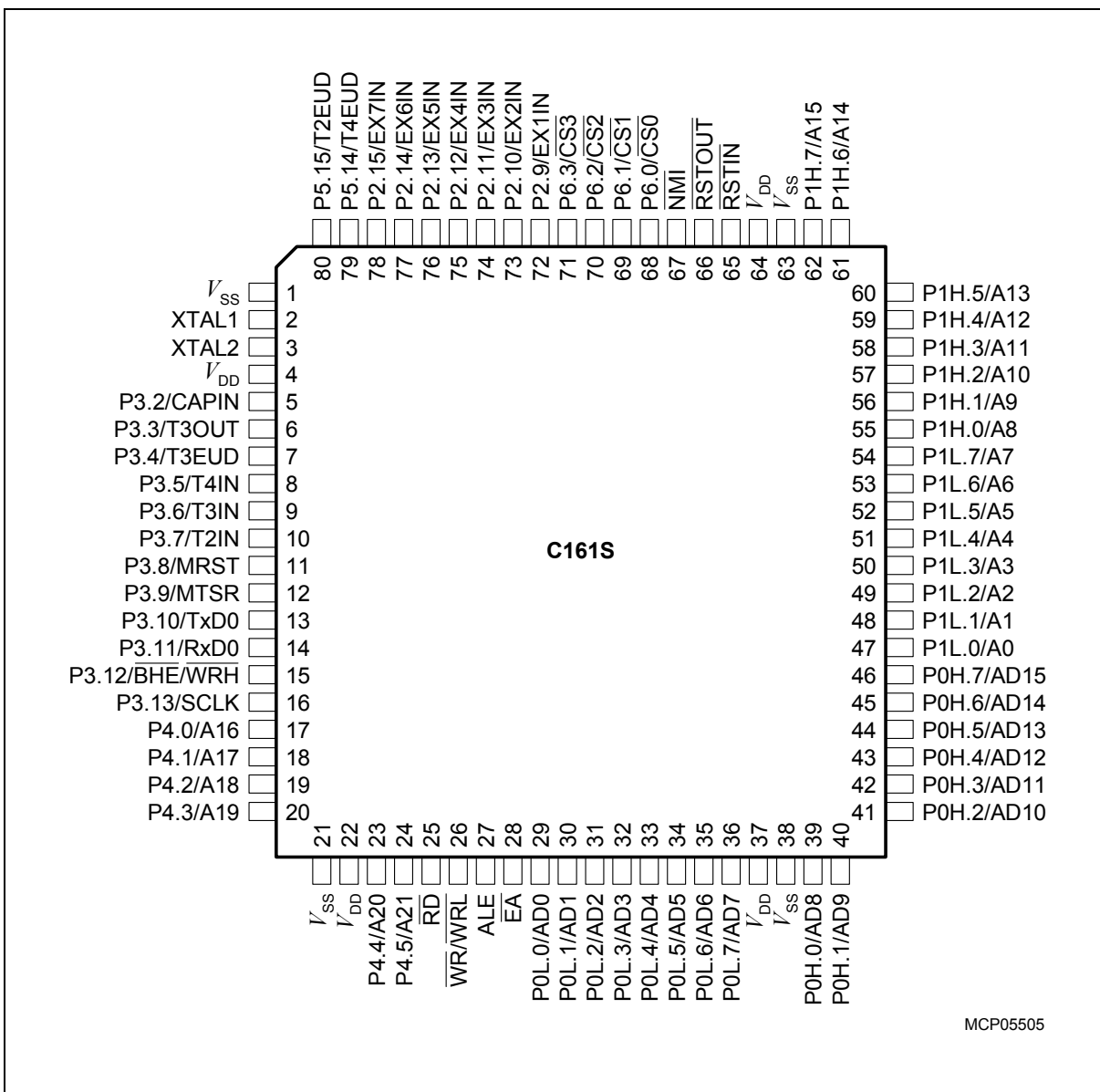


Figure 2 Pin Configuration (top view)

General Device Information
Table 2 Pin Definitions and Functions

Symbol	Pin No.	Input Outp.	Function
XTAL1	2	I	XTAL1: Input to the oscillator amplifier and input to the internal clock generator
XTAL2	3	O	XTAL2: Output of the oscillator amplifier circuit. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics (see Chapter 5.4) must be observed.
P3		IO	Port 3 is a 12-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The following Port 3 pins also serve for alternate functions:
P3.2	5	I	CAPIN GPT2 Register CAPREL Capture Input
P3.3	6	O	T3OUT GPT1 Timer T3 Toggle Latch Output
P3.4	7	I	T3EUD GPT1 Timer T3 External Up/Down Control Input
P3.5	8	I	T4IN GPT1 Timer T4 Count/Gate/Reload/Capture Inp.
P3.6	9	I	T3IN GPT1 Timer T3 Count/Gate Input
P3.7	10	I	T2IN GPT1 Timer T2 Count/Gate/Reload/Capture Inp.
P3.8	11	I/O	MRST SSC Master-Receive/Slave-Transmit Inp./Outp.
P3.9	12	I/O	MTSR SSC Master-Transmit/Slave-Receive Outp./Inp.
P3.10	13	O	TxD0 ASC0 Clock/Data Output (Async./Sync.)
P3.11	14	I/O	RxD0 ASC0 Data Input (Async.) or Inp./Outp. (Sync.)
P3.12	15	O	$\overline{\text{BHE}}$ External Memory High Byte Enable Signal,
		O	$\overline{\text{WRH}}$ External Memory High Byte Write Strobe
P3.13	16	I/O	SCLK SSC Master Clock Output / Slave Clock Input.
P4		IO	Port 4 is a 6-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 can be used to output the segment address lines:
P4.0	17	O	A16 Least Significant Segment Address Line
P4.1	18	O	A17 Segment Address Line
P4.2	19	O	A18 Segment Address Line
P4.3	20	O	A19 Segment Address Line
P4.4	23	O	A20 Segment Address Line
P4.5	24	O	A21 Segment Address Line

General Device Information

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function																		
\overline{RD}	25	O	External Memory Read Strobe. \overline{RD} is activated for every external instruction or data read access.																		
$\overline{WR}/\overline{WRL}$	26	O	External Memory Write Strobe. In \overline{WR} -mode this pin is activated for every external data write access. In \overline{WRL} -mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.																		
ALE	27	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.																		
\overline{EA}	28	I	External Access Enable pin. A low level at this pin during and after Reset forces the C161S to begin instruction execution out of external memory. A high level forces execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.																		
PORT0 P0L.0-7 P0H.0-7	29-36 39-46	IO	<p>PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state.</p> <p>In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes.</p> <p>Demultiplexed bus modes:</p> <table> <tr> <td>Data Path Width:</td> <td>8-bit</td> <td>16-bit</td> </tr> <tr> <td>P0L.0 – P0L.7:</td> <td>D0 – D7</td> <td>D0 – D7</td> </tr> <tr> <td>P0H.0 – P0H.7:</td> <td>I/O</td> <td>D8 – D15</td> </tr> </table> <p>Multiplexed bus modes:</p> <table> <tr> <td>Data Path Width:</td> <td>8-bit</td> <td>16-bit</td> </tr> <tr> <td>P0L.0 – P0L.7:</td> <td>AD0 – AD7</td> <td>AD0 – AD7</td> </tr> <tr> <td>P0H.0 – P0H.7:</td> <td>A8 – A15</td> <td>AD8 – AD15</td> </tr> </table>	Data Path Width:	8-bit	16-bit	P0L.0 – P0L.7:	D0 – D7	D0 – D7	P0H.0 – P0H.7:	I/O	D8 – D15	Data Path Width:	8-bit	16-bit	P0L.0 – P0L.7:	AD0 – AD7	AD0 – AD7	P0H.0 – P0H.7:	A8 – A15	AD8 – AD15
Data Path Width:	8-bit	16-bit																			
P0L.0 – P0L.7:	D0 – D7	D0 – D7																			
P0H.0 – P0H.7:	I/O	D8 – D15																			
Data Path Width:	8-bit	16-bit																			
P0L.0 – P0L.7:	AD0 – AD7	AD0 – AD7																			
P0H.0 – P0H.7:	A8 – A15	AD8 – AD15																			

General Device Information
Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
PORT1 P1L.0-7 P1H.0-7	47-54 55-62	IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode.
$\overline{\text{RSTIN}}$	65	I/O	<p>Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the C161S. An internal pull-up resistor permits power-on reset using only a capacitor connected to V_{SS}.</p> <p>A spike filter suppresses input pulses < 10 ns. Input pulses > 100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles.</p> <p>In bidirectional reset mode (enabled by setting bit BDRSTEN in register SYSCON) the $\overline{\text{RSTIN}}$ line is internally pulled low for the duration of the internal reset sequence upon any reset (HW, SW, WDT). See note below this table.</p> <p><i>Note: To let the reset configuration of PORT0 settle and to let the PLL lock a reset duration of approx. 1 ms is recommended.</i></p>
$\overline{\text{RSTOUT}}$	66	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{NMI}}$	67	I	<p>Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the C161S to go into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode.</p> <p>If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.</p>

General Device Information
Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
P6		IO	Port 6 is a 4-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The Port 6 pins also serve for alternate functions:
P6.0	68	O	$\overline{CS0}$ Chip Select 0 Output
P6.1	69	O	$\overline{CS1}$ Chip Select 1 Output
P6.2	70	O	$\overline{CS2}$ Chip Select 2 Output
P6.3	71	O	$\overline{CS3}$ Chip Select 3 Output
P2		IO	Port 2 is a 7-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The following Port 2 pins also serve for alternate functions:
P2.9	72	I	EX1IN Fast External Interrupt 1 Input
P2.10	73	I	EX2IN Fast External Interrupt 2 Input
P2.11	74	I	EX3IN Fast External Interrupt 3 Input
P2.12	75	I	EX4IN Fast External Interrupt 4 Input
P2.13	76	I	EX5IN Fast External Interrupt 5 Input
P2.14	77	I	EX6IN Fast External Interrupt 6 Input
P2.15	78	I	EX7IN Fast External Interrupt 7 Input
P5		I	Port 5 is a 2-bit input-only port with Schmitt-Trigger char. The pins of Port 5 also serve as timer inputs:
P5.14	79	I	T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Input
P5.15	80	I	T2EUD GPT1 Timer T5 Ext. Up/Down Ctrl. Input
V_{DD}	4, 22, 37, 64	–	Digital Supply Voltage: + 5 V during normal operation and idle mode. + 3.3 V during reduced supply operation and idle mode. ≥ 2.5 V during power down mode. <i>Note: Please refer to the Operating Conditions Parameters.</i>
V_{SS}	1, 21, 38, 63	–	Digital Ground.

General Device Information

Note: The following behavioural differences must be observed when the bidirectional reset is active:

- Bit BDRSTEN in register SYSCON cannot be changed after EINIT and is cleared automatically after a reset.
- The reset indication flags always indicate a long hardware reset.
- The PORT0 configuration is treated like on a hardware reset. Especially the bootstrap loader may be activated when P0L.4 is low.
- Pin RSTIN may only be connected to external reset devices with an open drain output driver.
- A short hardware reset is extended to the duration of the internal reset sequence.

3 Functional Description

The architecture of the C161S combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. In addition the on-chip memory blocks allow the design of compact systems with maximum performance. **Figure 3** gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C161S.

Note: All time specifications refer to a CPU clock of 20 MHz (see definition in the AC Characteristics section).

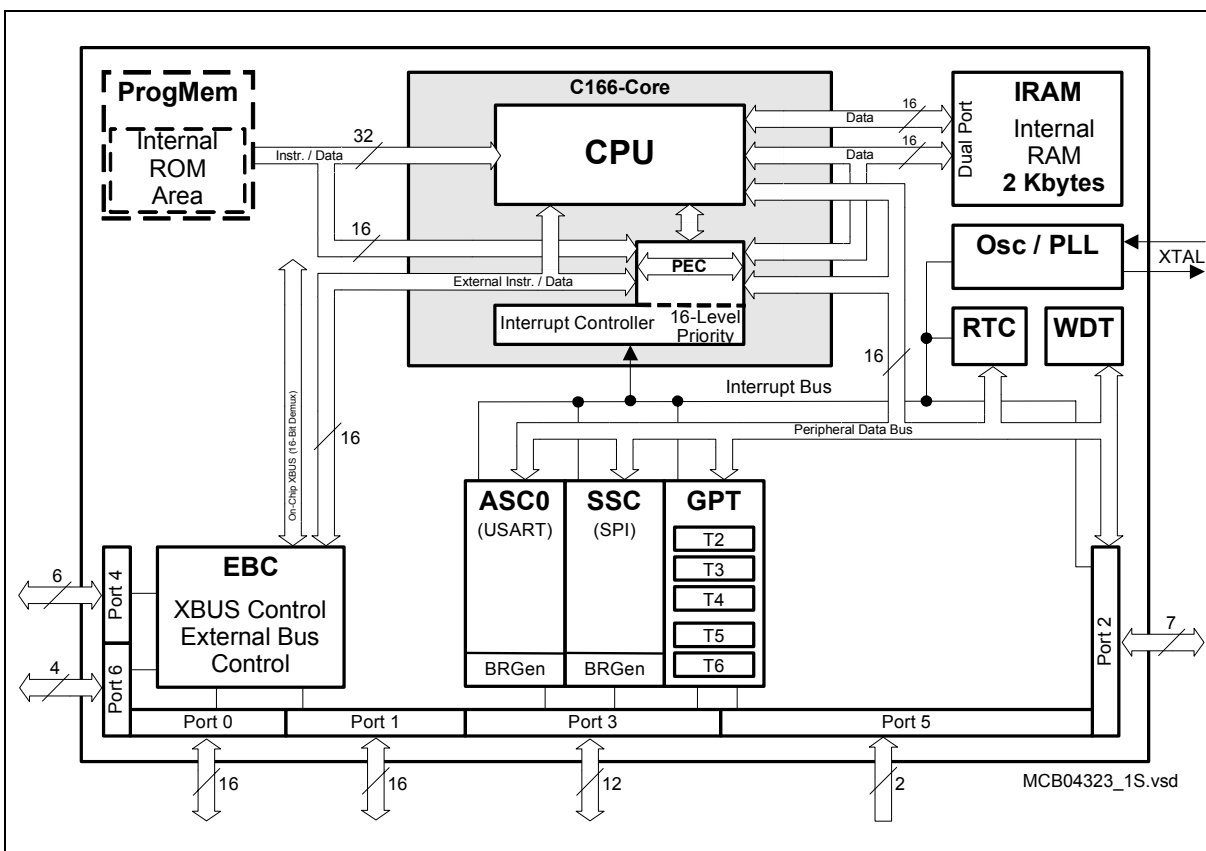


Figure 3 Block Diagram

The program memory, the internal RAM (IRAM) and the set of generic peripherals are connected to the CPU via separate buses. A fourth bus, the XBUS, connects external resources as well as additional on-chip resources, the X-Peripherals (see **Figure 3**).

3.1 Memory Organization

The memory space of the C161S is configured in a von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 16 Mbytes. The entire memory space can be accessed bitwise or wordwise. Particular portions of the on-chip memory have additionally been made directly bitaddressable.

The C161S is prepared to incorporate on-chip program memory (not in the ROM-less derivatives, of course) for code or constant data. The internal ROM area can be mapped either to segment 0 or segment 1.

2 Kbytes of on-chip Internal RAM (IRAM) are provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 wordwise (R0 to R15) and/or bitwise (RL0, RH0, ..., RL7, RH7) so-called General Purpose Registers (GPRs).

1024 bytes (2×512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwise registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the C166 Family.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 16 Mbytes of external RAM and/or ROM can be connected to the microcontroller. The maximum contiguous external address space is 4 Mbytes, i.e. this is the maximum address window size. Using the chip-select lines (multiple windows) this results in a maximum usable external address space of 16 Mbytes.

3.2 External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

- 16-/18-/20-/22-bit Addresses, 16-bit Data, Demultiplexed
- 16-/18-/20-/22-bit Addresses, 16-bit Data, Multiplexed
- 16-/18-/20-/22-bit Addresses, 8-bit Data, Multiplexed
- 16-/18-/20-/22-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.

In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.

Up to 4 external \overline{CS} signals (3 windows plus default) can be generated in order to save external glue logic. The C161S offers the possibility to switch the \overline{CS} outputs to an unlatched mode. In this mode the internal filter logic is switched off and the \overline{CS} signals are directly generated from the address. The unlatched \overline{CS} mode is enabled by setting CSCFG (SYSCON.6).

For applications which require less than 4 Mbytes of external memory space, this address space can be restricted to 1 Mbyte, 256 Kbytes, or to 64 Kbytes. In this case Port 4 outputs four, two, or no address lines at all. It outputs all 6 address lines, if the full address width is used.

3.3 Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C161S's instructions can be executed in just one machine cycle which requires 100 ns at 20 MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16×16 bit multiplication in 5 cycles and a 32-/16-bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.

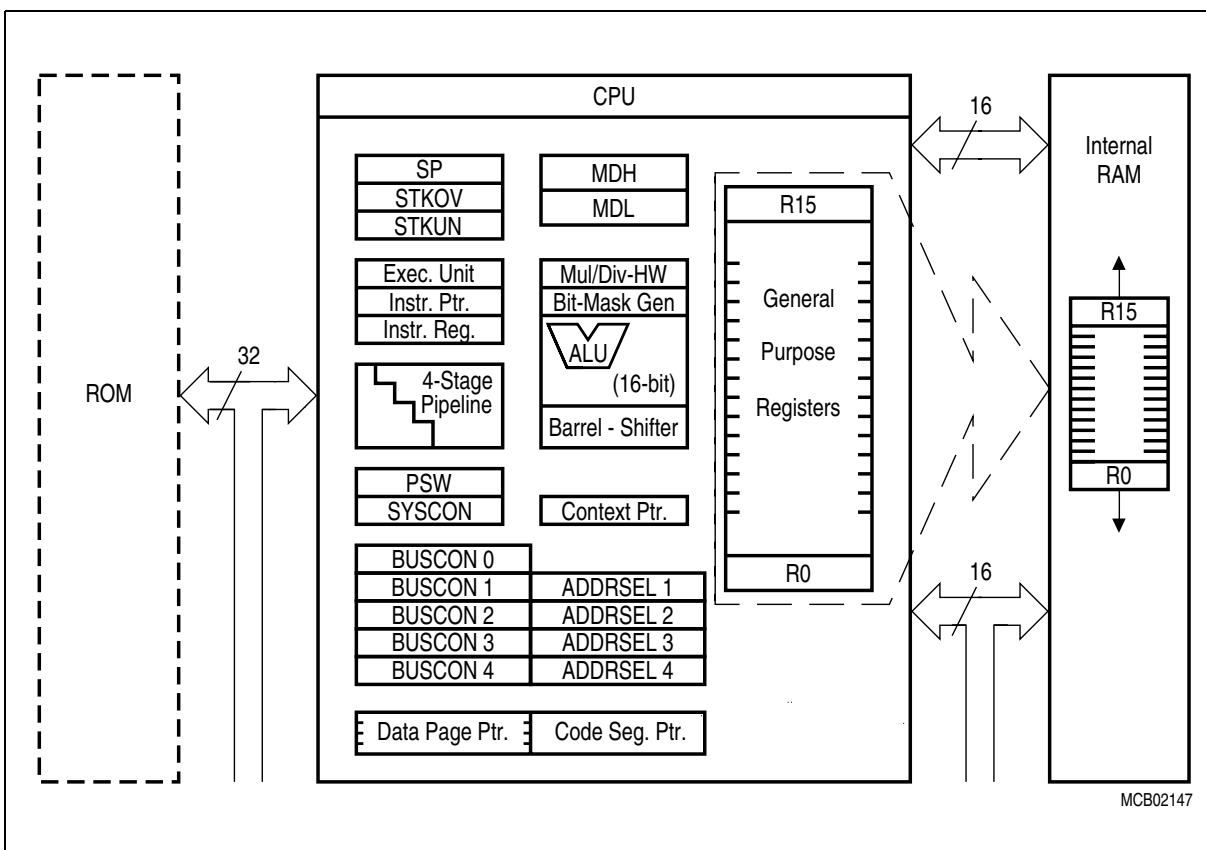


Figure 4 CPU Block Diagram

The CPU has a register context consisting of up to 16 wordwide GPRs at its disposal. These 16 GPRs are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

Functional Description

A system stack of up to 1024 words is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient C161S instruction set which includes the following instruction classes:

- Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

3.3.1 Interrupt System

With an interrupt response time within a range from just 5 to 12 CPU clocks (in case of internal program execution), the C161S is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C161S supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C161S has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

Table 3 shows all of the possible C161S interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not used by associated peripherals, may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

Functional Description
Table 3 C161S Interrupt Nodes

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
Unassigned node	CC8IR	CC8IE	CC8INT	00'0060 _H	18 _H
External Interrupt 1	CC9IR	CC9IE	CC9INT	00'0064 _H	19 _H
External Interrupt 2	CC10IR	CC10IE	CC10INT	00'0068 _H	1A _H
External Interrupt 3	CC11IR	CC11IE	CC11INT	00'006C _H	1B _H
External Interrupt 4	CC12IR	CC12IE	CC12INT	00'0070 _H	1C _H
External Interrupt 5	CC13IR	CC13IE	CC13INT	00'0074 _H	1D _H
External Interrupt 6	CC14IR	CC14IE	CC14INT	00'0078 _H	1E _H
External Interrupt 7	CC15IR	CC15IE	CC15INT	00'007C _H	1F _H
GPT1 Timer 2	T2IR	T2IE	T2INT	00'0088 _H	22 _H
GPT1 Timer 3	T3IR	T3IE	T3INT	00'008C _H	23 _H
GPT1 Timer 4	T4IR	T4IE	T4INT	00'0090 _H	24 _H
GPT2 Timer 5	T5IR	T5IE	T5INT	00'0094 _H	25 _H
GPT2 Timer 6	T6IR	T6IE	T6INT	00'0098 _H	26 _H
GPT2 CAPREL Reg.	CRIR	CRIE	CRINT	00'009C _H	27 _H
Unassigned node	ADCIR	ADCIE	ADCINT	00'00A0 _H	28 _H
Unassigned node	ADEIR	ADEIE	ADEINT	00'00A4 _H	29 _H
ASC0 Transmit	S0TIR	S0TIE	S0TINT	00'00A8 _H	2A _H
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	00'011C _H	47 _H
ASC0 Receive	S0RIR	S0RIE	S0RINT	00'00AC _H	2B _H
ASC0 Error	S0EIR	S0EIE	S0EINT	00'00B0 _H	2C _H
SSC Transmit	SCTIR	SCTIE	SCTINT	00'00B4 _H	2D _H
SSC Receive	SCRIR	SCRIE	SCRINT	00'00B8 _H	2E _H
SSC Error	SCEIR	SCEIE	SCEINT	00'00BC _H	2F _H
Unassigned node	XP0IR	XP0IE	XP0INT	00'0100 _H	40 _H
Unassigned node	XP1IR	XP1IE	XP1INT	00'0104 _H	41 _H
Unassigned node	XP2IR	XP2IE	XP2INT	00'0108 _H	42 _H
PLL/OWD and RTC	XP3IR	XP3IE	XP3INT	00'010C _H	43 _H
Unassigned node	CC29IR	CC29IE	CC29INT	00'0110 _H	44 _H
Unassigned node	CC30IR	CC30IE	CC30INT	00'0114 _H	45 _H
Unassigned node	CC31IR	CC31IE	CC31INT	00'0118 _H	46 _H

Functional Description

The C161S also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called 'Hardware Traps'. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 4 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 4 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions: <ul style="list-style-type: none"> Hardware Reset Software Reset W-dog Timer Overflow 	–	RESET RESET RESET	00'0000 _H 00'0000 _H 00'0000 _H	00 _H 00 _H 00 _H	III III III
Class A Hardware Traps: <ul style="list-style-type: none"> Non-Maskable Interrupt Stack Overflow Stack Underflow 	NMI STKOF STKUF	NMITRAP STOTRAP STUTRAP	00'0008 _H 00'0010 _H 00'0018 _H	02 _H 04 _H 06 _H	II II II
Class B Hardware Traps: <ul style="list-style-type: none"> Undefined Opcode Protected Instruction Fault Illegal Word Operand Access Illegal Instruction Access Illegal External Bus Access 	UNDOPC PRTFLT ILLOPA ILLINA ILLBUS	BTRAP BTRAP BTRAP BTRAP BTRAP	00'0028 _H 00'0028 _H 00'0028 _H 00'0028 _H 00'0028 _H	0A _H 0A _H 0A _H 0A _H 0A _H	I I I I I
Reserved	–	–	[2C _H – 3C _H]	[0B _H – 0F _H]	–
Software Traps <ul style="list-style-type: none"> TRAP Instruction 	–	–	Any [00'0000 _H – 00'01FC _H] in steps of 4 _H	Any [00 _H – 7F _H]	Current CPU Priority

3.4 General Purpose Timer (GPT) Unit

The GPT unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 16 TCL.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

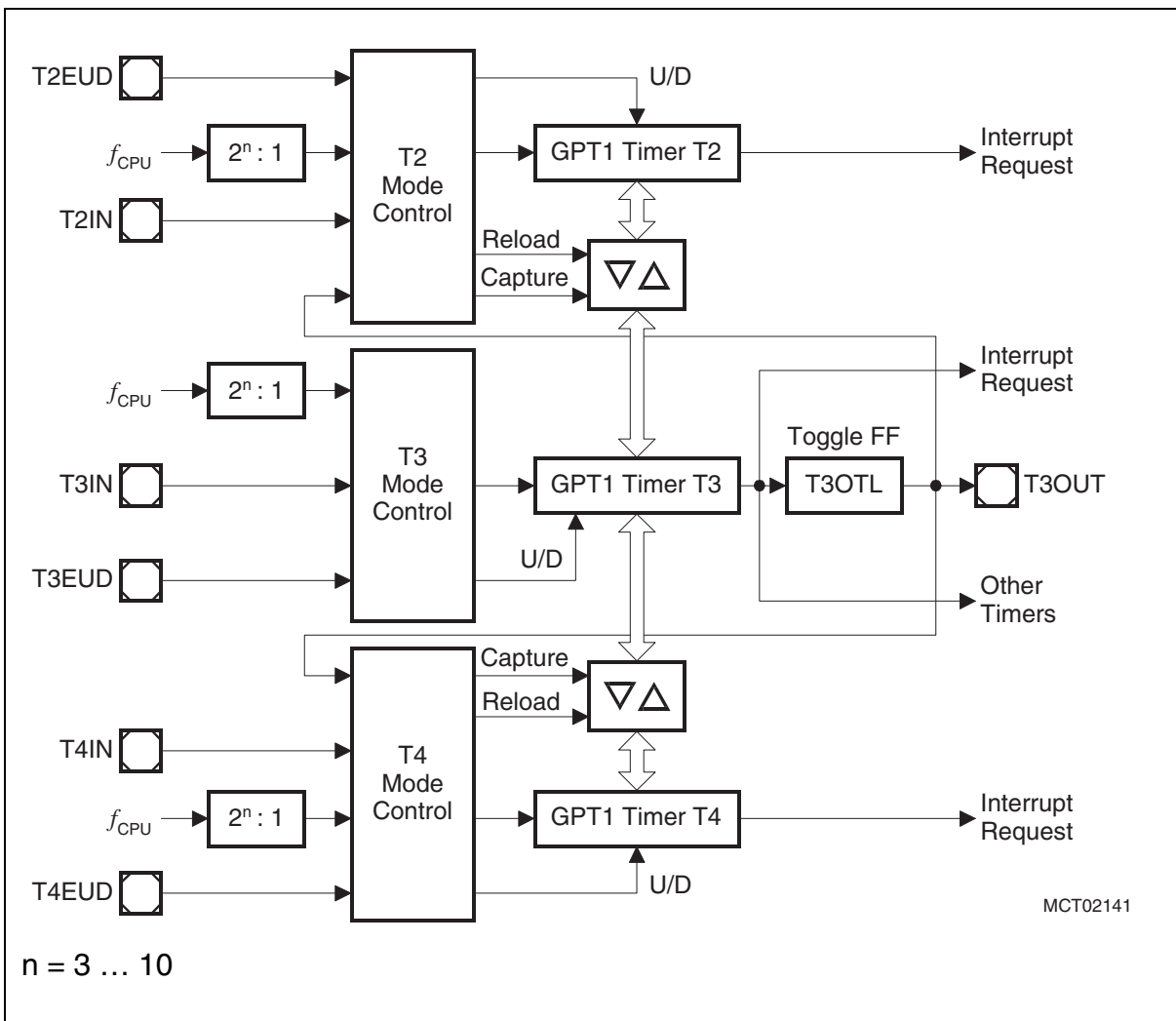


Figure 5 Block Diagram of GPT1

With its maximum resolution of 8 TCL, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock. The count direction (up/down) for each timer is programmable by software. Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5. The overflows/underflows of timer T6 can cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows the C161S to measure absolute time differences or to perform pulse multiplication without software overhead.

Functional Description

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

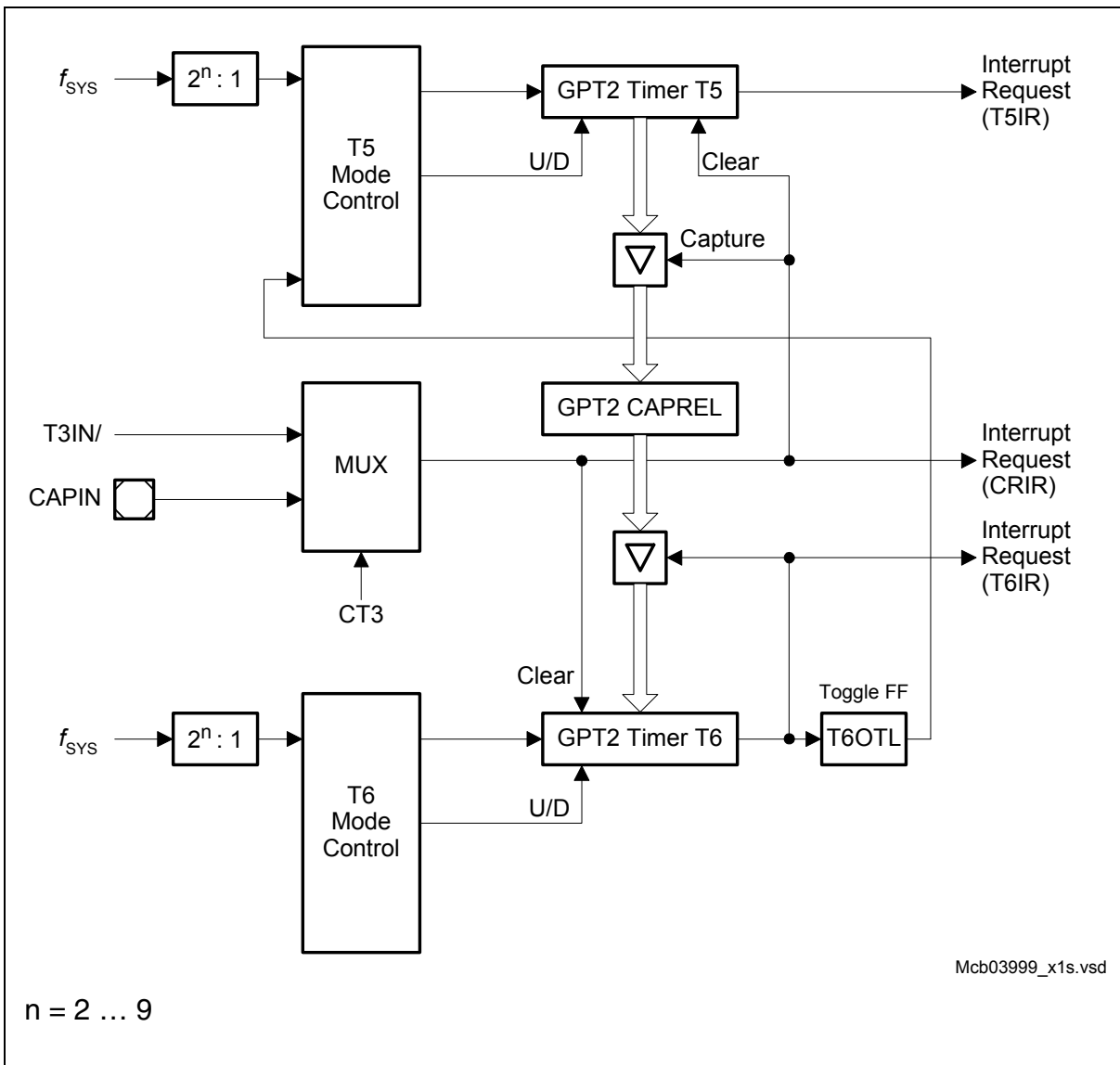


Figure 6 Block Diagram of GPT2

3.5 Real Time Clock

The Real Time Clock (RTC) module of the C161S consists of a chain of 3 divider blocks, a fixed 8:1 divider, the reloadable 16-bit timer T14, and the 32-bit RTC timer (accessible via registers RTCH and RTCL). The RTC module is directly clocked with the on-chip oscillator frequency divided by 32 via a separate clock driver ($f_{RTC} = f_{OSC}/32$) and is therefore independent from the selected clock generation mode of the C161S. All timers count up.

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time based interrupt
- 48-bit timer for long term measurements

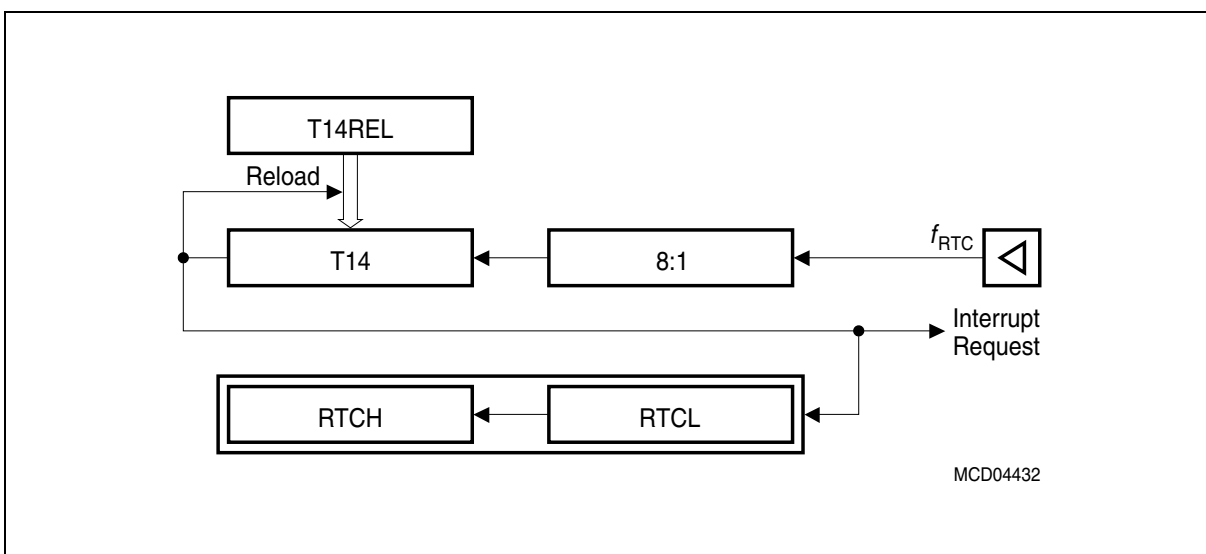


Figure 7 RTC Block Diagram

Note: The registers associated with the RTC are not affected by a reset in order to maintain the correct system time even when intermediate resets are executed.

3.6 Serial Channels

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces with different functionality, an Asynchronous/Synchronous Serial Channel (**ASC0**) and a High-Speed Synchronous Serial Channel (**SSC**).

The ASC0 is upward compatible with the serial ports of the Infineon 8-bit microcontroller families and supports full-duplex asynchronous communication at up to 625 kbit/s and half-duplex synchronous communication at up to 2.5 Mbit/s (@ 20 MHz CPU clock).

A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling 4 separate interrupt vectors are provided. In asynchronous mode, 8- or 9-bit data frames are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data plus wake-up bit mode).

In synchronous mode, the ASC0 transmits or receives bytes (8 bits) synchronously to a shift clock which is generated by the ASC0. The ASC0 always shifts the LSB first. A loop back option is available for testing purposes.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated, if the last character received has not been read out of the receive buffer register at the time the reception of a new character is complete.

The SSC supports full-duplex synchronous communication at up to 5 Mbit/s (@ 20 MHz CPU clock). It may be configured so it interfaces with serially linked peripheral components. A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception, and error handling three separate interrupt vectors are provided.

The SSC transmits or receives characters of 2 ... 16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB and allows the selection of shifting and latching clock edges as well as the clock polarity.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. Transmit and receive error supervise the correct handling of the data buffer. Phase and baudrate error detect incorrect serial data.

3.7 Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. Thus, the chip's start-up procedure is always monitored. The software has to be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset and pulls the $\overline{\text{RSTOUT}}$ pin low in order to allow external hardware components to be reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided by 2/128. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Thus, time intervals between 25 μs and 420 ms can be monitored (@ 20 MHz).

The default Watchdog Timer interval after reset is 6.55 ms (@ 20 MHz).

3.8 Parallel Ports

The C161S provides up to 63 I/O lines which are organized into six input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of three I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

PORT0 and PORT1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A21/19/17 ... A16 in systems where segmentation is enabled to access more than 64 Kbytes of memory.

Port 6 provides optional chip select signals.

Port 3 includes alternate functions of timers, serial interfaces, and the optional bus control signal $\overline{\text{BHE}}$.

Port 5 is used for timer control signals.

3.9 Oscillator Watchdog

The Oscillator Watchdog (OWD) monitors the clock signal generated by the on-chip oscillator (either with a crystal or via external clock drive). For this operation the PLL provides a clock signal which is used to supervise transitions on the oscillator clock. This PLL clock is independent from the XTAL1 clock. When the expected oscillator clock transitions are missing the OWD activates the PLL Unlock / OWD interrupt node and supplies the CPU with the PLL clock signal. Under these circumstances the PLL will oscillate with its basic frequency.

In direct drive mode the PLL base frequency is used directly ($f_{\text{CPU}} = 2 \dots 5 \text{ MHz}$).

In prescaler mode the PLL base frequency is divided by 2 ($f_{\text{CPU}} = 1 \dots 2.5 \text{ MHz}$).

Note: The CPU clock source is only switched back to the oscillator clock after a hardware reset.

The oscillator watchdog can be disabled by setting bit OWDDIS in register SYSCON. In this case (OWDDIS = '1') the PLL remains idle and provides no clock signal, while the CPU clock signal is derived directly from the oscillator clock or via prescaler or SDD. Also no interrupt request will be generated in case of a missing oscillator clock.

Note: At the end of a reset bit OWDDIS reflects the inverted level of pin \overline{RD} at that time. Thus the oscillator watchdog may also be disabled via hardware by (externally) pulling the \overline{RD} line low upon a reset, similar to the standard reset configuration via PORT0.

3.10 Power Management

The C161S provides several means to control the power it consumes either at a given time or averaged over a certain timespan. Three mechanisms can be used (partly in parallel):

- **Power Saving Modes** switch the C161S into a special operating mode (control via instructions).
Idle Mode stops the CPU while the peripherals can continue to operate.
Power Down Mode stops all clock signals and all operation (RTC may optionally continue running).
- **Clock Generation Management** controls the distribution and the frequency of internal and external clock signals (control via register SYSCON2).
Slow Down Mode lets the C161S run at a CPU clock frequency of $f_{OSC} / 1 \dots 32$ (half for prescaler operation) which drastically reduces the consumed power. The PLL can be optionally disabled while operating in Slow Down Mode.
- **Peripheral Management** permits temporary disabling of peripheral modules (control via register SYSCON3).
Each peripheral can separately be disabled/enabled. A group control option disables a major part of the peripheral set by setting one single bit.

The on-chip RTC supports intermittent operation of the C161S by generating cyclic wake-up signals. This offers full performance to quickly react on action requests while the intermittent sleep phases greatly reduce the average power consumption of the system.

3.11 Instruction Set Summary

Table 5 lists the instructions of the C161S in a condensed way.

The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the “**C166 Family Instruction Set Manual**”.

This document also provides a detailed description of each instruction.

Table 5 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise XOR, (word/byte operands)	2 / 4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2

Functional Description
Table 5 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
MOV(B)	Move word (byte) data	2 / 4
MOVBS	Move byte operand to word operand with sign extension	2 / 4
MOVBZ	Move byte operand to word operand with zero extension	2 / 4
JMPA, JMPI, JMPR	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
J(N)B	Jump relative if direct bit is (not) set	4
JBC	Jump relative and clear bit if direct bit is set	4
JNBS	Jump relative and set bit if direct bit is not set	4
CALLA, CALLI, CALLR	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH, POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET	Return from intra-segment subroutine	2
RETS	Return from inter-segment subroutine	2
RETP	Return from intra-segment subroutine and pop direct word register from system stack	2
RETI	Return from interrupt service subroutine	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$ -pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT	Disable Watchdog Timer	4
EINIT	Signify End-of-Initialization on $\overline{\text{RSTOUT}}$ -pin	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTENDED Register sequence	2
EXTP(R)	Begin EXTENDED Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTENDED Segment (and Register) sequence	2 / 4
NOP	Null operation	2

3.12 Special Function Registers Overview

Table 6 lists all SFRs which are implemented in the C161S in alphabetical order. The following markings assist in classifying the listed registers:

“b” in the “Name” column marks **Bit-addressable** SFRs.

“E” in the “Physical Address” column marks (E)SFRs in the **Extended SFR-Space**.

“X” in the “Physical Address” column marks registers within on-chip X-peripherals.

Table 6 C161S Registers, Ordered by Name

Name	Physical Address	8-Bit Addr.	Description	Reset Value
ADCIC	b FF98 _H	CC _H	Software Interrupt Control Register	0000 _H
ADDRSEL1	FE18 _H	0C _H	Address Select Register 1	0000 _H
ADDRSEL2	FE1A _H	0D _H	Address Select Register 2	0000 _H
ADDRSEL3	FE1C _H	0E _H	Address Select Register 3	0000 _H
ADDRSEL4	FE1E _H	0F _H	Address Select Register 4	0000 _H
ADEIC	b FF9A _H	CD _H	Software Interrupt Control Register	0000 _H
BUSCON0	b FF0C _H	86 _H	Bus Configuration Register 0	0XX0 _H
BUSCON1	b FF14 _H	8A _H	Bus Configuration Register 1	0000 _H
BUSCON2	b FF16 _H	8B _H	Bus Configuration Register 2	0000 _H
BUSCON3	b FF18 _H	8C _H	Bus Configuration Register 3	0000 _H
BUSCON4	b FF1A _H	8D _H	Bus Configuration Register 4	0000 _H
CAPREL	FE4A _H	25 _H	GPT2 Capture/Reload Register	0000 _H
CC10IC	b FF8C _H	C6 _H	EX2IN Interrupt Control Register	0000 _H
CC11IC	b FF8E _H	C7 _H	EX3IN Interrupt Control Register	0000 _H
CC12IC	b FF90 _H	C8 _H	EX4IN Interrupt Control Register	0000 _H
CC13IC	b FF92 _H	C9 _H	EX5IN Interrupt Control Register	0000 _H
CC14IC	b FF94 _H	CA _H	EX6IN Interrupt Control Register	0000 _H
CC15IC	b FF96 _H	CB _H	EX7IN Interrupt Control Register	0000 _H
CC29IC	b F184 _H E	C2 _H	Software Interrupt Control Register	0000 _H
CC30IC	b F18C _H E	C6 _H	Software Interrupt Control Register	0000 _H
CC31IC	b F194 _H E	CA _H	Software Interrupt Control Register	0000 _H
CC8IC	b FF88 _H	C4 _H	Software Interrupt Control Register	0000 _H
CC9IC	b FF8A _H	C5 _H	EX1IN Interrupt Control Register	0000 _H

Functional Description
Table 6 C161S Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
CP	FE10 _H	08 _H	CPU Context Pointer Register	FC00 _H
CRIC	b FF6A _H	B5 _H	GPT2 CAPREL Interrupt Ctrl. Reg.	0000 _H
CSP	FE08 _H	04 _H	CPU Code Seg. Pointer Reg. (read only)	0000 _H
DP0H	b F102 _H	E 81 _H	P0H Direction Control Register	00 _H
DP0L	b F100 _H	E 80 _H	P0L Direction Control Register	00 _H
DP1H	b F106 _H	E 83 _H	P1H Direction Control Register	00 _H
DP1L	b F104 _H	E 82 _H	P1L Direction Control Register	00 _H
DP2	b FFC2 _H	E1 _H	Port 2 Direction Control Register	0000 _H
DP3	b FFC6 _H	E3 _H	Port 3 Direction Control Register	0000 _H
DP4	b FFCA _H	E5 _H	Port 4 Direction Control Register	00 _H
DP6	b FFCE _H	E7 _H	Port 6 Direction Control Register	00 _H
DPP0	FE00 _H	00 _H	CPU Data Page Pointer 0 Reg. (10 bits)	0000 _H
DPP1	FE02 _H	01 _H	CPU Data Page Pointer 1 Reg. (10 bits)	0001 _H
DPP2	FE04 _H	02 _H	CPU Data Page Pointer 2 Reg. (10 bits)	0002 _H
DPP3	FE06 _H	03 _H	CPU Data Page Pointer 3 Reg. (10 bits)	0003 _H
EXICON	b F1C0 _H	E E0 _H	External Interrupt Control Register	0000 _H
IDCHIP	F07C _H	E 3E _H	Identifier	05XX _H
IDMANUF	F07E _H	E 3F _H	Identifier	1820 _H
IDMEM	F07A _H	E 3D _H	Identifier	0000 _H
IDMEM2	F076 _H	E 3B _H	Identifier	0000 _H
IDPROG	F078 _H	E 3C _H	Identifier	0000 _H
ISNC	b F1DE _H	E EF _H	Interrupt Subnode Control Register	0000 _H
MDC	b FF0E _H	87 _H	CPU Multiply Divide Control Register	0000 _H
MDH	FE0C _H	06 _H	CPU Multiply Divide Reg. – High Word	0000 _H
MDL	FE0E _H	07 _H	CPU Multiply Divide Reg. – Low Word	0000 _H
ODP2	b F1C2 _H	E E1 _H	Port 2 Open Drain Control Register	0000 _H
ODP3	b F1C6 _H	E E3 _H	Port 3 Open Drain Control Register	0000 _H
ODP6	b F1CE _H	E E7 _H	Port 6 Open Drain Control Register	00 _H
ONES	b FF1E _H	8F _H	Constant Value 1's Register (read only)	FFFF _H
P0H	b FF02 _H	81 _H	Port 0 High Reg. (Upper half of PORT0)	00 _H

Functional Description
Table 6 C161S Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
P0L	b FF00 _H	80 _H	Port 0 Low Reg. (Lower half of PORT0)	00 _H
P1H	b FF06 _H	83 _H	Port 1 High Reg. (Upper half of PORT1)	00 _H
P1L	b FF04 _H	82 _H	Port 1 Low Reg. (Lower half of PORT1)	00 _H
P2	b FFC0 _H	E0 _H	Port 2 Register	0000 _H
P3	b FFC4 _H	E2 _H	Port 3 Register	0000 _H
P4	b FFC8 _H	E4 _H	Port 4 Register (8 bits)	00 _H
P5	b FFA2 _H	D1 _H	Port 5 Register (read only)	XXXX _H
P6	b FFCC _H	E6 _H	Port 6 Register (8 bits)	00 _H
PECC0	FEC0 _H	60 _H	PEC Channel 0 Control Register	0000 _H
PECC1	FEC2 _H	61 _H	PEC Channel 1 Control Register	0000 _H
PECC2	FEC4 _H	62 _H	PEC Channel 2 Control Register	0000 _H
PECC3	FEC6 _H	63 _H	PEC Channel 3 Control Register	0000 _H
PECC4	FEC8 _H	64 _H	PEC Channel 4 Control Register	0000 _H
PECC5	FECA _H	65 _H	PEC Channel 5 Control Register	0000 _H
PECC6	FECC _H	66 _H	PEC Channel 6 Control Register	0000 _H
PECC7	FECE _H	67 _H	PEC Channel 7 Control Register	0000 _H
PSW	b FF10 _H	88 _H	CPU Program Status Word	0000 _H
RP0H	b F108 _H	E 84 _H	System Startup Config. Reg. (Rd. only)	XX _H
RTCH	F0D6 _H	E 6B _H	RTC High Register	XXXX _H
RTCL	F0D4 _H	E 6A _H	RTC Low Register	XXXX _H
S0BG	FEB4 _H	5A _H	Serial Channel 0 Baud Rate Generator Reload Register	0000 _H
S0CON	b FFBO _H	D8 _H	Serial Channel 0 Control Register	0000 _H
S0EIC	b FF70 _H	B8 _H	Serial Channel 0 Error Interrupt Ctrl. Reg	0000 _H
S0RBUF	FEB2 _H	59 _H	Serial Channel 0 Receive Buffer Reg. (read only)	XX _H
S0RIC	b FF6E _H	B7 _H	Serial Channel 0 Receive Interrupt Control Register	0000 _H
S0TBIC	b F19C _H	E CE _H	Serial Channel 0 Transmit Buffer Interrupt Control Register	0000 _H

Functional Description
Table 6 C161S Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
S0TBUF	FEB0 _H	58 _H	Serial Channel 0 Transmit Buffer Register (write only)	00 _H
S0TIC	b FF6C _H	B6 _H	Serial Channel 0 Transmit Interrupt Control Register	0000 _H
SP	FE12 _H	09 _H	CPU System Stack Pointer Register	FC00 _H
SSCBR	F0B4 _H E	5A _H	SSC Baudrate Register	0000 _H
SSCON	b FFB2 _H	D9 _H	SSC Control Register	0000 _H
SSCEIC	b FF76 _H	BB _H	SSC Error Interrupt Control Register	0000 _H
SSCRB	F0B2 _H E	59 _H	SSC Receive Buffer	XXXX _H
SSCRIC	b FF74 _H	BA _H	SSC Receive Interrupt Control Register	0000 _H
SSCTB	F0B0 _H E	58 _H	SSC Transmit Buffer	0000 _H
SSCTIC	b FF72 _H	B9 _H	SSC Transmit Interrupt Control Register	0000 _H
STKOV	FE14 _H	0A _H	CPU Stack Overflow Pointer Register	FA00 _H
STKUN	FE16 _H	0B _H	CPU Stack Underflow Pointer Register	FC00 _H
SYSCON	b FF12 _H	89 _H	CPU System Configuration Register	¹⁾ 0XX0 _H
SYSCON2	b F1D0 _H E	E8 _H	CPU System Configuration Register 2	0000 _H
SYSCON3	b F1D4 _H E	EA _H	CPU System Configuration Register 3	0000 _H
T14	F0D2 _H E	69 _H	RTC Timer 14 Register	XXXX _H
T14REL	F0D0 _H E	68 _H	RTC Timer 14 Reload Register	XXXX _H
T2	FE40 _H	20 _H	GPT1 Timer 2 Register	0000 _H
T2CON	b FF40 _H	A0 _H	GPT1 Timer 2 Control Register	0000 _H
T2IC	b FF60 _H	B0 _H	GPT1 Timer 2 Interrupt Control Register	0000 _H
T3	FE42 _H	21 _H	GPT1 Timer 3 Register	0000 _H
T3CON	b FF42 _H	A1 _H	GPT1 Timer 3 Control Register	0000 _H
T3IC	b FF62 _H	B1 _H	GPT1 Timer 3 Interrupt Control Register	0000 _H
T4	FE44 _H	22 _H	GPT1 Timer 4 Register	0000 _H
T4CON	b FF44 _H	A2 _H	GPT1 Timer 4 Control Register	0000 _H
T4IC	b FF64 _H	B2 _H	GPT1 Timer 4 Interrupt Control Register	0000 _H
T5	FE46 _H	23 _H	GPT2 Timer 5 Register	0000 _H
T5CON	b FF46 _H	A3 _H	GPT2 Timer 5 Control Register	0000 _H

Functional Description
Table 6 C161S Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
T5IC	b FF66 _H	B3 _H	GPT2 Timer 5 Interrupt Control Register	0000 _H
T6	FE48 _H	24 _H	GPT2 Timer 6 Register	0000 _H
T6CON	b FF48 _H	A4 _H	GPT2 Timer 6 Control Register	0000 _H
T6IC	b FF68 _H	B4 _H	GPT2 Timer 6 Interrupt Control Register	0000 _H
TFR	b FFAC _H	D6 _H	Trap Flag Register	0000 _H
WDT	FEAE _H	57 _H	Watchdog Timer Register (read only)	0000 _H
WDTCON	b FFAE _H	D7 _H	Watchdog Timer Control Register	²⁾ 00XX _H
XP0IC	b F186 _H E	C3 _H	Software Interrupt Control Register	0000 _H
XP1IC	b F18E _H E	C7 _H	Software Interrupt Control Register	0000 _H
XP2IC	b F196 _H E	CB _H	Software Interrupt Control Register	0000 _H
XP3IC	b F19E _H E	CF _H	RTC/PLL Interrupt Control Register	0000 _H
ZEROS	b FF1C _H	8E _H	Constant Value 0's Register (read only)	0000 _H

1) The system configuration is selected during reset.

2) The reset value depends on the indicated reset source.

4 Electrical Parameters

4.1 Absolute Maximum Ratings

Table 7 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_J	-40	150	°C	under bias
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	-0.5	6.5	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	$V_{DD} + 0.5$	V	–
Input current on any pin during overload condition	I_{OV}	-10	10	mA	–
Absolute sum of all input currents during overload condition	$\Sigma I_{OV} $	–	100	mA	–
Power dissipation	P_{DISS}	–	1.5	W	–

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

4.2 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C161S. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 8 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Standard digital supply voltage	V_{DD}	4.5	5.5	V	Active mode, $f_{CPUmax} = 25$ MHz
		2.5 ¹⁾	5.5	V	Power down mode
Reduced digital supply voltage	V_{DD}	3.0	3.6	V	Active mode, $f_{CPUmax} = 20$ MHz
		2.5 ¹⁾	3.6	V	Power down mode
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	–	±5	mA	Per pin ²⁾³⁾
Absolute sum of overload currents	$\Sigma I_{OV} $	–	50	mA	³⁾
External Load Capacitance	C_L	–	100	pF	–
Ambient temperature	T_A	0	70	°C	SAB-C161S ...
		-40	85	°C	SAF-C161S ...
		-40	125	°C	SAK-C161S ...

1) Output voltages and output currents will be reduced when V_{DD} leaves the range defined for active mode.

2) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD} + 0.5$ V or $V_{OV} < V_{SS} - 0.5$ V). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltage must remain within the specified limits. Proper operation is not guaranteed if overload conditions occur on functional pins such as XTAL1, RD, \overline{WR} , etc.

3) Not subject to production test, verified by design/characterization.

4.3 Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C161S and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column "Symbol":

CC (Controller Characteristics):

The logic of the C161S will provide signals with the respective timing characteristics.

SR (System Requirement):

The external system must provide signals with the respective timing characteristics to the C161S.

4.4 DC Parameters
Table 9 DC Characteristics (Standard Supply Voltage Range)
 (Operating Conditions apply)¹⁾

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Input low voltage (TTL, all except XTAL1)	V_{IL}	SR	-0.5	$0.2 V_{DD} - 0.1$	V	–
Input low voltage XTAL1	V_{IL2}	SR	-0.5	$0.3 V_{DD}$	V	–
Input high voltage (TTL, all except \overline{RSTIN} and XTAL1)	V_{IH}	SR	$0.2 V_{DD} + 0.9$	$V_{DD} + 0.5$	V	–
Input high voltage \overline{RSTIN} (when operated as input)	V_{IH1}	SR	$0.6 V_{DD}$	$V_{DD} + 0.5$	V	–
Input high voltage XTAL1	V_{IH2}	SR	$0.7 V_{DD}$	$V_{DD} + 0.5$	V	–
Output low voltage (PORT0, PORT1, Port 4, ALE, \overline{RD} , \overline{WR} , \overline{BHE} , \overline{RSTOUT} , \overline{RSTIN} ²⁾)	V_{OL}	CC	–	0.45	V	$I_{OL} = 2.4 \text{ mA}$
Output low voltage (all other outputs)	V_{OL1}	CC	–	0.45	V	$I_{OL} = 1.6 \text{ mA}$
Output high voltage ³⁾ (PORT0, PORT1, Port 4, ALE, \overline{RD} , \overline{WR} , \overline{BHE} , \overline{RSTOUT})	V_{OH}	CC	2.4	–	V	$I_{OH} = -2.4 \text{ mA}$
			$0.9 V_{DD}$	–	V	$I_{OH} = -0.5 \text{ mA}$
Output high voltage ³⁾ (all other outputs)	V_{OH1}	CC	2.4	–	V	$I_{OH} = -1.6 \text{ mA}$
			$0.9 V_{DD}$	–	V	$I_{OH} = -0.5 \text{ mA}$
Input leakage current (Port 5)	I_{OZ1}	CC	–	± 200	nA	$0 \text{ V} < V_{IN} < V_{DD}$
Input leakage current (all other)	I_{OZ2}	CC	–	± 500	nA	$0.45 \text{ V} < V_{IN} < V_{DD}$
\overline{RSTIN} inactive current ⁴⁾	I_{RSTH} ⁵⁾		–	-10	μA	$V_{IN} = V_{IH1}$
\overline{RSTIN} active current ⁴⁾	I_{RSTL} ⁶⁾		-100	–	μA	$V_{IN} = V_{IL}$
$\overline{RD}/\overline{WR}$ inactive current ⁷⁾	I_{RWH} ⁵⁾		–	-40	μA	$V_{OUT} = 2.4 \text{ V}$
$\overline{RD}/\overline{WR}$ active current ⁷⁾	I_{RWL} ⁶⁾		-500	–	μA	$V_{OUT} = V_{OLmax}$
ALE inactive current ⁷⁾	I_{ALEL} ⁵⁾		–	40	μA	$V_{OUT} = V_{OLmax}$
ALE active current ⁷⁾	I_{ALEH} ⁶⁾		500	–	μA	$V_{OUT} = 2.4 \text{ V}$
Port 6 inactive current ⁷⁾	I_{P6H} ⁵⁾		–	-40	μA	$V_{OUT} = 2.4 \text{ V}$

Electrical Parameters
Table 9 DC Characteristics (Standard Supply Voltage Range) (cont'd)
 (Operating Conditions apply)¹⁾

Parameter	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
Port 6 active current ⁷⁾	I_{P6L} ⁶⁾	-500	–	μA	$V_{OUT} = V_{OL1max}$
PORT0 configuration current ⁷⁾	I_{POH} ⁵⁾	–	-10	μA	$V_{IN} = V_{IHmin}$
	I_{POL} ⁶⁾	-100	–	μA	$V_{IN} = V_{ILmax}$
XTAL1 input current	I_{IL} CC	–	±20	μA	$0\text{ V} < V_{IN} < V_{DD}$
Pin capacitance ⁸⁾ (digital inputs/outputs)	C_{IO} CC	–	10	pF	$f = 1\text{ MHz}$, $T_A = 25\text{ °C}$

- 1) Keeping signal levels within the levels specified in this table, ensures operation without overload conditions. For signal levels outside these specifications also refer to the specification of the overload current I_{OV} .
- 2) Valid in bidirectional reset mode only.
- 3) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.
- 4) These parameters describe the \overline{RSTIN} pull-up, which equals a resistance of ca. 50 to 250 kΩ.
- 5) The maximum current may be drawn while the respective signal line remains inactive.
- 6) The minimum current must be drawn in order to drive the respective signal line active.
- 7) This specification is only valid during Reset and Adapt Mode.
- 8) Not subject to production test, verified by design/characterization.

Electrical Parameters
Table 10 DC Characteristics (Reduced Supply Voltage Range)
 (Operating Conditions apply)¹⁾

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Input low voltage (TTL, all except XTAL1)	V_{IL}	SR	-0.5	0.8	V	–
Input low voltage XTAL1	V_{IL2}	SR	-0.5	$0.3 V_{DD}$	V	–
Input high voltage (TTL, all except \overline{RSTIN} and XTAL1)	V_{IH}	SR	1.8	$V_{DD} + 0.5$	V	–
Input high voltage \overline{RSTIN} (when operated as input)	V_{IH1}	SR	$0.6 V_{DD}$	$V_{DD} + 0.5$	V	–
Input high voltage XTAL1	V_{IH2}	SR	$0.7 V_{DD}$	$V_{DD} + 0.5$	V	–
Output low voltage (PORT0, PORT1, Port 4, ALE, \overline{RD} , \overline{WR} , \overline{BHE} , \overline{RSTOUT} , \overline{RSTIN} ²⁾)	V_{OL}	CC	–	0.45	V	$I_{OL} = 1.6 \text{ mA}$
Output low voltage (all other outputs)	V_{OL1}	CC	–	0.45	V	$I_{OL} = 1.0 \text{ mA}$
Output high voltage ³⁾ (PORT0, PORT1, Port 4, ALE, \overline{RD} , \overline{WR} , \overline{BHE} , \overline{RSTOUT})	V_{OH}	CC	$0.9 V_{DD}$	–	V	$I_{OH} = -0.5 \text{ mA}$
Output high voltage ³⁾ (all other outputs)	V_{OH1}	CC	$0.9 V_{DD}$	–	V	$I_{OH} = -0.25 \text{ mA}$
Input leakage current (Port 5)	I_{OZ1}	CC	–	± 200	nA	$0 \text{ V} < V_{IN} < V_{DD}$
Input leakage current (all other)	I_{OZ2}	CC	–	± 500	nA	$0.45 \text{ V} < V_{IN} < V_{DD}$
\overline{RSTIN} inactive current ⁴⁾	I_{RSTH} ⁵⁾		–	-10	μA	$V_{IN} = V_{IH1}$
\overline{RSTIN} active current ⁴⁾	I_{RSTL} ⁶⁾		-100	–	μA	$V_{IN} = V_{IL}$
$\overline{RD}/\overline{WR}$ inactive current ⁷⁾	I_{RWH} ⁵⁾		–	-10	μA	$V_{OUT} = 2.4 \text{ V}$
$\overline{RD}/\overline{WR}$ active current ⁷⁾	I_{RWL} ⁶⁾		-500	–	μA	$V_{OUT} = V_{OLmax}$
ALE inactive current ⁷⁾	I_{ALEL} ⁵⁾		–	20	μA	$V_{OUT} = V_{OLmax}$
ALE active current ⁷⁾	I_{ALEH} ⁶⁾		500	–	μA	$V_{OUT} = 2.4 \text{ V}$
Port 6 inactive current ⁷⁾	I_{P6H} ⁵⁾		–	-10	μA	$V_{OUT} = 2.4 \text{ V}$
Port 6 active current ⁷⁾	I_{P6L} ⁶⁾		-500	–	μA	$V_{OUT} = V_{OL1max}$

Electrical Parameters
Table 10 DC Characteristics (Reduced Supply Voltage Range) (cont'd)
 (Operating Conditions apply)¹⁾

Parameter	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
PORT0 configuration current ⁷⁾	I_{POH} ⁵⁾	–	-5	μA	$V_{IN} = V_{IHmin}$
	I_{POL} ⁶⁾	-100	–	μA	$V_{IN} = V_{ILmax}$
XTAL1 input current	I_{IL} CC	–	±20	μA	$0\text{ V} < V_{IN} < V_{DD}$
Pin capacitance ⁸⁾ (digital inputs/outputs)	C_{IO} CC	–	10	pF	$f = 1\text{ MHz}$, $T_A = 25\text{ °C}$

- 1) Keeping signal levels within the levels specified in this table, ensures operation without overload conditions. For signal levels outside these specifications also refer to the specification of the overload current I_{OV} .
- 2) Valid in bidirectional reset mode only.
- 3) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.
- 4) These parameters describe the \overline{RSTIN} pull-up, which equals a resistance of ca. 50 to 250 kΩ.
- 5) The maximum current may be drawn while the respective signal line remains inactive.
- 6) The minimum current must be drawn in order to drive the respective signal line active.
- 7) This specification is only valid during Reset and Adapt Mode.
- 8) Not subject to production test, verified by design/characterization.

Electrical Parameters
Table 11 Power Consumption C161S (Standard Supply Voltage Range)
 (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
Power supply current (active) with all peripherals active	I_{DD5}	–	15 + $1.8 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IL2}$ f_{CPU} in [MHz] ¹⁾
Idle mode supply current with all peripherals active	I_{IDX5}	–	3 + $0.6 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IH1}$ f_{CPU} in [MHz] ¹⁾
Idle mode supply current with all peripherals deactivated, PLL off, SDD factor = 32	I_{IDO5} ²⁾	–	500 + $50 \times f_{OSC}$	μA	$\overline{RSTIN} = V_{IH1}$ f_{OSC} in [MHz] ¹⁾
Sleep and Power down mode supply current with RTC running	I_{PDR5} ²⁾	–	200 + $25 \times f_{OSC}$	μA	$V_{DD} = V_{DDmax}$ f_{OSC} in [MHz] ³⁾
Sleep and Power down mode supply current with RTC disabled	I_{PDO5}	–	50	μA	$V_{DD} = V_{DDmax}$ ³⁾

- 1) The supply current is a function of the operating frequency. This dependency is illustrated in [Figure 8](#). These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH} .
- 2) This parameter is determined mainly by the current consumed by the oscillator (see [Figure 9](#)). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The values given refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.
- 3) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at $V_{DD} - 0.1$ V to V_{DD} , $V_{REF} = 0$ V, all outputs (including pins configured as outputs) disconnected.

Electrical Parameters
Table 12 Power Consumption C161S (Reduced Supply Voltage Range)
 (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
Power supply current (active) with all peripherals active	I_{DD3}	–	7 + $1.2 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IL2}$ f_{CPU} in [MHz] ¹⁾
Idle mode supply current with all peripherals active	I_{IDX3}	–	1 + $0.4 \times f_{CPU}$	mA	$\overline{RSTIN} = V_{IH1}$ f_{CPU} in [MHz] ¹⁾
Idle mode supply current with all peripherals deactivated, PLL off, SDD factor = 32	I_{IDO3} ²⁾	–	300 + $30 \times f_{OSC}$	μA	$\overline{RSTIN} = V_{IH1}$ f_{OSC} in [MHz] ¹⁾
Sleep and Power down mode supply current with RTC running	I_{PDR3} ²⁾	–	100 + $10 \times f_{OSC}$	μA	$V_{DD} = V_{DDmax}$ f_{OSC} in [MHz] ³⁾
Sleep and Power down mode supply current with RTC disabled	I_{PDO3}	–	30	μA	$V_{DD} = V_{DDmax}$ ³⁾

- 1) The supply current is a function of the operating frequency. This dependency is illustrated in [Figure 8](#). These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH} .
- 2) This parameter is determined mainly by the current consumed by the oscillator (see [Figure 9](#)). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The values given refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.
- 3) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at $V_{DD} - 0.1$ V to V_{DD} , $V_{REF} = 0$ V, all outputs (including pins configured as outputs) disconnected.

Electrical Parameters

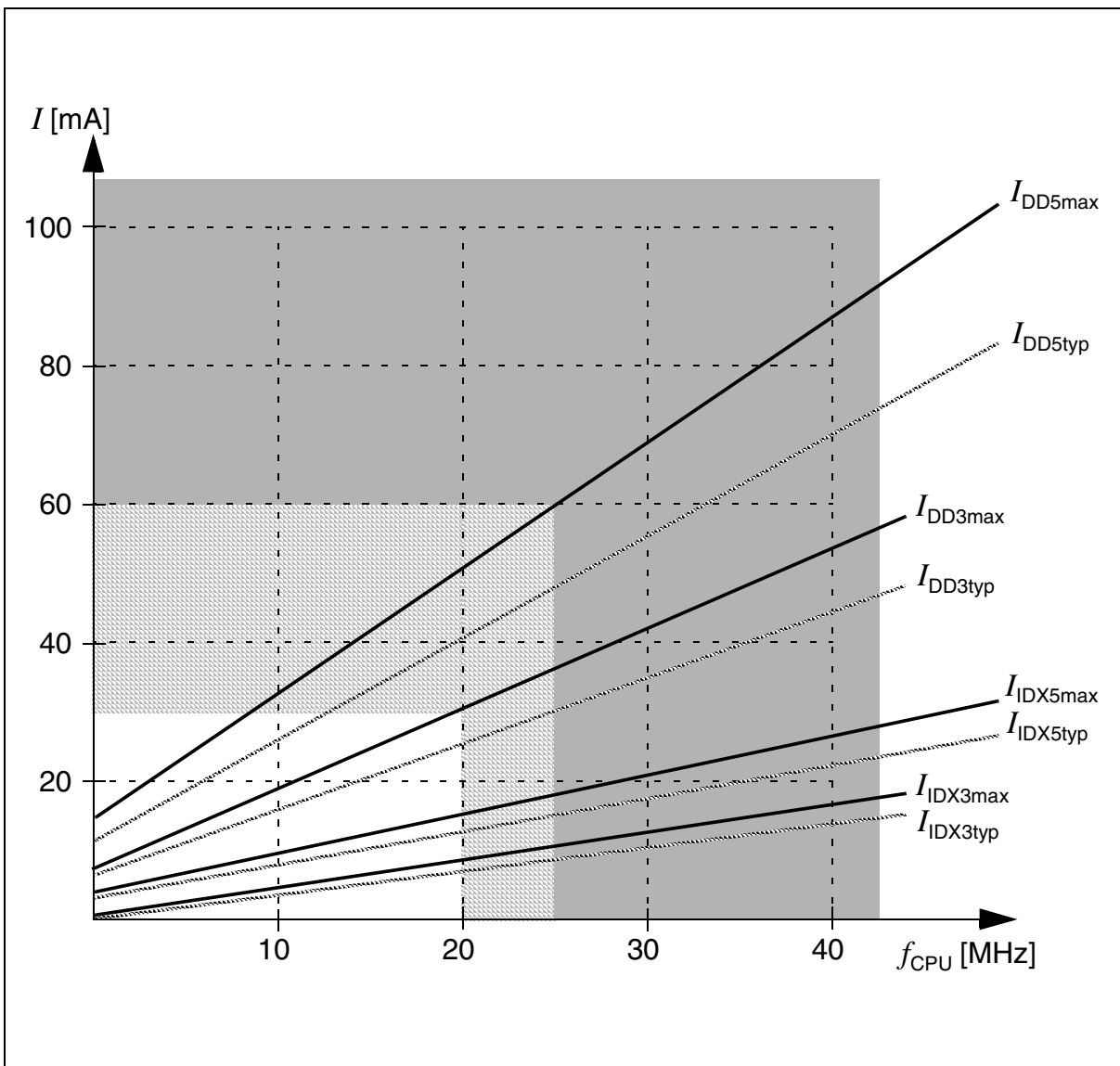


Figure 8 Supply and Idle Current as a Function of Operating Frequency

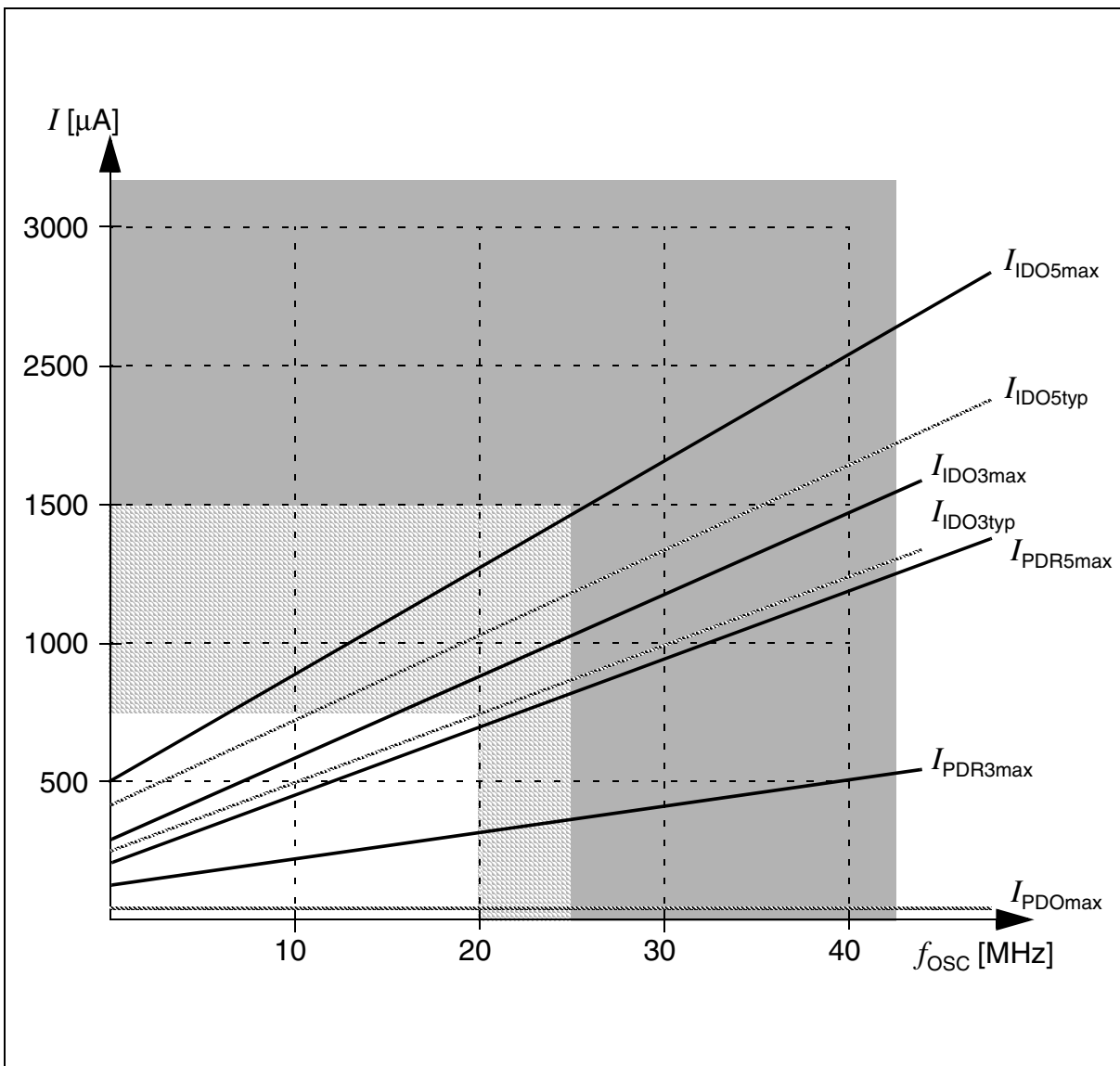


Figure 9 Sleep and Power Down Supply Current as a Function of Oscillator Frequency

5 Timing Characteristics

5.1 Definition of Internal Timing

The internal operation of the C161S is controlled by the internal CPU clock f_{CPU} . Both edges of the CPU clock can trigger internal (e.g. pipeline) or external (e.g. bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called “TCL” (see [Figure 10](#)).

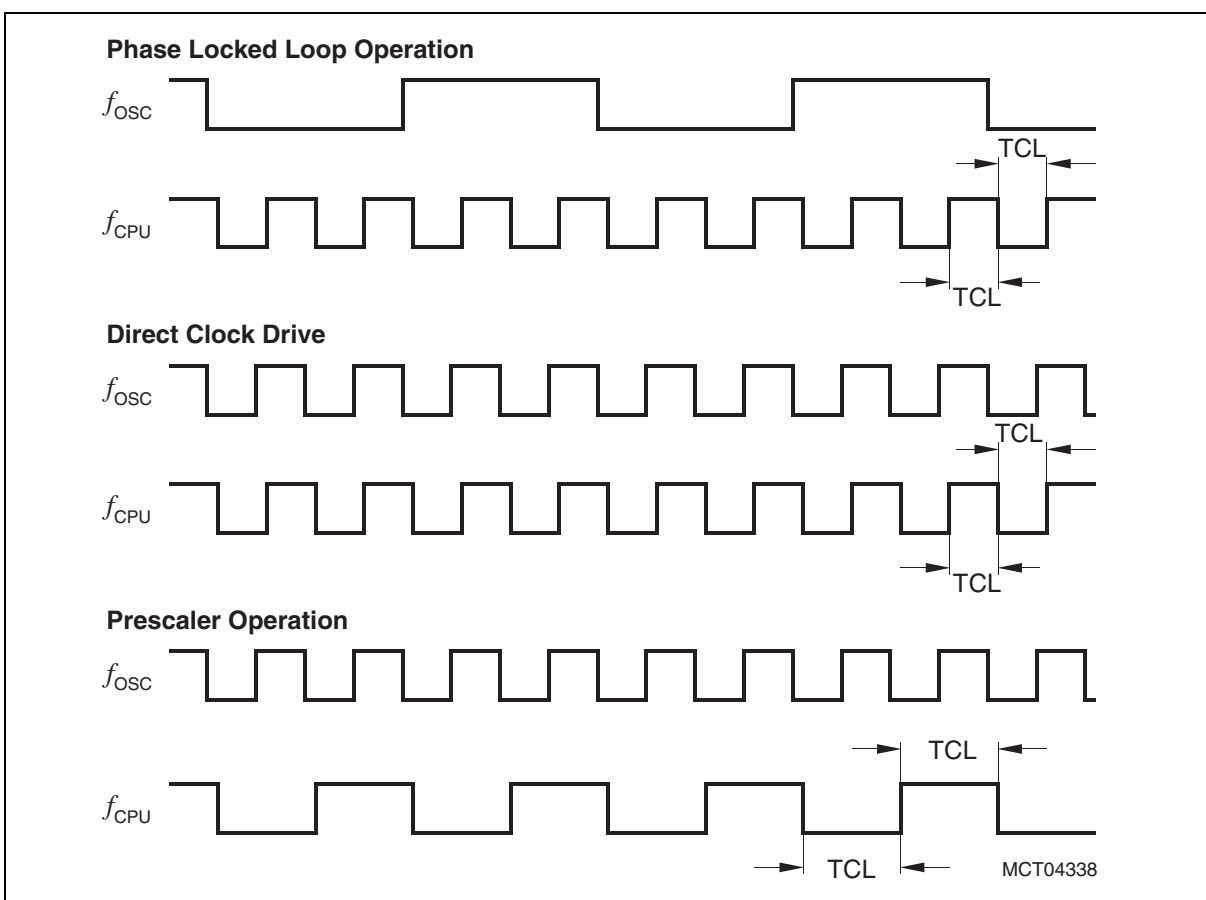


Figure 10 Generation Mechanisms for the CPU Clock

The CPU clock signal f_{CPU} can be generated from the oscillator clock signal f_{OSC} via different mechanisms. The duration of TCLs and their variation (and also the derived external timing) depends on the used mechanism to generate f_{CPU} . This influence must be regarded when calculating the timings for the C161S.

Note: The example for PLL operation shown in [Figure 10](#) refers to a PLL factor of 4.

The used mechanism to generate the basic CPU clock is selected by bitfield CLKCFG in register RP0H.7-5. Upon a long hardware reset register RP0H is loaded with the logic

Timing Characteristics

levels present on the upper half of PORT0 (P0H), i.e. bitfield CLKCFG represents the logic levels on pins P0.15-13 (P0H.7-5).

Table 13 associates the combinations of these three bits with the respective clock generation mode.

Table 13 C161S Clock Generation Modes

CLKCFG (P0H.7-5)	CPU Frequency $f_{\text{CPU}} = f_{\text{OSC}} \times F$	External Clock Input Range ¹⁾	Notes
1 1 1	$f_{\text{OSC}} \times 4$	2.5 to 6.25 MHz	Default configuration
1 1 0	$f_{\text{OSC}} \times 3$	3.33 to 8.33 MHz	–
1 0 1	$f_{\text{OSC}} \times 2$	5 to 12.5 MHz	–
1 0 0	$f_{\text{OSC}} \times 5$	2 to 5 MHz	–
0 1 1	$f_{\text{OSC}} \times 1$	1 to 25 MHz	Direct drive ²⁾
0 1 0	$f_{\text{OSC}} \times 1.5$	6.66 to 16.67 MHz	–
0 0 1	$f_{\text{OSC}} / 2$	2 to 50 MHz	CPU clock via prescaler
0 0 0	$f_{\text{OSC}} \times 2.5$	4 to 10 MHz	–

1) The external clock input range refers to a CPU clock range of 10 ... 25 MHz (PLL operation). If the on-chip oscillator is used together with a crystal, the oscillator frequency is limited to a range of 4 MHz to 16 MHz.

2) The maximum frequency depends on the duty cycle of the external clock signal.

Prescaler Operation

When prescaler operation is configured (CLKCFG = 001_B) the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.

The frequency of f_{CPU} is half the frequency of f_{OSC} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{OSC} .

The timings listed in the AC Characteristics that refer to TCLs therefore can be calculated using the period of f_{OSC} for any TCL.

Phase Locked Loop

When PLL operation is configured (via CLKCFG) the on-chip phase locked loop is enabled and provides the CPU clock (see **Table 13**). The PLL multiplies the input frequency by the factor **F** which is selected via the combination of pins P0.15-13 (i.e. $f_{\text{CPU}} = f_{\text{OSC}} \times F$). With every **F**'th transition of f_{OSC} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, i.e. the CPU clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{OSC} . The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

Timing Characteristics

The timings listed in the AC Characteristics that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances.

The actual minimum value for TCL depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCL is lower than for one single TCL (see formula and **Figure 11**).

For a period of $N \times \text{TCL}$ the minimum value is computed using the corresponding deviation D_N :

$$(N \times \text{TCL})_{\min} = N \times \text{TCL}_{\text{NOM}} - D_N, \quad D_N [\text{ns}] = \pm(13.3 + N \times 6.3) / f_{\text{CPU}} [\text{MHz}] \quad (1)$$

where N = number of consecutive TCLs and $1 \leq N \leq 40$.

So for a period of 3 TCLs @ 20 MHz (i.e. $N = 3$): $D_3 = (13.3 + 3 \times 6.3) / 20 = 1.61 \text{ ns}$, and $(3\text{TCL})_{\min} = 3\text{TCL}_{\text{NOM}} - 1.61 \text{ ns} = 73.39 \text{ ns}$ (@ $f_{\text{CPU}} = 20 \text{ MHz}$).

This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

*Note: For all periods longer than 40 TCL the $N = 40$ value can be used (see **Figure 11**).*

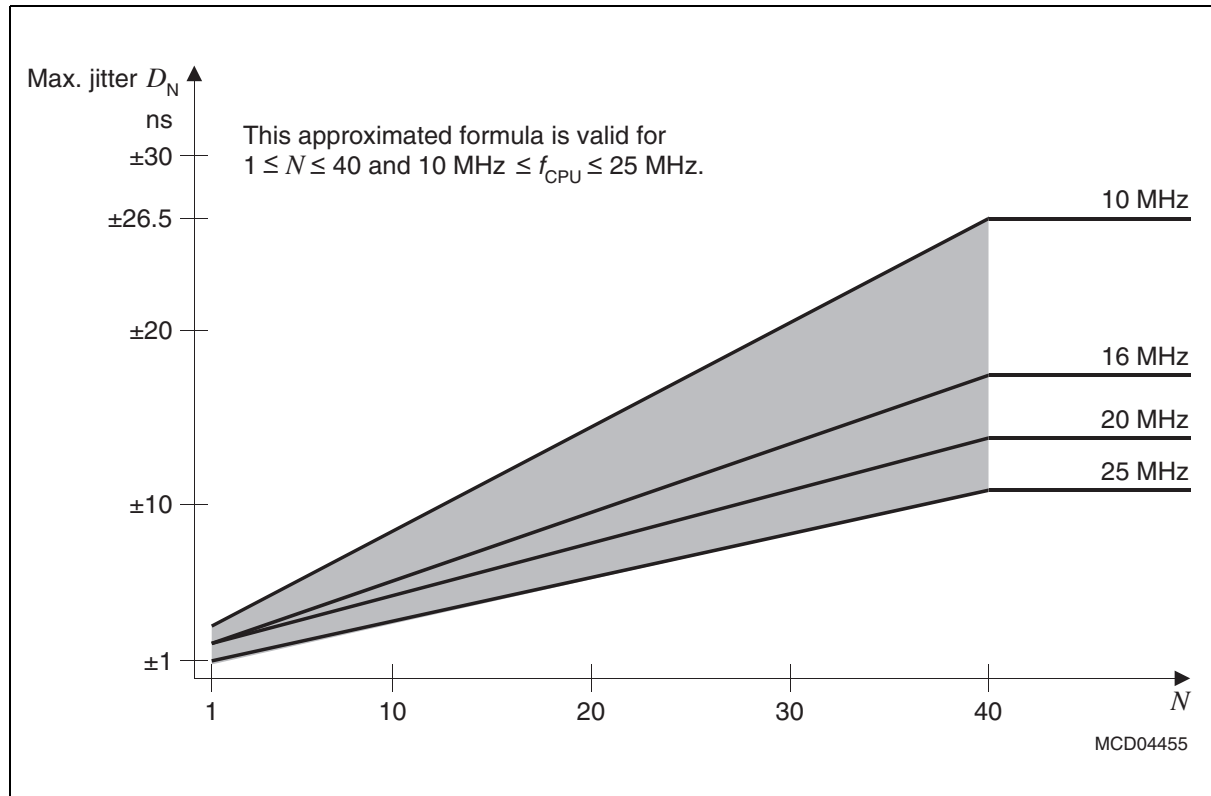


Figure 11 Approximated Maximum Accumulated PLL Jitter

Direct Drive

When direct drive is configured (CLKCFG = 011_B) the on-chip phase locked loop is disabled and the CPU clock is directly driven from the internal oscillator with the input clock signal.

The frequency of f_{CPU} directly follows the frequency of f_{OSC} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{OSC} .

The timings listed below that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances. This minimum value can be calculated via the following formula:

$$\text{TCL}_{\text{min}} = 1/f_{\text{OSC}} \times \text{DC}_{\text{min}} \quad (\text{DC} = \text{duty cycle}) \quad (2)$$

For two consecutive TCLs the deviation caused by the duty cycle of f_{OSC} is compensated so the duration of 2TCL is always $1/f_{\text{OSC}}$. The minimum value TCL_{min} therefore has to be used only once for timings that require an odd number of TCLs (1, 3, ...). Timings that require an even number of TCLs (2, 4, ...) may use the formula $2\text{TCL} = 1/f_{\text{OSC}}$.

5.2 External Clock Drive XTAL1

Table 14 External Clock Drive XTAL1 (Operating Conditions apply)

Parameter	Symbol	SR	Direct Drive 1:1		Prescaler 2:1		PLL 1:N		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Oscillator period	t_{OSC}		40	–	20	–	60 ¹⁾	500 ¹⁾	ns
High time ²⁾	t_1		20 ³⁾	–	5	–	10	–	ns
Low time ²⁾	t_2		20 ³⁾	–	5	–	10	–	ns
Rise time ²⁾	t_3		–	8	–	5	–	10	ns
Fall time ²⁾	t_4		–	8	–	5	–	10	ns

- 1) The minimum and maximum oscillator periods for PLL operation depend on the selected CPU clock generation mode. Please see respective table above.
- 2) The clock input signal must reach the defined levels V_{IL2} and V_{IH2} .
- 3) The minimum high and low time refers to a duty cycle of 50%. The maximum operating frequency (f_{CPU}) in direct drive mode depends on the duty cycle of the clock input signal.

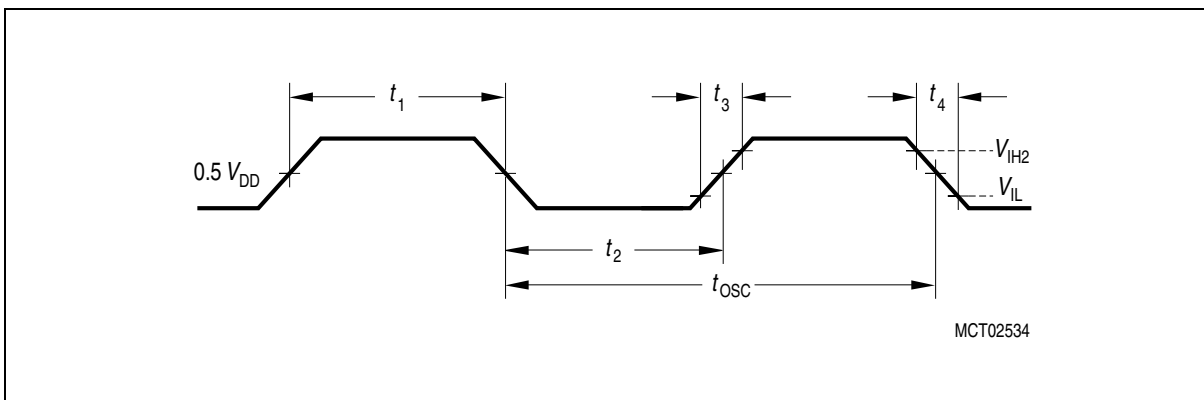


Figure 12 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal, the oscillator frequency is limited to a range of 4 MHz to 16 MHz.

It is strongly recommended to measure the oscillation allowance (or margin) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.

When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is verified by design only (not tested in production).

5.3 Testing Waveforms

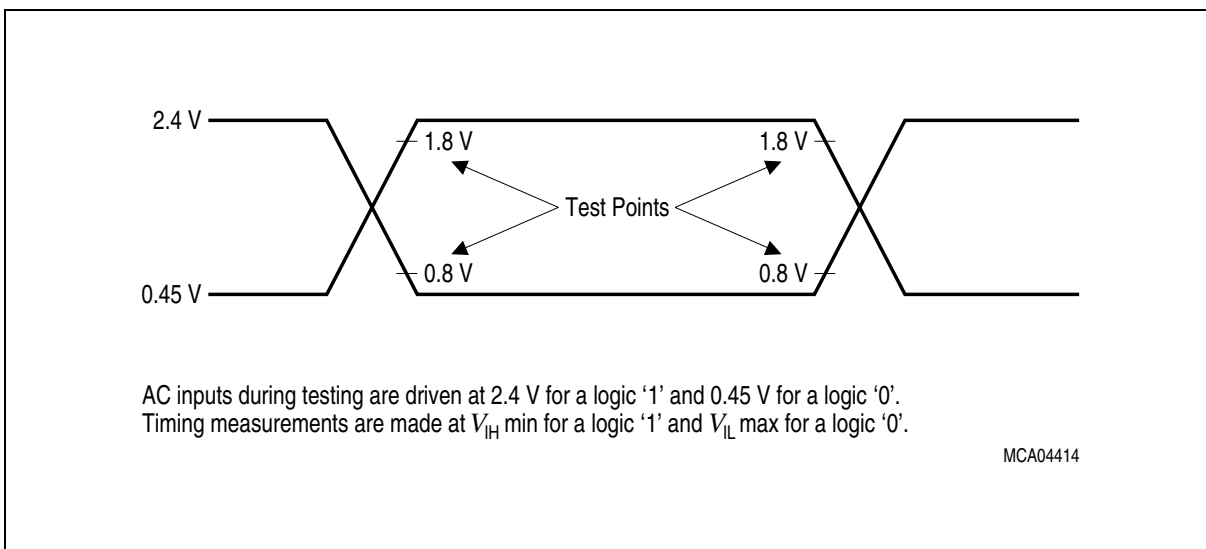


Figure 13 Input Output Waveforms

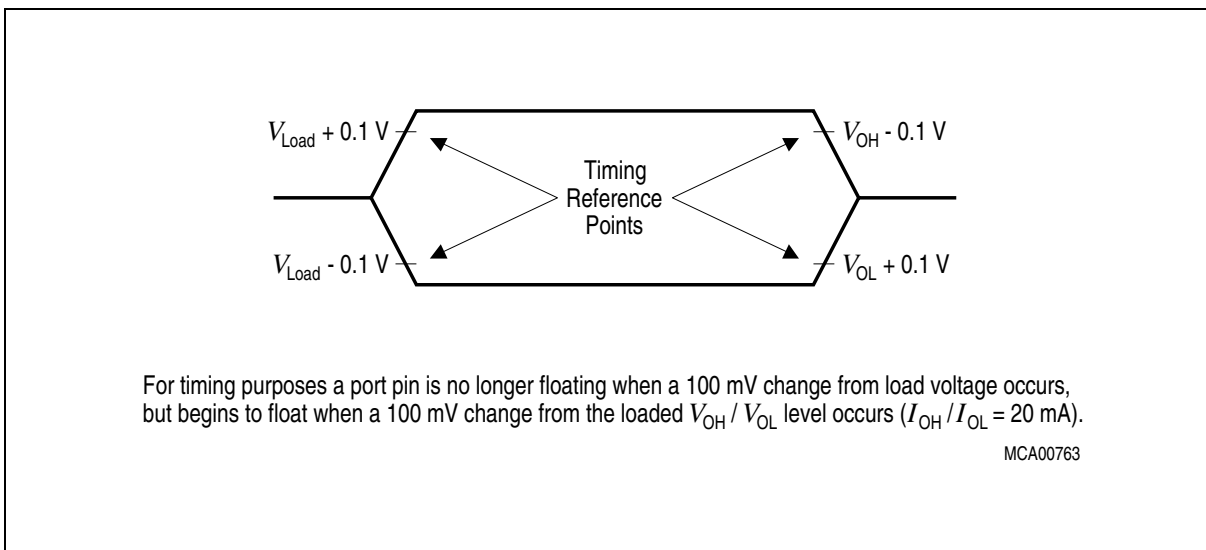


Figure 14 Float Waveforms

Timing Characteristics
Memory Cycle Variables

The timing tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. **Table 15** describes, how these variables are to be computed.

Table 15 Memory Cycle Variables

Description	Symbol	Values
ALE Extension	t_A	$TCL \times \langle ALECTL \rangle$
Memory Cycle Time Waitstates	t_C	$2TCL \times (15 - \langle MCTC \rangle)$
Memory Tristate Time	t_F	$2TCL \times (1 - \langle MTTC \rangle)$

Note: Please respect the maximum operating frequency of the respective derivative.

5.4 AC Characteristics
Table 16 Multiplexed Bus (Standard Supply Voltage Range)
 (Operating Conditions apply)

ALE cycle time = $6 \text{ TCL} + 2t_A + t_C + t_F$ (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol	Max. CPU Clock = 25 MHz	Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit	
			Min.	Max.		Min.
ALE high time	t_5 CC	$10 + t_A$	–	TCL - 10 + t_A	–	ns
Address setup to ALE	t_6 CC	$4 + t_A$	–	TCL - 16 + t_A	–	ns
Address hold after ALE	t_7 CC	$10 + t_A$	–	TCL - 10 + t_A	–	ns
ALE falling edge to \overline{RD} , \overline{WR} (with RW-delay)	t_8 CC	$10 + t_A$	–	TCL - 10 + t_A	–	ns
ALE falling edge to \overline{RD} , \overline{WR} (no RW-delay)	t_9 CC	$-10 + t_A$	–	$-10 + t_A$	–	ns
Address float after \overline{RD} , \overline{WR} (with RW-delay)	t_{10} CC	–	6	–	6	ns
Address float after \overline{RD} , \overline{WR} (no RW-delay)	t_{11} CC	–	26	–	TCL + 6	ns

Timing Characteristics
Table 16 Multiplexed Bus (Standard Supply Voltage Range) (cont'd)
 (Operating Conditions apply)

 ALE cycle time = $6 \text{ TCL} + 2t_A + t_C + t_F$ (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			Min.	Max.	Min.	Max.	
$\overline{\text{RD}}, \overline{\text{WR}}$ low time (with RW-delay)	t_{12}	CC	$30 + t_C$	–	$2\text{TCL} - 10$ $+ t_C$	–	ns
$\overline{\text{RD}}, \overline{\text{WR}}$ low time (no RW-delay)	t_{13}	CC	$50 + t_C$	–	$3\text{TCL} - 10$ $+ t_C$	–	ns
$\overline{\text{RD}}$ to valid data in (with RW-delay)	t_{14}	SR	–	$20 + t_C$	–	$2\text{TCL} - 20$ $+ t_C$	ns
$\overline{\text{RD}}$ to valid data in (no RW-delay)	t_{15}	SR	–	$40 + t_C$	–	$3\text{TCL} - 20$ $+ t_C$	ns
ALE low to valid data in	t_{16}	SR	–	$40 + t_A$ $+ t_C$	–	$3\text{TCL} - 20$ $+ t_A + t_C$	ns
Address to valid data in	t_{17}	SR	–	$50 + 2t_A$ $+ t_C$	–	$4\text{TCL} - 30$ $+ 2t_A + t_C$	ns
Data hold after $\overline{\text{RD}}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{\text{RD}}$	t_{19}	SR	–	$26 + t_F$	–	$2\text{TCL} - 14$ $+ t_F$	ns
Data valid to $\overline{\text{WR}}$	t_{22}	CC	$20 + t_C$	–	$2\text{TCL} - 20$ $+ t_C$	–	ns
Data hold after $\overline{\text{WR}}$	t_{23}	CC	$26 + t_F$	–	$2\text{TCL} - 14$ $+ t_F$	–	ns
ALE rising edge after $\overline{\text{RD}},$ $\overline{\text{WR}}$	t_{25}	CC	$26 + t_F$	–	$2\text{TCL} - 14$ $+ t_F$	–	ns
Address hold after $\overline{\text{RD}},$ $\overline{\text{WR}}$	t_{27}	CC	$26 + t_F$	–	$2\text{TCL} - 14$ $+ t_F$	–	ns
ALE falling edge to $\overline{\text{CS}}^{(1)}$	t_{38}	CC	$-4 - t_A$	$10 - t_A$	$-4 - t_A$	$10 - t_A$	ns
$\overline{\text{CS}}$ low to Valid Data In ⁽¹⁾	t_{39}	SR	–	$40 + t_C$ $+ 2t_A$	–	$3\text{TCL} - 20$ $+ t_C + 2t_A$	ns
$\overline{\text{CS}}$ hold after $\overline{\text{RD}}, \overline{\text{WR}}^{(1)}$	t_{40}	CC	$46 + t_F$	–	$3\text{TCL} - 14$ $+ t_F$	–	ns

Timing Characteristics
Table 16 Multiplexed Bus (Standard Supply Voltage Range) (cont'd)
 (Operating Conditions apply)

 ALE cycle time = $6 \text{ TCL} + 2t_A + t_C + t_F$ (120 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			Min.	Max.	Min.	Max.	
ALE fall. edge to $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (with RW delay)	t_{42}	CC	$16 + t_A$	–	TCL - 4 + t_A	–	ns
ALE fall. edge to $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (no RW delay)	t_{43}	CC	$-4 + t_A$	–	-4 + t_A	–	ns
Address float after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (with RW delay)	t_{44}	CC	–	0	–	0	ns
Address float after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (no RW delay)	t_{45}	CC	–	20	–	TCL	ns
$\overline{\text{RdCS}}$ to Valid Data In (with RW delay)	t_{46}	SR	–	$16 + t_C$	–	$2\text{TCL} - 24$ + t_C	ns
$\overline{\text{RdCS}}$ to Valid Data In (no RW delay)	t_{47}	SR	–	$36 + t_C$	–	$3\text{TCL} - 24$ + t_C	ns
$\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ Low Time (with RW delay)	t_{48}	CC	$30 + t_C$	–	$2\text{TCL} - 10$ + t_C	–	ns
$\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ Low Time (no RW delay)	t_{49}	CC	$50 + t_C$	–	$3\text{TCL} - 10$ + t_C	–	ns
Data valid to $\overline{\text{WrCS}}$	t_{50}	CC	$26 + t_C$	–	$2\text{TCL} - 14$ + t_C	–	ns
Data hold after $\overline{\text{RdCS}}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{\text{RdCS}}$	t_{52}	SR	–	$20 + t_F$	–	$2\text{TCL} - 20$ + t_F	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{54}	CC	$20 + t_F$	–	$2\text{TCL} - 20$ + t_F	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{56}	CC	$20 + t_F$	–	$2\text{TCL} - 20$ + t_F	–	ns

 1) These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).

Timing Characteristics
Table 17 Multiplexed Bus (Reduced Supply Voltage Range)
 (Operating Conditions apply)

 ALE cycle time = $6 \text{ TCL} + 2t_A + t_C + t_F$ (150 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			Min.	Max.	Min.	Max.	
ALE high time	t_5	CC	$11 + t_A$	–	TCL - 14 + t_A	–	ns
Address setup to ALE	t_6	CC	$5 + t_A$	–	TCL - 20 + t_A	–	ns
Address hold after ALE	t_7	CC	$15 + t_A$	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{\text{RD}}$, $\overline{\text{WR}}$ (with RW-delay)	t_8	CC	$15 + t_A$	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{\text{RD}}$, $\overline{\text{WR}}$ (no RW-delay)	t_9	CC	$-10 + t_A$	–	$-10 + t_A$	–	ns
Address float after $\overline{\text{RD}}$, $\overline{\text{WR}}$ (with RW-delay)	t_{10}	CC	–	6	–	6	ns
Address float after $\overline{\text{RD}}$, $\overline{\text{WR}}$ (no RW-delay)	t_{11}	CC	–	31	–	TCL + 6	ns
$\overline{\text{RD}}$, $\overline{\text{WR}}$ low time (with RW-delay)	t_{12}	CC	$34 + t_C$	–	$2\text{TCL} - 16$ + t_C	–	ns
$\overline{\text{RD}}$, $\overline{\text{WR}}$ low time (no RW-delay)	t_{13}	CC	$59 + t_C$	–	$3\text{TCL} - 16$ + t_C	–	ns
$\overline{\text{RD}}$ to valid data in (with RW-delay)	t_{14}	SR	–	$22 + t_C$	–	$2\text{TCL} - 28$ + t_C	ns
$\overline{\text{RD}}$ to valid data in (no RW-delay)	t_{15}	SR	–	$47 + t_C$	–	$3\text{TCL} - 28$ + t_C	ns
ALE low to valid data in	t_{16}	SR	–	$45 + t_A$ + t_C	–	$3\text{TCL} - 30$ + $t_A + t_C$	ns
Address to valid data in	t_{17}	SR	–	$57 + 2t_A$ + t_C	–	$4\text{TCL} - 43$ + $2t_A + t_C$	ns
Data hold after $\overline{\text{RD}}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{\text{RD}}$	t_{19}	SR	–	$36 + t_F$	–	$2\text{TCL} - 14$ + t_F	ns

Timing Characteristics
Table 17 Multiplexed Bus (Reduced Supply Voltage Range) (cont'd)
 (Operating Conditions apply)

 ALE cycle time = $6 \text{ TCL} + 2t_A + t_C + t_F$ (150 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			Min.	Max.	Min.	Max.	
Data valid to $\overline{\text{WR}}$	t_{22}	CC	$24 + t_C$	–	$2\text{TCL} - 26$ $+ t_C$	–	ns
Data hold after $\overline{\text{WR}}$	t_{23}	CC	$36 + t_F$	–	$2\text{TCL} - 14$ $+ t_F$	–	ns
ALE rising edge after $\overline{\text{RD}}$, $\overline{\text{WR}}$	t_{25}	CC	$36 + t_F$	–	$2\text{TCL} - 14$ $+ t_F$	–	ns
Address hold after $\overline{\text{RD}}$, $\overline{\text{WR}}$	t_{27}	CC	$36 + t_F$	–	$2\text{TCL} - 14$ $+ t_F$	–	ns
ALE falling edge to $\overline{\text{CS}}^{(1)}$	t_{38}	CC	$-8 - t_A$	$10 - t_A$	$-8 - t_A$	$10 - t_A$	ns
$\overline{\text{CS}}$ low to Valid Data In ⁽¹⁾	t_{39}	SR	–	$47 + t_C$ $+ 2t_A$	–	$3\text{TCL} - 28$ $+ t_C + 2t_A$	ns
$\overline{\text{CS}}$ hold after $\overline{\text{RD}}$, $\overline{\text{WR}}^{(1)}$	t_{40}	CC	$57 + t_F$	–	$3\text{TCL} - 18$ $+ t_F$	–	ns
ALE fall. edge to $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (with RW delay)	t_{42}	CC	$19 + t_A$	–	$\text{TCL} - 6$ $+ t_A$	–	ns
ALE fall. edge to $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (no RW delay)	t_{43}	CC	$-6 + t_A$	–	-6 $+ t_A$	–	ns
Address float after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (with RW delay)	t_{44}	CC	–	0	–	0	ns
Address float after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (no RW delay)	t_{45}	CC	–	25	–	TCL	ns
$\overline{\text{RdCS}}$ to Valid Data In (with RW delay)	t_{46}	SR	–	$20 + t_C$	–	$2\text{TCL} - 30$ $+ t_C$	ns
$\overline{\text{RdCS}}$ to Valid Data In (no RW delay)	t_{47}	SR	–	$45 + t_C$	–	$3\text{TCL} - 30$ $+ t_C$	ns
$\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ Low Time (with RW delay)	t_{48}	CC	$38 + t_C$	–	$2\text{TCL} - 12$ $+ t_C$	–	ns
$\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ Low Time (no RW delay)	t_{49}	CC	$63 + t_C$	–	$3\text{TCL} - 12$ $+ t_C$	–	ns

Timing Characteristics
Table 17 Multiplexed Bus (Reduced Supply Voltage Range) (cont'd)
 (Operating Conditions apply)

 ALE cycle time = $6 \text{ TCL} + 2t_A + t_C + t_F$ (150 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			Min.	Max.	Min.	Max.	
Data valid to $\overline{\text{WrCS}}$	t_{50}	CC	$28 + t_C$	–	$2\text{TCL} - 22$ $+ t_C$	–	ns
Data hold after $\overline{\text{RdCS}}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{\text{RdCS}}$	t_{52}	SR	–	$30 + t_F$	–	$2\text{TCL} - 20$ $+ t_F$	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{54}	CC	$30 + t_F$	–	$2\text{TCL} - 20$ $+ t_F$	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{56}	CC	$30 + t_F$	–	$2\text{TCL} - 20$ $+ t_F$	–	ns

 1) These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).

Timing Characteristics

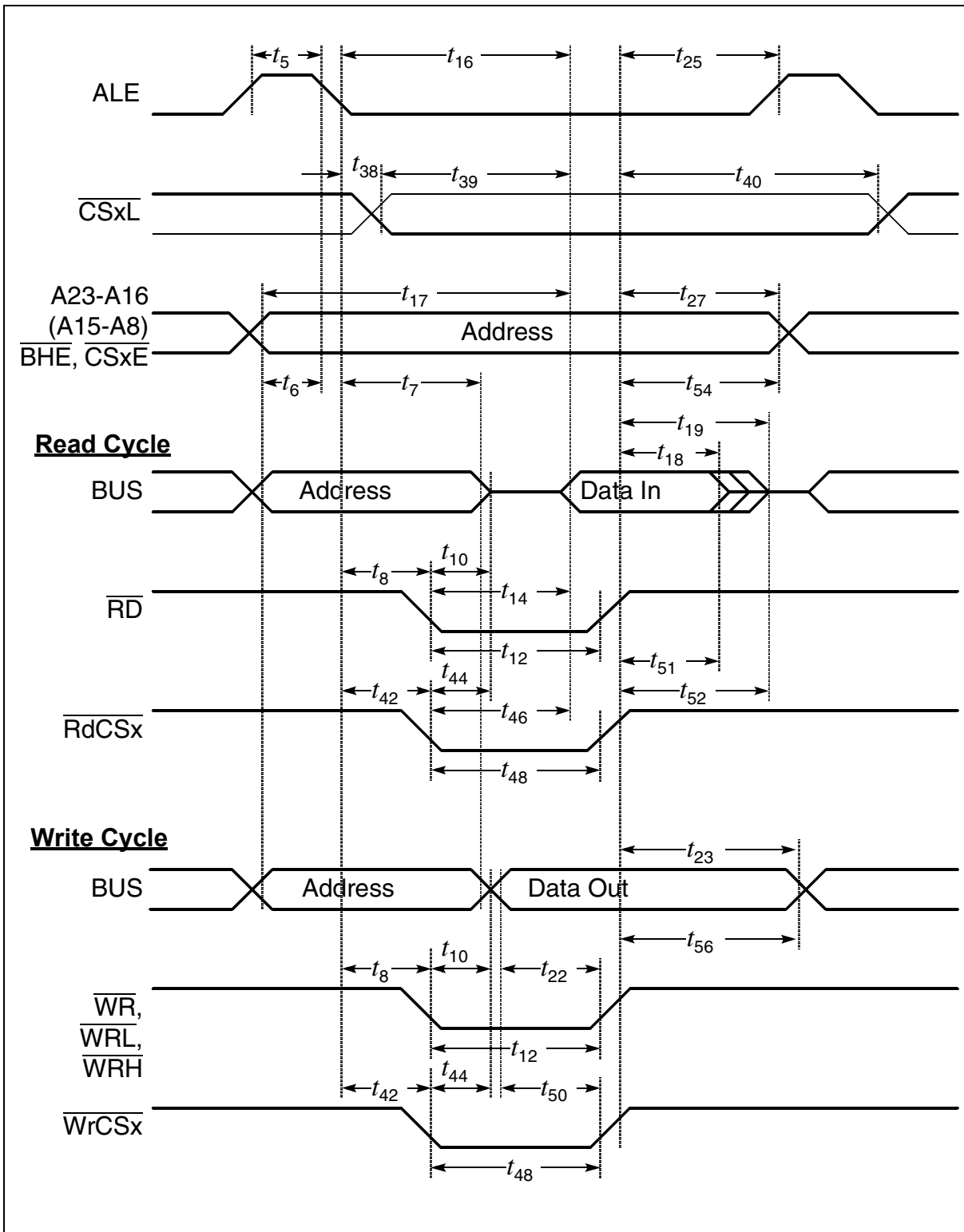


Figure 15 External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Normal ALE

Timing Characteristics

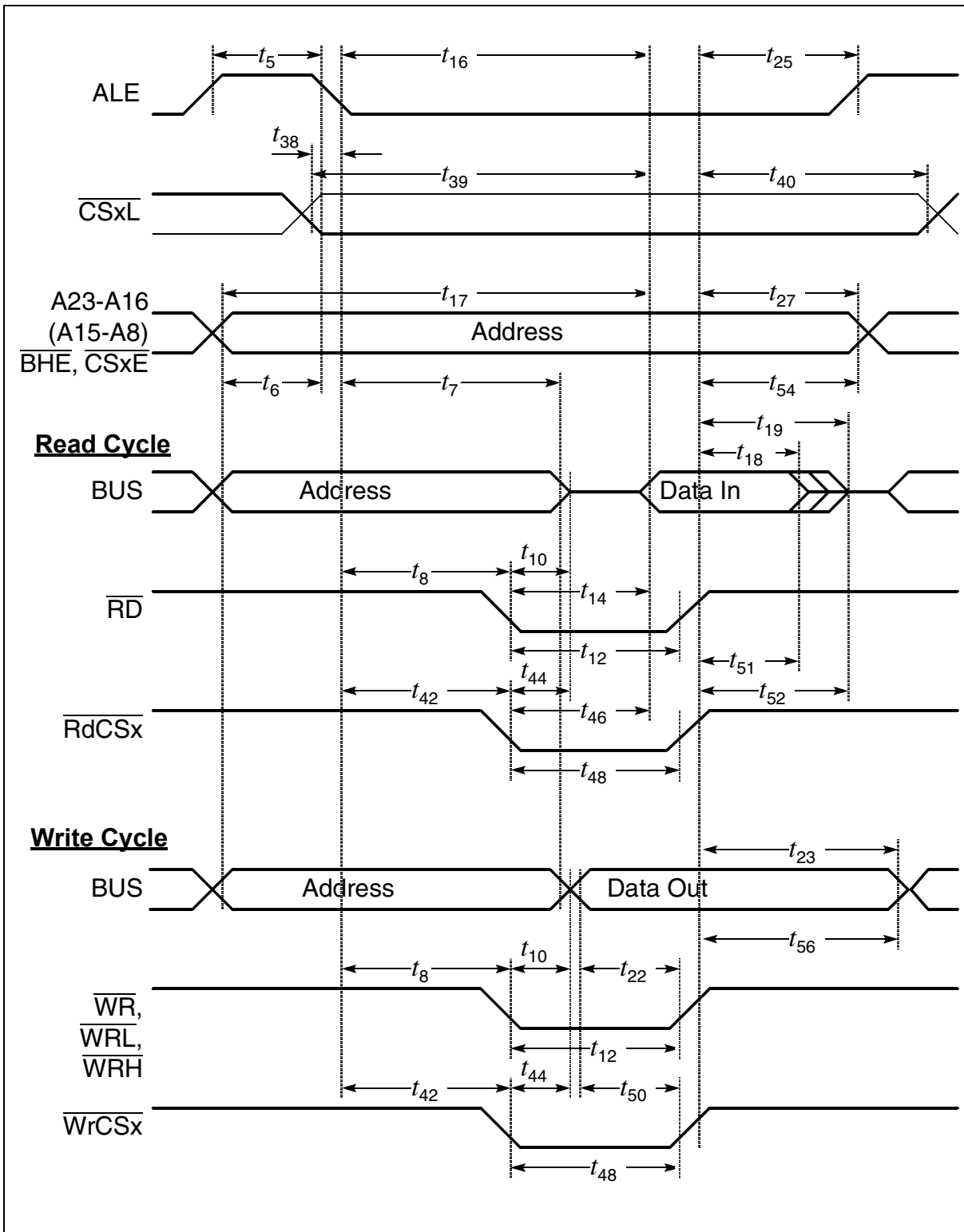


Figure 16 External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Extended ALE

Timing Characteristics

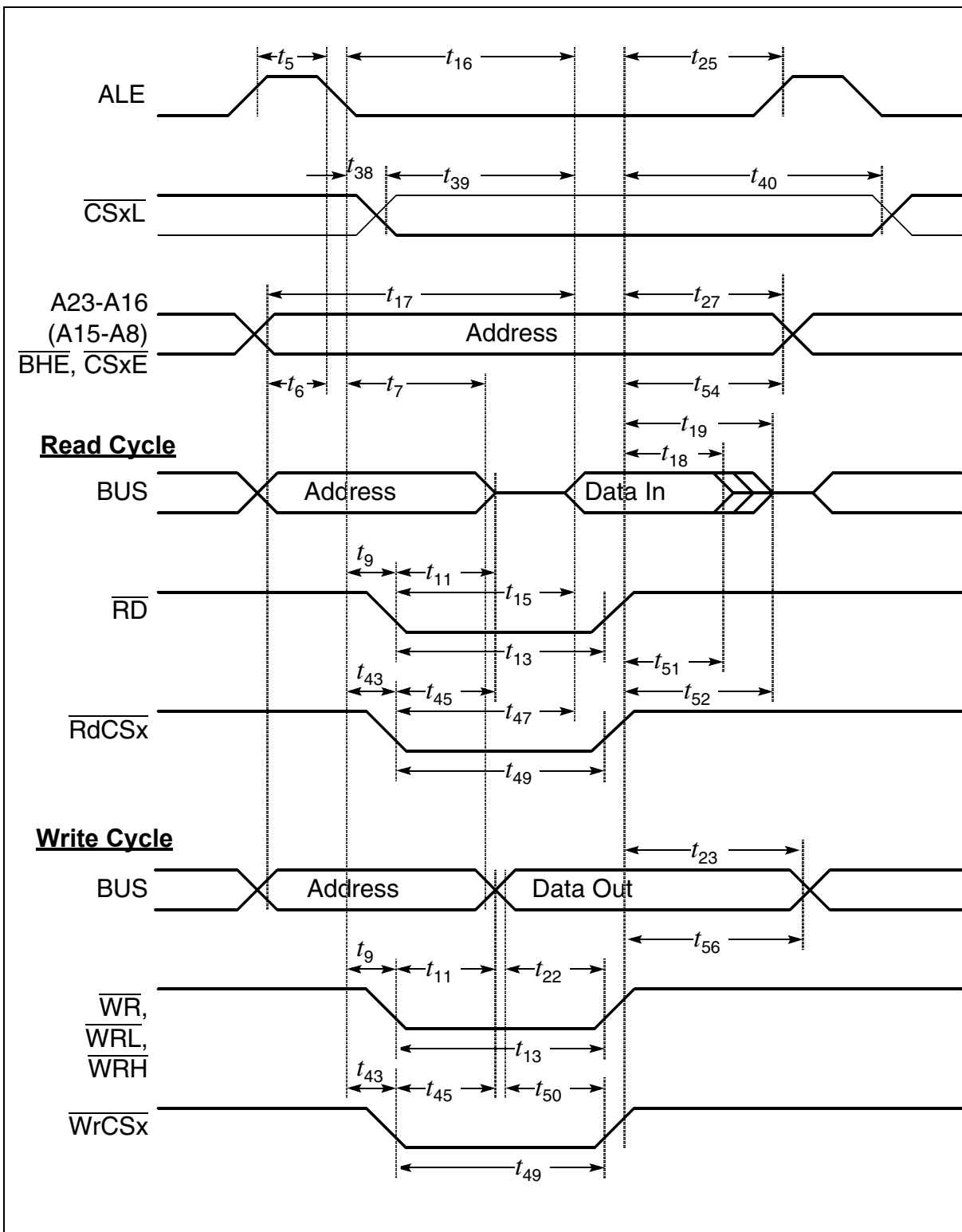


Figure 17 External Memory Cycle: Multiplexed Bus, No Read/Write Delay, Normal ALE

Timing Characteristics

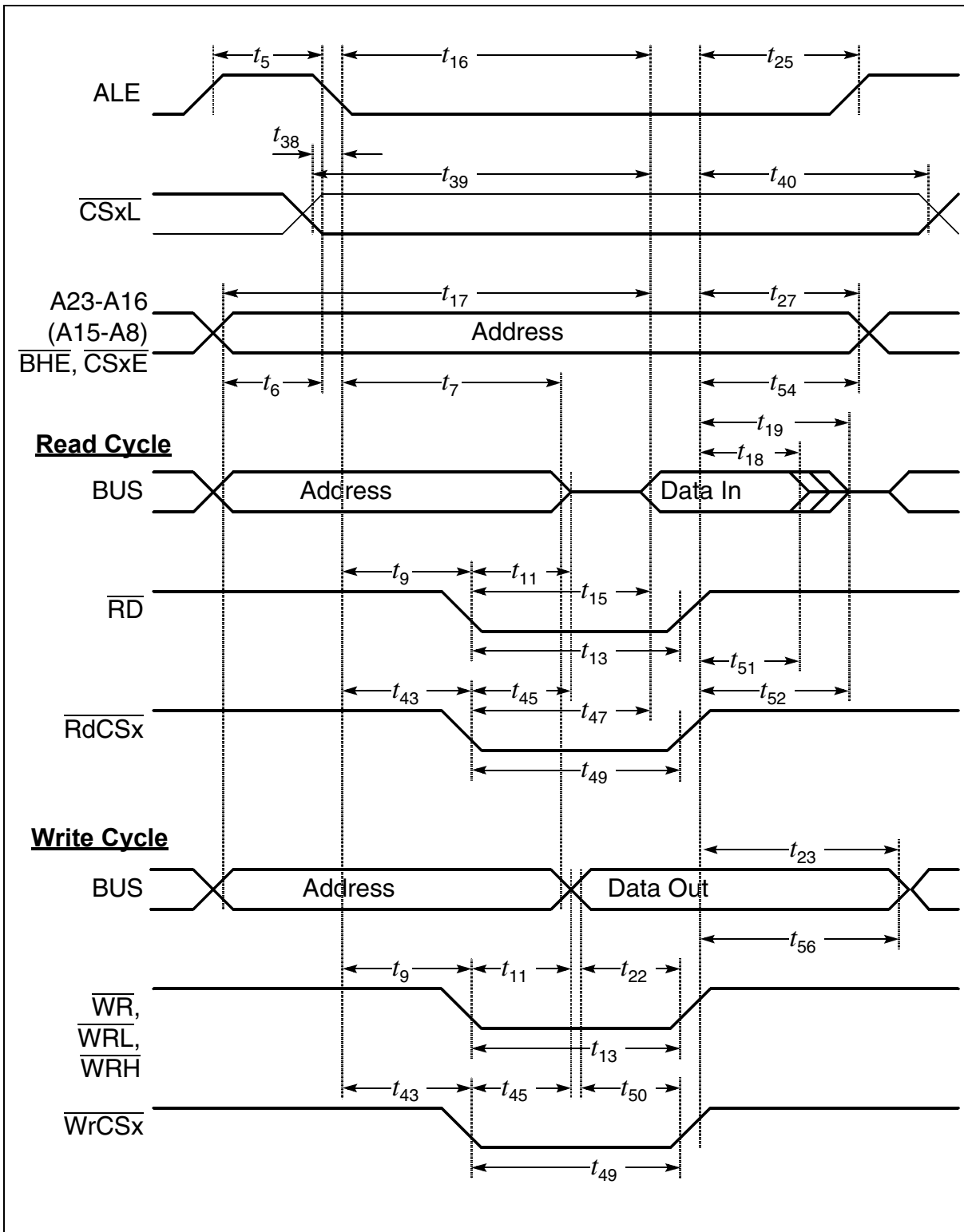


Figure 18 External Memory Cycle: Multiplexed Bus, No Read/Write Delay, Extended ALE

Timing Characteristics
Table 18 Demultiplexed Bus (Standard Supply Voltage Range)
 (Operating Conditions apply)

 ALE cycle time = $4 \text{ TCL} + 2t_A + t_C + t_F$ (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			Min.	Max.	Min.	Max.	
ALE high time	t_5	CC	$10 + t_A$	–	$\text{TCL} - 10 + t_A$	–	ns
Address setup to ALE	t_6	CC	$4 + t_A$	–	$\text{TCL} - 16 + t_A$	–	ns
ALE falling edge to $\overline{\text{RD}}$, $\overline{\text{WR}}$ (with RW-delay)	t_8	CC	$10 + t_A$	–	$\text{TCL} - 10 + t_A$	–	ns
ALE falling edge to $\overline{\text{RD}}$, $\overline{\text{WR}}$ (no RW-delay)	t_9	CC	$-10 + t_A$	–	$-10 + t_A$	–	ns
$\overline{\text{RD}}$, $\overline{\text{WR}}$ low time (with RW-delay)	t_{12}	CC	$30 + t_C$	–	$2\text{TCL} - 10 + t_C$	–	ns
$\overline{\text{RD}}$, $\overline{\text{WR}}$ low time (no RW-delay)	t_{13}	CC	$50 + t_C$	–	$3\text{TCL} - 10 + t_C$	–	ns
$\overline{\text{RD}}$ to valid data in (with RW-delay)	t_{14}	SR	–	$20 + t_C$	–	$2\text{TCL} - 20 + t_C$	ns
$\overline{\text{RD}}$ to valid data in (no RW-delay)	t_{15}	SR	–	$40 + t_C$	–	$3\text{TCL} - 20 + t_C$	ns
ALE low to valid data in	t_{16}	SR	–	$40 + t_A + t_C$	–	$3\text{TCL} - 20 + t_A + t_C$	ns
Address to valid data in	t_{17}	SR	–	$50 + 2t_A + t_C$	–	$4\text{TCL} - 30 + 2t_A + t_C$	ns
Data hold after $\overline{\text{RD}}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{\text{RD}}$ rising edge (with RW-delay ¹⁾)	t_{20}	SR	–	$26 + 2t_A + t_F^{(1)}$	–	$2\text{TCL} - 14 + 22t_A + t_F^{(1)}$	ns
Data float after $\overline{\text{RD}}$ rising edge (no RW-delay ¹⁾)	t_{21}	SR	–	$10 + 2t_A + t_F^{(1)}$	–	$\text{TCL} - 10 + 22t_A + t_F^{(1)}$	ns
Data valid to $\overline{\text{WR}}$	t_{22}	CC	$20 + t_C$	–	$2\text{TCL} - 20 + t_C$	–	ns

Timing Characteristics
Table 18 Demultiplexed Bus (Standard Supply Voltage Range) (cont'd)
 (Operating Conditions apply)

 ALE cycle time = $4 \text{ TCL} + 2t_A + t_C + t_F$ (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			Min.	Max.	Min.	Max.	
Data hold after $\overline{\text{WR}}$	t_{24}	CC	$10 + t_F$	–	TCL - 10 + t_F	–	ns
ALE rising edge after $\overline{\text{RD}}$, $\overline{\text{WR}}$	t_{26}	CC	$-10 + t_F$	–	$-10 + t_F$	–	ns
Address hold after $\overline{\text{WR}}^{(2)}$	t_{28}	CC	$0 + t_F$	–	$0 + t_F$	–	ns
ALE falling edge to $\overline{\text{CS}}^{(3)}$	t_{38}	CC	$-4 - t_A$	$10 - t_A$	$-4 - t_A$	$10 - t_A$	ns
$\overline{\text{CS}}$ low to Valid Data In ⁽³⁾	t_{39}	SR	–	$40 + t_C + 2t_A$	–	$3\text{TCL} - 20 + t_C + 2t_A$	ns
$\overline{\text{CS}}$ hold after $\overline{\text{RD}}$, $\overline{\text{WR}}^{(3)}$	t_{41}	CC	$6 + t_F$	–	TCL - 14 + t_F	–	ns
ALE falling edge to $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (with RW-delay)	t_{42}	CC	$16 + t_A$	–	TCL - 4 + t_A	–	ns
ALE falling edge to $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (no RW-delay)	t_{43}	CC	$-4 + t_A$	–	$-4 + t_A$	–	ns
$\overline{\text{RdCS}}$ to Valid Data In (with RW-delay)	t_{46}	SR	–	$16 + t_C$	–	$2\text{TCL} - 24 + t_C$	ns
$\overline{\text{RdCS}}$ to Valid Data In (no RW-delay)	t_{47}	SR	–	$36 + t_C$	–	$3\text{TCL} - 24 + t_C$	ns
$\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ Low Time (with RW-delay)	t_{48}	CC	$30 + t_C$	–	$2\text{TCL} - 10 + t_C$	–	ns
$\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ Low Time (no RW-delay)	t_{49}	CC	$50 + t_C$	–	$3\text{TCL} - 10 + t_C$	–	ns
Data valid to $\overline{\text{WrCS}}$	t_{50}	CC	$26 + t_C$	–	$2\text{TCL} - 14 + t_C$	–	ns
Data hold after $\overline{\text{RdCS}}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{\text{RdCS}}$ (with RW-delay) ⁽¹⁾	t_{53}	SR	–	$20 + t_F$	–	$2\text{TCL} - 20 + 2t_A + t_F^{(1)}$	ns

Timing Characteristics
Table 18 Demultiplexed Bus (Standard Supply Voltage Range) (cont'd)
 (Operating Conditions apply)

 ALE cycle time = $4 \text{ TCL} + 2t_A + t_C + t_F$ (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol	Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
		Min.	Max.	Min.	Max.	
Data float after $\overline{\text{RdCS}}$ (no RW-delay) ¹⁾	t_{68} SR	–	$0 + t_F$	–	$\text{TCL} - 20 + 2t_A + t_F$ ¹⁾	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{55} CC	$-6 + t_F$	–	$-6 + t_F$	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{57} CC	$6 + t_F$	–	$\text{TCL} - 14 + t_F$	–	ns

- 1) RW-delay and t_A refer to the next following bus cycle (including an access to an on-chip X-Peripheral).
- 2) Read data are latched with the same clock edge that triggers the address change and the rising $\overline{\text{RD}}$ edge. Therefore address changes before the end of $\overline{\text{RD}}$ have no impact on read cycles.
- 3) These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).

Timing Characteristics
Table 19 Demultiplexed Bus (Reduced Supply Voltage Range)
 (Operating Conditions apply)

 ALE cycle time = $4 \text{ TCL} + 2t_A + t_C + t_F$ (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			Min.	Max.	Min.	Max.	
ALE high time	t_5	CC	$11 + t_A$	–	TCL - 14 + t_A	–	ns
Address setup to ALE	t_6	CC	$5 + t_A$	–	TCL - 20 + t_A	–	ns
ALE falling edge to $\overline{\text{RD}}$, $\overline{\text{WR}}$ (with RW-delay)	t_8	CC	$15 + t_A$	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{\text{RD}}$, $\overline{\text{WR}}$ (no RW-delay)	t_9	CC	$-10 + t_A$	–	-10 + t_A	–	ns
$\overline{\text{RD}}$, $\overline{\text{WR}}$ low time (with RW-delay)	t_{12}	CC	$34 + t_C$	–	2TCL - 16 + t_C	–	ns
$\overline{\text{RD}}$, $\overline{\text{WR}}$ low time (no RW-delay)	t_{13}	CC	$59 + t_C$	–	3TCL - 16 + t_C	–	ns
$\overline{\text{RD}}$ to valid data in (with RW-delay)	t_{14}	SR	–	$22 + t_C$	–	2TCL - 28 + t_C	ns
$\overline{\text{RD}}$ to valid data in (no RW-delay)	t_{15}	SR	–	$47 + t_C$	–	3TCL - 28 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	$45 + t_A + t_C$	–	3TCL - 30 + $t_A + t_C$	ns
Address to valid data in	t_{17}	SR	–	$57 + 2t_A + t_C$	–	4TCL - 43 + $2t_A + t_C$	ns
Data hold after $\overline{\text{RD}}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{\text{RD}}$ rising edge (with RW-delay ¹⁾)	t_{20}	SR	–	$36 + 2t_A + t_F^{(1)}$	–	2TCL - 14 + $22t_A + t_F^{(1)}$	ns
Data float after $\overline{\text{RD}}$ rising edge (no RW-delay ¹⁾)	t_{21}	SR	–	$15 + 2t_A + t_F^{(1)}$	–	TCL - 10 + $22t_A + t_F^{(1)}$	ns
Data valid to $\overline{\text{WR}}$	t_{22}	CC	$24 + t_C$	–	2TCL - 26 + t_C	–	ns

Timing Characteristics
Table 19 Demultiplexed Bus (Reduced Supply Voltage Range) (cont'd)
 (Operating Conditions apply)

 ALE cycle time = $4 \text{ TCL} + 2t_A + t_C + t_F$ (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			Min.	Max.	Min.	Max.	
Data hold after $\overline{\text{WR}}$	t_{24}	CC	$15 + t_F$	–	$\text{TCL} - 10 + t_F$	–	ns
ALE rising edge after $\overline{\text{RD}}$, $\overline{\text{WR}}$	t_{26}	CC	$-12 + t_F$	–	$-12 + t_F$	–	ns
Address hold after $\overline{\text{WR}}^{(2)}$	t_{28}	CC	$0 + t_F$	–	$0 + t_F$	–	ns
ALE falling edge to $\overline{\text{CS}}^{(3)}$	t_{38}	CC	$-8 - t_A$	$10 - t_A$	$-8 - t_A$	$10 - t_A$	ns
$\overline{\text{CS}}$ low to Valid Data In ⁽³⁾	t_{39}	SR	–	$47 + t_C + 2t_A$	–	$3\text{TCL} - 28 + t_C + 2t_A$	ns
$\overline{\text{CS}}$ hold after $\overline{\text{RD}}$, $\overline{\text{WR}}^{(3)}$	t_{41}	CC	$9 + t_F$	–	$\text{TCL} - 16 + t_F$	–	ns
ALE falling edge to $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (with RW-delay)	t_{42}	CC	$19 + t_A$	–	$\text{TCL} - 6 + t_A$	–	ns
ALE falling edge to $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ (no RW-delay)	t_{43}	CC	$-6 + t_A$	–	$-6 + t_A$	–	ns
$\overline{\text{RdCS}}$ to Valid Data In (with RW-delay)	t_{46}	SR	–	$20 + t_C$	–	$2\text{TCL} - 30 + t_C$	ns
$\overline{\text{RdCS}}$ to Valid Data In (no RW-delay)	t_{47}	SR	–	$45 + t_C$	–	$3\text{TCL} - 30 + t_C$	ns
$\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ Low Time (with RW-delay)	t_{48}	CC	$38 + t_C$	–	$2\text{TCL} - 12 + t_C$	–	ns
$\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$ Low Time (no RW-delay)	t_{49}	CC	$63 + t_C$	–	$3\text{TCL} - 12 + t_C$	–	ns
Data valid to $\overline{\text{WrCS}}$	t_{50}	CC	$28 + t_C$	–	$2\text{TCL} - 22 + t_C$	–	ns
Data hold after $\overline{\text{RdCS}}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{\text{RdCS}}$ (with RW-delay) ⁽¹⁾	t_{53}	SR	–	$30 + t_F$	–	$2\text{TCL} - 20 + 2t_A + t_F^{(1)}$	ns

Timing Characteristics
Table 19 Demultiplexed Bus (Reduced Supply Voltage Range) (cont'd)
 (Operating Conditions apply)

 ALE cycle time = $4 \text{ TCL} + 2t_A + t_C + t_F$ (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol	Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
		Min.	Max.	Min.	Max.	
Data float after $\overline{\text{RdCS}}$ (no RW-delay) ¹⁾	t_{68} SR	–	$5 + t_F$	–	$\text{TCL} - 20 + 2t_A + t_F$ ¹⁾	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{55} CC	$-16 + t_F$	–	$-16 + t_F$	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{57} CC	$9 + t_F$	–	$\text{TCL} - 16 + t_F$	–	ns

- 1) RW-delay and t_A refer to the next following bus cycle (including an access to an on-chip X-Peripheral).
- 2) Read data are latched with the same clock edge that triggers the address change and the rising $\overline{\text{RD}}$ edge. Therefore address changes before the end of $\overline{\text{RD}}$ have no impact on read cycles.
- 3) These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).

Timing Characteristics

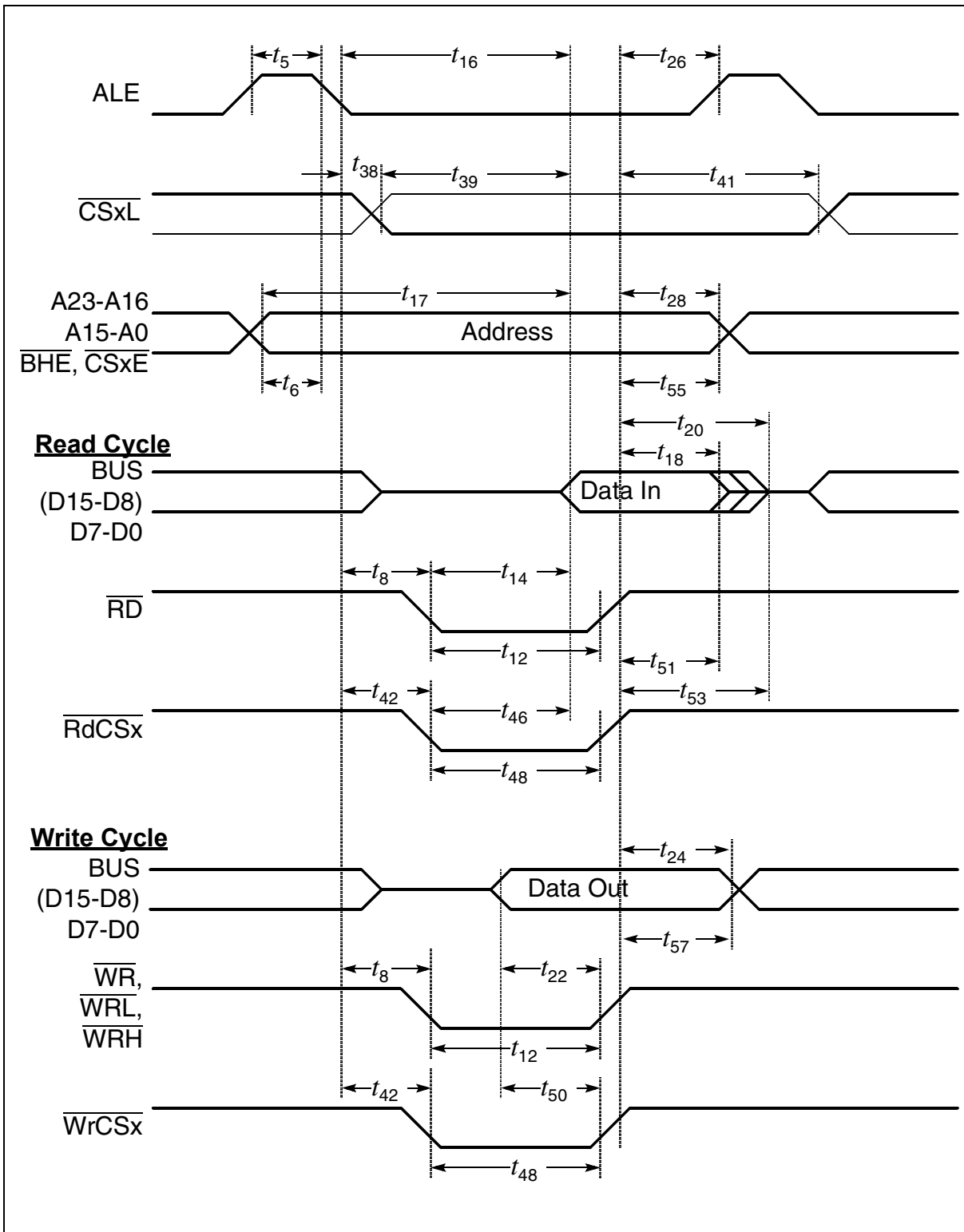


Figure 19 External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Normal ALE

Timing Characteristics

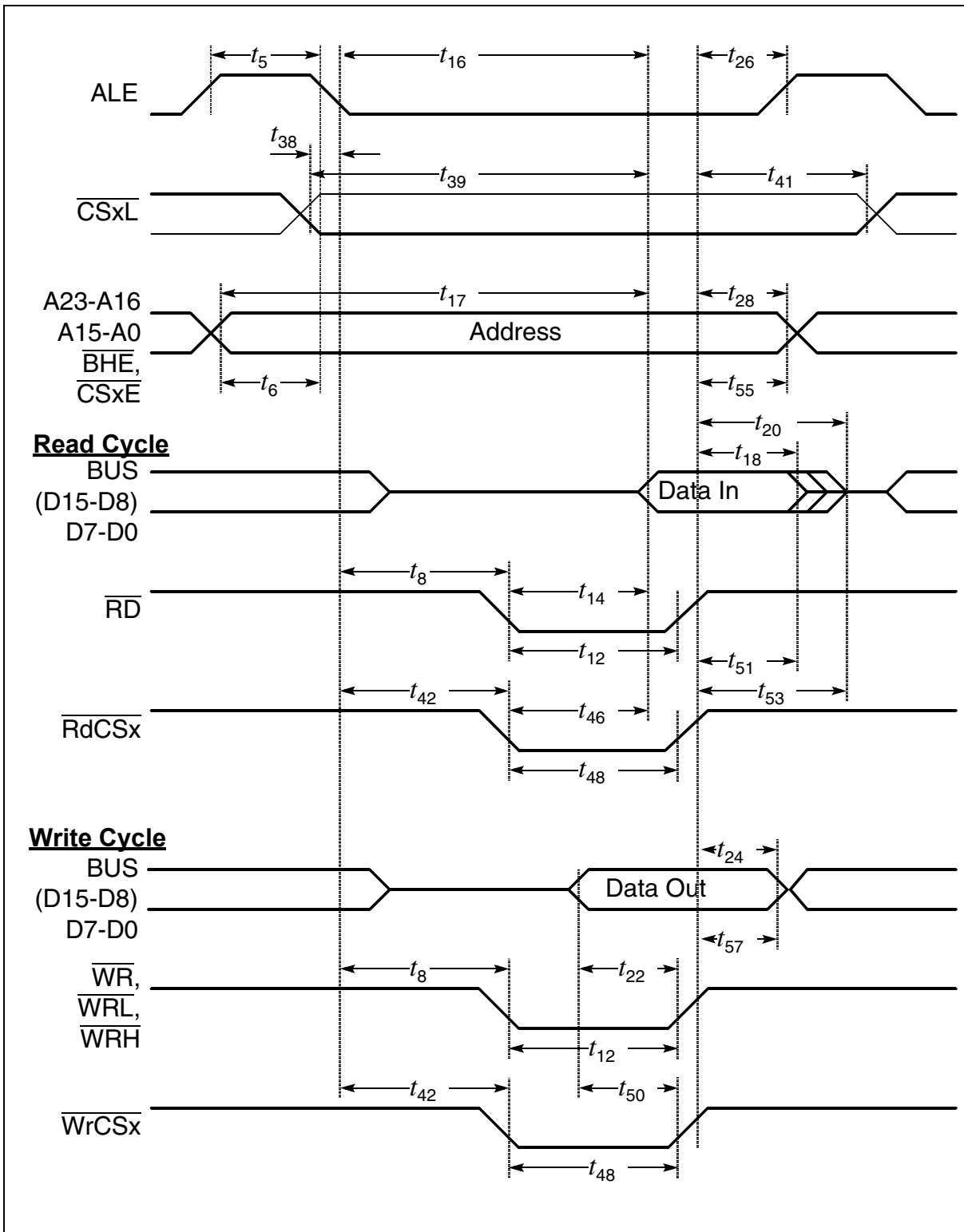


Figure 20 External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Extended ALE

Timing Characteristics

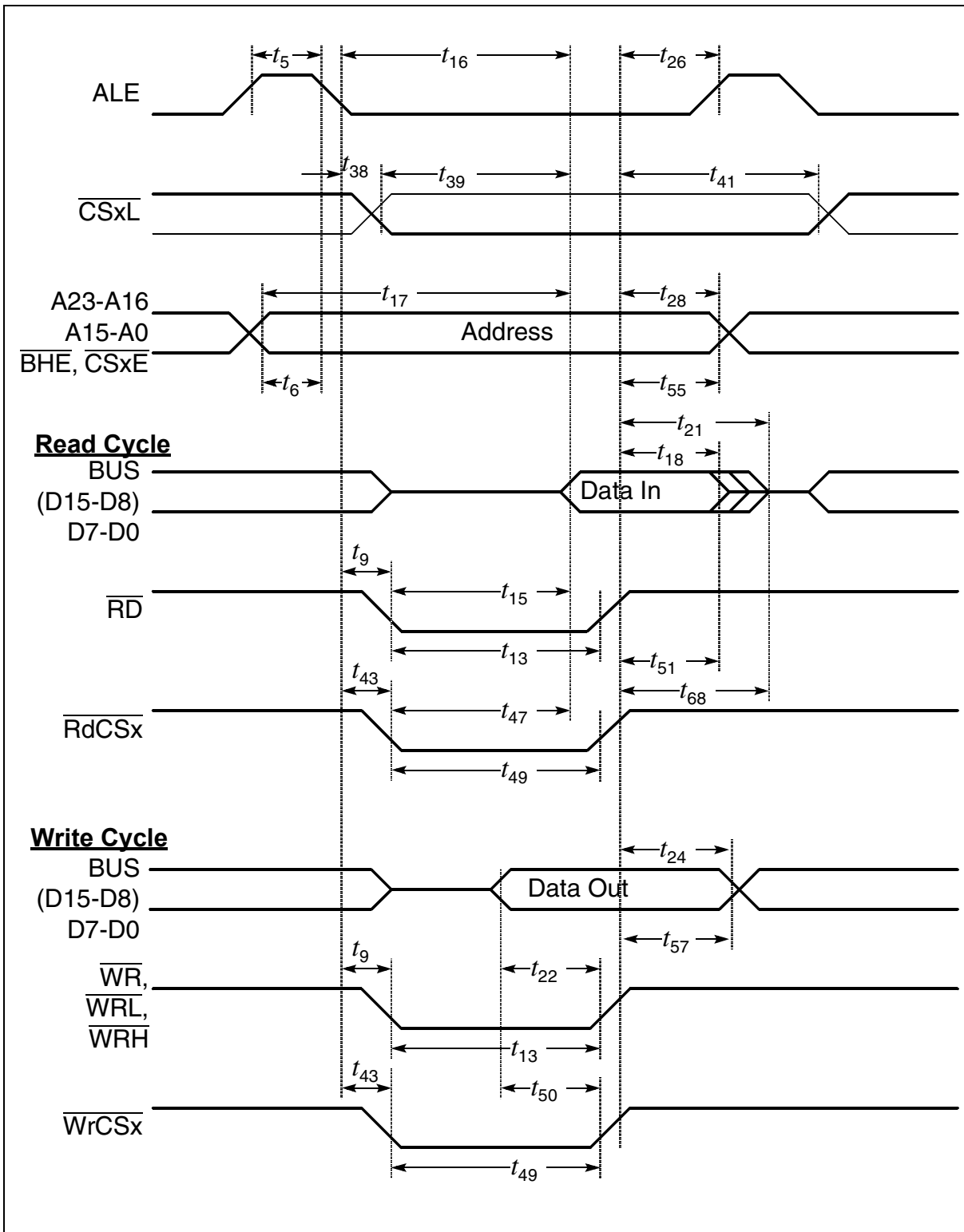


Figure 21 External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Normal ALE

Timing Characteristics

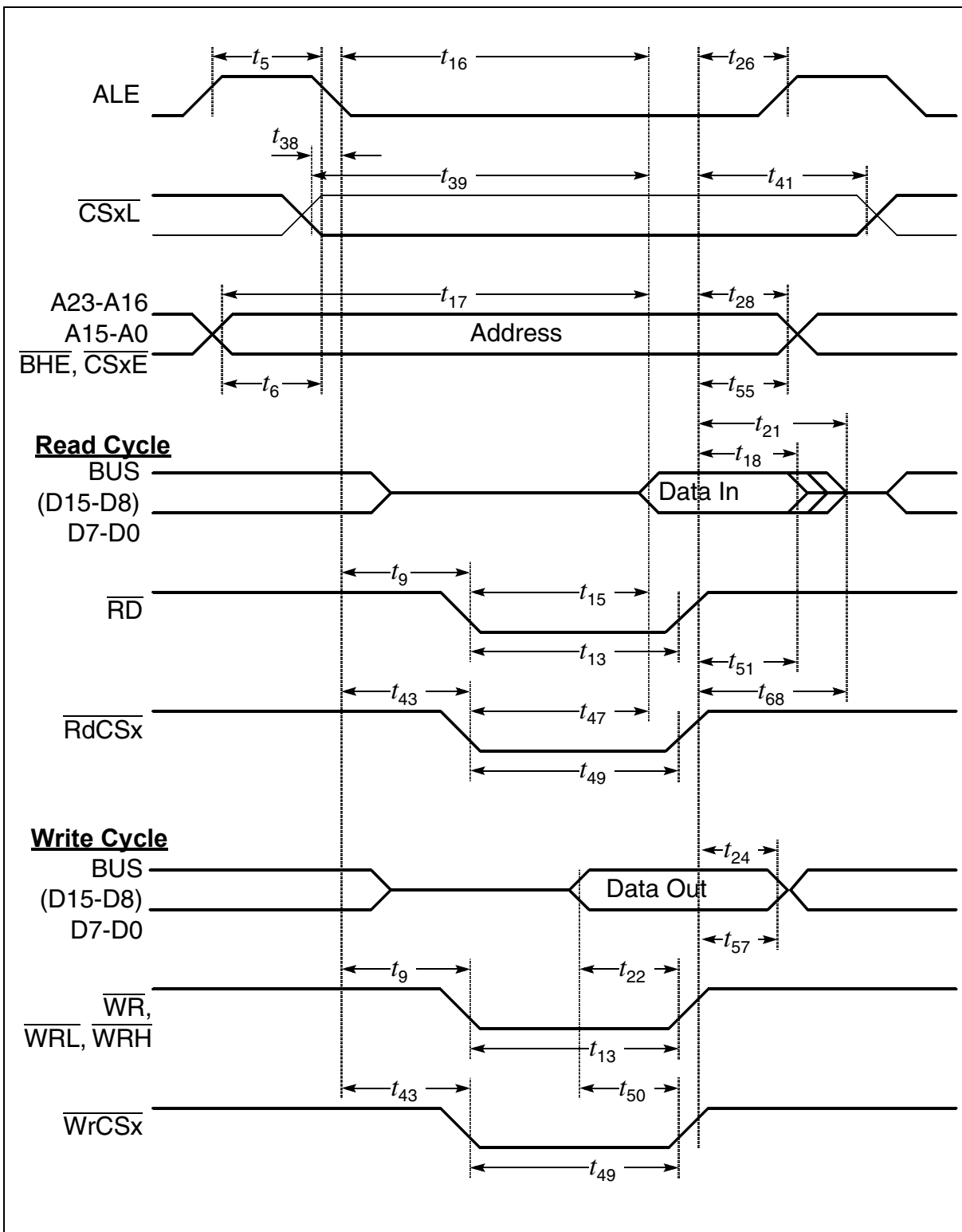


Figure 22 External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Extended ALE

6 Package Outlines

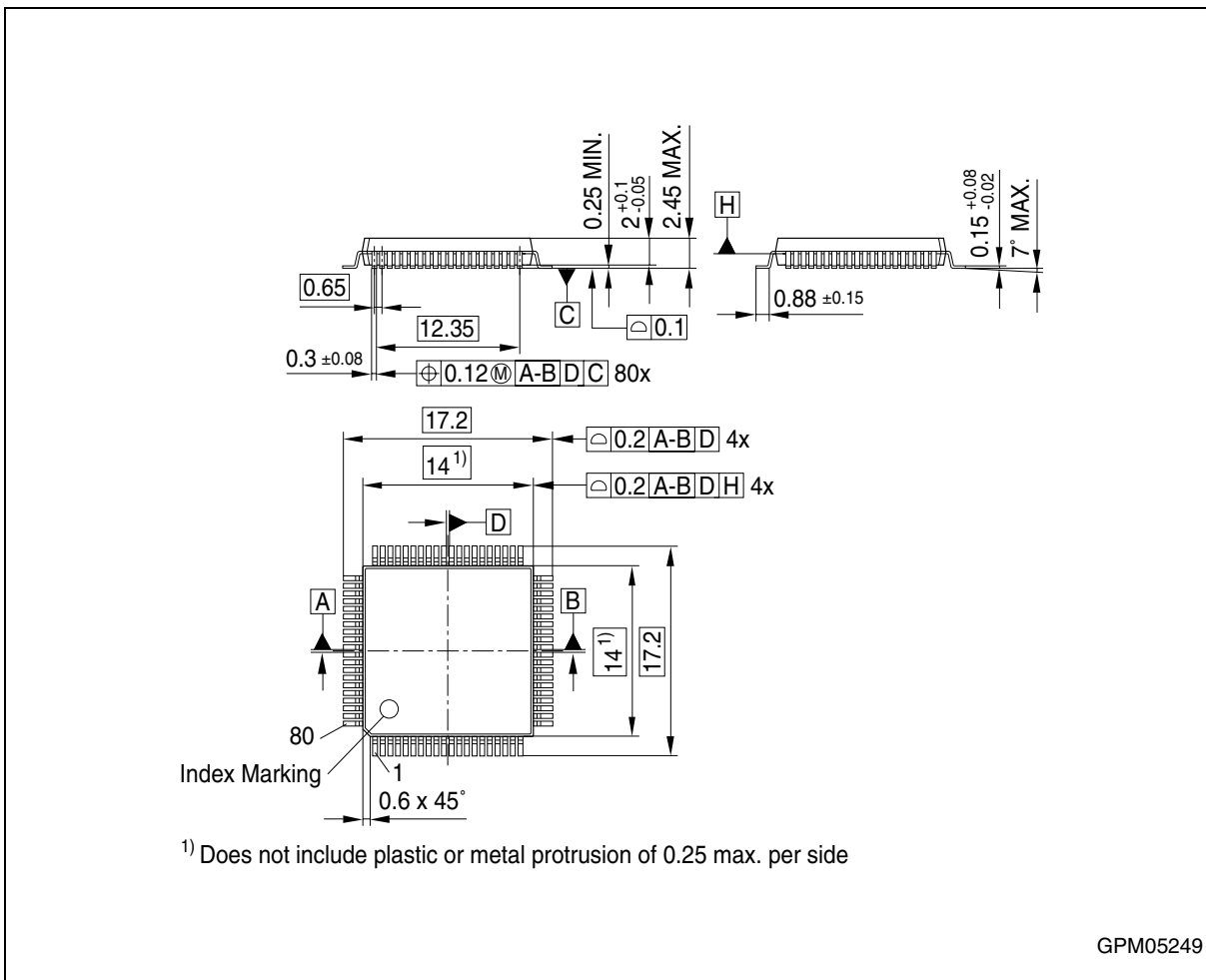


Figure 23 P-MQFP-80-7 (Plastic Metric Quad Flat Package)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": <http://www.infineon.com/products>.

SMD = Surface Mounted Device

Dimensions in mm

w w w . i n f i n e o n . c o m

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