MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

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by MRF19090/D

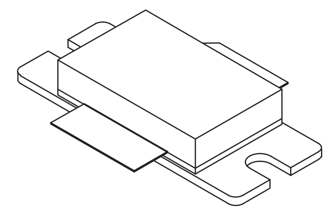
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF19090
MRF19090S
MRF19090SR3

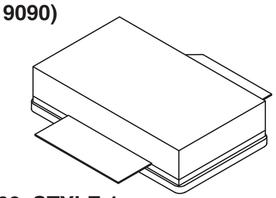
Designed for Class AB PCN and PCS base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for CDMA, TDMA, GSM, and multicarrier amplifier applications.

- Typical CDMA Performance: 1990 MHz, 26 Volts
  IS–97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
  - Output Power — 9 Watts
  - Power Gain — 10 dB
  - Adjacent Channel Power —
    - 885 kHz: –47 dBc @ 30 kHz BW
    - 1.25 MHz: –55 dBc @ 12.5 kHz BW
    - 2.25 MHz: –55 dBc @ 1 MHz BW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1.93 GHz, 90 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

1990 MHz, 90 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs



CASE 465B–03, STYLE 1
(NI–880)
(MRF19090)



CASE 465C–02, STYLE 1
(NI–880S)
(MRF19090S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C > = 25°C Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

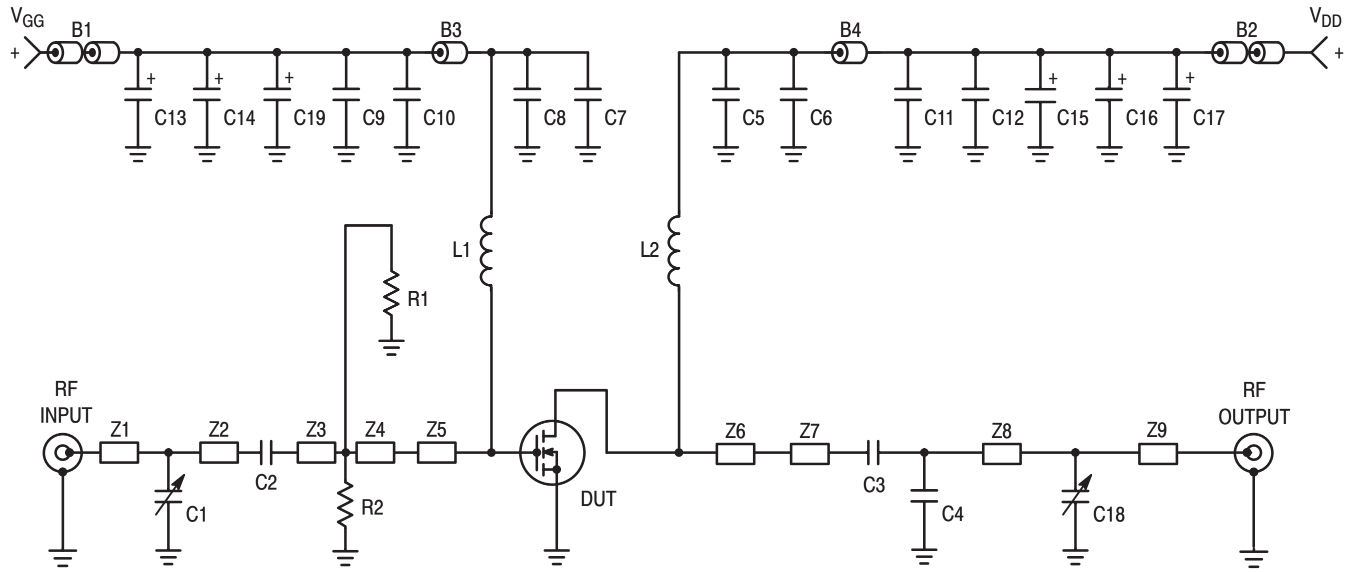
REV 3

MOTOROLA intelligence everywhere™ digital dna™

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	—	7.2	—	S
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$VGS_{(th)}$	2.0	—	4.0	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 750 mAdc)	$V_{GS(Q)}$	2.5	3.8	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.10	—	Vdc
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	4.2	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	G_{ps}	10	11.5	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	η	33	35	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	IMD	—	–30	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f = 1930 MHz and 1990 MHz, Tone Spacing = 100 kHz)	IRL	—	–12	—	dB
P_{out}, 1 dB Compression Point (V_{DD} = 26 Vdc, P_{out} = 90 W CW, f = 1990 MHz)	P1dB	—	90	—	W
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 750 mA, f = 1930 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B1, B2	2 Ferrite Beads, Round, Ferroxcube #56–590–65–3B
B3, B34	Ferrite Beads, Surface Mount, Ferroxcube
C1, C18	0.4 – 2.5 pF Variable Capacitors, Johanson Gigatrim #27285
C2, C5, C8	10 pF Chip Capacitors, B Case, ATC #100B100CCA500X
C3	12 pF Chip Capacitor, B Case, ATC #100B120CCA500X
C4	0.3 pF Chip Capacitor, B Case, ATC #100B0R3CCA500X
C6, C7	120 pF Chip Capacitors, B Case, ATC #100B12R1CCA500X
C9, C12	0.1 μF Chip Capacitors, Kemet #CDR33BX104AKWS
C10, C11	1000 pF Chip Capacitors, B Case, ATC #100B102JCA50X
C13, C17	22 μF, 35 V Tantalum Chip Capacitors, Kemet #T491X226K035AS4394
C14, C16	10 μF, 35 V Tantalum Chip Capacitors, Kemet #T495X106K035AS4394
C15, C19	1 μF, 35 V Tantalum Chip Capacitors, Kemet #T495X105K035AS4394
L1, L2	8 Turns, #26 AWG, 0.085″ OD, 0.330″ Long, Copper Wire
R1, R2	270 Ω, 1/4 W Chip Resistors, Garrett Instruments #RM73B2B271JT
Z1	ZO = 50 Ohms
Z2	ZO = 50 Ohms, Lambda = 0.123
Z3	ZO = 15.24 Ohms, Lambda = 0.0762
Z4	ZO = 10.11 Ohms, Lambda = 0.0392
Z5	ZO = 6.34 Ohms, Lambda = 0.0711
Z6	ZO = 5.02 Ohms, Lambda = 0.0476
Z7	ZO = 5.54 Ohms, Lambda = 0.0972
Z8	ZO = 50.0 Ohms, Lambda = 0.194
Z9	ZO = 50.0 Ohms
Raw PCB Material	0.030″ Glass Teflon®, ε_r = 2.55, 2 oz Copper, 3″ x 5″ Dimensions

Figure 1. MRF19090 Test Circuit Schematic

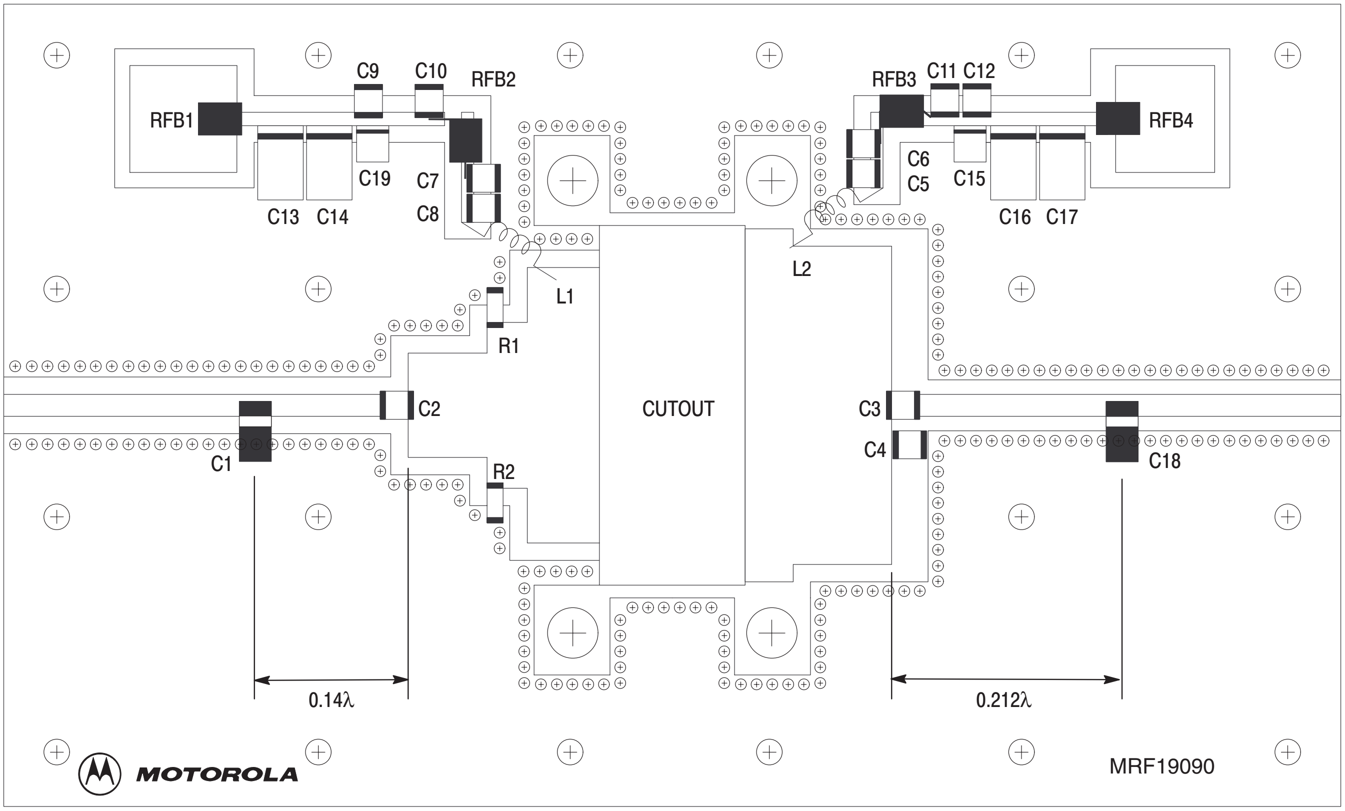


Figure 2. MRF19090 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

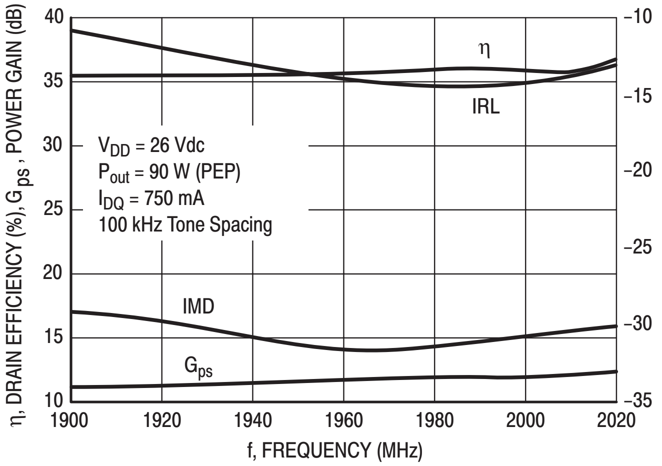


Figure 3. Class AB Performance versus Frequency

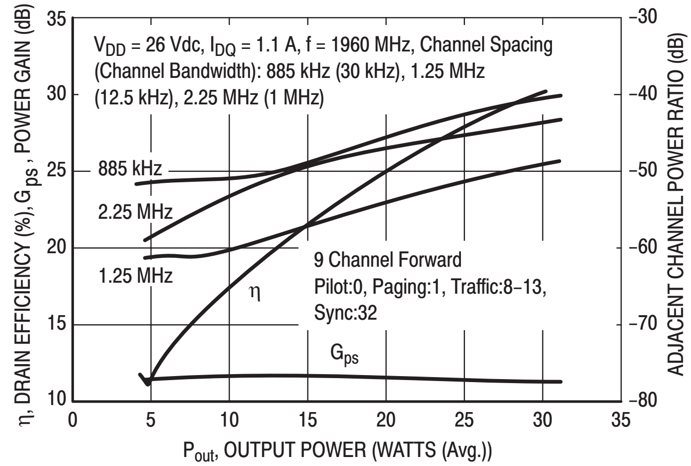


Figure 4. CDMA Performance ACPR, Gain and Drain Efficiency versus Output Power

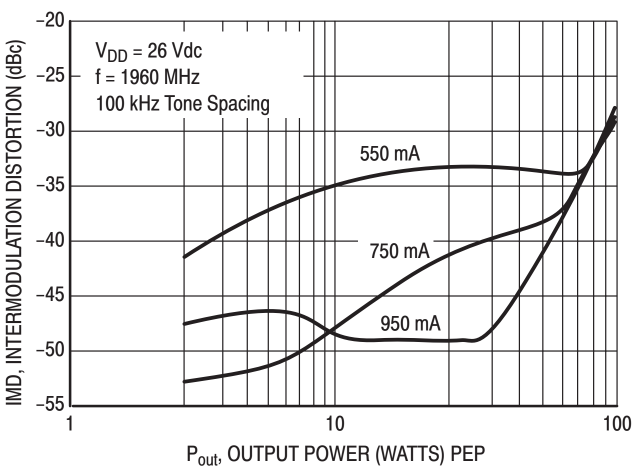


Figure 5. Third Order Intermodulation Distortion versus Output Power

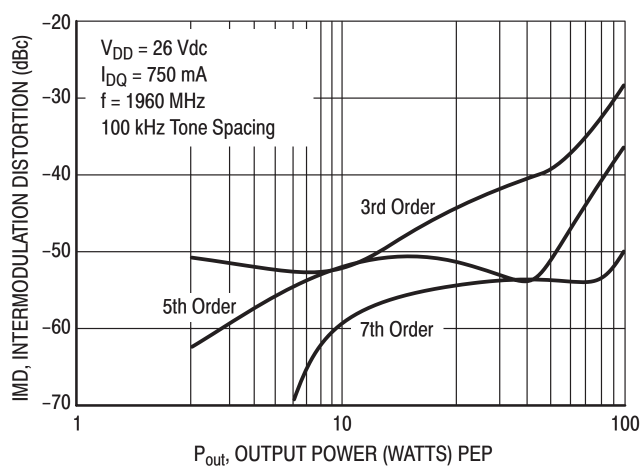


Figure 6. Intermodulation Products versus Output Power

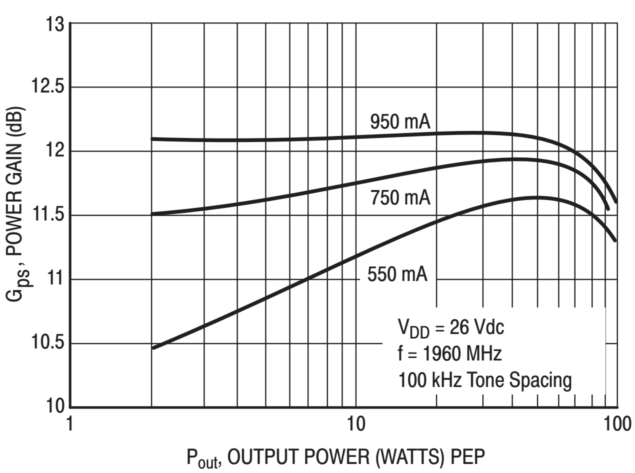


Figure 7. Power Gain versus Output Power

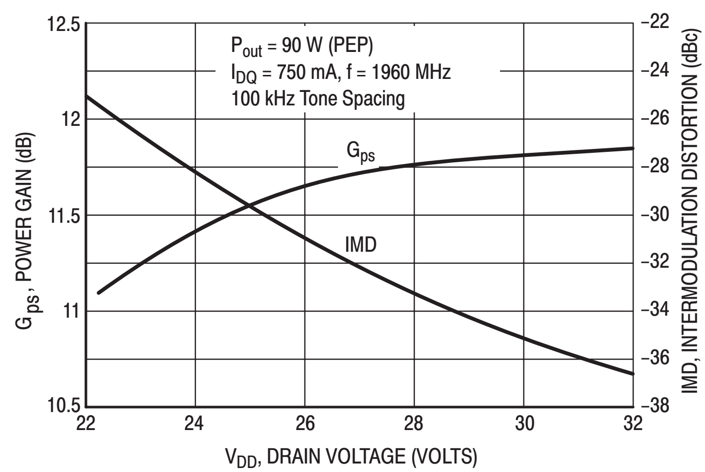
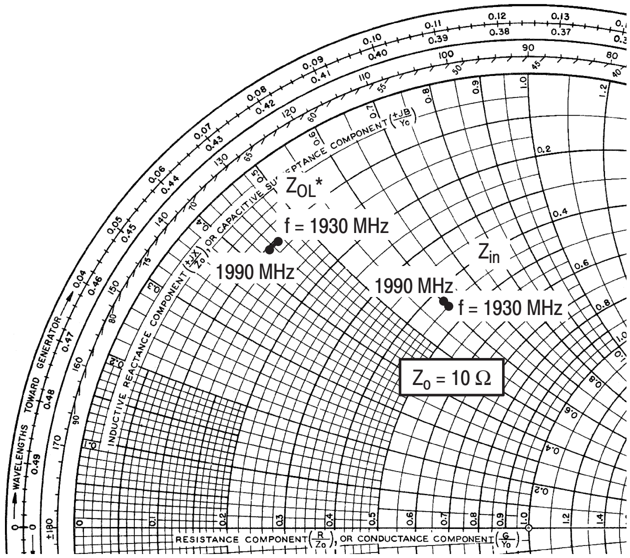


Figure 8. Third Order Intermodulation Distortion and Gain versus Supply Voltage



V_{DD} = 26 V, I_{DQ} = 750 mA, P_{out} = 90 Watts (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1930	4.5 + j6.1	1.1 + j4.5
1960	4.4 + j6.0	1.1 + j4.4
1990	4.3 + j6.1	1.1 + j4.3

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

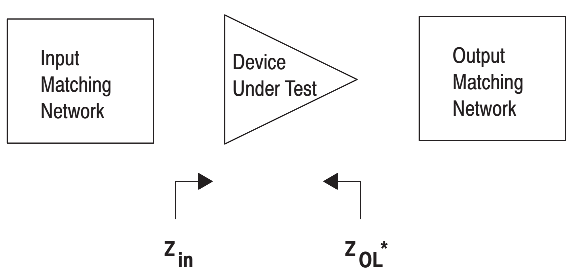
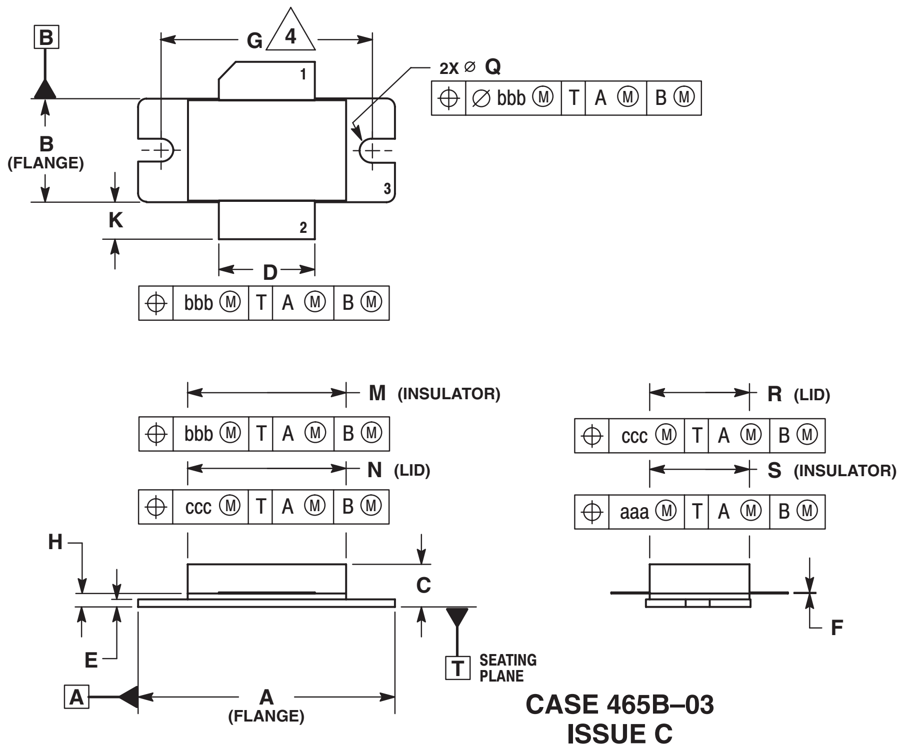


Figure 9. Series Equivalent Input and Output Impedance

PACKAGE DIMENSIONS

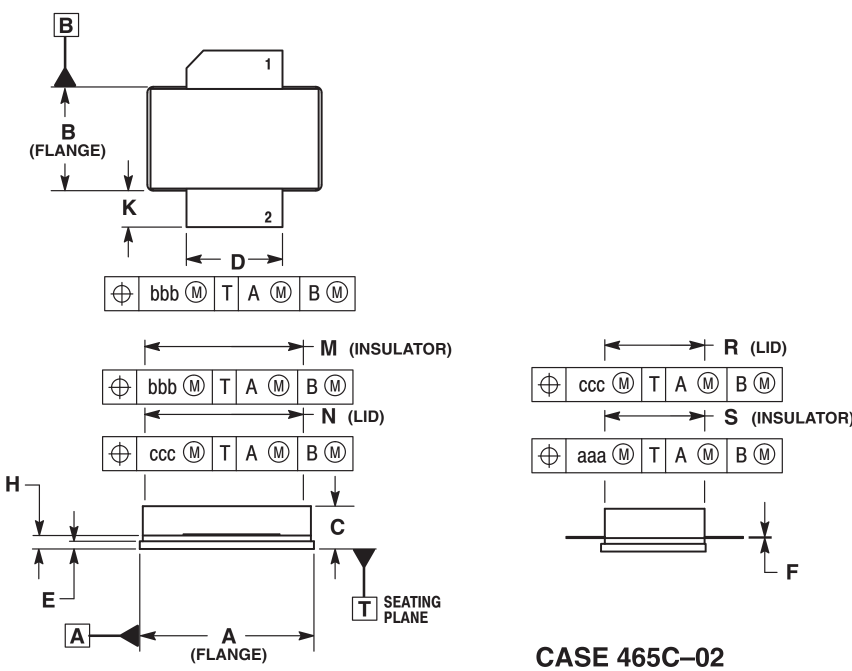


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
4. RECOMMENDED BOLT CENTER DIMENSION OF 1.16 (29.57) BASED ON M3 SCREW.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.535	0.545	13.6	13.8
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.175	0.205	4.44	5.21
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
Q	∅.118	∅.138	∅3.00	∅3.51
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465B–03
ISSUE C
(NI–880)
(MRF19090)



NOTES:
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	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.905	0.915	22.99	23.24
B	0.535	0.545	13.60	13.80
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465C–02
ISSUE A
(NI–880S)
(MRF19090S)

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