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MC68HC11A8
MC68HC11A1
MC68HC11A0

Technical Summary
8-Bit Microcontrollers

1 Introduction

The MC68HC11A8, MC68HC11A1, and MC68HC11A0 high-performance microcontroller units (MCUs) are based on the M68HC11 Family. These high speed, low power consumption chips have multiplexed buses and a fully static design. The chips can operate at frequencies from 3 MHz to dc. The three MCUs are created from the same masks; the only differences are the value stored in the CONFIG register, and whether or not the ROM or EEPROM is tested and guaranteed.

For detailed information about specific characteristics of these MCUs, refer to the *M68HC11 Reference Manual* (M68HC11RM/AD).

1.1 Features

- M68HC11 CPU
- Power Saving STOP and WAIT Modes
- 8 Kbytes ROM
- 512 Bytes of On-Chip EEPROM
- 256 Bytes of On-Chip RAM (All Saved During Standby)
- 16-Bit Timer System
  - — 3 Input Capture Channels
  - — 5 Output Compare Channels
- 8-Bit Pulse Accumulator
- Real-Time Interrupt Circuit
- Computer Operating Properly (COP) Watchdog System
- Synchronous Serial Peripheral Interface (SPI)
- Asynchronous Nonreturn to Zero (NRZ) Serial Communications Interface (SCI)
- 8-Channel, 8-Bit Analog-to-Digital (A/D) Converter
- 38 General-Purpose Input/Output (I/O) Pins
  - — 15 Bidirectional I/O Pins
  - — 11 Input-Only Pins and 12 Output-Only Pins (Eight Output-Only Pins in 48-Pin Package)
- Available in 48-Pin Dual In-Line Package (DIP) or 52-Pin Plastic Leaded Chip Carrier (PLCC)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Table 1 MC68HC11Ax Family Members

Device Number	ROM	EEPROM	RAM	CONFIG*	Comments
MC68HC11A8	8K	512	256	$0F	Family built around this device
MC68HC11A1	0	512	256	$0D	ROM disabled
MC68HC11A0	0	0	256	$0C	ROM and EEPROM disabled

Table 2 Ordering Information

Package	Temperature	CONFIG	Description	MC Order Number
48-Pin Plastic DIP (P suffix)	–40°to + 85°C	$0F	BUFFALO ROM	MC68HC11A8P1
	–40°to + 85°C	$0D	No ROM	MC68HC11A1P
	–40°to + 105°C	$0D	No ROM	MC68HC11A1VP
	–40°to + 125°C	$0D	No ROM	MC68HC11A1MP
	–40°to + 85°C	$09	No ROM, COP On	MC68HCP11A1P
	–40°to + 105°C	$09	No ROM, COP On	MC68HCP11A1VP
	–40°to + 125°C	$09	No ROM, COP On	MC68HCP11A1MP
	–40°to + 85°C	$0C	No ROM, No EEPROM	MC68HC11A0P
52-Pin PLCC (FN suffix)	–40°to + 85°C	$0F	BUFFALO ROM	MC68HC11A8FN1
	–40°to + 85°C	$0D	No ROM	MC68HC11A1FN
	–40°to + 105°C	$0D	No ROM	MC68HC11A1VFN
	–40°to + 125°C	$0D	No ROM	MC68HC11A1MFN
	–40°to + 85°C	$09	No ROM, COP On	MC68HCP11A1FN
	–40°to + 105°C	$09	No ROM, COP On	MC68HCP11A1VFN
	–40°to + 125°C	$09	No ROM, COP On	MC68HCP11A1MFN
	–40°to + 85°C	$0C	No ROM, No EEPROM	MC68HC11A0FN

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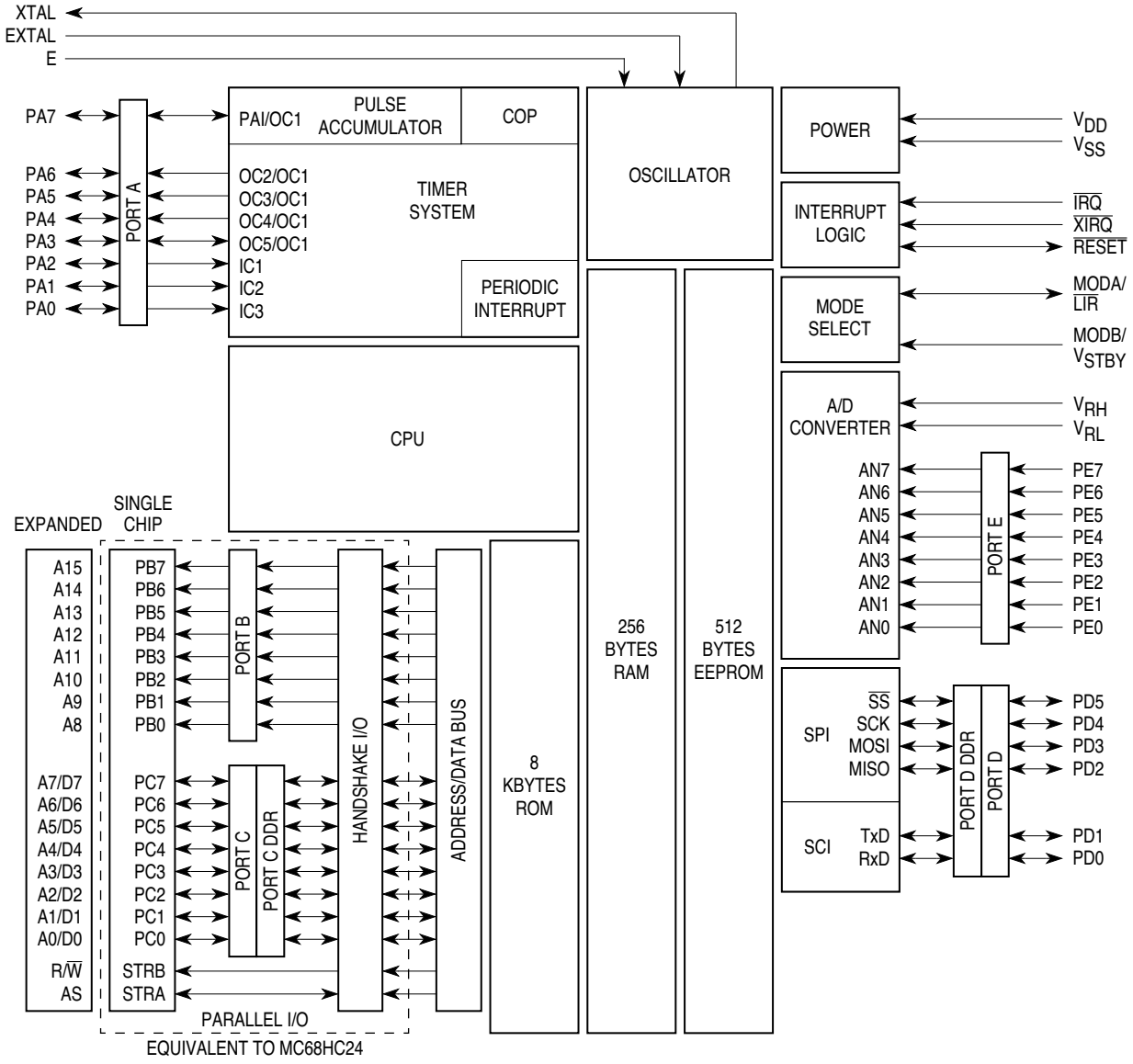


Figure 1 MC68HC11A8 Block Diagram

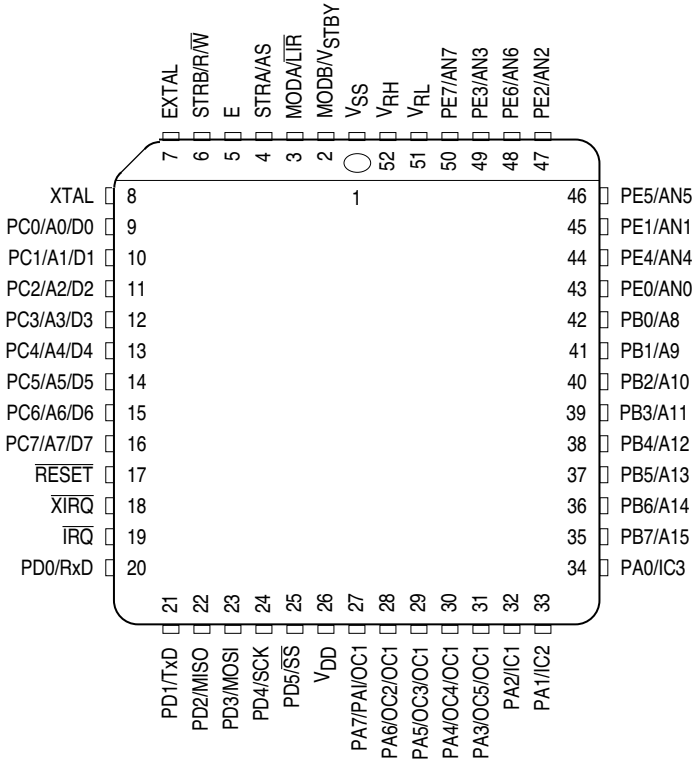


Figure 2 52-Pin PLCC Pin Assignments

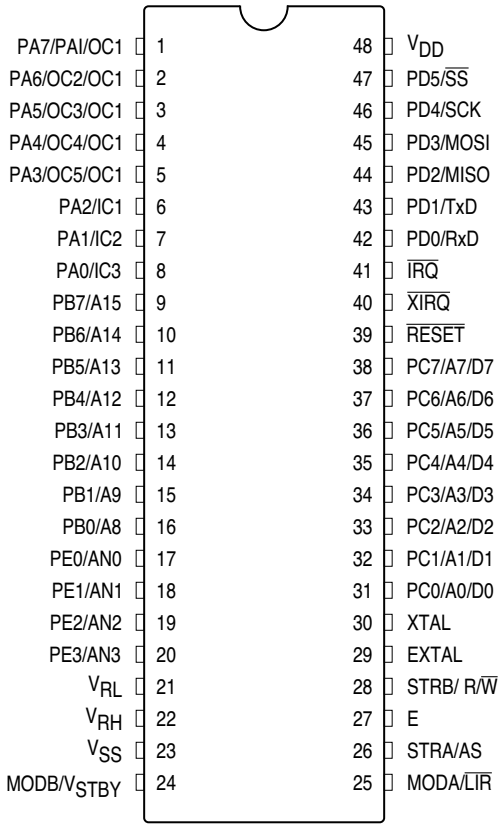


Figure 3 48-Pin DIP Pin Assignments

2 Operating Modes and Memory Maps

In single-chip operating mode, the MC68HC11A8 is a monolithic microcontroller without external address or data buses.

In expanded multiplexed operating mode, the MCU can access a 64 Kbyte address space. The space includes the same on-chip memory addresses used for single-chip mode plus external peripheral and memory devices. The expansion bus is made up of ports B and C and control signals AS and R/$\overline{W}$. The address, R/$\overline{W}$, and AS signals are active and valid for all bus cycles including accesses to internal memory locations. The following figure illustrates a recommended method of demultiplexing low-order addresses from data at port C.

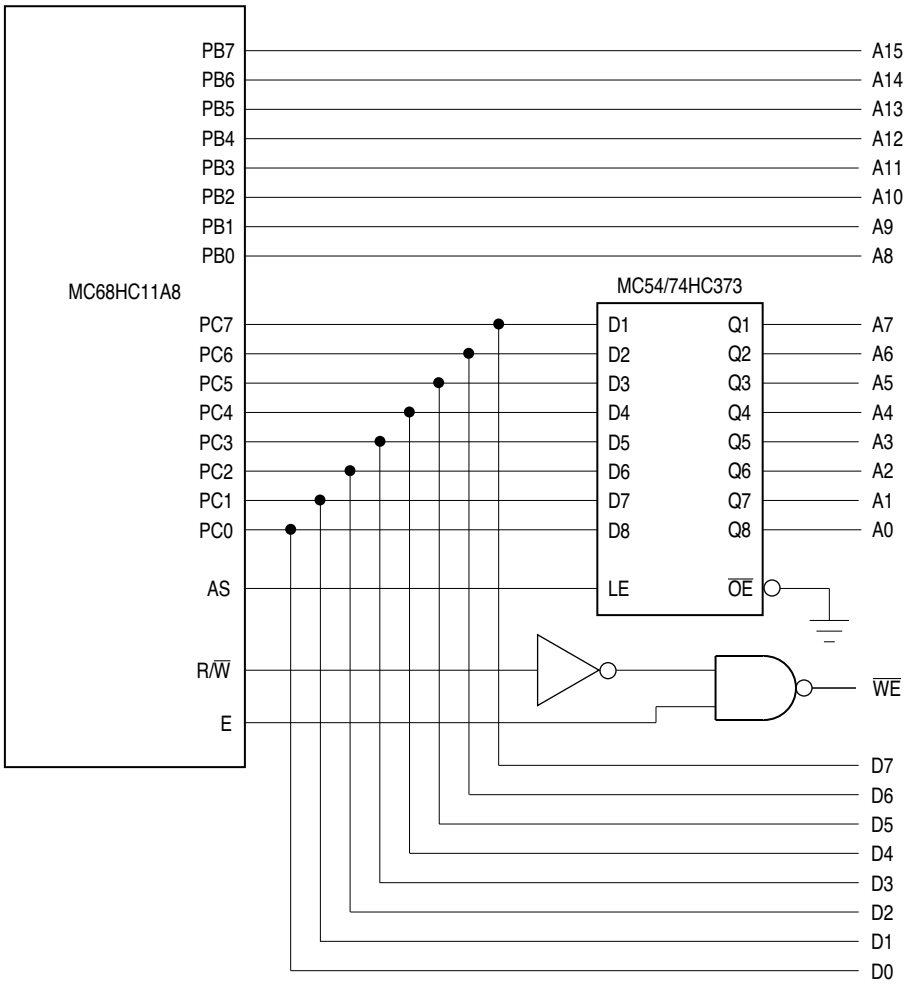


Figure 4 Address/Data Demultiplexing

Special bootstrap mode allows special purpose programs to be entered into internal RAM. The bootloader program uses the SCI to read a 256-byte program into on-chip RAM at $0000 through $00FF. After receiving the character for address $00FF, control passes to the loaded program at $0000.

Special test mode is used primarily for factory testing.

2.1 Memory Maps

Memory locations are the same for expanded multiplexed and single-chip modes. The on-board 256-byte RAM is initially located at $0000 after reset. The 64-byte register block originates at $1000 after reset. RAM and/or the register block can be placed at any other 4K boundary ($x000) after reset by writing an appropriate value to the INIT register. The 512-byte EEPROM is located at $B600 through $B7FF after reset if it is enabled. The 8 Kbyte ROM is located at $E000 through $FFFF if it is enabled.

Hardware priority is built into the memory remapping. Registers have priority over RAM, and RAM has priority over ROM. The higher priority resource covers the lower, making the underlying locations inaccessible.

In special bootstrap mode, a bootloader ROM is enabled at locations $BF40 through $BFFF.

In special test and special bootstrap modes, reset and interrupt vectors are located at $BFC0 through $BFFF.

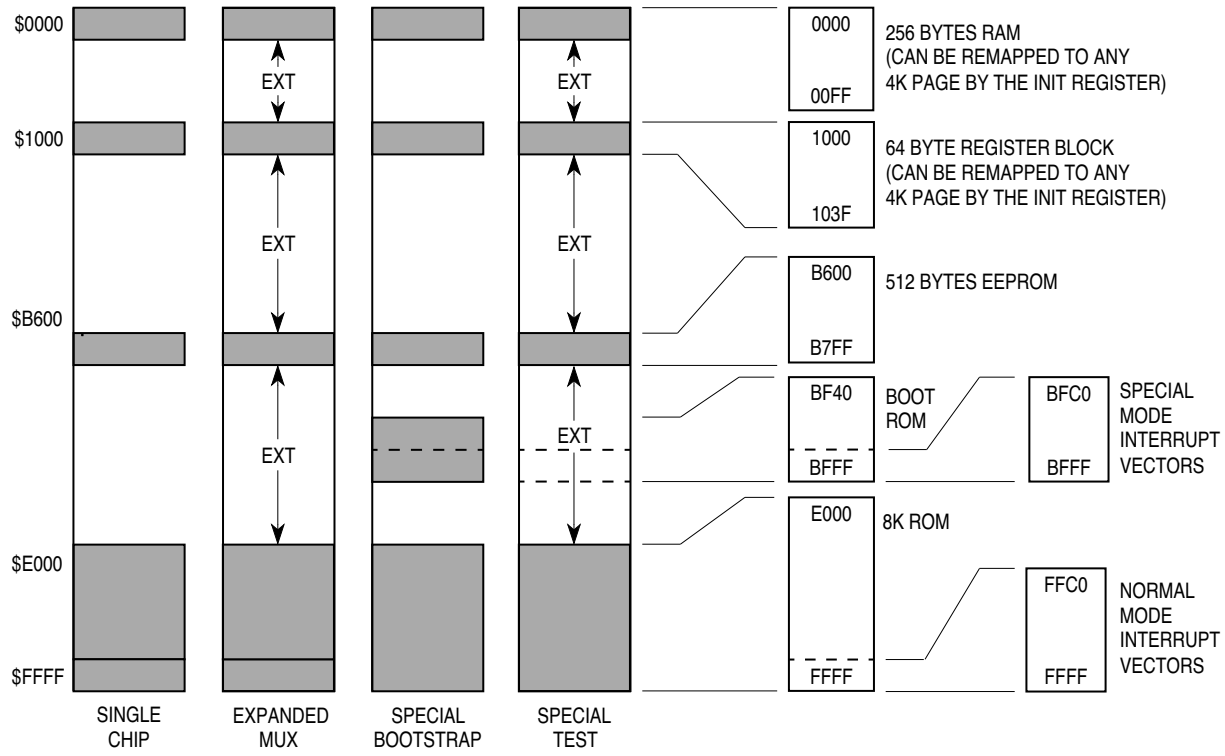


Figure 5 Memory Map

Table 3 MC68HC11A8 Register and Control Bit Assignments (Sheet 1 of 2)

(The register block can be remapped to any 4K boundary.)

	Bit 7	6	5	4	3	2	1	Bit 0	
$1000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA
$1001									Reserved
$1002	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB	PIOC
$1003	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	PORTC
$1004	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PORTB
$1005	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0	PORTCL
$1006									Reserved
$1007	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
$1008	0	0	PD5	PD4	PD3	PD2	PD1	PD0	PORTD
$1009	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
$100A	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	PORTE
$100B	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0	CFORC
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0	OC1M
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0	OC1D
$100E	Bit 15	14	13	12	11	10	9	Bit 8	TCNT (High)
$100F	Bit 7	6	5	4	3	2	1	Bit 0	TCNT (Low)
$1010	Bit 15	14	13	12	11	10	9	Bit 8	TIC1 (High)
$1011	Bit 7	6	5	4	3	2	1	Bit 0	TIC1 (Low)
$1012	Bit 15	14	13	12	11	10	9	Bit 8	TIC2 (High)
$1013	Bit 7	6	5	4	3	2	1	Bit 0	TIC2 (Low)
$1014	Bit 15	14	13	12	11	10	9	Bit 8	TIC3 (High)
$1015	Bit 7	6	5	4	3	2	1	Bit 0	TIC3 (Low)
$1016	Bit 15	14	13	12	11	10	9	Bit 8	TOC1(High)
$1017	Bit 7	6	5	4	3	2	1	Bit 0	TOC1 (Low)
$1018	Bit 15	14	13	12	11	10	9	Bit 8	TOC2 (High)
$1019	Bit 7	6	5	4	3	2	1	Bit 0	TOC2 (Low)
$101A	Bit 15	14	13	12	11	10	9	Bit 8	TOC3 (High)
$101B	Bit 7	6	5	4	3	2	1	Bit 0	TOC3 (Low)
$101C	Bit 15	14	13	12	11	10	9	Bit 8	TOC4 (High)
$101D	Bit 7	6	5	4	3	2	1	Bit 0	TOC4 (Low)
$101E	Bit 15	14	13	12	11	10	9	Bit 8	TOC5 (High)
$101F	Bit 7	6	5	4	3	2	1	Bit 0	TOC5 (Low)
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1
$1021	0	0	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2
$1022	OC1I	OC2I	OC3I	OC4I	OC5I	IC1I	IC2I	IC3I	TMSK1
$1023	OC1F	OC2F	OC3F	OC4F	OC5F	IC1F	IC2F	IC3F	TFLG1
$1024	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0	TMSK2
$1025	TOF	RTIF	PAOVF	PAIF	0	0	0	0	TFLG2

Table 3 MC68HC11A8 Register and Control Bit Assignments (Sheet 2 of 2)

(The register block can be remapped to any 4K boundary.)

	Bit 7	6	5	4	3	2	1	Bit 0	
$1026	DDRA7	PAEN	PAMOD	PEDGE	0	0	RTR1	RTR0	PACTL
$1027	Bit 7	6	5	4	3	2	1	Bit 0	PACNT
$1028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
$1029	SPIF	WCOL	0	MODF	0	0	0	0	SPSR
$102A	Bit 7	6	5	4	3	2	1	Bit 0	SPDR
$102B	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD
$102C	R8	T8	0	M	WAKE	0	0	0	SCCR1
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2
$102E	TDRE	TC	RDRF	IDLE	OR	NF	FE	0	SCSR
$102F	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0	SCDR
$1030	CCF	0	SCAN	MULT	CD	CC	CB	CA	ADCTL
$1031	Bit 7	6	5	4	3	2	1	Bit 0	ADR1
$1032	Bit 7	6	5	4	3	2	1	Bit 0	ADR2
$1033	Bit 7	6	5	4	3	2	1	Bit 0	ADR3
$1034	Bit 7	6	5	4	3	2	1	Bit 0	ADR4
$1035									Reserved
$1038									Reserved
$1039	ADPU	CSEL	IRQE	DLY	CME	0	CR1	CR0	OPTION
$103A	Bit 7	6	5	4	3	2	1	Bit 0	COPRST
$103B	ODD	EVEN	0	BYTE	ROW	ERASE	EELAT	EEPGM	PPROG
$103C	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT
$103E	TILOP	0	OCCR	CBYP	DISR	FCM	FCOP	TCON	TEST1
$103F	0	0	0	0	NOSEC	NOCOP	ROMON	EEON	CONFIG

HPRIO — Highest Priority I-Bit Interrupt and Miscellaneous **$103C**

	Bit 7	6	5	4	3	2	1	Bit 0
	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0
RESET:	—	—	—	—	0	1	0	1

RBOOT, SMOD, and MDA reset depend on conditions at reset and can only be written in special modes (SMOD = 1).

RBOOT — Read Bootstrap ROM
0 = Bootloader ROM disabled and not in map
1 = Bootloader ROM enabled and in map at $BF40–$BFFF

SMOD —Special Mode Select

MDA — Mode Select A

Inputs		Mode	Latched at Reset		
MODB	**MODA**		**RBOOT**	**SMOD**	**MDA**
1	0	Single Chip	0	0	0
1	1	Expanded Multiplexed	0	0	1
0	0	Special Bootstrap	1	1	0
0	1	Special Test	0	1	1

IRV — Internal Read Visibility
0 = No internal read visibility on external bus
1 = Data from internal reads is driven out through the external data bus

PSEL3–PSEL0 — Priority Select Bits 3 through 0
Refer to **3 Resets and Interrupts**.

INIT — RAM and I/O Mapping **$103D**

	Bit 7	6	5	4	3	2	1	Bit 0
	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0
RESET:	0	0	0	0	0	0	0	1

RAM[3:0] —256-Byte Internal RAM Map Position
RAM[3:0] determine the upper four bits of the RAM address, positioning RAM at the selected 4K boundary.

REG[3:0] —64-Byte Register Block Map Position
REG[3:0] determine the upper four bits of the register address, positioning registers at the selected 4K boundary. Register can be written only once in the first 64 cycles out of reset in normal modes, or any time in special modes.

TEST1 — Factory Test **$103E**

	Bit 7	6	5	4	3	2	1	Bit 0
	TILOP	0	OCCR	CBYP	DISR	FCM	FCOP	TCON
RESET:	0	0	0	0	—	0	0	0

Test Modes Only

TILOP — Test Illegal Opcode

OCCR — Output Condition Code Register to Timer Port

CBYP — Timer Divider Chain Bypass

DISR — Disable Resets from COP and Clock Monitor
DISR is forced to one out of reset in special test and bootstrap modes.

FCM — Force Clock Monitor Failure

FCOP — Force COP Watchdog Failure

TCON — Test Configuration Register

CONFIG — COP, ROM, EEPROM Enables **$103F**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	0	0	NOSEC	NOCOP	ROMON	EEON
RESET:	0	0	0	0	—	—	—	—

NOTE

The bits of this register are implemented with EEPROM cells. Programming and erasing follow normal EEPROM procedures. The erased state of CONFIG is $0F. A new value is not readable until after a subsequent reset sequence. CONFIG can only be programmed or erased in special modes.

NOSEC — EEPROM Security Disable
Refer to **4 Electrically Erasable Programmable Read-Only Memory (EEPROM)**.

NOCOP — COP System Disable
Refer to **3 Resets and Interrupts**.

ROMON — ROM Enable
In single-chip mode, ROMON is forced to one out of reset.
0 = 8K ROM removed from the memory map
1 = 8K ROM present in the memory map

EEON — EEPROM Enable
0 = EEPROM is removed from the memory map
1 = EEPROM is present in the memory map

3 Resets and Interrupts

The MC68HC11A8 has three reset vectors and 18 interrupt vectors. The reset vectors are as follows:

- $\overline{\text{RESET}}$, or Power-On
- COP Clock Monitor Fail
- COP Failure

The eight interrupt vectors service 23 interrupt sources (three non-maskable, 20 maskable). The three non-maskable interrupt vectors are as follows:

- Illegal Opcode Trap
- Software Interrupt
- $\overline{\text{XIRQ}}$ Pin (Pseudo Non-Maskable Interrupt)

The 20 maskable interrupt sources are subject to masking by a global interrupt mask, the I bit in the condition code register (CCR). In addition to the global I bit, all of these sources except the external interrupt ($\overline{\text{IRQ}}$) pin are controlled by local enable bits in control registers. Most interrupt sources in the M68HC11 have separate interrupt vectors. For this reason, there is usually no need for software to poll control registers to determine the cause of an interrupt. The maskable interrupt sources respond to a fixed priority relationship, except that any one source can be dynamically elevated to the highest priority position of any maskable source. Refer to the table of interrupt and reset vector assignments.

On-chip peripheral systems generate maskable interrupts that are recognized only if the I bit in the CCR is clear. Maskable interrupts are prioritized according to a default arrangement, but any one source can be elevated to the highest maskable priority position by the HPRIO register. The HPRIO register can be written at any time, provided the I bit in the CCR is set.

For some interrupt sources, such as the parallel I/O and SCI interrupts, the flags are automatically cleared during the course of responding to the interrupt requests. For example, the RDRF flag in the SCI system is cleared by the automatic clearing mechanism, which consists of a read of the SCI status register while RDRF is set, followed by a read of the SCI data register. The normal response to an RDRF interrupt request is to read the SCI status register to check for receive errors, then to read the received data from the SCI data register. These two steps satisfy the automatic clearing mechanism without requiring any special instructions.

The real-time interrupt (RTI) function generates hardware interrupts at a fixed periodic rate. These hardware interrupts provide a time reference signal for routines that measure real time. The routine notes the number of times a particular interrupt has occurred and multiplies that number by the predetermined subroutine execution time.

There are four RTI signal rates available in the MC68HC11A8. The MCU oscillator frequency and the value of two software-accessible control bits, RTR1 and RTR0, in the pulse accumulator control register (PACTL) determine these signal rates. Refer to **8 Main Timer** for more information about PACTL.

Table 4 Interrupt and Reset Vector Assignments

Vector Address	Interrupt Source	CCR Mask	Local Mask
FFC0, C1 – FFD4, D5	Reserved	—	—
FFD6, D7	SCI Serial System	I Bit	
	• SCI Transmit Complete		TCIE
	• SCI Transmit Data Register Empty		TIE
	• SCI Idle Line Detect		ILIE
	• SCI Receiver Overrun		RIE
	• SCI Receive Data Register Full		RIE
FFD8, D9	SPI Serial Transfer Complete	I Bit	SPIE
FFDA, DB	Pulse Accumulator Input Edge	I Bit	PAII
FFDC, DD	Pulse Accumulator Overflow	I Bit	PAOVI
FFDE, DF	Timer Overflow	I Bit	TOI
FFE0, E1	Timer Input Capture 4/Output Compare 5	I Bit	I4O5I
FFE3, E2	Timer Output Compare 4	I Bit	OC4I
FFE4, E5	Timer Output Compare 3	I Bit	OC3I
FFE6, E7	Timer Output Compare 2	I Bit	OC2I
FFE8, E9	Timer Output Compare 1	I Bit	OC1I
FFEA, EB	Timer Input Capture 3	I Bit	IC3
FFEC, ED	Timer Input Capture 2	I Bit	IC2I
FFEE, EF	Timer Input Capture 1	I Bit	IC1I
FFF0, F1	Real-Time Interrupt	I Bit	RTII
FFF2, F3	Parallel I/O Handshake	I Bit	STAI
	$\overline{\text{IRQ}}$		None
FFF4, F5	$\overline{\text{XIRQ}}$ Pin	X Bit	None
FFF6, F7	Software Interrupt	None	None
FFF8, F9	Illegal Opcode Trap	None	None
FFFA, FB	COP Failure	None	NOCOP
FFFC, FD	COP Clock Monitor Fail	None	CME
FFFE, FF	RESET	None	None

OPTION —System Configuration Options **$1039**

	Bit 7	6	5	4	3	2	1	Bit 0
	ADPU	CSEL	IRQE*	DLY*	CME	0	CR1*	CR0*
RESET:	0	0	0	1	0	0	0	0

*Can be written only once in first 64 cycles out of reset in normal modes, or any time in special modes.

ADPU —A/D Converter Power-up
Refer to **10 Analog-to-Digital Converter**.

CSEL —Clock Select
Refer to **10 Analog-to-Digital Converter**.

IRQE — $\overline{\text{IRQ}}$ Select Edge-Sensitive Only
0 = Low logic level recognition
1 = Falling edge recognition

DLY — Enable Oscillator Start-Up Delay on Exit from STOP
0 = No stabilization delay on exit from STOP
1 = Stabilization delay enabled on exit from STOP

CME — Clock Monitor Enable
0 = Clock monitor disabled; slow clocks can be used
1 = Slow or stopped clocks cause clock failure reset

CR1, CR0 — COP Timer Rate Select

CR [1:0]	Divide E/2^{15} By	XTAL = 4.0 Mhz Timeout –0/+32.8 ms	XTAL = 8.0 MHz Timeout –0/+16.4 ms	XTAL = 12.0 MHz Timeout –0/+10.9 ms
0 0	1	32.768 ms	16.384 ms	10.923 ms
0 1	4	131.072 ms	65.536 ms	43.691 ms
1 0	16	524.288 ms	262.140 ms	174.76 ms
1 1	64	2.097 sec	1.049 sec	699.05 ms
	E =	1.0 MHz	2.0 MHz	3.0 MHz

COPRST — Arm/Reset COP Timer Circuitry **$103A**

	Bit 7	6	5	4	3	2	1	Bit 0
	7	6	5	4	3	2	1	0
RESET:	0	0	0	0	0	0	0	0

Write $55 to COPRST to arm COP watchdog clearing mechanism. Write $AA to COPRST to reset COP watchdog.

HPRIO — Highest Priority I-Bit Interrupt and Miscellaneous **$103C**

	Bit 7	6	5	4	3	2	1	Bit 0
	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0
RESET:	—	—	—	—	0	1	0	1

RBOOT — Read Bootstrap ROM Bits 7–4
Refer to **2 Operating Modes and Memory Maps**.

SMOD — Special Mode Select
Refer to **2 Operating Modes and Memory Maps**.

MDA — Mode Select A
Refer to **2 Operating Modes and Memory Maps**.

IRV — Internal Read Visibility
Refer to **2 Operating Modes and Memory Maps**.

PSEL[3:0] — Priority Select Bits 3 through 0
Can be written only while the I bit in the CCR is set (interrupts disabled). These bits select one interrupt source to be elevated above all other I-bit related sources.

PSEL[3:0]	Interrupt Source Promoted
0000	Timer Overflow
0001	Pulse Accumulator Overflow
0010	Pulse Accumulator Input Edge
0011	SPI Serial Transfer Complete
0100	SCI Serial System
0101	Reserved (Default to $\overline{IRQ}$)
0110	$\overline{IRQ}$
0111	Real-Time Interrupt
1000	Timer Input Capture 1
1001	Timer Input Capture 2
1010	Timer Input Capture 3
1011	Timer Output Compare 1
1100	Timer Output Compare 2
1101	Timer Output Compare 3
1110	Timer Output Compare 4
1111	Timer Output Compare 5

CONFIG — COP, ROM, EEPROM Enables **$103F**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	0	0	NOSEC	NOCOP	ROMON	EEON
RESET:	0	0	0	0	—	—	—	—

NOTE

The bits of this register are implemented with EEPROM cells. Programming and erasing follow normal EEPROM procedures. The erased state of CONFIG is $0F. A new value is not readable until after a subsequent reset sequence. CONFIG can only be programmed or erased in special modes.

NOSEC — EEPROM Security Disable

Refer to **4 Electrically Erasable Programmable Read-Only Memory (EEPROM)**.

NOCOP — COP system disable

0 = COP enabled (forces reset on timeout)

1 = COP disabled (does not force reset on timeout)

ROMON — ROM Enable

Refer to **2 Operating Modes and Memory Maps**.

EEON — EEPROM Enable

Refer to **2 Operating Modes and Memory Maps**.

4 Electrically Erasable Programmable Read-Only Memory (EEPROM)

The 512 bytes of EEPROM in the MC68HC11A8 are located at $B600 through $B7FF. The EEON bit in CONFIG controls the presence or absence of the EEPROM in the memory map. When EEON = 1 (erased state), the EEPROM is enabled. When EEON = 0, the EEPROM is disabled and out of the memory map. EEON is reset to the value last programmed into CONFIG. An on-chip charge pump develops the high voltage required for programming and erasing. When the E clock is less than 1 MHz, select an internal clock. This drives the EEPROM charge pump by writing a one to the CSEL bit in the OPTION register.

The PPROG register controls the programming and erasing of the EEPROM. To erase the EEPROM, complete the following steps using the PPROG register:

1. Write to PPROG with the ERASE, EELAT, and appropriate BYTE and ROW bits set.
2. Write to the appropriate EEPROM address with any data. Row erase only requires a write to any location in the row. Bulk erase is accomplished by writing to any location in the array.
3. Write to PPROG with ERASE, EELAT, EEPGM, and the appropriate BYTE and ROW bits set.
4. Delay for 10 ms or more, as appropriate.
5. Clear the EEPGM bit in PPROG to turn off the high voltage.
6. Clear the PPROG register to reconfigure the EEPROM address and data buses for normal operation.

To program the EEPROM, complete the following steps using the PPROG register:

1. Write to PPROG with the EELAT bit set.
2. Write data to the desired address.
3. Write to PPROG with the EELAT and EEPGM bits set.
4. Delay for 10 ms or more, as appropriate.
5. Clear the EEPGM bit in PPROG to turn off the high voltage.
6. Clear the PPROG register to reconfigure the EEPROM address and data buses for normal operation.

PPROG — EEPROM Programming Control **$103B**

	Bit 7	6	5	4	3	2	1	Bit 0
	ODD	EVEN	0	BYTE	ROW	ERASE	EELAT	EEPGM
RESET:	0	0	0	0	0	0	0	0

ODD — Program Odd Rows in Half of EEPROM (TEST)

EVEN — Program Even Rows in Half of EEPROM (TEST)

BYTE — Byte/Other EEPROM Erase Mode
The BYTE bit overrides the ROW bit.
0 = Row or bulk erase mode is used
1 = Erase only one byte of EEPROM

ROW — Row/All EEPROM Erase Mode
The ROW bit is only valid when BYTE = 0.
0 = All 512 bytes of EEPROM are erased
1 = Erase only one 16-byte row of EEPROM

BYTE	ROW	Action
0	0	Bulk Erase (All 512 Bytes)
0	1	Row Erase (16 Bytes)
1	0	Byte Erase
1	1	Byte Erase

ERASE — Erase/Normal Control for EEPROM

0 = Normal read or program mode
1 = Erase mode

EELAT — EEPROM Latch Control

0 = EEPROM address and data bus configured for normal reads
1 = EEPROM address and data bus configured for programming or erasing

EEPGM — EEPROM Program Command

0 = Programming or erase voltage switched off to EEPROM array
1 = Programming or erase voltage switched on to EEPROM array

CONFIG — COP, ROM, EEPROM Enables **$103F**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	0	0	NOSEC	NOCOP	ROMON	EEON
RESET:	0	0	0	0	—	—	—	—

NOTE

The bits of this register are implemented with EEPROM cells. Programming and erasing follow normal EEPROM procedures. The erased state of CONFIG is $0F. A new value is not readable until after a subsequent reset sequence. CONFIG can only be programmed or erased in special modes.

NOSEC — EEPROM Security Disable

NOSEC has no meaning unless the security mask option was specified before the MCU was manufactured.

0 = Security enabled (available as a mask option on MC68HC11A8 only)
1 = Security disabled

NOCOP — COP system disable

Refer to **3 Resets and Interrupts**.

ROMON — ROM Enable

Refer to **2 Operating Modes and Memory Maps**.

EEON — EEPROM Enable

0 = EEPROM is removed from the memory map
1 = EEPROM is present in the memory map

5 Parallel Input/Output

The MC68HC11A8 has up to 38 input/output lines, depending on the operating mode. Port A has three input-only pins, four output-only pins, and one bidirectional I/O pin. Port A shares functions with the timer system.

Port B is an 8-bit output-only port in single-chip modes and is the high-order address in expanded modes.

Port C is an 8-bit bidirectional port in single-chip modes and the multiplexed address and data bus in expanded modes.

Port D is a 6-bit bidirectional port that shares functions with the serial systems.

Port E is an 8-bit input-only port that shares functions with the A/D system.

Simple and full handshake input and output functions are available on ports B and C lines in single-chip mode. A description of the handshake functions follows.

In port B simple strobed output mode, the STRB output is pulsed for two E-clock periods each time there is a write to the PORTB register. The INVB bit in the PIOC register controls the polarity of STRB pulses.

In port C simple strobed input mode, port C levels are latched into the alternate port C latch (PORTCL) register on each assertion of the STRA input. STRA edge select, flag and interrupt enable bits are located in the PIOC register. Any or all of the port C lines can still be used as general purpose I/O while in strobed input mode.

Port C full handshake mode involves port C pins and the STRA and STRB lines. Input and output handshake modes are supported, and output handshake mode has a three-stated variation. STRA is an edge detecting input, and STRB is a handshake output. Control and enable bits are located in the PIOC register.

In full input handshake mode, the MCU uses STRB as a “ready” line to an external system. Port C logic levels are latched into PORTCL when the STRA line is asserted by the external system. The MCU then negates STRB. The MCU reasserts STRB after the PORTCL register is read. A mix of latched inputs, static inputs, and static outputs is allowed on port C, differentiated by the data direction bits and use of the PORTC and PORTCL registers.

In full output handshake mode, the MCU writes data to PORTCL, which in turn asserts the STRB output to indicate that data is ready. The external system reads port C (the STRB output) and asserts the STRA input to acknowledge that data has been received.

In the three-state variation of output handshake mode, lines intended as three-state handshake outputs are configured as inputs by clearing the corresponding DDRC bits. The MCU writes data to PORTCL and asserts STRB. The external system responds by activating the STRA input, which forces the MCU to drive the data in PORTCL out on all of the port C lines. This mode variation does not allow part of port C to be used for static inputs while other port C pins are being used for handshake outputs. Refer to the PIOC register description.

PORTA — Port A Data **$1000**

	Bit 7	6	5	4	3	2	1	Bit 0
	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
RESET:	HiZ	0	0	0	0	HiZ	HiZ	HiZ
Alt. Pin Func.:	PAI	OC2	OC3	OC4	OC5	IC1	IC2	IC3
And/or:	OC1	OC1	OC1	OC1	OC1	—	—	—

PIOC — Parallel I/O Control **$1002**

	Bit 7	6	5	4	3	2	1	Bit 0
	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB
RESET:	0	0	0	0	0	U	1	1

STAF — Strobe A Interrupt Status Flag

Set when selected edge occurs on Strobe A. Cleared by PIOC read with STAF set followed by PORTCL read (simple strobed or full input handshake mode) or PORTCL write (output handshake mode).

STAI — Strobe A Interrupt Enable Mask

0 = STAF interrupts disabled
1 = STAF interrupts enabled

CWOM — Port C Wire-OR Mode (affects all eight port C pins)

0 = Port C outputs are normal CMOS outputs
1 = Port C outputs are open-drain outputs

HNDS — Handshake Mode

0 = Simple strobe mode
1 = Full input or output handshake mode

OIN — Output or Input Handshake Select

HNDS must be set to one for this bit to have meaning.

0 = Input handshake
1 = Output handshake

PLS — Pulse/Interlocked Handshake Operation

HNDS must be set to one for this bit to have meaning.

0 = Interlocked handshake
1 = Pulsed handshake (strobe B pulses high for two E-clock cycles)

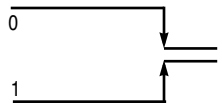
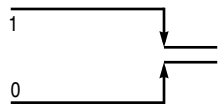
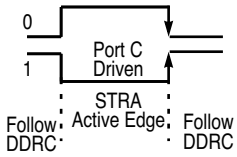
EGA — Active Edge for Strobe A

0 = STRA falling edge selected
1 = STRA rising edge selected

INVB — Invert Strobe B

0 = Active level is logic zero
1 = Active level is logic one

Table 5 Parallel I/O Control

	STAF Clearing Sequence	HNDS	OIN	PLS	EGA	Port C	Port B
Simple strobed mode	Read PIOC with STAF=1 then read PORTCL	0	X	X		Inputs latched into PORTCL on any active edge on STRA	STRB pulses on writes to port B
Full input handshake	Read PIOC with STAF=1 then read PORTCL	1	0	0 = STRB active level 1 = STRB active pulse		Inputs latched into PORTCL on any active edge on STRA	Normal output port, unaffected in handshake modes
Full output handshake	Read PIOC with STAF=1 then write to PORTCL	1	1	0 = STRB active level 1 = STRB active pulse		Driven as outputs if STRA at active level, follows DDRC if STRA not at active level	Normal output port, unaffected in handshake modes

PORTC — Port C Data **$1003**

	Bit 7	6	5	4	3	2	1	Bit 0
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
S. Chip or Boot:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
RESET:	0	0	0	0	0	0	0	0
Expan. or Test:	ADDR7/ DATA7	ADDR6/ DATA6	ADDR5/ DATA5	ADDR4/ DATA4	ADDR3/ DATA3	ADDR2/ DATA2	ADDR1/ DATA1	ADDR0/ DATA0

NOTE

In single chip and boot modes, port C pins reset to high impedance inputs (DDRC registers are set to zero). In expanded and special test modes, port C is a multiplexed address/data bus and the port C register address is treated as an external memory location.

PORTB — Port B Data **$1004**

	Bit 7	6	5	4	3	2	1	Bit 0
	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
S. Chip or Boot:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
RESET:	0	0	0	0	0	0	0	0
Expan. or Test:	ADDR15	ADDR14	ADDR13	ADDR12	ADDR11	ADDR10	ADDR9	ADDR8

PORTCL — Port C Latched **$1005**

	Bit 7	6	5	4	3	2	1	Bit 0
	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0
RESET:	U	U	U	U	U	U	U	U

Writes affect port C pins. PORTCL is used in the handshake clearing mechanism. When an active edge occurs on the STRA pin, port C data is latched into the PORTCL register.

DDRC — Data Direction Register for Port C **$1007**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
RESET:	0	0	0	0	0	0	0	0

DDC[7:0] — Data Direction Register for Port C
0 = Input
1 = Output

PORTD — Port D Data **$1008**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	PD5	PD4	PD3	PD2	PD1	PD0
RESET:	0	0	0	0	0	0	0	0
Alt. Pin Func.:	—	—	$\overline{SS}$	SCK	MOSI	MISO	TxD	RxD

DDRD — Data Direction Register for Port D **$1009**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
RESET:	0	0	0	0	0	0	0	0
Alt. Pin Func.:	—	—	PD5/ $\overline{SS}$	PD4/ SCK	PD3/ MOSI	PD2/ MISO	PD1/ TxD	PD0/ RxD

DDD[5:0] — Data Direction for Port D
0 = Input
1 = Output

PORTE — Port E Data **$100A**

	Bit 7	6	5	4	3	2	1	Bit 0
	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
RESET:	U	U	U	U	U	U	U	U
Alt. Pin Func.:	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

PACTL — Pulse Accumulator Control **$1026**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRA7	PAEN	PAMOD	PEDGE	0	0	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

DDRA7 — Data Direction for Port A Bit 7
0 = Input
1 = Output

PAEN — Pulse Accumulator System Enable
Refer to **9 Pulse Accumulator**.

PAMOD — Pulse Accumulator Mode
Refer to **9 Pulse Accumulator**.

PEDGE — Pulse Accumulator Edge Control
Refer to **9 Pulse Accumulator**.

RTR1, RTR0 — Real-Time Interrupt Rate
Refer to **8 Main Timer**.

6 Serial Communications Interface (SCI)

The SCI, a universal asynchronous receiver transmitter (UART) serial communications interface, is one of two independent serial I/O subsystems in the MC68HC11A8. It has a standard NRZ format (one start, eight or nine data, and one stop bit) and several baud rates available. The SCI transmitter and receiver are independent, but use the same data format and bit rate.

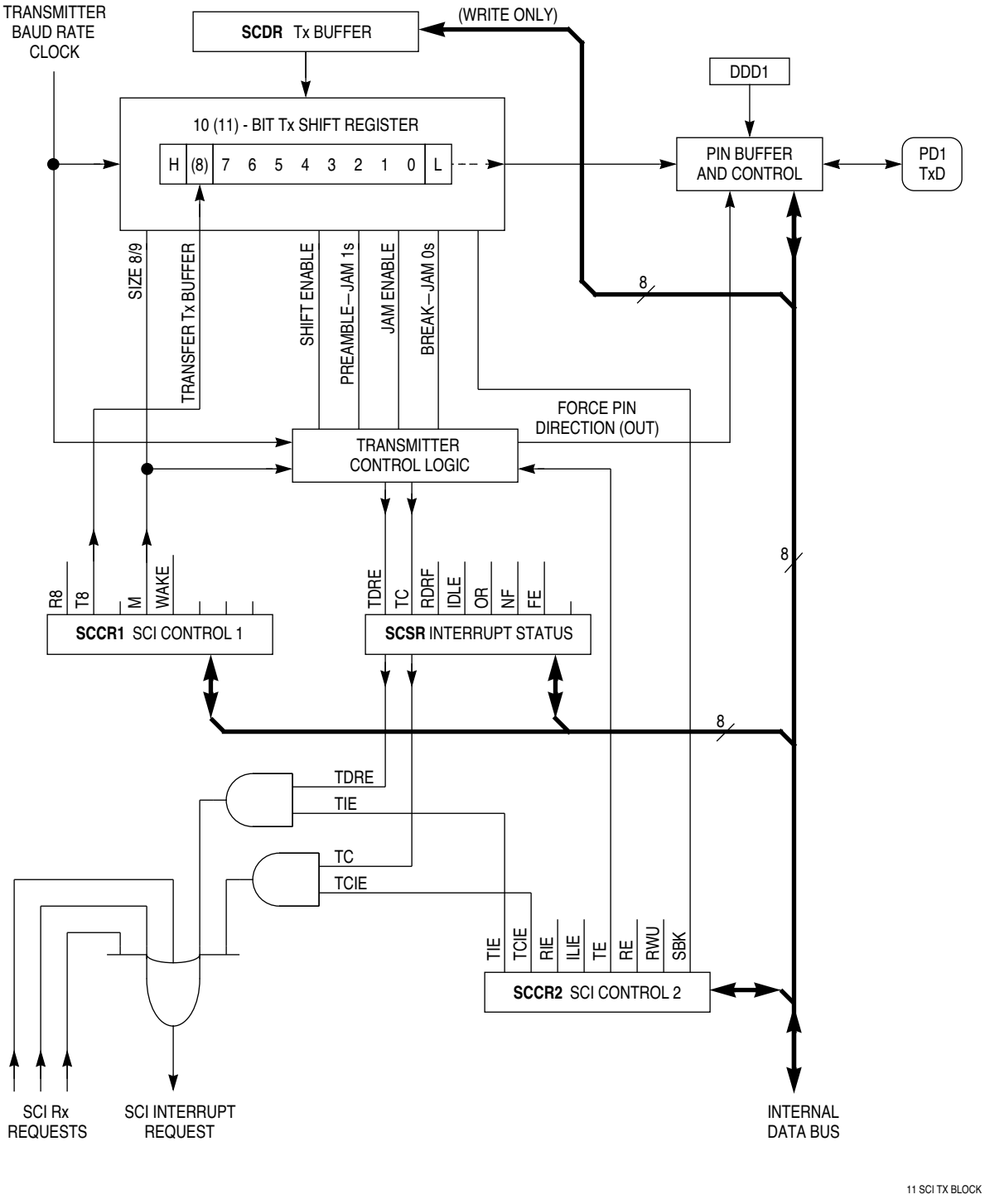


Figure 6 SCI Transmitter Block Diagram

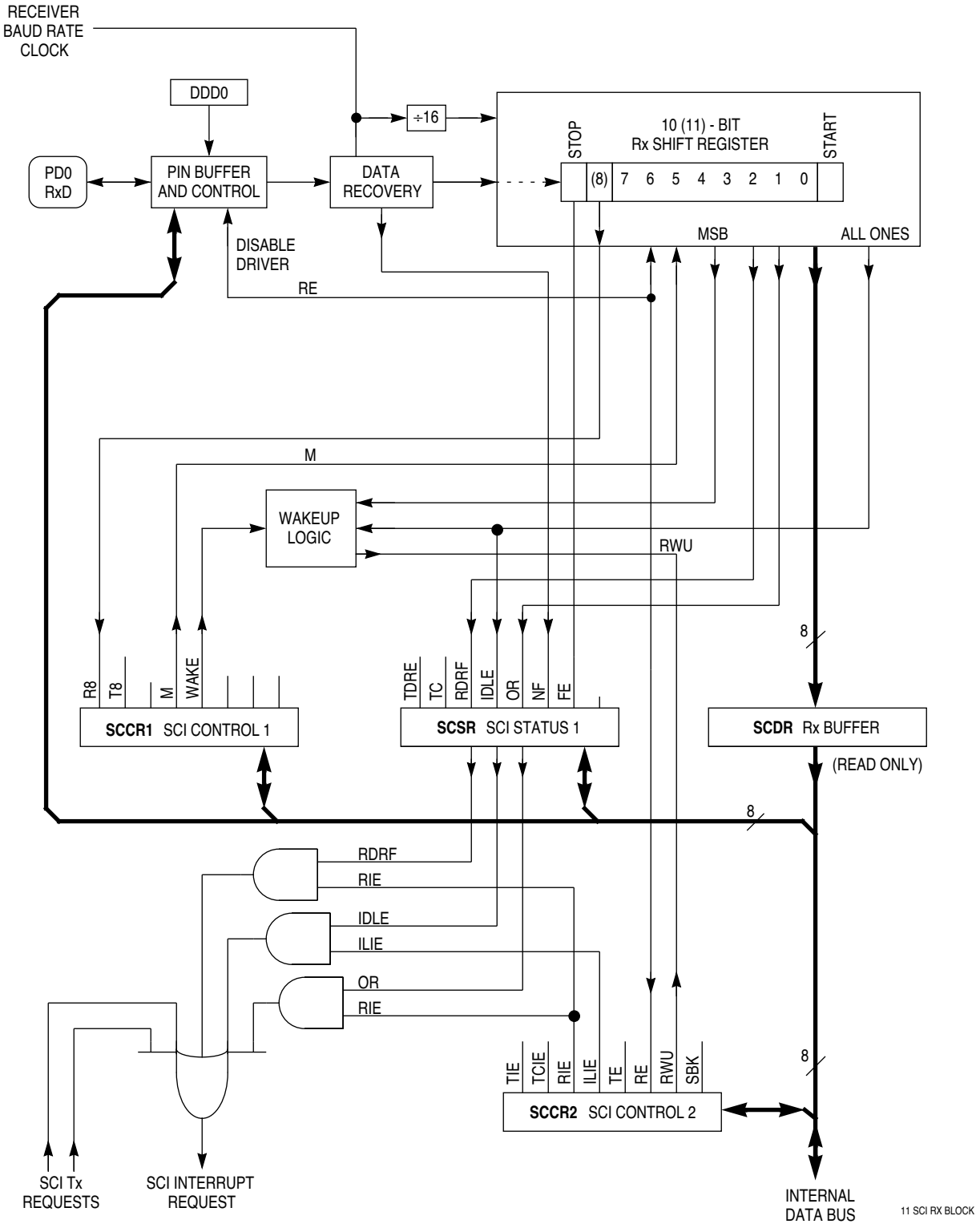


Figure 7 SCI Receiver Block Diagram

BAUD — Baud Rate **$102B**

	Bit 7	6	5	4	3	2	1	Bit 0
	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
RESET:	0	0	0	0	0	U	U	U

TCLR — Clear Baud Rate Counters (TEST)

SCP1, SCP0 — SCI Baud Rate Prescaler Selects

SCP[1:0]	Divide Internal Clock By	Crystal Frequency in MHz			
		4.0 MHz (Baud)	8.0 MHz (Baud)	10.0 MHz (Baud)	12.0 MHz (Baud)
00	1	62.50K	125.0K	156.25K	187.5K
01	3	20.83K	41.67K	52.08K	62.5K
10	4	15.625K	31.25K	38.4K	46.88K
11	13	4800	9600	12.02K	14.42K

RCKB — SCI Baud Rate Clock Check (TEST)

SCR2, SCR1, and SCR0 — SCI Baud Rate Selects

Selects receiver and transmitter bit rate based on output from baud rate prescaler stage.

SCP[2:0]	Divide Prescaler By	Highest Baud Rate (Prescaler Output from Previous Table)		
		4800	9600	38.4K
000	1	4800	9600	38.4K
001	2	2400	4800	19.2K
010	4	1200	2400	9600
011	8	600	1200	4800
100	16	300	600	2400
101	32	150	300	1200
110	64	—	150	600
111	128	—	—	300

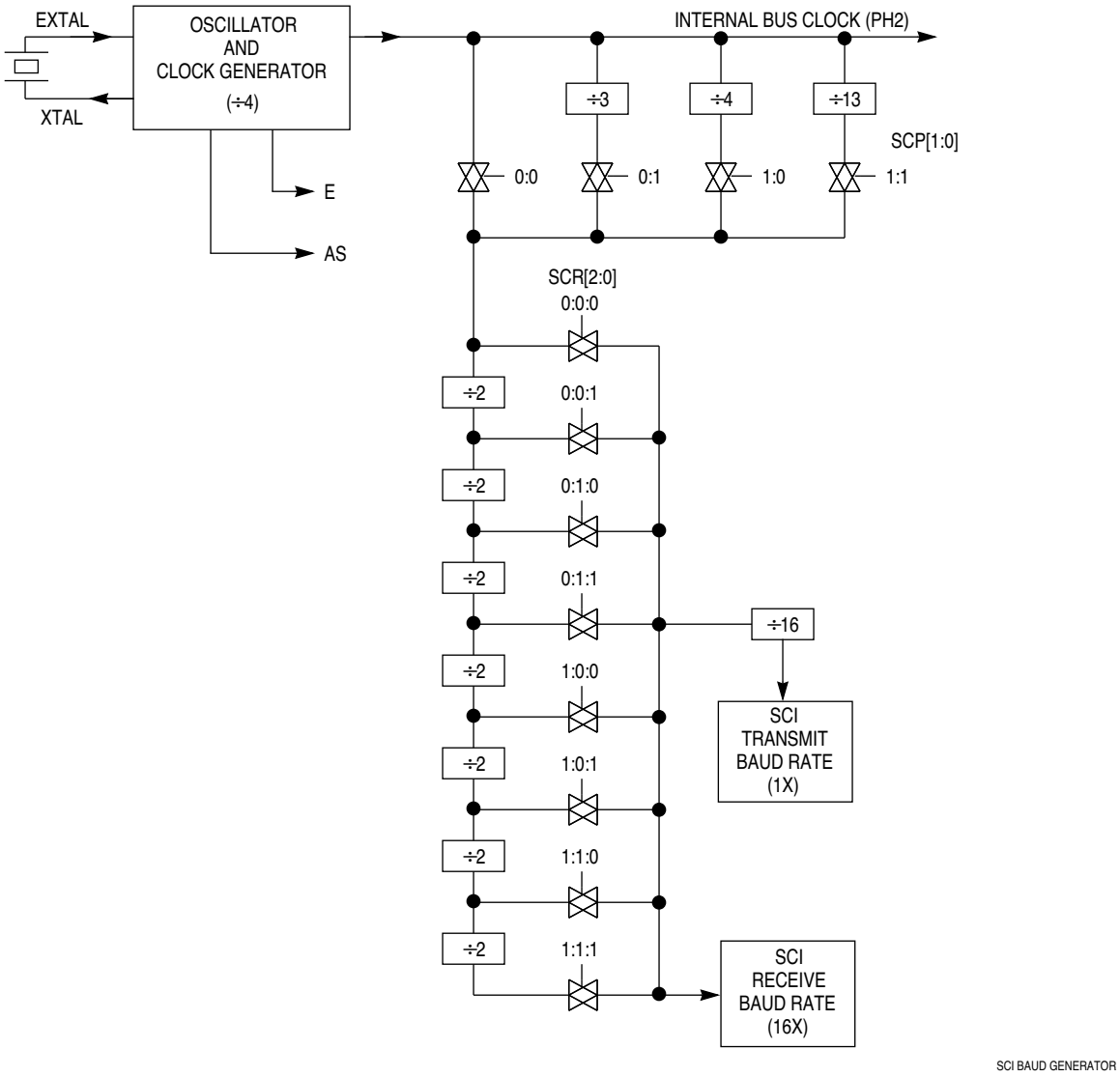


Figure 8 SCI Baud Rate Diagram

SCCR1 — SCI Control Register 1 **$102C**

	Bit 7	6	5	4	3	2	1	Bit 0
	R8	T8	0	M	WAKE	0	0	0
RESET:	U	U	0	0	0	0	0	0

R8 — Receive Data Bit 8
If M bit is set, R8 stores ninth bit in receive data character.

T8 — Transmit Data Bit 8
If M bit is set, T8 stores ninth bit in transmit data character.

M — Mode (Select Character Format)
0 = Start bit, 8 data bits, 1 stop bit
1 = Start bit, 9 data bits, 1 stop bit

WAKE — Wake Up by Address Mark/Idle
0 = Wake up by IDLE line recognition
1 = Wake up by address mark (most significant data bit set)

SCCR2 — SCI Control Register 2 **$102D**

	Bit 7	6	5	4	3	2	1	Bit 0
	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
RESET:	0	0	0	0	0	0	0	0

TIE — Transmit Interrupt Enable
0 = TDRE interrupts disabled
1 = SCI interrupt requested when TDRE status flag is set

TCIE — Transmit Complete Interrupt Enable
0 = TC interrupts disabled
1 = SCI interrupt requested if TC is set to one

RIE — Receiver Interrupt Enable
0 = RDRF and OR interrupts disabled
1 = SCI interrupt requested when RDRF flag or the OR status flag is set

ILIE — Idle Line Interrupt Enable
0 = IDLE interrupts disabled
1 = SCI interrupt requested when IDLE status flag is set

TE — Transmitter Enable
0 = Transmitter disabled
1 = Transmitter enabled

RE — Receiver Enable
0 = Receiver disabled
1 = Receiver enabled

RWU — Receiver Wake Up Control
0 = Normal SCI receiver
1 = Wake up enabled and receiver interrupts inhibited

SBK — Send Break
0 = Break generator off
1 = Break codes generated as long as SBK is set to one

SCSR — SCI Status Register **$102E**

	Bit 7	6	5	4	3	2	1	Bit 0
	TDRE	TC	RDRF	IDLE	OR	NF	FE	0
RESET:	1	1	0	0	0	0	0	0

TDRE — Transmit Data Register Empty Flag
Set if transmit data can be written to SCDR; if TDRE is zero, transmit data register is busy. Cleared by SCSR read with TDRE set followed by SCDR write.

TC — Transmit Complete Flag
Set if transmitter is idle (no data, preamble, or break transmission in progress). Cleared by SCSR read with TC set followed by SCDR write.

RDRF — Receive Data Register Full Flag

Set if a received character is ready to be read from SCDR. Cleared by SCSR read with RDRF set followed by SCDR read.

IDLE — Idle Line Detected Flag

Set if the RxD line is idle. IDLE flag is inhibited when RWU is set to one. Cleared by SCSR read with IDLE set followed by SCDR read. Once cleared, IDLE is not set again until the RxD line has been active and becomes idle again.

OR — Overrun Error Flag

Set if a new character is received before a previously received character is read from SCDR. Cleared by SCSR read with OR set followed by SCDR read.

NF — Noise Error Flag

Set if majority sample logic detects anything other than a unanimous decision. Cleared by SCSR read with NF set followed by SCDR read.

FE — Framing Error

Set if a zero is detected where a stop bit was expected. Cleared by SCSR read with FE set followed by SCDR read.

SCDR — SCI Data Register **$102F**

	Bit 7	6	5	4	3	2	1	Bit 0
	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0
RESET:	U	U	U	U	U	U	U	U

NOTE

Receive and transmit are double buffered. Reads access the receive data buffer and writes access the transmit data buffer.

7 Serial Peripheral Interface (SPI)

The SPI is one of two independent serial communications subsystems that allow the MCU to communicate synchronously with peripheral devices and other microprocessors. Data rates can be as high as one half of the E-clock rate when configured as master, and as fast as the E clock when configured as slave.

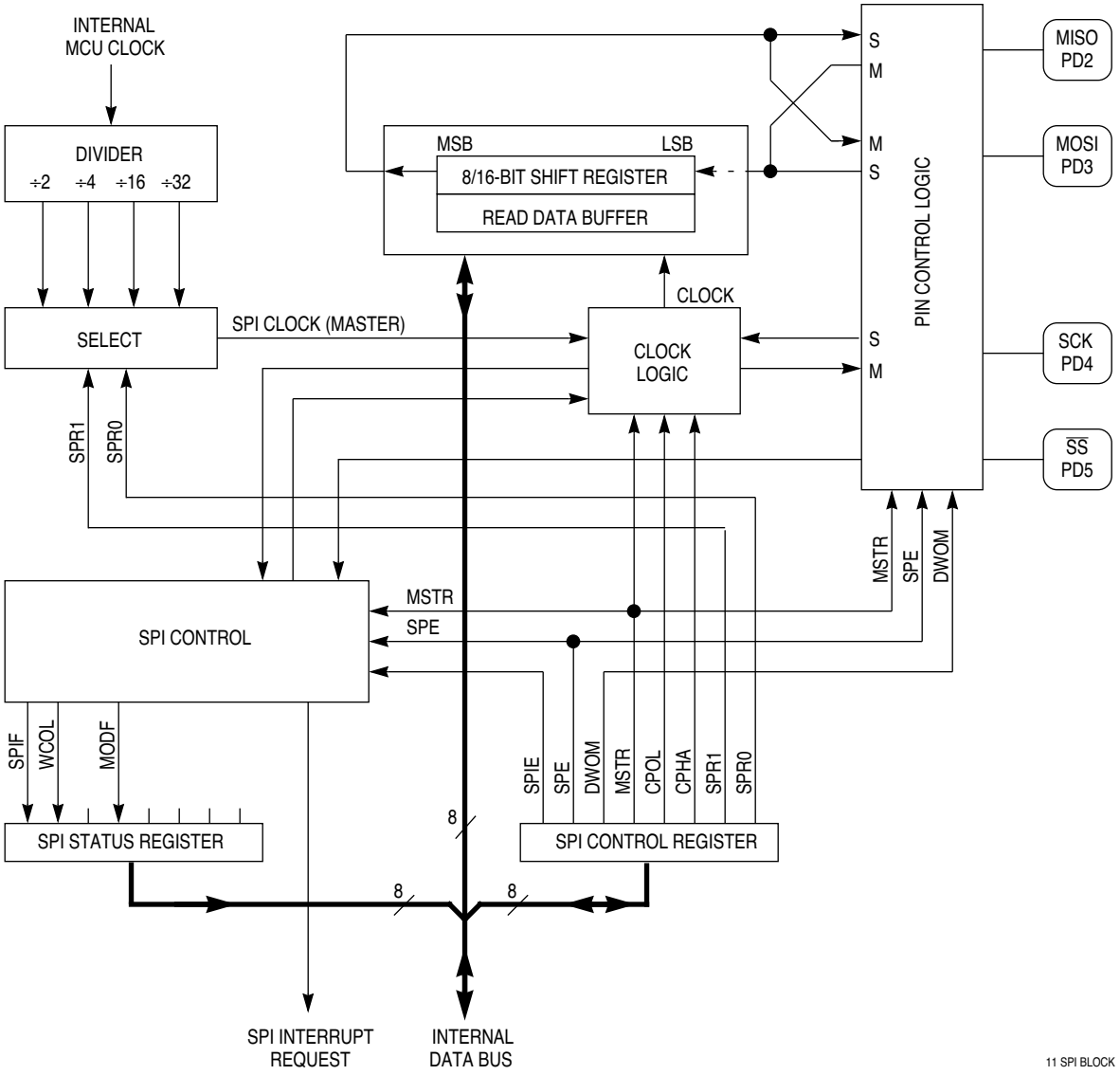


Figure 9 SPI Block Diagram

DDRD — Data Direction Register for Port D **$1009**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
RESET:	0	0	0	0	0	0	0	0
Alt. Pin Func.:	—	—	PD5/ $\overline{SS}$	PD4/ SCK	PD3/ MOSI	PD2/ MISO	PD1/ TxD	PD0/ RxD

DDD[5:0] — Data Direction for Port D

When DDRD bit 5 is zero and MSTR = 1 in SPCR, PD5/$\overline{SS}$ is a general-purpose output and mode fault logic is disabled.

0 = Input
1 = Output

SPCR — Serial Peripheral Control Register **$1028**

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
RESET:	0	0	0	0	0	1	U	U

SPIE — Serial Peripheral Interrupt Enable

0 = SPI interrupts disabled
1 = SPI interrupts enabled

SPE — Serial Peripheral System Enable

0 = SPI off
1 = SPI on

DWOM — Port D Wired-OR Mode

DWOM affects all six port D pins.

0 = Normal CMOS outputs
1 = Open-drain outputs

MSTR — Master Mode Select

0 = Slave mode
1 = Master mode

CPOL, CPHA — Clock Polarity, Clock Phase

Refer to Figure 10

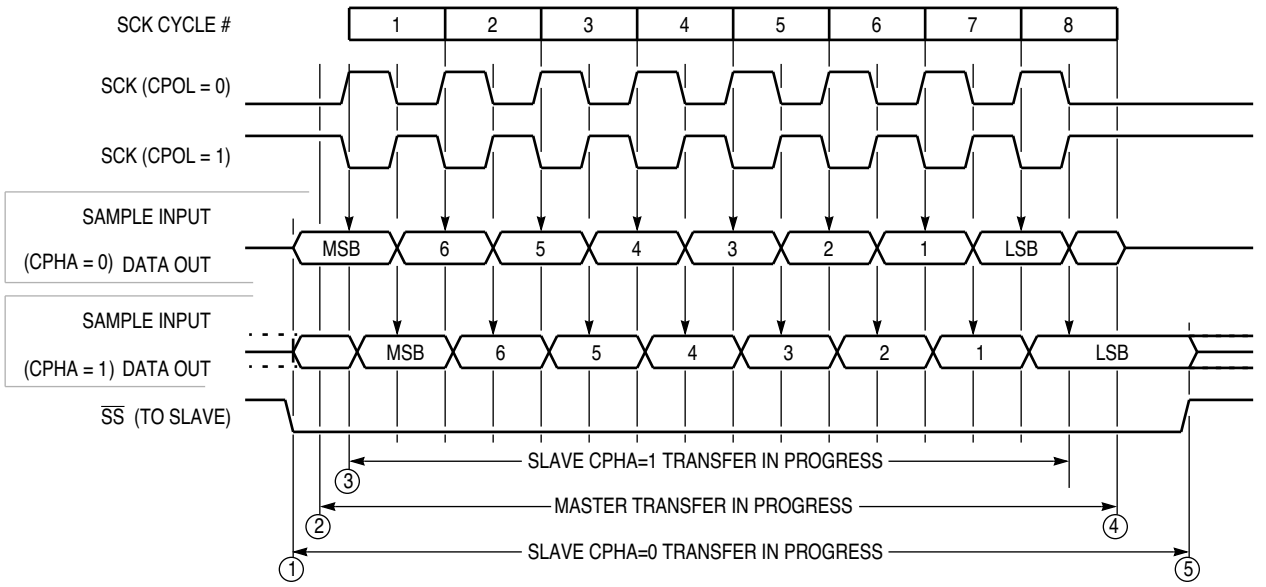


Figure 10 SPI Transfer Format

SPR1 and SPR0 — SPI Clock Rate Selects

SPR [1:0]	E-Clock Divide By	Frequency at E = 2 MHz (Baud)
00	2	1.0 MHz
01	4	500 kHz
10	16	125 kHz
11	32	62.5 kHz

SPSR — Serial Peripheral Status Register **$1029**

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIF	WCOL	0	MODF	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

SPIF — SPI Transfer Complete Flag

Set when an SPI transfer is complete. Cleared by reading SPSR with SPIF set followed by SPDR access.

WCOL — Write Collision

Set when SPDR is written while transfer is in progress. Cleared by SPSR with WCOL set followed by SPDR access.

MODF — Mode Fault (A Mode Fault Terminates SPI Operation)

Set when $\overline{SS}$ is pulled low while MSTR = 1. Cleared by SPSR read with MODF set followed by SPCR write.

SPDR — SPI Data Register **$102A**

Bit 7	6	5	4	3	2	1	Bit 0
Bit 7	6	5	4	3	2	1	Bit 0

NOTE

SPI is double buffered in, single buffered out.

8 Main Timer

The main timer is based on a free-running 16-bit counter with a four-stage programmable prescaler. A timer overflow function allows software to extend the system's timing capability beyond the counter's 16-bit range.

The timer has three channels of input capture and five channels of output compare.

Refer to the following table for a summary of crystal-related frequencies and periods.

Table 6 Timer Summary

Control Bits	XTAL Frequencies			
	4.0 MHz	**8.0 MHz**	**12.0 MHz**	**Other Rates**
	1.0 MHz	**2.0 MHz**	**3.0 MHz**	**(E)**
	1000 ns	**500 ns**	**333 ns**	**(1/E)**
PR[1:0]	**Main Timer Count Rates**			
0 0 1 count — overflow —	1.0 µs 65.536 ms	500 ns 32.768 ms	333 ns 21.845 ms	(E/1) ($E/2^{16}$)
0 1 1 count — overflow —	4.0 µs 262.14 ms	2.0 µs 131.07 ms	1.333 µs 87.381 ms	(E/4) ($E/2^{18}$)
1 0 1 count — overflow —	8.0 µs 524.29 ms	4.0 µs 262.14 ms	2.667 µs 174.76 ms	(E/8) ($E/2^{19}$)
1 1 1 count — overflow —	16.0 µs 1.049 s	8.0 µs 524.29 ms	5.333 µs 349.52 ms	(E/16) ($E/2^{20}$)
RTR[1:0]	**Periodic (RTI) Interrupt Rates**			
0 0 0 1 1 0 1 1	8.192 ms 16.384 ms 32.768 ms 65.536 ms	4.096 ms 8.192 ms 16.384 ms 32.768 ms	2.731 ms 5.461 ms 10.923 ms 21.845 ms	($E/2^{13}$) ($E/2^{14}$) ($E/2^{15}$) ($E/2^{16}$)

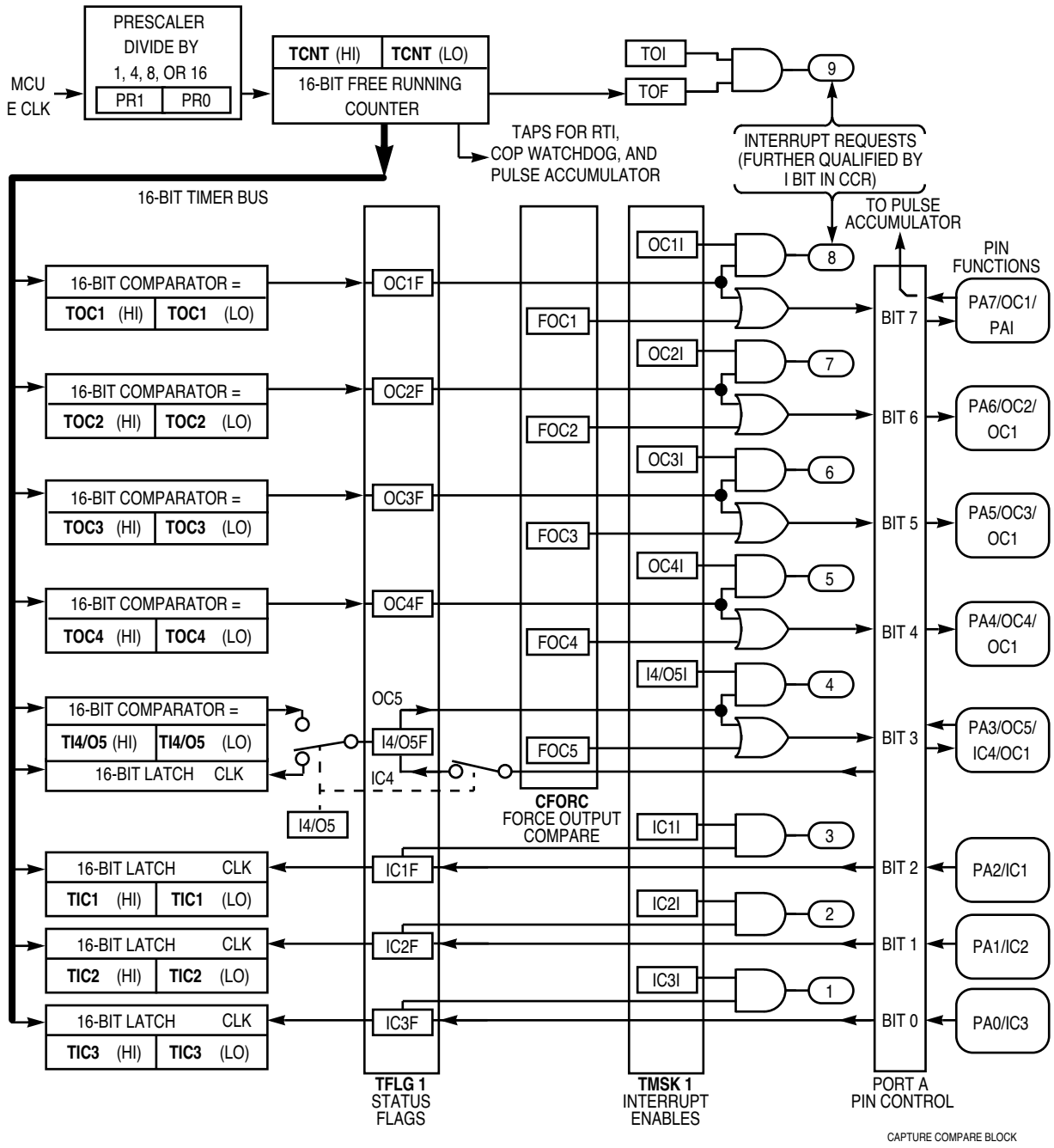


Figure 11 Main Timer

NOTE: Port A pin actions are controlled by OC1M, OC1D, PACTL, TCTL1, and TCTL2 registers.

CFORC — Timer Compare Force **$100B**

	Bit 7	6	5	4	3	2	1	Bit 0
	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0
RESET:	0	0	0	0	0	0	0	0

FOC5–FOC1 — Write ones to Force Compare(s)
0 = Not affected
1 = Output compare x action occurs, but OCxF flag bit not set

OC1M — Output Compare 1 Mask **$100C**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0
RESET:	0	0	0	0	0	0	0	0

Set bit(s) to enable OC1 to control corresponding pin(s) of port A.

OC1D — Output Compare 1 Data **$100D**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0
RESET:	0	0	0	0	0	0	0	0

If OC1Mx is set, data in OC1Dx is output to port A bit x on successful OC1 compares.

TCNT — Timer Counter **$100E, $100F**

$**1**00E	Bit 15	14	13	12	11	10	9	Bit 8	High	**TCNT**
	Bit 7	6	5	4	3	2	1	Bit 0	Low	

TCNT resets to $0000. In normal modes, TCNT is read-only.

TIC1–TIC3 — Timer Input Capture **$1010–$1015**

$**1**010	Bit 15	14	13	12	11	10	9	Bit 8	High	**TIC1**
$**1**011	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$**1**012	Bit 15	14	13	12	11	10	9	Bit 8	High	**TIC2**
$**1**013	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$**1**014	Bit 15	14	13	12	11	10	9	Bit 8	High	**TIC3**
$**1**015	Bit 7	6	5	4	3	2	1	Bit 0	Low	

TICx not affected by reset.

TOC1–TOC5 — Timer Output Compare **$1016–$101F**

$1016	Bit 15	14	13	12	11	10	9	Bit 8	High	**TOC1**
$1017	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$1018	Bit 15	14	13	12	11	10	9	Bit 8	High	**TOC2**
$1019	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$101A	Bit 15	14	13	12	11	10	9	Bit 8	High	**TOC3**
$101B	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$101C	Bit 15	14	13	12	11	10	9	Bit 8	High	**TOC4**
$101D	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$101E	Bit 15	14	13	12	11	10	9	Bit 8	High	**TOC5**
$101F	Bit 7	6	5	4	3	2	1	Bit 0	Low	

All TOCx register pairs reset to ones ($FFFF).

TCTL1 — Timer Control 1 **$1020**

	Bit 7	6	5	4	3	2	1	Bit 0
	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
RESET:	0	0	0	0	0	0	0	0

OM2–OM5 — Output Mode

OL2–OL5 — Output Level

OMx	OLx	Action Taken on Successful Compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to 0
1	1	Set OCx output line to 1

TCTL2 — Timer Control 2 **$1021**

	Bit 7	6	5	4	3	2	1	Bit 0
	—	—	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A
RESET:	0	0	0	0	0	0	0	0

Table 7 Timer Control Configuration

EDGxB	EDGxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge

TMSK1 — Timer Interrupt Mask 1 **$1022**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1I	OC2I	OC3I	OC4I	OC5I	IC1I	IC2I	IC3I
RESET:	0	0	0	0	0	0	0	0

OC1I–OC5I — Output Compare x Interrupt Enable
If the OCxI enable bit is set when the OCxF flag bit is set, a hardware interrupt sequence is requested.

IC1I–IC3I — Input Capture x Interrupt Enable
If the ICxI enable bit is set when the ICxF flag bit is set, a hardware interrupt sequence is requested.

NOTE

Bits in TMSK1 correspond bit for bit with flag bits in TFLG1. Ones in TMSK1 enable the corresponding interrupt sources.

TFLG1 — Timer Interrupt Flag 1 **$1023**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1F	OC2F	OC3F	OC4F	OC5F	IC1F	IC2F	IC3F
RESET:	0	0	0	0	0	0	0	0

Clear flags by writing a one to the corresponding bit position(s).

OC1F–OC5F — Output Compare x Flag
Set each time the counter matches output compare x value.

IC1F–IC3F — Input Capture x Flag
Set each time a selected active edge is detected on the ICx input line.

TMSK2 — Timer Interrupt Mask 2 **$1024**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

TOI — Timer Overflow Interrupt Enable
0 = TOF interrupts disabled
1 = Interrupt requested when TOF is set to one

RTII — Real-Time Interrupt Enable
0 = RTIF interrupts disabled
1 = Interrupt requested when RTIF is set to one

PAOVI — Pulse Accumulator Overflow Interrupt Enable
Refer to **9 Pulse Accumulator**.

PAII — Pulse Accumulator Input Edge Interrupt Enable
Refer to **9 Pulse Accumulator**.

NOTE

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2. Ones in TMSK2 enable the corresponding interrupt sources.

PR1 and PR0 — Timer Prescaler Select
In normal modes, PR1 and PR0 can only be written once, and the write must be within 64 cycles after reset. Refer to **Table 6** for specific timing values.

PR[1:0]	Prescaler
0 0	1
0 1	4
1 0	8
1 1	16

TFLG2 — Timer Interrupt Flag 2 **$1025**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOF	RTIF	PAOVF	PAIF	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

Clear flags by writing a one to the corresponding bit position(s).

TOF — Timer Overflow Flag
Set when TCNT changes from $FFFF to $0000.

RTIF — Real-Time (Periodic) Interrupt Flag
Set periodically. Refer to RTR[1:0] bits in PACTL register.

PAOVF — Pulse Accumulator Overflow Interrupt Flag
Refer to **9 Pulse Accumulator**.

PAIF — Pulse Accumulator Input Edge Interrupt Flag
Refer to **9 Pulse Accumulator**.

PACTL — Pulse Accumulator Control **$1026**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRA7	PAEN	PAMOD	PEDGE	0	0	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

DDRA7 — Data Direction for Port A Bit 7
Refer to **5 Parallel Input/Output**.

PAEN — Pulse Accumulator Enable
Refer to **9 Pulse Accumulator**.

PAMOD — Pulse Accumulator Mode Select
Refer to **9 Pulse Accumulator**.

PEDGE — Pulse Accumulator Edge Select
Refer to **9 Pulse Accumulator**.

RTR [1:0] — Real-Time Interrupt (RTI) Rate

Table 8 Real-Time Interrupt Rates

RTR[1:0]	Divide E By	XTAL = 4.0 MHz	XTAL = 8.0 MHz	XTAL = 12.0 MHz
0 0	2^{13}	8.19 ms	4.096 ms	2.731 ms
0 1	2^{14}	16.38 ms	8.192 ms	5.461 ms
1 0	2^{15}	32.77 ms	16.384 ms	10.923 ms
1 1	2^{16}	65.54 ms	32.768 ms	21.845 ms
	E =	1.0 MHz	2.0 MHz	3.0 MHz

9 Pulse Accumulator

The MC68HC11A8 has an 8-bit counter that can be configured to operate as a simple event counter or for gated time accumulation, depending on the PAMOD bit in the PACTL register. The pulse accumulator counter can be read or written at any time.

The port A bit 7 I/O pin can be configured as a clock in event counting mode, or as a gate signal to enable a free-running clock (E divided by 64) in gated time accumulation mode.

Table 9 Pulse Accumulator Timing

		Common XTAL Frequencies		
	Selected Crystal	**4.0 MHz**	**8.0 MHz**	**12.0 MHz**
CPU Clock	**(E)**	**1.0 MHz**	**2.0 MHz**	**3.0 MHz**
Cycle Time	**(1/E)**	**1000 ns**	**500 ns**	**333 ns**
Pulse Accumulator (in Gated Mode)				
($E/2^6$) ($E/2^{14}$)	1 count — overflow —	64.0 µs 16.384 ms	32.0 µs 8.192 ms	21.33 µs 5.461 ms

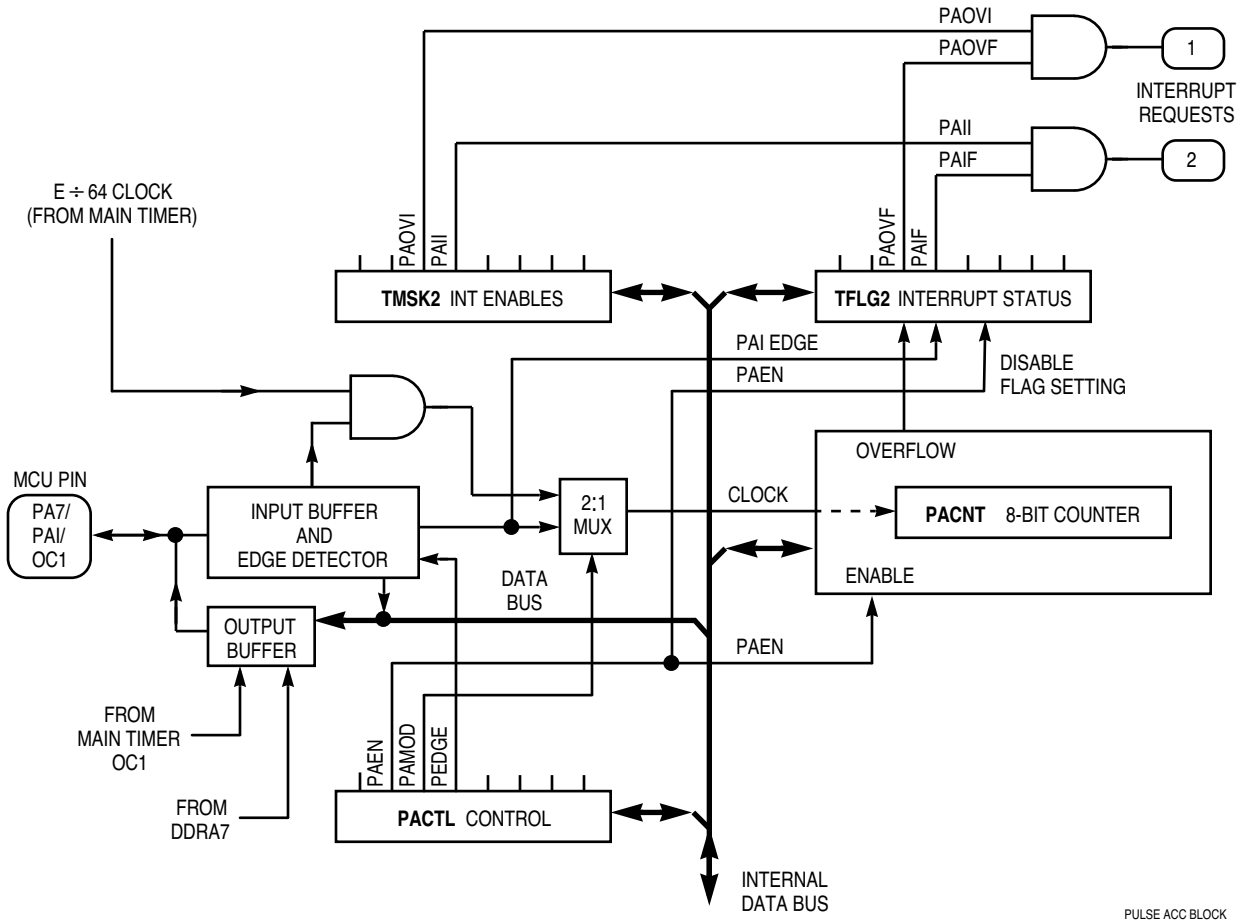


Figure 12 Pulse Accumulator System Block Diagram

TMSK2 — Timer Interrupt Mask 2 **$1024**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

TOI — Timer Overflow Interrupt Enable
Refer to **8 Main Timer**.

RTII — Real-Time Interrupt Enable
Refer to **8 Main Timer**.

PAOVI — Pulse Accumulator Overflow Interrupt Enable
0 = PAOVF interrupts disabled
1 = Interrupt requested when RTIF is set to one

PAII — Pulse Accumulator Input Edge Interrupt Enable
0 = PAIF interrupts disabled
1 = Interrupt requested when PAIF is set to one

PR1, PR0 — Timer Prescaler Select
Refer to **8 Main Timer**.

NOTE

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2. Ones in TMSK2 enable the corresponding interrupt sources.

TFLG2 — Timer Interrupt Flag 2 **$1025**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOF	RTIF	PAOVF	PAIF	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

Clear flags by writing a one to the corresponding bit position(s).

TOF — Timer Overflow Flag
Refer to **8 Main Timer**.

RTIF — Real-Time Interrupt Flag
Refer to **8 Main Timer**.

PAOVF — Pulse Accumulator Overflow Flag
Set when PACNT changes from $FF to $00.

PAIF — Pulse Accumulator Input Edge Flag
Set each time a selected active edge is detected on the PAI input line.

PACTL — Pulse Accumulator Control **$1026**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRA7	PAEN	PAMOD	PEDGE	0	0	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

DDRA7 — Data Direction for Port A Bit 7
Refer to **5 Parallel Input/Output**.

PAEN — Pulse Accumulator System Enable
0 = Pulse Accumulator disabled
1 = Pulse Accumulator enabled

PAMOD — Pulse Accumulator Mode
0 = Event counter
1 = Gated time accumulation

PEDGE — Pulse Accumulator Edge Control

PAMOD	PEDGE	Action on Clock
0	0	PAI falling edge increments the counter
0	1	PAI rising edge increments the counter
1	0	A zero on PAI inhibits counting
1	1	A one on PAI inhibits counting

RTR1 and RTR0 — Real-Time Interrupt (RTI) Rate
Refer to **8 Main Timer**.

PACNT — Pulse Accumulator Counter **$1027**

	Bit 7	6	5	4	3	2	1	Bit 0
	Bit 7	6	5	4	3	2	1	Bit 0
RESET:	0	0	0	0	0	0	0	0

Can be read and written.

10 Analog-to-Digital Converter

The A/D converter system uses an all capacitive charge redistribution technique to convert analog signals to digital values. The MC68HC11A8 A/D system is an 8-channel, 8-bit, multiplexed-input, successive-approximation converter and is accurate to ±1 least significant bit (LSB). It does not require external sample and hold circuits because of the type of charge redistribution technique used.

Dedicated lines V_{RH} and V_{RL} provide the reference supply voltage inputs. Refer to the A/D converter block diagram.

A multiplexer allows the single A/D converter to select one of 16 analog signals, as shown in the ADCTL register description.

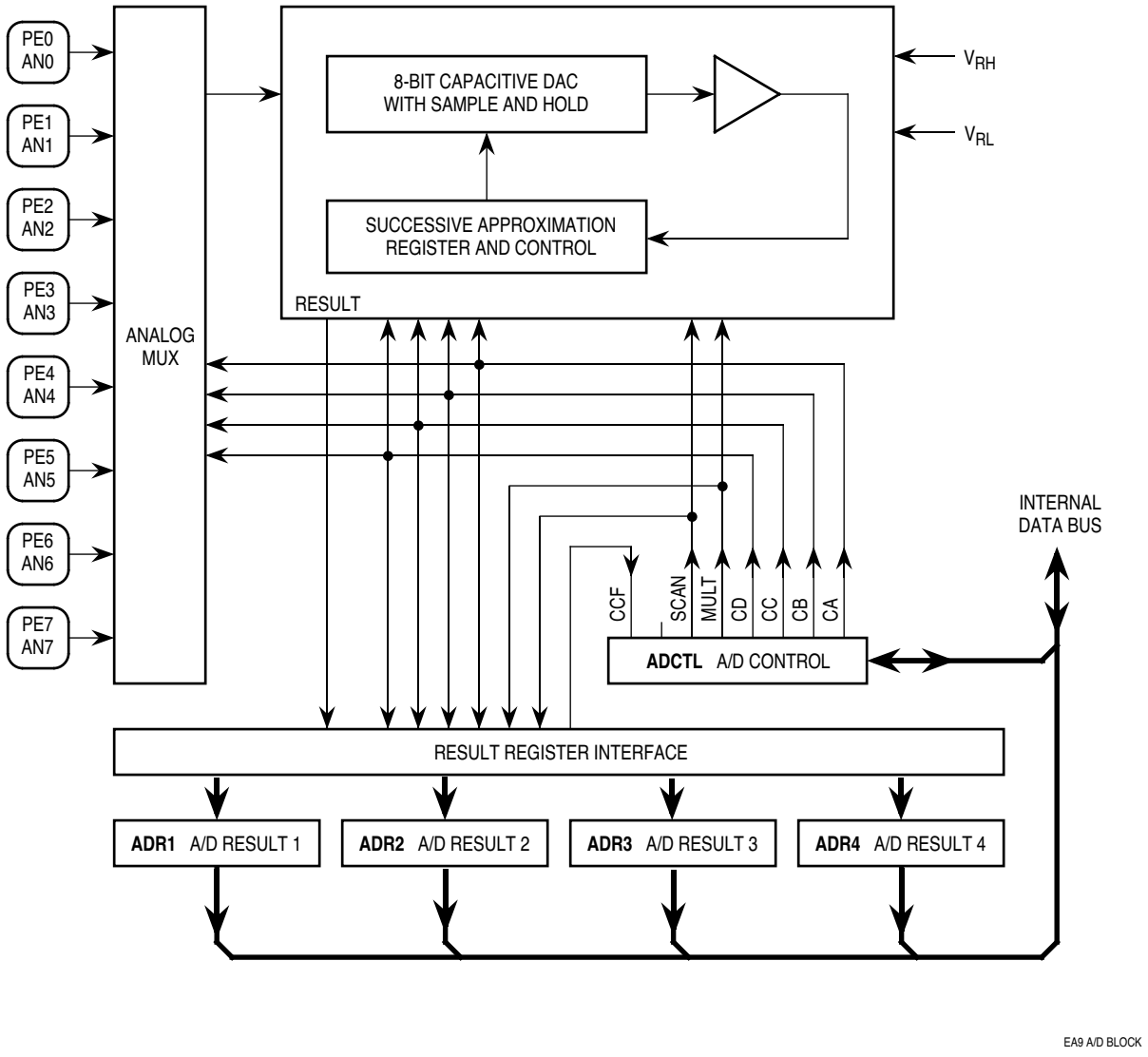


Figure 13 A/D Converter Block Diagram

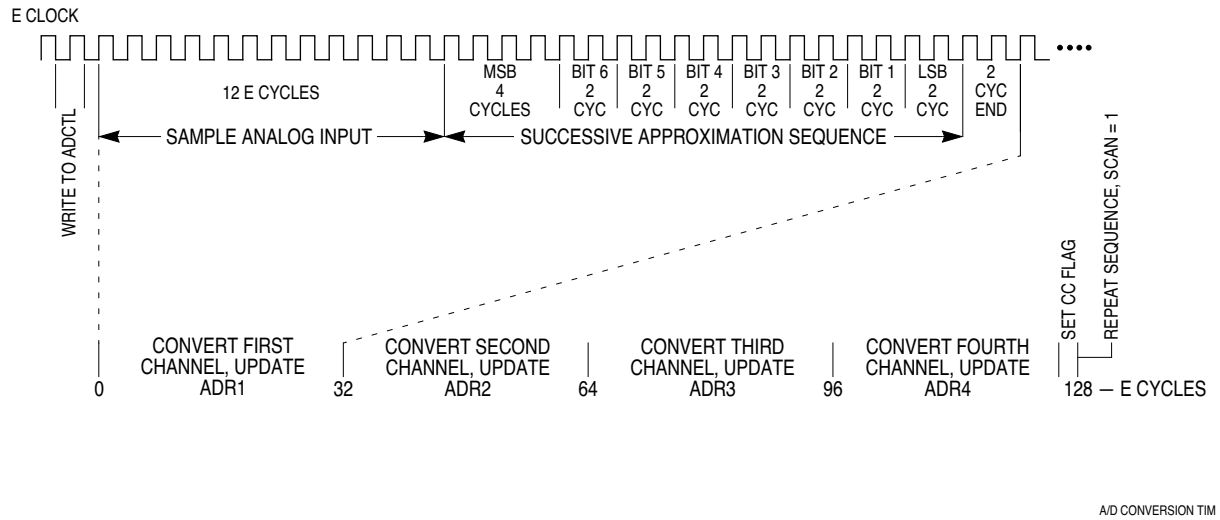


Figure 14 A/D Conversion Sequence

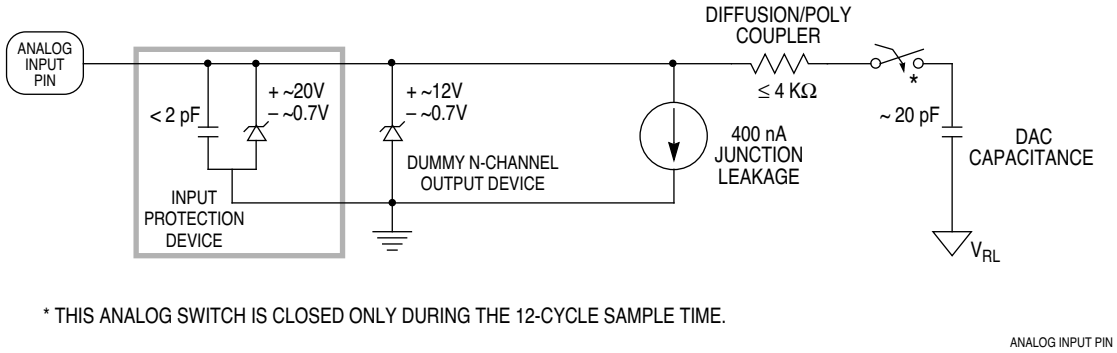


Figure 15 Electrical Model of an Analog Input Pin (Sample Mode)

ADCTL — A/D Control/Status **$1030**

	Bit 7	6	5	4	3	2	1	Bit 0
	CCF	0	SCAN	MULT	CD	CC	CB	CA
RESET:	U	0	U	U	U	U	U	U

CCF — Conversions Complete Flag
Set after an A/D conversion cycle. Cleared when ADCTL is written.

SCAN — Continuous Scan Control
0 = Do four conversions and stop
1 = Convert four channels in selected group continuously

MULT — Multiple Channel/Single Channel Control
0 = Convert single channel selected
1 = Convert four channels in selected group

CD–CA — Channel Select D through A

Table 10 A/D Converter Channel Assignments

Channel Select Control Bits				Channel Signal	Result in ADRx if MULT = 1
CD	CC	CB	CA		
0	0	0	0	AN0	ADR1
0	0	0	1	AN1	ADR2
0	0	1	0	AN2	ADR3
0	0	1	1	AN3	ADR4
0	1	0	0	AN4*	ADR1
0	1	0	1	AN5*	ADR2
0	1	1	0	AN6*	ADR3
0	1	1	1	AN7*	ADR4
1	0	X	X	Reserved	ADR1–ADR4
1	1	0	0	V_{RH}**	ADR1
1	1	0	1	V_{RL}**	ADR2
1	1	1	0	$(V_{RH})/2$**	ADR3
1	1	1	1	Reserved**	ADR4

* Not available in 48-pin package
**Used for factory testing

ADR1–ADR4 — A/D Results **$1031–$1034**

	Bit 7	6	5	4	3	2	1	Bit 0	
$1031	Bit 7	6	5	4	3	2	1	Bit 0	ADR1
$1032	Bit 7	6	5	4	3	2	1	Bit 0	ADR2
$1033	Bit 7	6	5	4	3	2	1	Bit 0	ADR3
$1034	Bit 7	6	5	4	3	2	1	Bit 0	ADR4

Table 11 Analog Input to 8-Bit Result Translation Table

	Bit 7	6	5	4	3	2	1	Bit 0
% (1)	50%	25%	12.5%	6.25%	3.12%	1.56%	0.78%	0.39%
Volts (2)	2.500	1.250	0.625	0.3125	0.1562	0.0781	0.0391	0.0195

(1) % of V_{RH}–V_{RL} (2) V_{RL} = 0.0 V; V_{RH} = 5.0 V

OPTION — System Configuration Options **$1039**

	Bit 7	6	5	4	3	2	1	Bit 0
	ADPU	CSEL	IRQE*	DLY*	CME	0	CR1*	CR0*
RESET:	0	0	0	1	0	0	0	0

*Can be written only once in first 64 cycles out of reset in normal modes, or any time in special modes.

ADPU — A/D Power Up
0 = A/D Converter powered down
1 = A/D Converter powered up

CSEL — Clock Select
0 = A/D and EEPROM use system E clock
1 = A/D and EEPROM use internal RC clock

IRQE — $\overline{\text{IRQ}}$ Select Edge Sensitive Only
Refer to **3 Resets and Interrupts**.

DLY — Enable Oscillator Start-Up Delay on Exit from STOP
Refer to **3 Resets and Interrupts**.

CME — Clock Monitor Enable
Refer to **3 Resets and Interrupts**.

CR1, CR0 — COP Timer Rate Select
Refer to **3 Resets and Interrupts**.

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