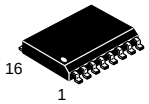
MC145532

ADPCM Transcoder

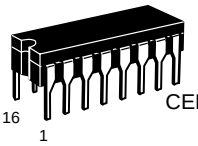
Conforms to G.721–1988 and T1.301–1987

The MC145532 Adaptive Differential Pulse Code Modulation (ADPCM) Transcoder provides a low–cost, full–duplex, single–channel transcoder to (from) a 64 kbps PCM channel from (to) either a 16 kbps, 24 kbps, 32 kbps, or 64 kbps channel.

- Complies with CCITT Recommendation G.721–1988
- Complies with the American National Standard (T1.301–1987)
- Full–Duplex, Single–Channel Operation
- Mu–Law or A–Law Coding is Pin Selectable
- Synchronous or Asynchronous Operation
- Easily Interfaces with Any Member of Motorola's PCM Codec–Filter Mono–Circuit Family or Other Industry Standard Codec
- Serial PCM and ADPCM Data Transfer Rate from 64 kbps to 5.12 Mbps
- Power–Down Capability for Low Current Consumption
- The Reset State, an Option Specified in the Standards, is Automatically Initiated When the RESET Pin is Released
- Simple Time Slot Assignment Timing for Transcoder Applications
- Single 5 V Power Supply
- 16–Pin Package
- The MC145536EVK is the Evaluation Platform for the MC145532 and Also Includes the MC145480 5 V PCM Codec–Filter



DW SUFFIX
SOG PACKAGE
CASE 751G

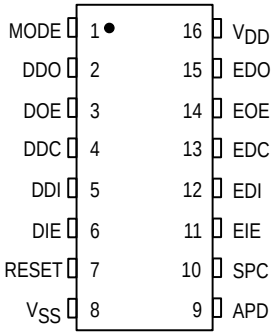


L SUFFIX
CERAMIC PACKAGE
CASE 620

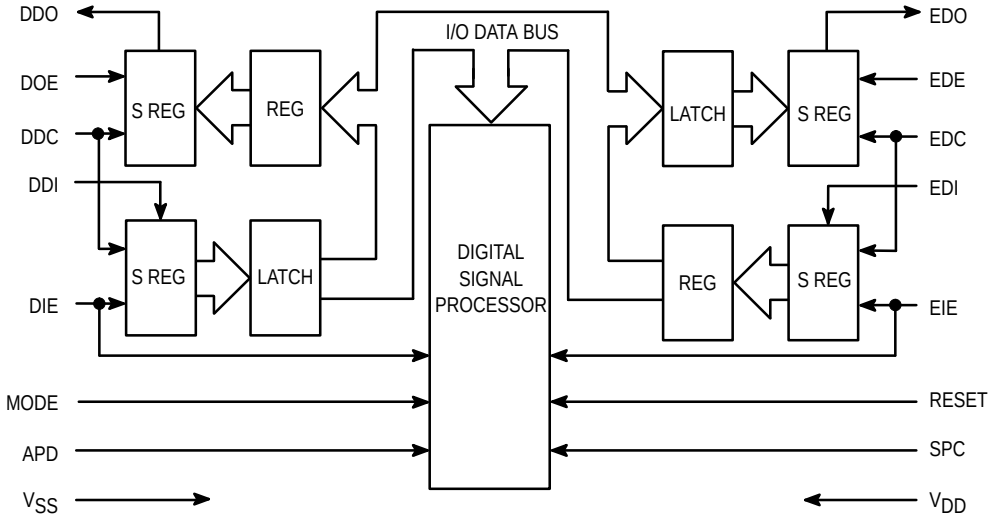
ORDERING INFORMATION

MC145532DW	SOG Package
MC145532L	Ceramic Package

PIN ASSIGNMENT



BLOCK DIAGRAM



REV 1
9/95 (Replaces NP470)

DEVICE DESCRIPTION

An Adaptive Differential PCM (ADPCM) transcoder is used to reduce the data rate required to transmit a PCM encoded voice signal while maintaining the voice fidelity and intelligibility of the PCM signal.

The transcoder is used on 64 kbps data streams which represent either voice or voice band data signals that have been digitized by a codec (e.g., MC145557). The transcoder uses a filter to attempt to predict the next PCM input value based on previous PCM input values. The error between the predicted and the true PCM input value is the information that is sent to the other end of the line. Hence the word differential, since the ADPCM data stream is the difference between the true PCM input value and the predicted value. The term “adaptive” applies to the filter that is performing the prediction. It is adaptive in that its transfer function changes based on the PCM input data. That is, it adapts to the statistics of the signals presented to it.

PIN DESCRIPTIONS

ENCODER INPUT

EDI
Encoder Data Input (Pin 12)

PCM data to be encoded are applied to this input pin which operates synchronously with EDC and EIE to enter the data in a serial format.

EDC
Encoder Data Clock (Pin 13)

Data applied to EDI are latched into the transcoder on a falling edge of EDC and data are output from EDO on a rising edge of this input pin. The frequency of EDC may be as low as 64 kHz or as high as 5.12 MHz.

EIE
Encoder Input Enable (Pin 11)

The beginning of a new PCM word is indicated to the transcoder by a rising edge applied to this input. The frequency of EIE may not exceed 8 kHz.

ENCODER OUTPUT

EDO
Encoder Data Output (Pin 15)

ADPCM data are available in a serial format from this output, which operates synchronously with EDC and EOE. EDO is a three–state output which remains in a high–impedance state, except when presenting data.

EOE
Encoder Output Enable (Pin 14)

Each ADPCM word is requested by a rising edge on this input, which causes the EDO pin to provide the data when clocked by EDC. One EOE must occur for each EIE.

DECODER INPUT

DDI
Decoder Data Input (Pin 5)

ADPCM data to be decoded are applied to this input pin, which operates in conjunction with DDC and DIE to enter the data in a serial format.

DDC
Decoder Data Clock (Pin 4)

Data applied to DDI are latched into the transcoder on the falling edge of DDC and data are output from DDO on the rising edge of DDC. The frequency of DDC may be as low as 64 kHz or as high as 5.12 MHz.

DIE
Decoder Input Enable (Pin 6)

The beginning of a new ADPCM word is indicated by a rising edge applied to this input. Data are serially clocked into DDI on the subsequent falling edges of DDC following the DIE rising edge. The frequency of DIE may not exceed 8 kHz.

DECODER OUTPUT

DDO
Decoder Data Output (Pin 2)

PCM data are available in a serial format from this output, which operates in conjunction with DDC and DOE. DDO is a three–state output that remains at a high–impedance state except when presenting data.

DOE
Decoder Output Enable (Pin 3)

Each ADPCM word is requested by a rising edge on this input which causes the DDO pin to provide the data when clocked by DDC. One DOE must occur for each DIE.

CONTEXT

MODE
Mode Select (Pin 1)

A logic 0 applied to this input makes the transcoder compatible with Mu–255 companding and D3 data format. A logic 1 applied to this pin makes the transcoder compatible with A–Law companding with even bit inversion data format.

SPC
Signal Processor Clock (Pin 10)

This input is typically clocked with a 20.48 MHz clock signal which is used as the digital signal processor master clock. This pin has a CMOS compatible input.

RESET
Reset (Pin 7)

A logic 0 applied to this input forces the transcoder into a low power dissipation mode. A rising edge on this pin causes power to be restored and the optional transcoder RESET state (specified in the standards) to be forced. Valid data is available at the output pins four input enables after a rising edge on this pin. This pin has a CMOS compatible input.

APD
Absolute Power Down (Pin 9)

A logic 1 applied to this input forces the transcoder into a power saving mode. This pin has a CMOS compatible input.

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 16)

The most positive power supply pin, normally 5 V.

V_{SS}
Negative Power Supply (Pin 8)

The most negative power supply pin, normally 0 V.

FUNCTIONAL DESCRIPTION

ENCODING/DECODING RATES

The MC145532 allows for the encoding and decoding of data at one of four rates on a sample–by–sample basis. Each data sample that is provided to the part is accompanied by an indication of the rate at which it is to be encoded or decoded. The width of the enable pulse determines the encoding/decoding rate chosen for each sample.

The 64 kbps rate allows for PCM data to be passed directly through the part. The 32 kbps rate is either the G.721–1988 or the T1.301–1987 standard, depending on the state of the mode pin. The 24 kbps encoding rate is compliant with CCITT G.723–1988 and G.726. The 16 kbps rate is a modified quantizer from the 32 kbps technique and is not a standard.

TIMING

Figures 1 through 8 show the timing of the input and output pins. The MC145532 determines the mode of the timing signals, either short or long frame, for each enable, independent of the mode of any previous enables. A transition from short frame to long frame mode or vice versa will cause at least one frame of data to be destroyed. Each of the four sets of I/O pins determines its mode independent of the other sets. Thus the encoder input could be operating with long frame timing and the output could be operating with short frame timing. Note that the short frame timing on the input enables can only be used with the 32 kbps transcoding rate. The number of data clock falling edges enclosed by the input enable line (EIE or DIE) determines both the short frame or long frame mode and the transcoding rate. The mode of the input or output is determined each frame. In all modes, the data is captured by the MC145532 on the falling edge of either EDC or DDC.

ENCODER INPUT — SHORT FRAME

Figure 1 shows the timing of the encoder data clock (EDC), the encoder input enable (EIE), and the encoder data input (EDI) pins in short frame operation.

The determination of short frame mode is made by the MC145532 based on one falling EDC edge while EIE is high. Note that only a 32 kbps encoding rate can be specified when using short frame mode on the encoder input.

ENCODER INPUT — LONG FRAME

Figure 2 shows the clock, enable, and data signals for the encoder input in long frame mode. In this mode, the data is captured by the MC145532 on the falling edge of EDC.

The determination of the encoding rate is made based on the number of falling EDC edges seen by the MC145532 while EIE is high. Four edges implies a 32 kbps encoding rate, three edges implies a 24 kbps encoding rate, two edges implies a 16 kbps rate, and from five to eight inclusive imply a 64 kbps rate. The encoding rate may be changed on a frame–by–frame basis. The encoded word is available at EDO (via EOE and EDC) from 250 μs to 375 μs after it is requested.

ENCODER OUTPUT — SHORT FRAME

Figure 3 shows the timing of the encoder output in short frame mode. The length of the LSB is always one half of an EDC cycle.

The EDO will provide the correct number of bits for the encoding rate that was selected for this frame of data on the encoder input pins. The data is loaded into the MC145532 during one frame, encoded on the next frame, and read during the third frame.

ENCODER OUTPUT — LONG FRAME

Figure 4 shows the timing of the encoder output in long frame mode. The enable must be wider than two falling edges of the EDC to be in long frame mode. If the enable falls before the correct number of bits have been presented to the output (EDO), the transcoder will complete the presentation of the bits to the output with the LSB being one half of an EDC period wide. If the enable falls after the one half EDC period of the LSB, then the LSB will be extended up to the full EDC clock period and the subsequent data will be a recirculation of the previous data, which repeats until the enable pin falls. This is shown on the second enable for the 16 kbps encoding rate example in Figure 4.

DECODER INPUT — SHORT FRAME

Figure 5 shows the timing of the decoder data clock, the decoder input enable, and the decoder data input pins in short frame operation. Note that in this mode only a 32 kbps decoding rate can be selected.

DECODER INPUT — LONG FRAME

Figure 6 shows the clock, enable, and data signals for the decoder input in long frame mode.

The determination of the decoding rate is made based on the number of falling DDC edges seen by the MC145532 while DIE is high. Four edges implies a 32 kbps decoding rate, three edges implies a 24 kbps decoding rate, two edges implies a 16 kbps rate, and from five to eight edges inclusive imply a 64 kbps rate. The decoding rate may be changed on a frame–by–frame basis.

DECODER OUTPUT — SHORT FRAME

Figure 7 shows the timing of the decoder output in short frame mode.

The DDO will provide the 8–bit PCM word for the decoding rate that was selected for this frame of data on the decoder input pins. The data is loaded into the MC145532 during one frame, decoded on the next frame, and read during the third frame.

DECODER OUTPUT — LONG FRAME

Figure 8 shows the timing of the decoder output in long frame mode. Note that at least eight bits are presented to the output, provided that at least two falling edges of DDC are seen while DOE is high. The enable can be used to extend the LSB to a full DDC period and/or cause the eight bits of data to be recirculated to the output pin until the enable falls.

STANDARDS INFORMATION

The following standards apply to the MC145532:

T1.301–1987 — 32 kbps ADPCM
T1.303–1988 — 24 kbps ADPCM
CCITT G.721–1988, G.723–1988, and G.726 — 32 kbps and 24 kbps

CCITT, ITU–T, TIA, and EIA documents may be obtained by contacting Global Engineering Documents in the USA at (800) 854–7179, or internationally at (303) 397–7956.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 7.0	V
Voltage, Any Pin to V_{SS}	V	– 0.5 to V_{DD} + 0.5	V
DC Current, Any Pin	I_{in}	± 10	mA
Operating Temperature	T_A	– 40 to + 85	°C
Storage Temperature	T_{stg}	– 85 to + 150	°C

This device contains circuitry to protect against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS (T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
DC Supply Voltage	V_{DD}	4.50	5.50	V
Power Dissipation	P_D	—	0.28	W

DIGITAL CHARACTERISTICS (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter		Symbol	Min	Max	Unit
High Level Input Voltage	Mode, DOE, DDC, DDI, DIE, EIE, EDI, EDC, EOE	V_{IH}	2.0	—	V
Low Level Input Voltage	Mode, DOE, DDC, DDI, DIE, EIE, EDI, EDC, EOE	V_{IL}	—	0.8	V
High Level Input Voltage	RESET, APD, SPC	V_{IH}	0.7 V_{DD}	—	V
Low Level Input Voltage	RESET, APD, SPC	V_{IL}	—	0.3 V_{DD}	V
Input Current		I_{in}	—	± 1.0	µA
Input Capacitance		C_{in}	—	10	pF
High Level Output Voltage (I_{OH} = – 2.0 mA)	DDO, EDO	V_{OH}	4.6	—	V
Low Level Output Voltage (I_{OL} = 2.0 MA)	DDO, EDO	V_{OL}	—	0.4	V
Output Leakage Current (V_{DD} = 5.5 V)	DDO, EDO	I_{lkg}	—	± 5.0	µA

SWITCHING CHARACTERISTICS (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Min	Max	Unit
SPC Frequency	19.990	23	MHz
SPC Duty Cycle	45	55	%

ENCODER INPUT — SHORT FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Setup Time	$t_{su(EIE)L}$	15	—	ns
Enable Low Hold Time	$t_{h(EIE)H}$	30	—	ns
Enable Valid Time	$t_{V(EIE)}$	15	—	ns
Enable Hold Time	$t_{h(EIE)}$	15	—	ns
Data Valid Time	$t_{v(EDI)}$	15	—	ns
Data Hold Time	$t_{h(EDI)}$	15	—	ns

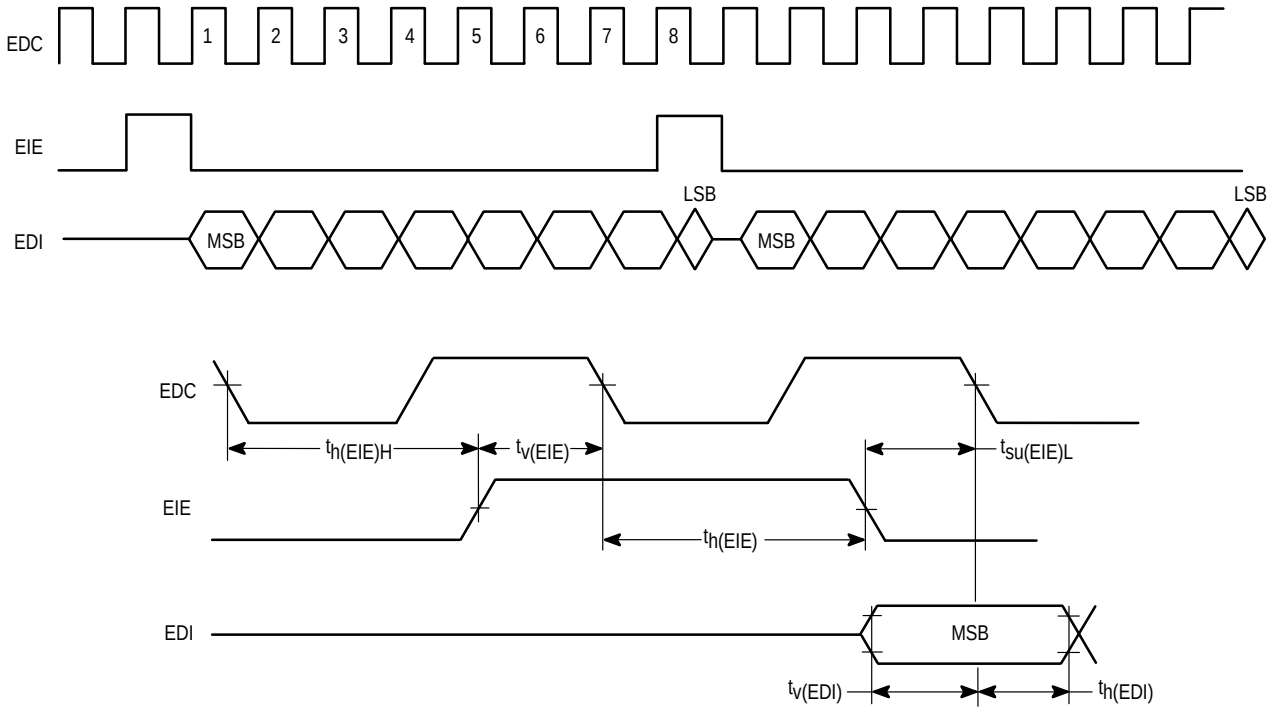


Figure 1. Encoder Input Timing — Short Frame

ENCODER INPUT — LONG FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(EIE)L}$	30	—	ns
Enable Valid Time	$t_{v(EIE)}$	15	—	ns
Data Valid Time	$t_{v(EDI)}$	15	—	ns
Data Hold Time	$t_{h(EDI)}$	15	—	ns

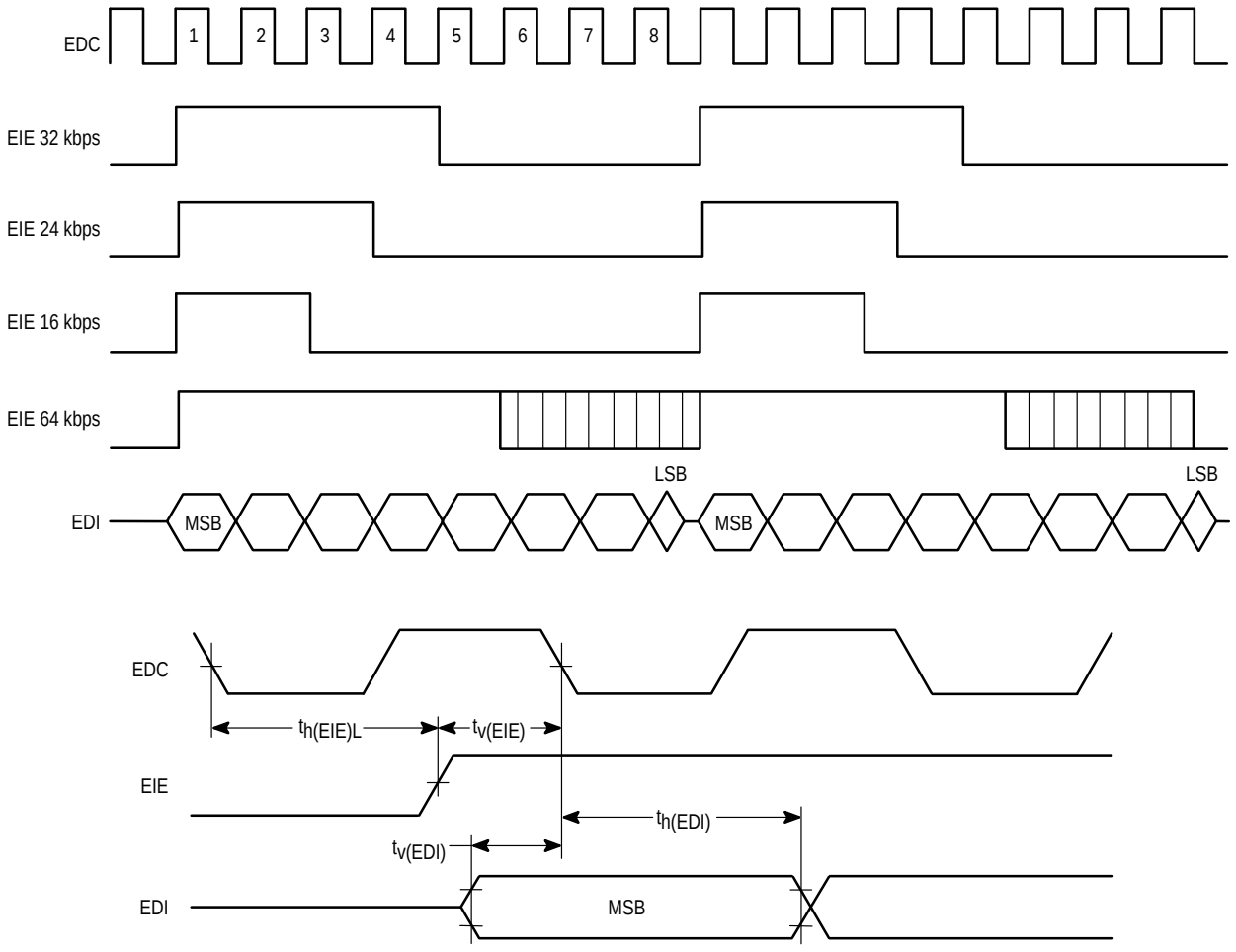


Figure 2. Encoder Input Timing — Long Frame

ENCODER OUTPUT — SHORT FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(EOE)L}$	30	—	ns
Enable Valid Time	$t_{v(EOE)}$	15	—	ns
Enable Hold Time	$t_{h(EOE)}$	15	—	ns
Data Valid Time	$t_{v(EDO)}$	—	40	ns
Data Three–State Time (with 150 pF Load)	$t_{z(EDO)}$	1	30	ns

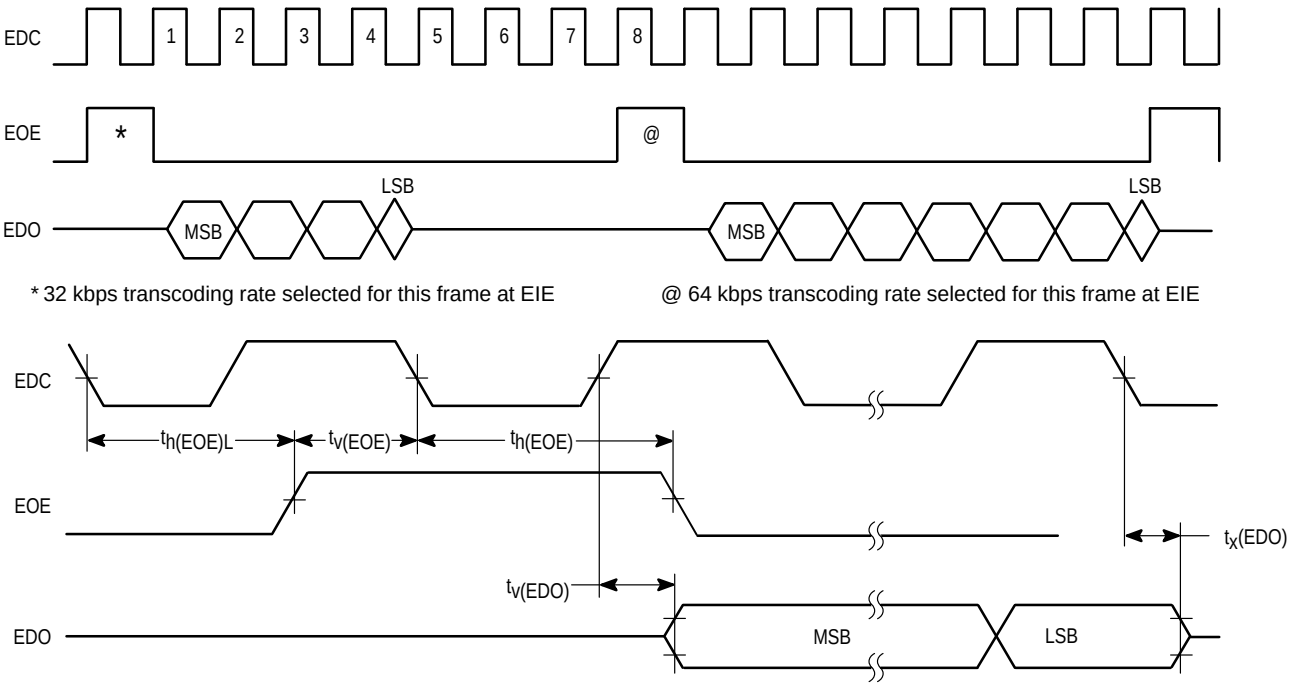
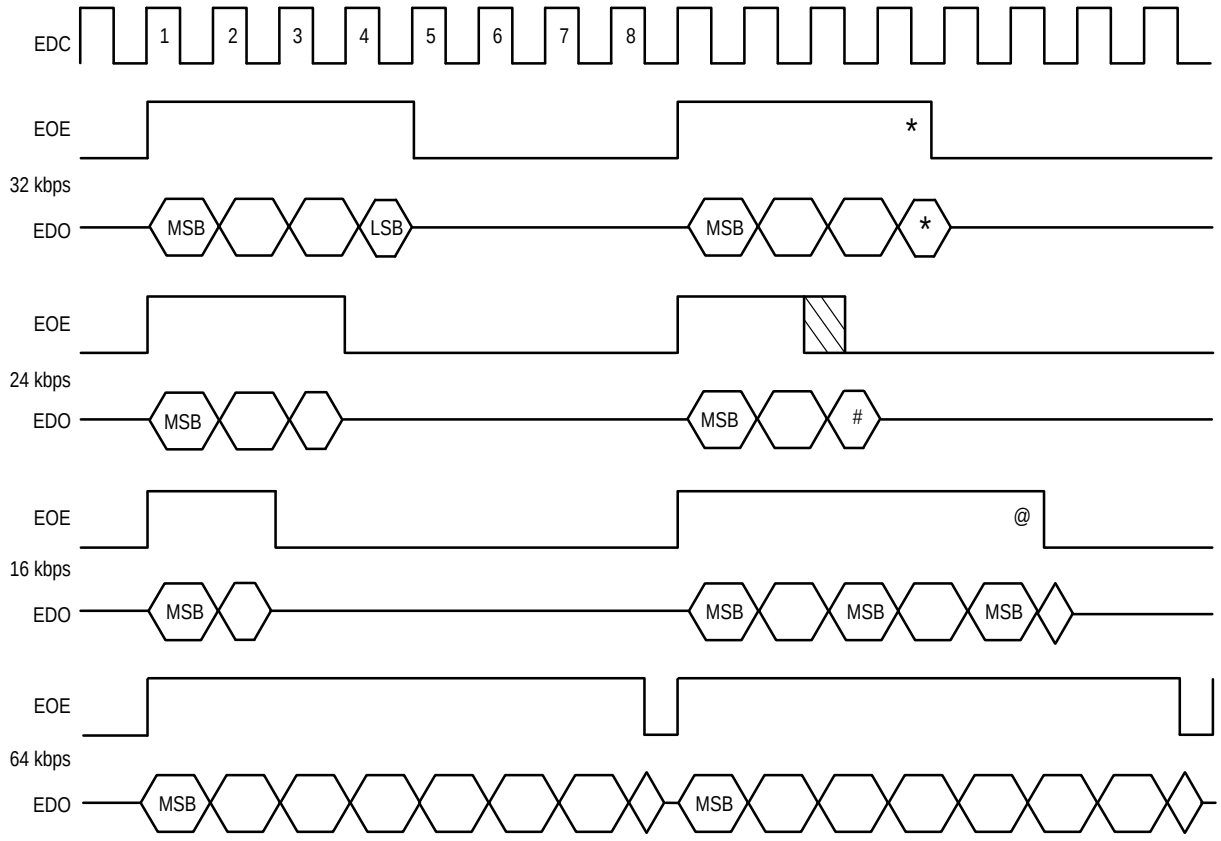


Figure 3. Encoder Output Timing — Short Frame

ENCODER OUTPUT — LONG FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(EOE)L}$	30	—	ns
Enable Valid Time	$t_{v(EOE)}$	15	—	ns
Enable to Data Time (Whichever Edge Occurs Last)	$t_{EOE–EDO}$	—	40	ns
Clock to Data Time (Whichever Edge Occurs Last)	$t_{EDC–EDO}$	—	45	ns



* EDO Driver is controlled by EOE
\# EDO completes the presentation of data
@ Data recirculates

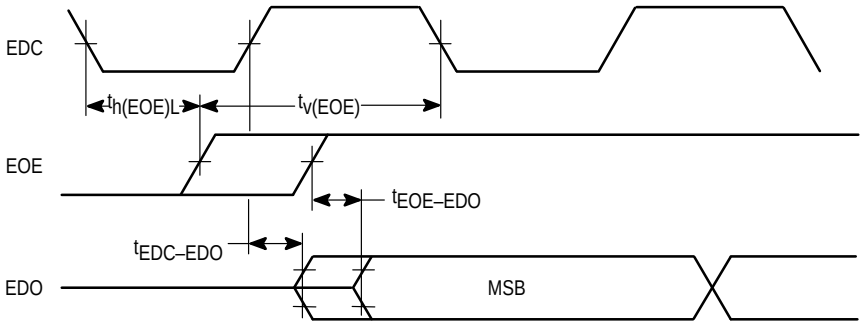


Figure 4. Encoder Output Timing — Long Frame

DECODER INPUT — SHORT FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Setup Time to Falling DDC	$t_{su(DIE)L}$	15	—	ns
Enable Low Hold Time from Falling DDC	$t_{h(DIE)H}$	30	—	ns
Enable Valid Time to Falling DDC	$t_{v(DIE)}$	15	—	ns
Enable Hold Time from Falling DDC	$t_{h(DIE)}$	15	—	ns
Data Valid Time Before Falling DDC	$t_{v(DDI)}$	15	—	ns
Data Hold Time from Falling DDC	$t_{h(DDI)}$	15	—	ns

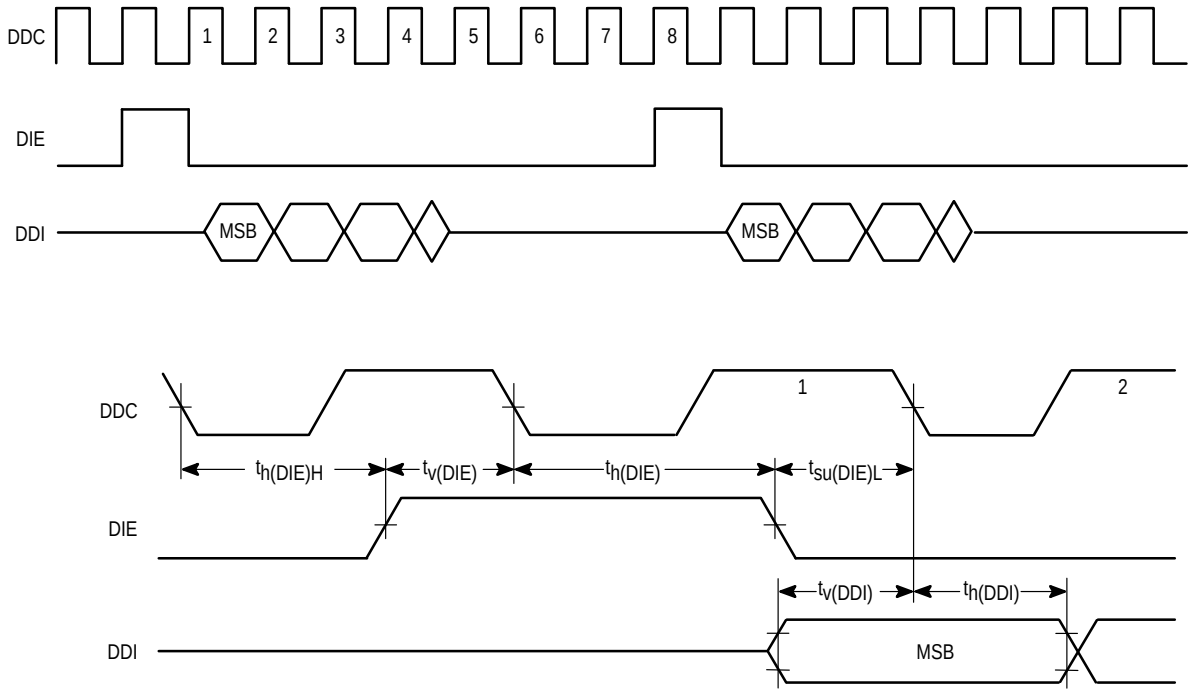


Figure 5. Decoder Input Timing — Short Frame

DECODER INPUT — LONG FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Hold Time from Falling DDC	$t_{h(DIE)}$	30	—	ns
Enable Valid Time to Falling DDC	$t_{v(DIE)}$	15	—	ns
Data Valid Time to Falling DDC	$t_{v(DDI)}$	15	—	ns
Data Hold Time from Falling DDC	$t_{h(DDI)}$	15	—	ns

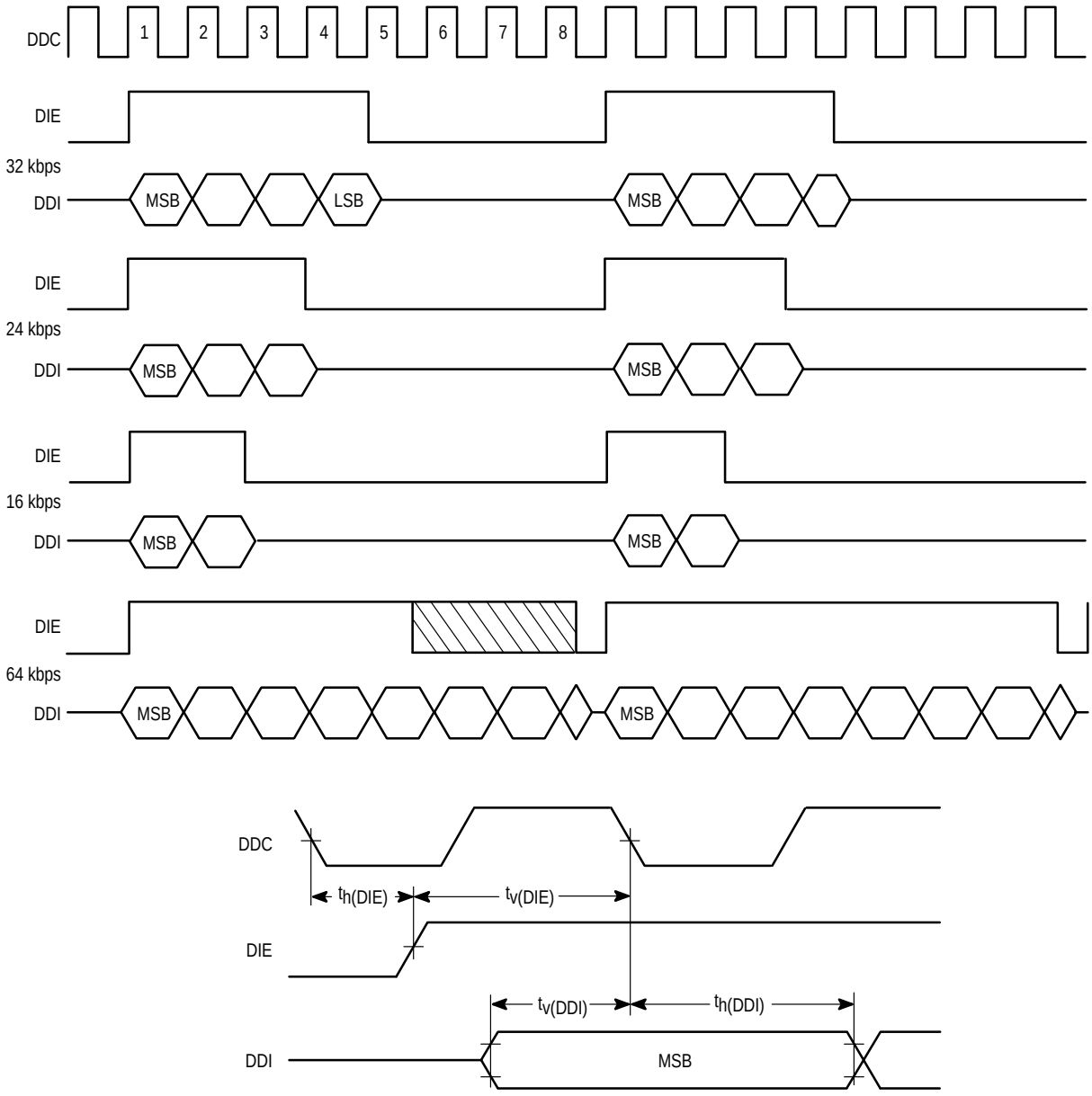


Figure 6. Decoder Input Timing — Long Frame

DECODER OUTPUT — SHORT FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(DOE)L}$	30	—	ns
Enable Valid Time	$t_{v(DOE)}$	15	—	ns
Enable Hold Time	$t_{h(DOE)}$	15	—	ns
Rising Edge of DDC to Valid DDO	$t_{v(DDO)}$	—	40	ns
Delay Time from 8th DDC Low to DDO Output Disabled	$t_{z(DDO)}$	—	30	ns

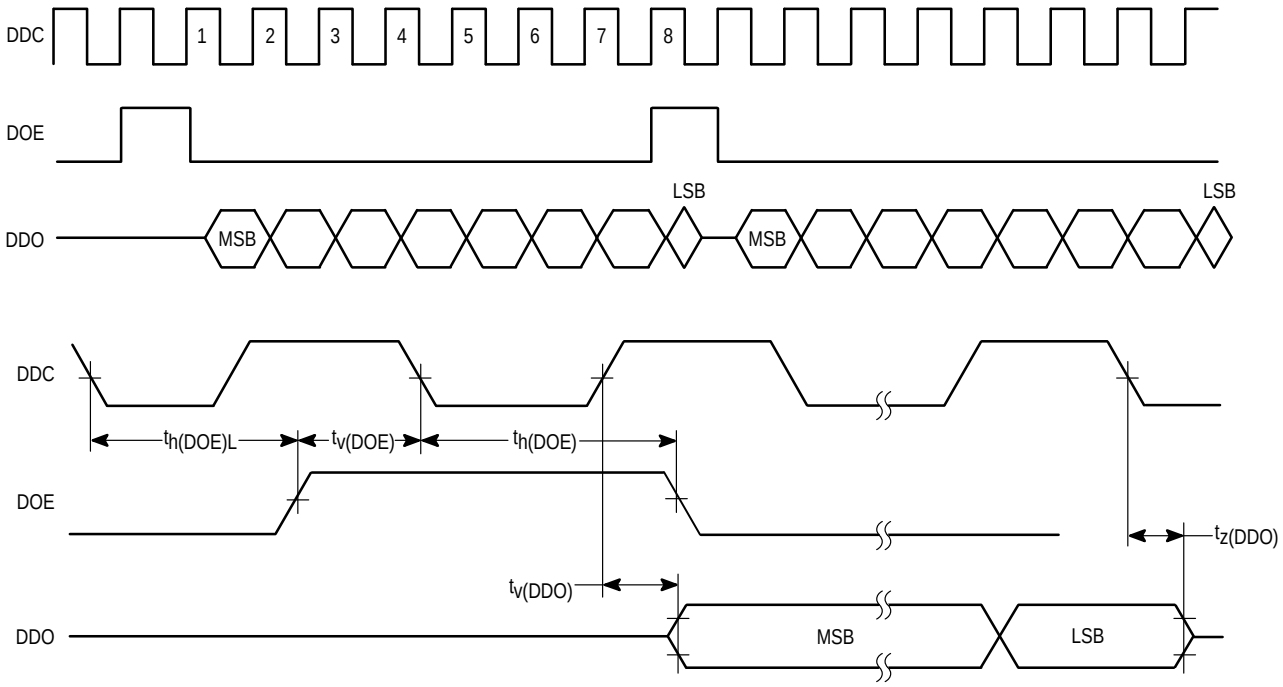


Figure 7. Decoder Output Timing — Short Frame

DECODER OUTPUT — LONG FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(DOE)L}$	30	—	ns
Enable Valid Time	$t_{v(DOE)}$	15	—	ns
Rising Edge of DDE to Valid DDO (When DDC is High)	$t_{DOE–DDO}$	—	40	ns
Rising Edge of DDC to Valid DDO (When DOE is High)	$t_{DDC–DDO}$	—	45	ns
Delay Time from 8th DDC Low or DOE Low to DDO Output Disabled	$t_{z(DDO)}$	0	30	ns

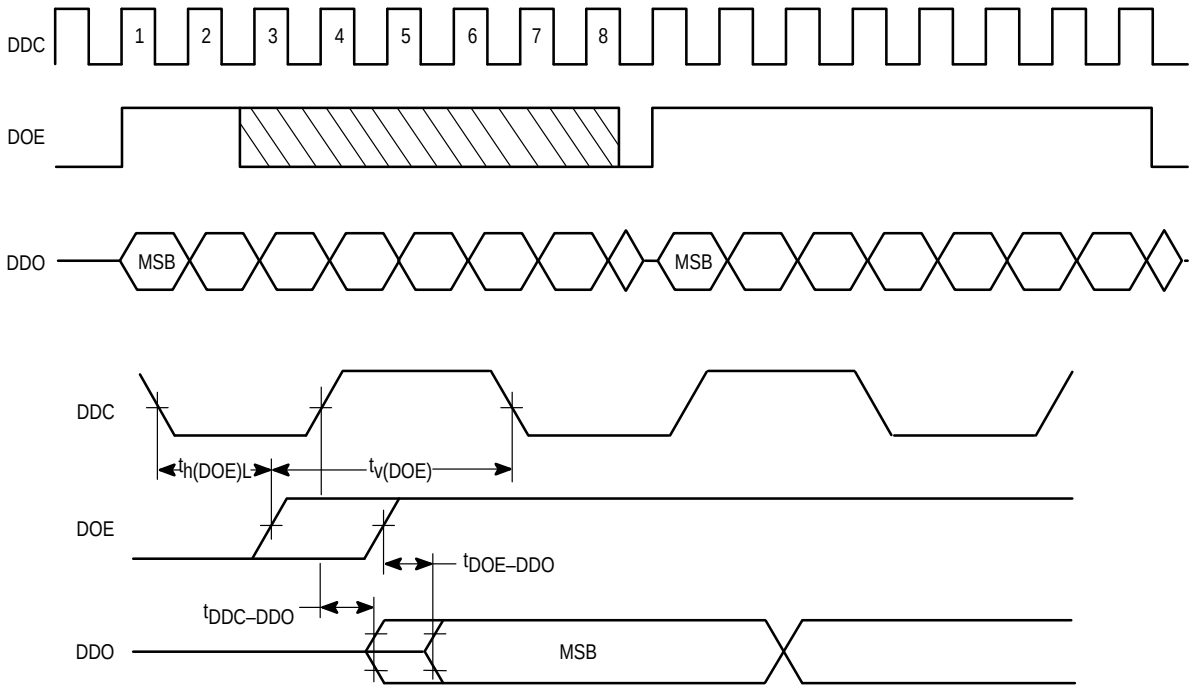


Figure 8. Decoder Output Timing — Long Frame

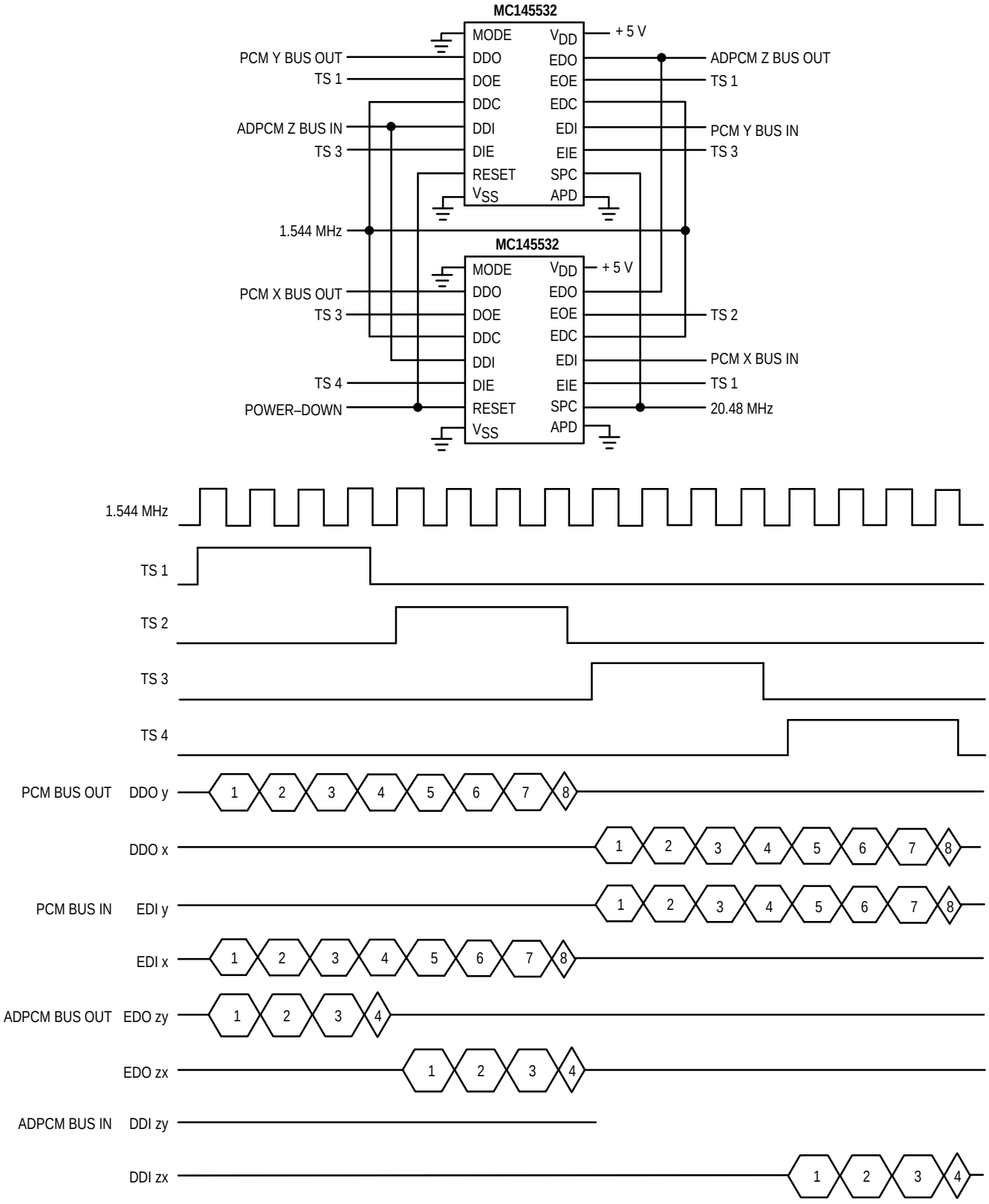


Figure 9. ADPCM Transcoder Application

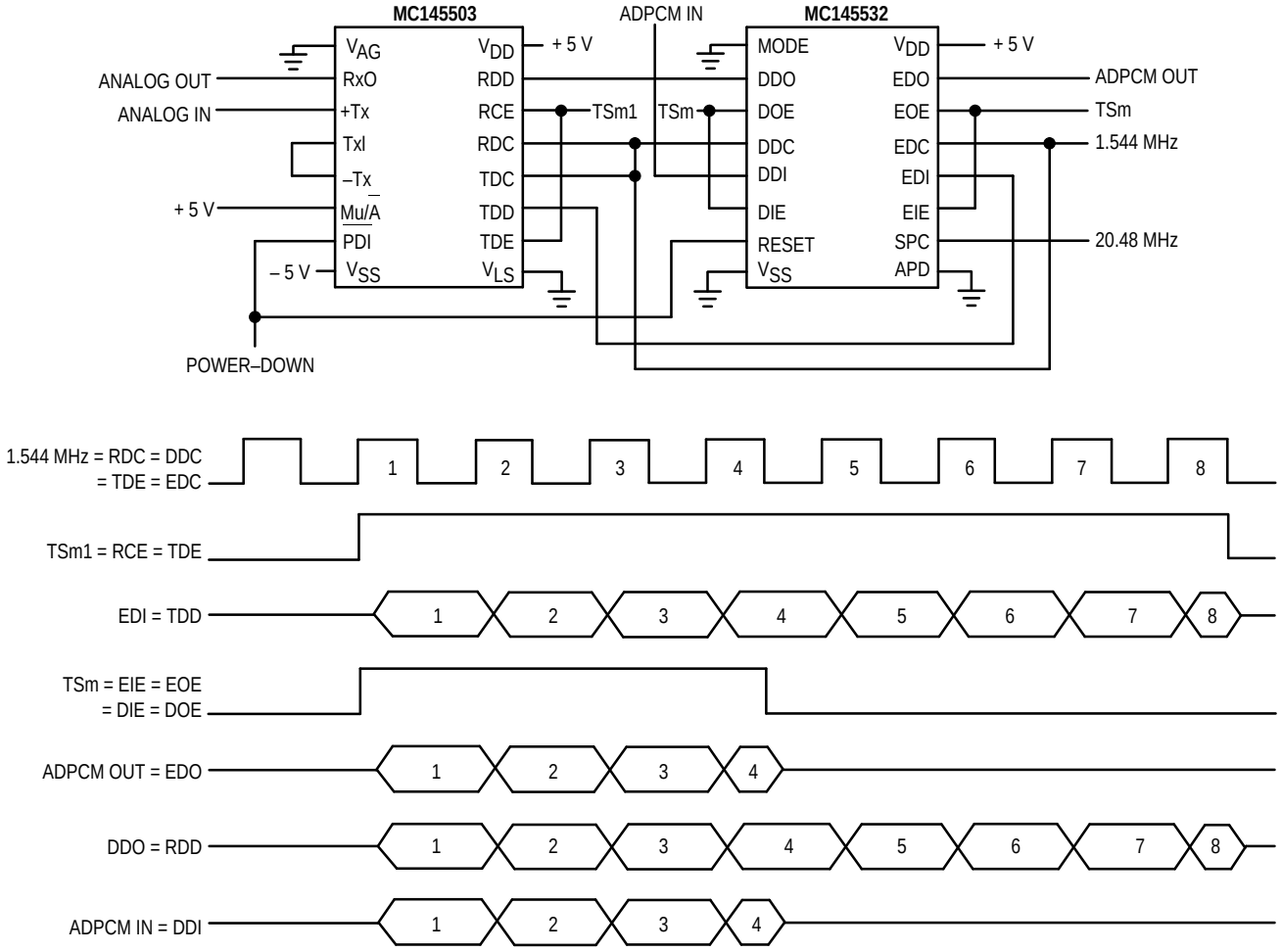


Figure 10. ADPCM Transcoder/Codec Application

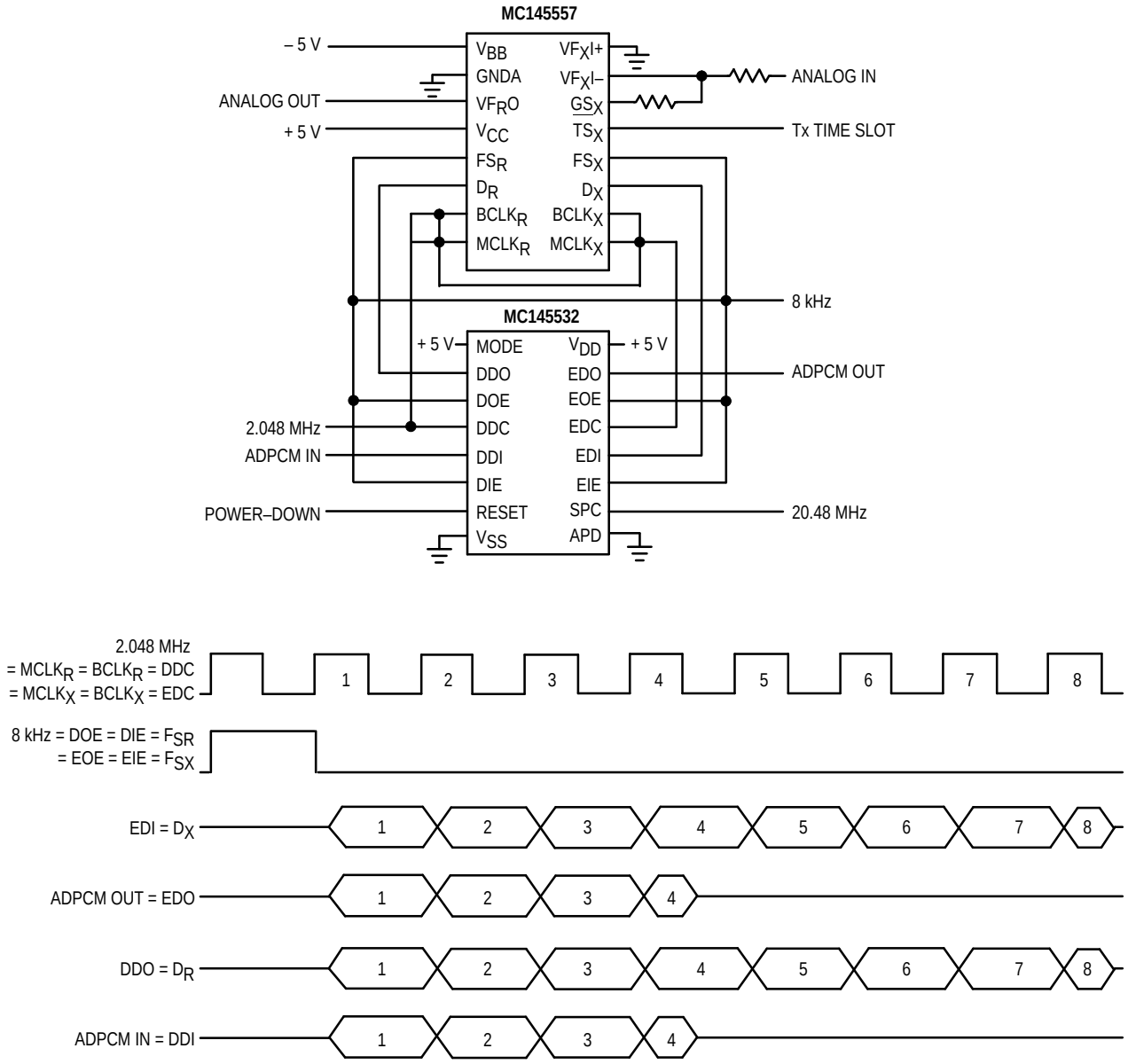
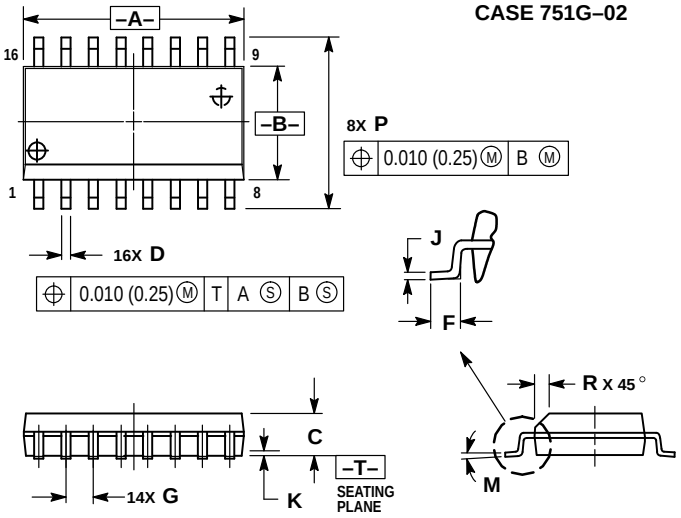


Figure 11. ADPCM Transcoder/Codec Application (A–Law)

PACKAGE DIMENSIONS

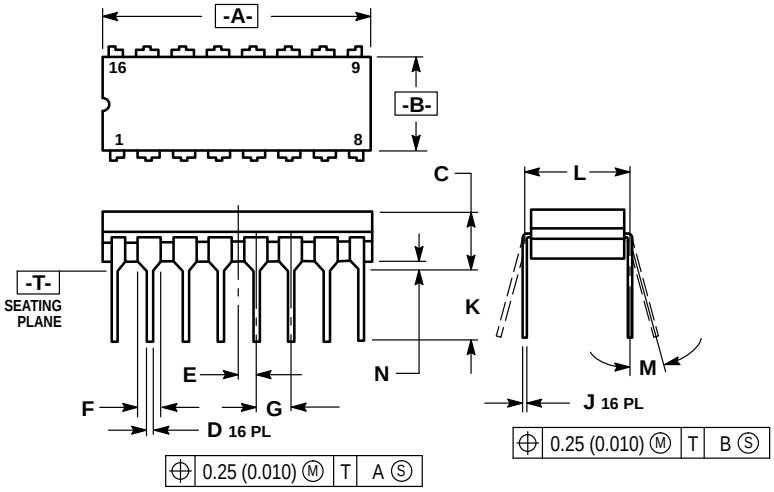
DW SUFFIX
SOG PACKAGE
CASE 751G–02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

L SUFFIX
CERAMIC PACKAGE
CASE 620–09



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.770	19.05	19.55
B	0.240	0.290	6.10	7.36
C	—	0.165	—	4.19
D	0.015	0.021	0.39	0.53
E	0.050 BSC		1.27 BSC	
F	0.055	0.070	1.40	1.77
G	0.100 BSC		2.54 BSC	
J	0.009	0.011	0.23	0.27
K	—	0.200	—	5.08
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.015	0.035	0.39	0.88

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