

SDRAM 256Mb E-die (x4, x8, x16)

CMOS SDRAM

256Mb E-die SDRAM Specification
54 TSOP-II with Pb-Free
(RoHS compliant)

Revision 1.3

August 2004

* Samsung Electronics reserves the right to change products or specification without notice.



Rev. 1.3 August 2004

Revision History

Revision 1.0 (May. 2003)

- First generation for Pb_free products

Revision 1.1 (August. 2003)

- Corrected typo in Page #8, 9

Revision 1.2 (May. 2004)

- Added Note 5. sentence of tRDL parameter

Revision 1.3 (August. 2004)

- Corrected typo.

16M x 4Bit x 4 Banks / 8M x 8Bit x 4 Banks / 4M x 16Bit x 4 Banks SDRAM**FEATURES**

- JEDEC standard 3.3V power supply
- LVTTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
 - CAS latency (2 & 3)
 - Burst length (1, 2, 4, 8 & Full page)
 - Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM (x4,x8) & L(U)DQM (x16) for masking
- Auto & self refresh
- 64ms refresh period (8K Cycle)
- **54 TSOP(II) Pb-free Package**
- **RoHS compliant**

GENERAL DESCRIPTION

The K4S560432E / K4S560832E / K4S561632E is 268,435,456 bits synchronous high data rate Dynamic RAM organized as 4 x 16,785,216 / 4 x 8,392,608 / 4 x 4,196,304 words by 4bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

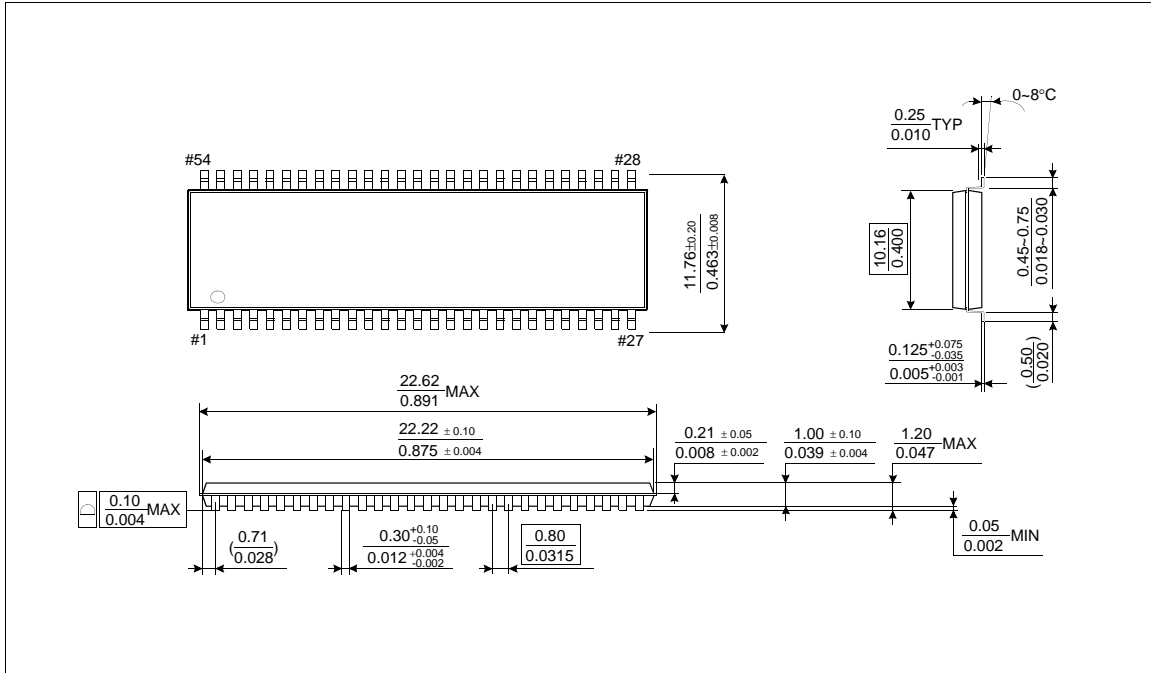
Ordering Information

| Part No. | Organization | Max Freq. | Interface | Package |
|-----------------------|--------------|-----------|-----------|----------------|
| K4S560432E-UC(L)75 | 64M x 4 | 133MHz | LVTTTL | 54pin TSOP(II) |
| K4S560832E-UC(L)75 | 32M x 8 | 133MHz | LVTTTL | 54pin TSOP(II) |
| K4S561632E-UC(L)60/75 | 16M x 16 | 133MHz | LVTTTL | 54pin TSOP(II) |

| Organization | Row Address | Column Address |
|--------------|-------------|----------------|
| 64Mx4 | A0~A12 | A0-A9, A11 |
| 32Mx8 | A0~A12 | A0-A9 |
| 16Mx16 | A0~A12 | A0-A8 |

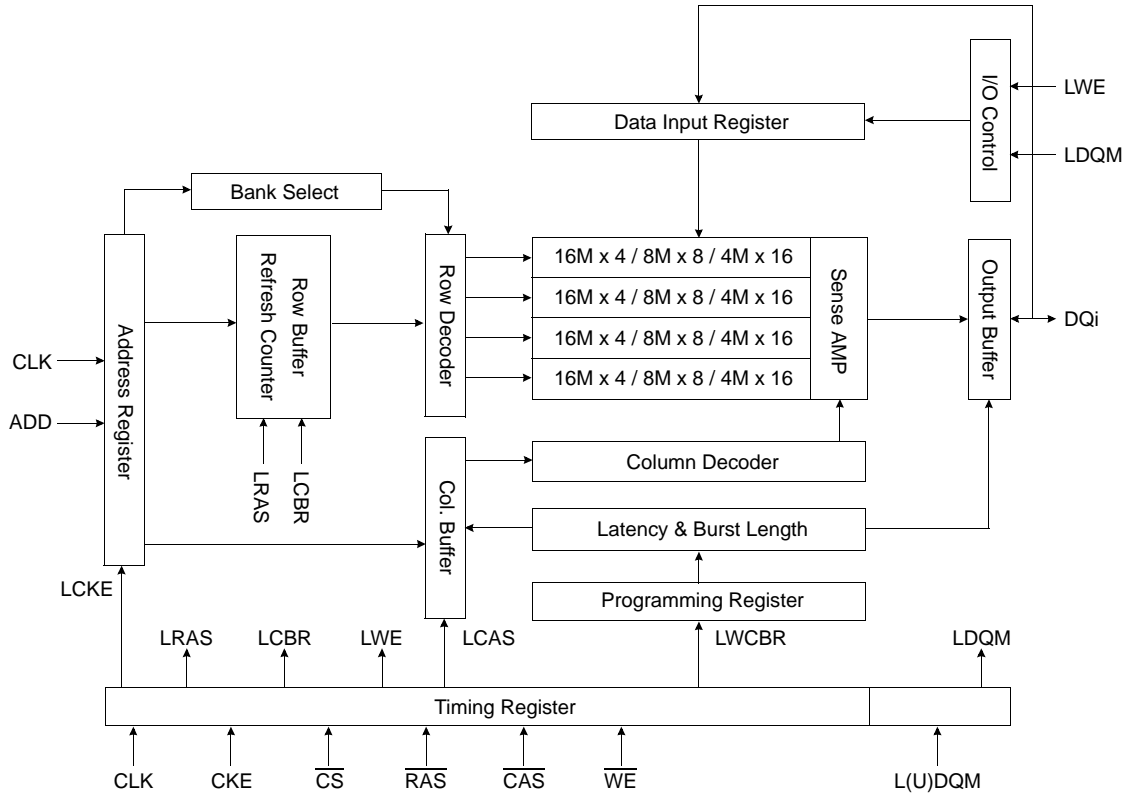
Row & Column address configuration

Package Physical Dimension



54Pin TSOP(II) Package Dimension

FUNCTIONAL BLOCK DIAGRAM

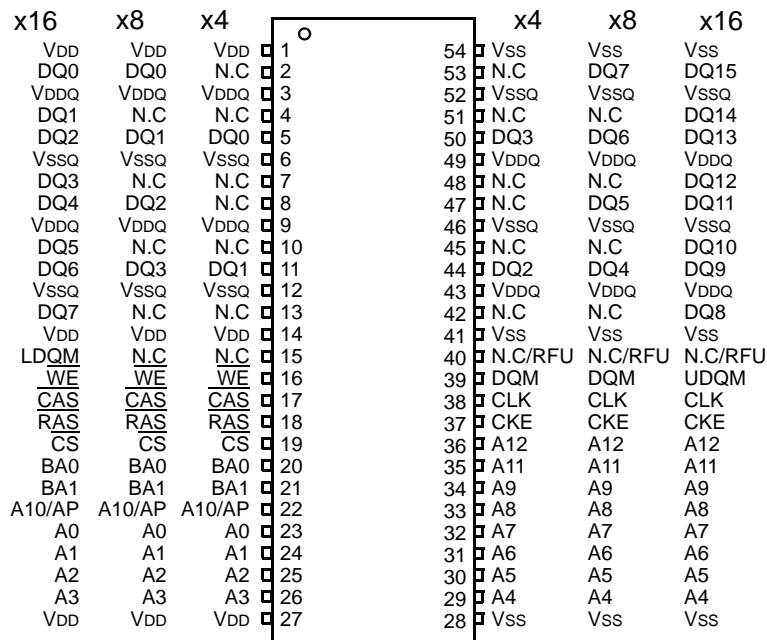


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SDRAM 256Mb E-die (x4, x8, x16)

CMOS SDRAM

PIN CONFIGURATION (Top view)



54Pin TSOP
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

| Pin | Name | Input Function |
|------------------|--|---|
| CLK | System clock | Active on the positive going edge to sample all inputs. |
| \overline{CS} | Chip select | Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM |
| CKE | Clock enable | Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. |
| A0 ~ A12 | Address | Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : (x4 : CA0 ~ CA9,CA11), (x8 : CA0 ~ CA9), (x16 : CA0 ~ CA8) |
| BA0 ~ BA1 | Bank select address | Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time. |
| \overline{RAS} | Row address strobe | Latches row addresses on the positive going edge of the CLK with \overline{RAS} low. Enables row access & precharge. |
| \overline{CAS} | Column address strobe | Latches column addresses on the positive going edge of the CLK with \overline{CAS} low. Enables column access. |
| \overline{WE} | Write enable | Enables write operation and row precharge. Latches data in starting from \overline{CAS} , \overline{WE} active. |
| DQM | Data input/output mask | Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. |
| DQ0 ~ N | Data input/output | Data inputs/outputs are multiplexed on the same pins. (x4 : DQ0 ~ 3), (x8 : DQ0 ~ 7), (x16 : DQ0 ~ 15) |
| VDD/VSS | Power supply/ground | Power and ground for the input buffers and the core logic. |
| VDDQ/VSSQ | Data output power/ground | Isolated power supply and ground for the output buffers to provide improved noise immunity. |
| N.C/RFU | No connection /reserved for future use | This pin is recommended to be left No Connection on the device. |



Rev. 1.3 August 2004

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---------------------------------------|------------------------------------|------------|------|
| Voltage on any pin relative to Vss | V _{IN} , V _{OUT} | -1.0 ~ 4.6 | V |
| Voltage on VDD supply relative to Vss | V _{DD} , V _{DDQ} | -1.0 ~ 4.6 | V |
| Storage temperature | T _{STG} | -55 ~ +150 | °C |
| Power dissipation | P _d | 1 | W |
| Short circuit current | I _{OS} | 50 | mA |

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---------------------------|------------------------------------|------|-----|----------------------|------|------------------------|
| Supply voltage | V _{DD} , V _{DDQ} | 3.0 | 3.3 | 3.6 | V | |
| Input logic high voltage | V _{IH} | 2.0 | 3.0 | V _{DD} +0.3 | V | 1 |
| Input logic low voltage | V _{IL} | -0.3 | 0 | 0.8 | V | 2 |
| Output logic high voltage | V _{OH} | 2.4 | - | - | V | I _{OH} = -2mA |
| Output logic low voltage | V _{OL} | - | - | 0.4 | V | I _{OL} = 2mA |
| Input leakage current | I _{LI} | -10 | - | 10 | uA | 3 |

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200 mV)

| Pin | Symbol | Min | Max | Unit | Note |
|---|------------------|-----|-----|------|------|
| Clock | C _{CLK} | 2.5 | 3.5 | pF | |
| RAS, CAS, WE, CS, CKE, DQM | C _{IN} | 2.5 | 3.8 | pF | |
| Address | C _{ADD} | 2.5 | 3.8 | pF | |
| (x4 : DQ ₀ ~ DQ ₃), (x8 : DQ ₀ ~ DQ ₇), (x16 : DQ ₀ ~ DQ ₁₅) | C _{OUT} | 4.0 | 6.0 | pF | |

DC CHARACTERISTICS (x4, x8)

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

| Parameter | Symbol | Test Condition | Version | Unit | Note | |
|---|--------|--|---------|------|------|---|
| | | | 75 | | | |
| Operating current (One bank active) | ICC1 | Burst length = 1 $t_{RC} \geq t_{RC}(\text{min})$ $I_o = 0$ mA | 80 | mA | 1 | |
| Precharge standby current in power-down mode | ICC2P | $\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$ | 2 | mA | | |
| | ICC2PS | $\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ | 2 | | | |
| Precharge standby current in non power-down mode | ICC2N | $\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns | 20 | mA | | |
| | ICC2NS | $\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable | 10 | | | |
| Active standby current in power-down mode | ICC3P | $\text{CKE} \leq V_{IL}(\text{max})$, $t_{CC} = 10\text{ns}$ | 6 | mA | | |
| | ICC3PS | $\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ | 6 | | | |
| Active standby current in non power-down mode (One bank active) | ICC3N | $\text{CKE} \geq V_{IH}(\text{min})$, $\overline{\text{CS}} \geq V_{IH}(\text{min})$, $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns | 25 | mA | | |
| | ICC3NS | $\text{CKE} \geq V_{IH}(\text{min})$, $\text{CLK} \leq V_{IL}(\text{max})$, $t_{CC} = \infty$ Input signals are stable | 25 | mA | | |
| Operating current (Burst mode) | ICC4 | $I_o = 0$ mA Page burst 4banks Activated. $t_{CCD} = 2\text{CLKs}$ | 100 | mA | 1 | |
| Refresh current | ICC5 | $t_{RC} \geq t_{RC}(\text{min})$ | 180 | mA | 2 | |
| Self refresh current | ICC6 | $\text{CKE} \leq 0.2\text{V}$ | C | 3 | mA | 3 |
| | | | L | 1.5 | mA | 4 |

Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

3. K4S5604(08)32E-UC

4. K4S5604(08)32E-UL

5. Unless otherwise noticed, input swing level is CMOS($V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$).

DC CHARACTERISTICS (x16)

(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

| Parameter | Symbol | Test Condition | Version | | Unit | Note |
|---|--------------------|---|---------|-----|------|------|
| | | | 60 | 75 | | |
| Operating current (One bank active) | I _{CC1} | Burst length = 1 t _{RC} ≥ t _{RC(min)} I _O = 0 mA | 140 | 90 | mA | 1 |
| Precharge standby current in power-down mode | I _{CC2P} | CKE ≤ V _{IL(max)} , t _{CC} = 10ns | 2 | | mA | |
| | I _{CC2PS} | CKE & CLK ≤ V _{IL(max)} , t _{CC} = ∞ | 2 | | | |
| Precharge standby current in non power-down mode | I _{CC2N} | CKE ≥ V _{IH(min)} , CS ≥ V _{IH(min)} , t _{CC} = 10ns Input signals are changed one time during 20ns | 20 | | mA | |
| | I _{CC2NS} | CKE ≥ V _{IH(min)} , CLK ≤ V _{IL(max)} , t _{CC} = ∞ Input signals are stable | 10 | | | |
| Active standby current in power-down mode | I _{CC3P} | CKE ≤ V _{IL(max)} , t _{CC} = 10ns | 6 | | mA | |
| | I _{CC3PS} | CKE & CLK ≤ V _{IL(max)} , t _{CC} = ∞ | 6 | | | |
| Active standby current in non power-down mode (One bank active) | I _{CC3N} | CKE ≥ V _{IH(min)} , CS ≥ V _{IH(min)} , t _{CC} = 10ns Input signals are changed one time during 20ns | 25 | | mA | |
| | I _{CC3NS} | CKE ≥ V _{IH(min)} , CLK ≤ V _{IL(max)} , t _{CC} = ∞ Input signals are stable | 25 | | mA | |
| Operating current (Burst mode) | I _{CC4} | I _O = 0 mA Page burst 4banks Activated. t _{CCD} = 2CLKs | 170 | 130 | mA | 1 |
| Refresh current | I _{CC5} | t _{RC} ≥ t _{RC(min)} | 200 | 180 | mA | 2 |
| Self refresh current | I _{CC6} | CKE ≤ 0.2V | C | 3 | mA | 3 |
| | | | L | 1.5 | mA | 4 |

Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

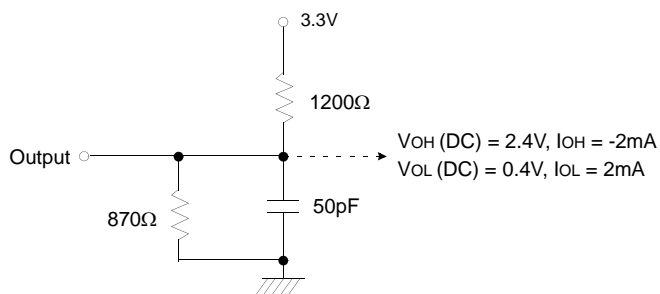
3. K4S561632E-UC

4. K4S561632E-UL

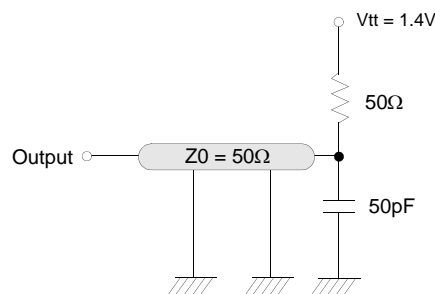
5. Unless otherwise noticed, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}).

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

| Parameter | Value | Unit |
|---|-----------------|------|
| AC input levels (V_{ih}/V_{il}) | 2.4/0.4 | V |
| Input timing measurement reference level | 1.4 | V |
| Input rise and fall time | $t_r/t_f = 1/1$ | ns |
| Output timing measurement reference level | 1.4 | V |
| Output load condition | See Fig. 2 | |



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

| Parameter | Symbol | Version | | Unit | Note |
|--|-----------------|------------------|----|------|------|
| | | 60 | 75 | | |
| Row active to row active delay | $t_{RRD}(\min)$ | 12 | 15 | ns | 1 |
| RAS to CAS delay | $t_{RCD}(\min)$ | 18 | 20 | ns | 1 |
| Row precharge time | $t_{RP}(\min)$ | 18 | 20 | ns | 1 |
| Row active time | $t_{RAS}(\min)$ | 42 | 45 | ns | 1 |
| | $t_{RAS}(\max)$ | 100 | | us | |
| Row cycle time | $t_{RC}(\min)$ | 60 | 65 | ns | 1 |
| Last data in to row precharge | $t_{RDL}(\min)$ | 2 | | CLK | 2, 5 |
| Last data in to Active delay | $t_{DAL}(\min)$ | 2 CLK + t_{RP} | | - | 5 |
| Last data in to new col. address delay | $t_{CDL}(\min)$ | 1 | | CLK | 2 |
| Last data in to burst stop | $t_{BDL}(\min)$ | 1 | | CLK | 2 |
| Col. address to col. address delay | $t_{CCD}(\min)$ | 1 | | CLK | 3 |
| Number of valid output data | CAS latency=3 | 2 | | ea | 4 |
| | CAS latency=2 | - | 1 | | |

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write.
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.
 5. In 100MHz and below 100MHz operating conditions, $t_{RDL}=1CLK$ and $t_{DAL}=1CLK + 20ns$ is also supported. SAMSUNG recommends $t_{RDL}=2CLK$ and $t_{DAL}=2CLK + t_{RP}$.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

| Parameter | | Symbol | 60 | | 75 | | Unit | Note |
|---------------------------|---------------|--------|-----|------|-----|------|------|------|
| | | | Min | Max | Min | Max | | |
| CLK cycle time | CAS latency=3 | tCC | 6 | 1000 | 7.5 | 1000 | ns | 1 |
| | CAS latency=2 | | - | | 10 | | | |
| CLK to valid output delay | CAS latency=3 | tsAC | | 5 | | 5.4 | ns | 1,2 |
| | CAS latency=2 | | | - | | 6 | | |
| Output data hold time | CAS latency=3 | tOH | 2.5 | | 3 | | ns | 2 |
| | CAS latency=2 | | - | | 3 | | | |
| CLK high pulse width | | tCH | 2.5 | | 2.5 | | ns | 3 |
| CLK low pulse width | | tCL | 2.5 | | 2.5 | | ns | 3 |
| Input setup time | | tSS | 1.5 | | 1.5 | | ns | 3 |
| Input hold time | | tSH | 1 | | 0.8 | | ns | 3 |
| CLK to output in Low-Z | | tSLZ | 1 | | 1 | | ns | 2 |
| CLK to output in Hi-Z | CAS latency=3 | tSHZ | | 5 | | 5.4 | ns | |
| | CAS latency=2 | | | - | | 6 | | |

- Notes :**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 - Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered, i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

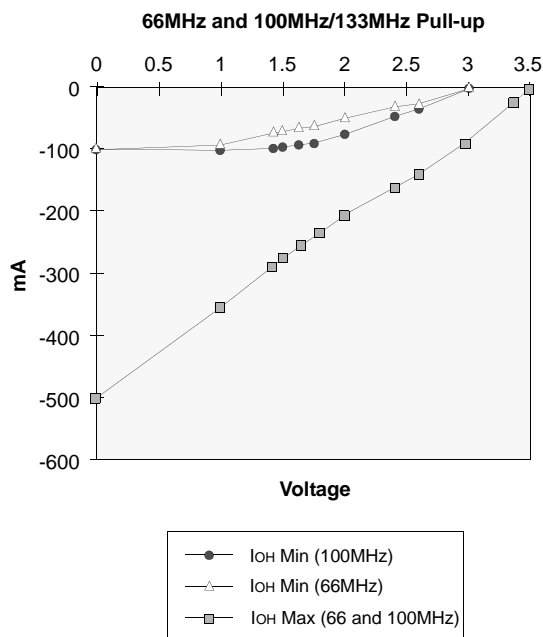
| Parameter | Symbol | Condition | Min | Typ | Max | Unit | Notes |
|------------------|--------|--|------|-----|------|----------|-------|
| Output rise time | trh | Measure in linear region : 1.2V ~ 1.8V | 1.37 | | 4.37 | Volts/ns | 3 |
| Output fall time | tfh | Measure in linear region : 1.2V ~ 1.8V | 1.30 | | 3.8 | Volts/ns | 3 |
| Output rise time | trh | Measure in linear region : 1.2V ~ 1.8V | 2.8 | 3.9 | 5.6 | Volts/ns | 1,2 |
| Output fall time | tfh | Measure in linear region : 1.2V ~ 1.8V | 2.0 | 2.9 | 5.0 | Volts/ns | 1,2 |

- Notes :**
- Rise time specification based on $0pF + 50\Omega$ to V_{SS} , use these values to design to.
 - Fall time specification based on $0pF + 50\Omega$ to V_{DD} , use these values to design to.
 - Measured into $50pF$ only, use these values to characterize to.
 - All measurements done with respect to V_{SS} .

IBIS SPECIFICATION

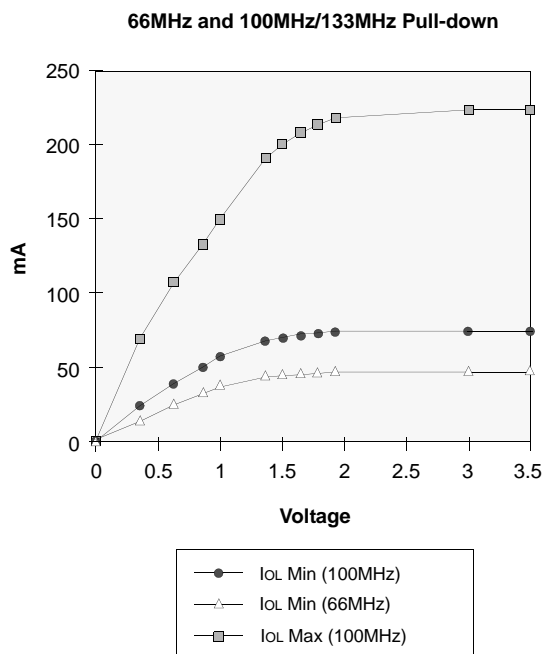
I_{OH} Characteristics (Pull-up)

| Voltage | 100MHz 133MHz Min | 100MHz 133MHz Max | 66MHz Min |
|---------|-------------------------|-------------------------|--------------|
| (V) | I (mA) | I (mA) | I (mA) |
| 3.45 | | -2.4 | |
| 3.3 | | -27.3 | |
| 3.0 | 0.0 | -74.1 | -0.7 |
| 2.6 | -21.1 | -129.2 | -7.5 |
| 2.4 | -34.1 | -153.3 | -13.3 |
| 2.0 | -58.7 | -197.0 | -27.5 |
| 1.8 | -67.3 | -226.2 | -35.5 |
| 1.65 | -73.0 | -248.0 | -41.1 |
| 1.5 | -77.9 | -269.7 | -47.9 |
| 1.4 | -80.8 | -284.3 | -52.4 |
| 1.0 | -88.6 | -344.5 | -72.5 |
| 0.0 | -93.0 | -502.4 | -93.0 |



I_{OL} Characteristics (Pull-down)

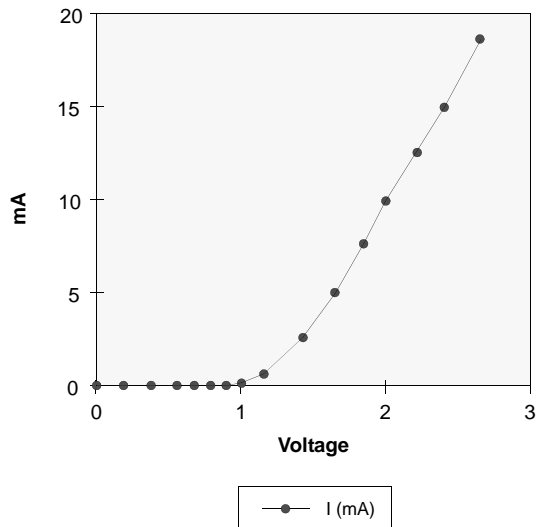
| Voltage | 100MHz 133MHz Min | 100MHz 133MHz Max | 66MHz Min |
|---------|-------------------------|-------------------------|--------------|
| (V) | I (mA) | I (mA) | I (mA) |
| 0.0 | 0.0 | 0.0 | 0.0 |
| 0.4 | 27.5 | 70.2 | 17.7 |
| 0.65 | 41.8 | 107.5 | 26.9 |
| 0.85 | 51.6 | 133.8 | 33.3 |
| 1.0 | 58.0 | 151.2 | 37.6 |
| 1.4 | 70.7 | 187.7 | 46.6 |
| 1.5 | 72.9 | 194.4 | 48.0 |
| 1.65 | 75.4 | 202.5 | 49.5 |
| 1.8 | 77.0 | 208.6 | 50.7 |
| 1.95 | 77.6 | 212.0 | 51.5 |
| 3.0 | 80.3 | 219.6 | 54.2 |
| 3.45 | 81.4 | 222.6 | 54.9 |



V_{DD} Clamp @ CLK, CKE, \overline{CS} , DQM & DQ

| V _{DD} (V) | I (mA) |
|---------------------|--------|
| 0.0 | 0.0 |
| 0.2 | 0.0 |
| 0.4 | 0.0 |
| 0.6 | 0.0 |
| 0.7 | 0.0 |
| 0.8 | 0.0 |
| 0.9 | 0.0 |
| 1.0 | 0.23 |
| 1.2 | 1.34 |
| 1.4 | 3.02 |
| 1.6 | 5.06 |
| 1.8 | 7.35 |
| 2.0 | 9.83 |
| 2.2 | 12.48 |
| 2.4 | 15.30 |
| 2.6 | 18.31 |

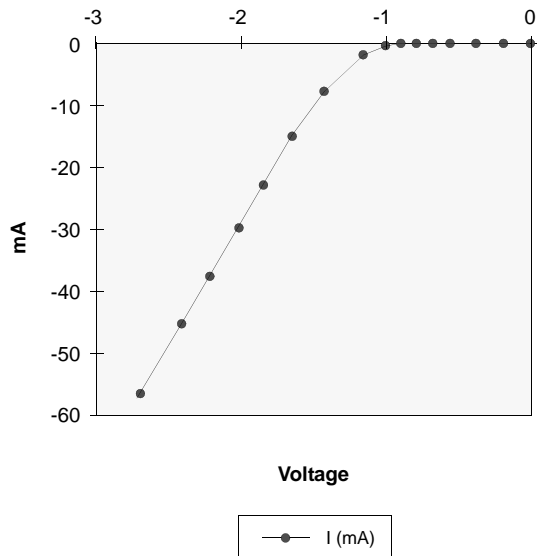
Minimum V_{DD} clamp current
(Referenced to V_{DD})



V_{SS} Clamp @ CLK, CKE, \overline{CS} , DQM & DQ

| V _{SS} (V) | I (mA) |
|---------------------|--------|
| -2.6 | -57.23 |
| -2.4 | -45.77 |
| -2.2 | -38.26 |
| -2.0 | -31.22 |
| -1.8 | -24.58 |
| -1.6 | -18.37 |
| -1.4 | -12.56 |
| -1.2 | -7.57 |
| -1.0 | -3.37 |
| -0.9 | -1.75 |
| -0.8 | -0.58 |
| -0.7 | -0.05 |
| -0.6 | 0.0 |
| -0.4 | 0.0 |
| -0.2 | 0.0 |
| 0.0 | 0.0 |

Minimum V_{SS} clamp current



SDRAM 256Mb E-die (x4, x8, x16)

CMOS SDRAM

SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

| Command | | CKEn-1 | CKEn | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | DQM | BA0,1 | A10/AP | A0 ~ A9 A11, A12 | Note |
|------------------------------------|------------------------|--------|-------|-----------------|------------------|------------------|-----------------|-----|---------|-------------|---------------------|------|
| Register | Mode register set | H | X | L | L | L | L | X | OP code | | | 1,2 |
| Refresh | Auto refresh | H | H | L | L | L | H | X | X | | | 3 |
| | Self refresh | | Entry | | | | | | | | | L |
| | | Exit | L | H | L | H | H | X | X | | | 3 |
| | H | | X | X | X | 3 | | | | | | |
| Bank active & row addr. | | H | X | L | L | H | H | X | V | Row address | | |
| Read & column address | Auto precharge disable | H | X | L | H | L | H | X | V | L | Column address | 4 |
| | Auto precharge enable | | | | | | | | | H | | 4,5 |
| Write & column address | Auto precharge disable | H | X | L | H | L | L | X | V | L | Column address | 4 |
| | Auto precharge enable | | | | | | | | | H | | 4,5 |
| Burst stop | | H | X | L | H | H | L | X | X | | | 6 |
| Precharge | Bank selection | H | X | L | L | H | L | X | V | L | X | |
| | All banks | | | | | | | | X | H | | |
| Clock suspend or active power down | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | L | V | V | V | | | | | |
| | Exit | L | H | X | X | X | X | X | | | | |
| | | | | | | | | | | | | |
| Precharge power down mode | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | L | H | H | H | | | | | |
| | Exit | L | H | H | X | X | X | X | X | | | |
| | | | | L | V | V | V | | | | | |
| DQM | | H | X | | | | | V | X | | 7 | |
| No operation command | | H | X | H | X | X | X | X | X | | | |
| | | | | L | H | H | H | | | | | |

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.

If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at TRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),

but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)