



| HYUNDAI | |
|---|--|
| HY62256A-(I) Series | |
| 32Kx8bit CMOS SRAM | |
| Description | Features |
| <p>The HY62256A/HY62256A-I is a high-speed, low power and 32,786 x 8-bits CMOS Static Random Access Memory fabricated using Hyundai's high performance CMOS process technology. The HY62256A/HY62256A-I has a data retention mode that guarantees data to remain valid at the minimum power supply voltage of 2.0 volt. Using the CMOS technology, supply voltages from 2.0 to 5.5 volt has little effect on supply current in the data retention mode. The HY62256A/HY62256A-I is suitable for use in low voltage operation and battery back-up application.</p> | <ul style="list-style-type: none"> ● Fully static operation and Tri-state outputs ● TTL compatible inputs and outputs ● Low power consumption -2.0V(min.) data retention ● Standard pin configuration <ul style="list-style-type: none"> -28 pin 600 mil PDIP -28 pin 330 mil SOP -28 pin 8x13.4 mm TSOP-1 (standard and reversed) |

| Product No. | Voltage (V) | Speed (ns) | Operation Current(mA) | Standby Current(uA) | | | Temperature (°C) |
|---|-------------|------------|-----------------------|---------------------|-----|----|------------------|
| | | | | | L | LL | |
| HY62256A | 5.0 | 55/70/85 | 50 | 1mA | 100 | 25 | 0-70(Normal) |
| HY62256A-I | 5.0 | 55/70/85 | 50 | 1mA | 100 | - | -40-85(E.T.) |
| Note 1. E T. Extended Temperature, Normal: Normal Temperature 2. Current value is max. | | | | | | | |
| Features Pins Ratings Timing Package Ordering | | | | | | | |

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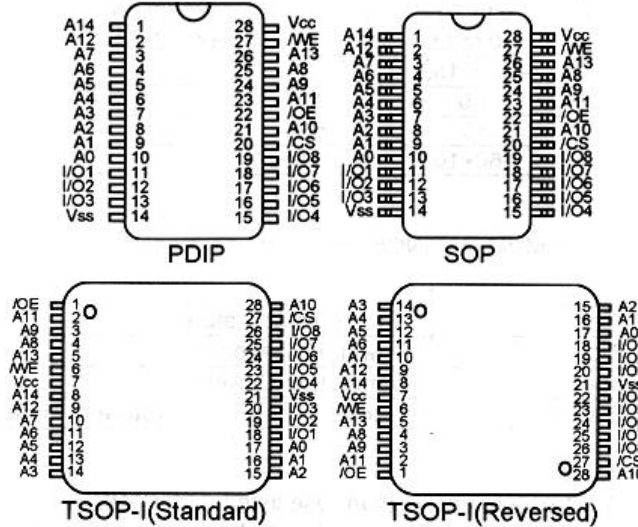
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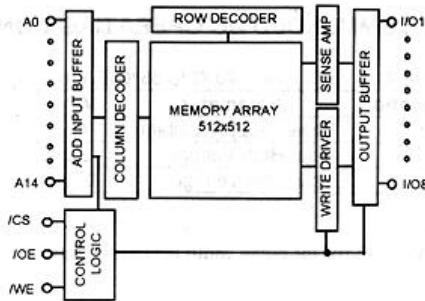


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| HYUNDAI ELECTRONICS AMERICA HY62256A-(I) Series 32Kx8bit CMOS SRAM | PIN INFORMATION |
|---|------------------------|

PIN CONNECTION



BLOCK DIAGRAM



| PIN DESCRIPTION | |
|---|-------------------|
| Pin Name | Pin Function |
| /CS | Chip Select |
| /WE | Write Enable |
| /OE | Output Enable |
| A0-A14 | Address Inputs |
| I/O1-I/O8 | Data Input/Output |
| Vcc | Power(+5.0V) |
| Vss | Ground |
| Features Pins Ratings Timing Package Ordering | |

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| HYUNDAI ELECTRONICS AMERICA HY62256A-(I) Series 32Kx8bit CMOS SRAM | RATINGS INFORMATION |
|---|----------------------------|

| ABSOLUTE MAXIMUM RATING (1) | | | | |
|--|-----------------------------------|---------------|-------------|---------------|
| Symbol | Parameter | Rating | Unit | Remark |
| V _{CC} V _{IN} V _{OUT} | Power Supply Input/Output Voltage | -0.5 to 7.0 | V | |
| T _A | Operating Temperature | 0 to 70 | °C | HY62256A |
| | | -40 to 85 | °C | HY62256A-I |
| T _{STG} | Storage Temperature | -65 to 150 | °C | |
| P _D | Power Dissipation | 1.0 | W | |
| I _{OUT} | Data OutPut Current | 50 | mA | |
| T _{SOLDER} | Lead Soldering Temperature & Time | 260 /10 | °C / sec | |
| Note 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability. | | | | |

| RECOMMENDED DC OPERATING CONDITIONS | | | | | |
|---|----------------------|------------|------------|----------------------|-------------|
| T _A =0°C to 70°C / T _A = -40°C to 85°C (E.T.) | | | | | |
| Symbol | Parameter | Min | Typ | Max | Unit |
| V _{CC} | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | Input High Voltage | 2.2 | - | V _{CC} +0.5 | V |
| V _{IL} | Input Low Voltage | -0.5(1) | - | 0.8 | V |
| Note 1. V _{IL} = -3.0V for pulse width less than 30ns | | | | | |

| TRUTH TABLE | | | | |
|-------------|-----|-----|-----------------|---------------|
| /CS | /WE | /OE | MODE | I/O OPERATION |
| H | X | X | Standby | High-Z |
| L | H | H | Output Disabled | High-Z |
| L | H | L | Read | Data Out |
| L | L | X | Write | Data In |

Note:
1. H=V_{IH}, L=V_{IL}, X=Don't Care

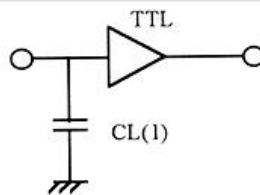
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| DC CHARACTERISTICS | | | | | | | | |
|---|-----------------------------------|------------|---|-----|-----|-----|------|----|
| V _{CC} = 5V ?% T _A = 0°C to 70°C (Normal) / -40°C to 85°C (E.T.) unless otherwise specified | | | | | | | | |
| Symbol | Parameter | | Test Condition | Min | Typ | Max | Unit | |
| I _{LI} | Input Leakage Current | | V _{SS} <= V _{IN} <= V _{CC} | -1 | - | 1 | uA | |
| I _{LO} | Output Leakage Current | | V _{SS} <= V _{OUT} <= V _{CC} /CS=V _{IH} or /OE=V _{IH} or /WE = V _{IL} | -1 | - | 1 | uA | |
| I _{CC} | Operating Power Supply Current | | /CS= V _{IL} , V _{IN} =V _{IH} or V _{IL} , I _{I/O} = 0mA | - | 30 | 50 | mA | |
| I _{CC1} | Average Operating Current | | /CS = V _{IL} Min. Duty Cycle = 100%, I _{I/O} =0mA | - | 40 | 70 | mA | |
| I _{SB} | TTL Standby Current (TTL Inputs) | | /CS = V _{IH} V _{IN} = V _{IH} or V _{IL} | - | 0.4 | 2 | mA | |
| I _{SB1} | CMOS Standby Current (CMOS Input) | HY62256A | /CS >= V _{CC} - 0.2V | | - | - | 1 | mA |
| | | | V _{IN} <= 0.2V or | L | - | 2 | 100 | uA |
| | | HY62256A-I | V _{IN} >= | LL | - | 1 | 25 | uA |
| | | | V _{CC} -0.2V | | - | - | 1 | mA |
| | | | | L | - | 2 | 100 | uA |
| V _{OL} | Output Low Voltage | | I _{OL} = 2.1 mA | - | - | 0.4 | V | |
| V _{OH} | Output High Voltage | | I _{OH} = 1mA | 2.4 | - | - | V | |

Note: Typical values are at V_{CC} = 5.0V T_A = 25°C

| AC CHARACTERISTICS | | | | | | | | | |
|---|------------------|--------------------------------------|------|------|------|------|------|------|------|
| V _{CC} = 5V(±)10%, T _A = 0°C to 70°C (Normal)/ -40°C to 85°C (E.T.) unless otherwise specified. | | | | | | | | | |
| # | Symbol | Parameter | -55 | | -70 | | -85 | | Unit |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | | |
| 1 | t _{RC} | Read Cycle Time | 55 | - | 70 | - | 85 | - | ns |
| 2 | t _{AA} | Address Access Time | - | 55 | - | 70 | - | 85 | ns |
| 3 | t _{ACS} | Chip Select Access Time | - | 55 | - | 70 | - | 85 | ns |
| 4 | t _{OE} | Output Enable to Output Valid | - | 30 | - | 35 | - | 45 | ns |
| 5 | t _{CLZ} | Chip Select to Output in Low Z | 5 | - | 5 | - | 5 | - | ns |
| 6 | t _{OLZ} | Output Enable to Output in Low Z | 5 | - | 5 | - | 5 | - | ns |
| 7 | t _{CHZ} | Chip Deselection to Output in High Z | 0 | 20 | 0 | 30 | 0 | 30 | ns |
| 8 | t _{OHZ} | Out Disable to Output in High Z | 0 | 20 | 0 | 30 | 0 | 30 | ns |
| 9 | t _{OH} | Output Hold from Address Change | 5 | - | 5 | - | 5 | - | ns |
| WRITE CYCLE | | | | | | | | | |
| 10 | t _{WC} | Write Cycle Time | 55 | - | 70 | - | 85 | - | ns |
| 11 | t _{CW} | Chip Selection to End of Write | 50 | - | 65 | - | 75 | - | ns |
| 12 | t _{AW} | Address Valid to End of Write | 50 | - | 65 | - | 75 | - | ns |
| 13 | t _{AS} | Address Set-up Time | 0 | - | 0 | - | 0 | - | ns |
| 14 | t _{WP} | Write Pulse Width | 40 | - | 50 | - | 55 | - | ns |
| 15 | t _{WR} | Write Recovery Time | 0 | - | 0 | - | 0 | - | ns |
| 16 | t _{WHZ} | Write to Output in High Z | 0 | 20 | 0 | 30 | 0 | 30 | ns |
| 17 | t _{DW} | Data to Write Time Overlap | 25 | - | 35 | - | 40 | - | ns |
| 18 | t _{DH} | Data Hold from Write Time | 0 | - | 0 | - | 0 | - | ns |
| 19 | t _{OW} | Output Active from End of Write | 5 | - | 5 | - | 5 | - | ns |

| AC TEST CONDITIONS | | |
|--|-------------|------------------------|
| T _A = 0°C to 70°C (Normal) / -40°C to 85°C (E.T.) unless otherwise specified. | | |
| PARAMETER | | VALUE |
| Input Pulse Level | | 0.8V to 2.4V |
| Input Rise and Fall Time | | 5ns |
| Input and Output Timing Reference Levels | | 1.5V |
| Output Load | 70/85/100ns | CL = 100pF + 1TTL Load |
| | 55ns | CL = 50pF + 1TTL Load |

AC TEST LOADS

Note: Including jig and scope capacitance

CAPACITANCE

$T_{A_A} = 25\text{ }^{\circ}\text{C}$, $f = 1.0\text{MHz}$

| Symbol | Parameter | Condition | Max | Unit |
|-----------|--------------------------|----------------|-----|------|
| C_{IN} | Input Capacitance | $V_{IN} = 0V$ | 6 | pF |
| $C_{I/O}$ | Input/Output Capacitance | $V_{I/O} = 0V$ | 8 | pF |

Note: These parameters are sampled and not 100% tested

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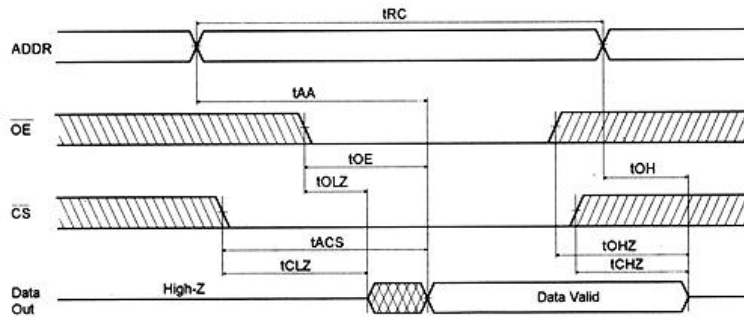
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| HYUNDAI ELECTRONICS AMERICA HY62256A-I 32K x 8bit CMOS SRAM | TIMING INFORMATION |
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TIMING DIAGRAM

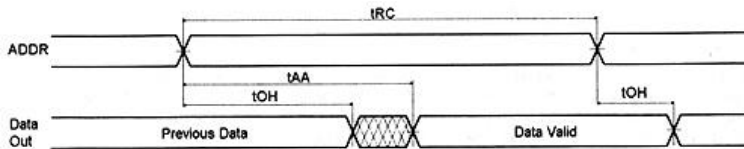
READ CYCLE 1



Note (READ CYCLE):

1. tCHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tCHZ max. is less than tCLZ min. both for a given device and from device to device.
3. /WE is high for the read cycle.

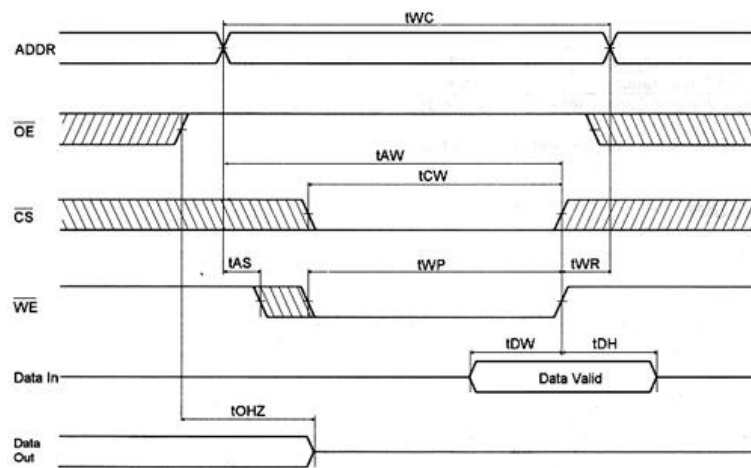
READ CYCLE 2



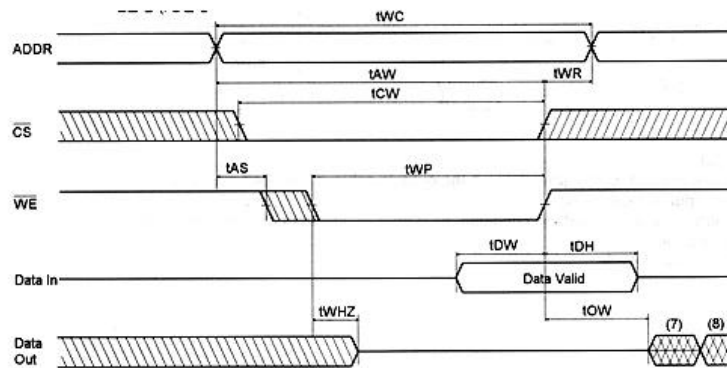
Note (READ CYCLE):

1. /WE is high for the read cycle.
2. Device is continuously selected /CS= VIL.
3. /OE =VIL.

WRITE CYCLE 1 (/OE Clocked)



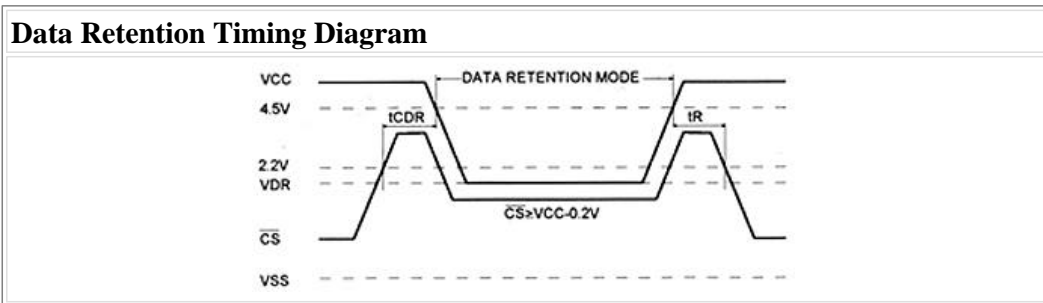
WRITE CYCLE 2 (/OE Low Fixed)



Notes (WRITE CYCLE):

1. A write occurs during the overlap of a low /CS and a low /WE. A write begins at the latest transition among /CS going low and /WE going low: A write ends at the earliest transition among /CS going high and /WE going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of /CS going low to the end of write .
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends as /CS, or /WE going high.
5. If /OE and /WE are in the read mode during this period, and the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS goes low simultaneously with /WE going low, or after /WE going low, the outputs remain in high impedance state.
7. DOUT is the same phase of latest written data in this write cycle.
8. DOUT is the read data of the new address.

| DATA RETENTION CHARACTERISTIC | | | | | | | | |
|--|-------------------------------------|------------|---|--------------------|-----|-----|-------------------|----|
| T _A = 0°C to 70°C (normal) /-40°C to 85°C (E.T.) | | | | | | | | |
| Symbol | Parameter | | Test Condition | Min | Typ | Max | Unit | |
| V _{DR} | V _{CC} for Data Retention | | /CS >= V _{CC} -0.2V V _{SS} <= V _{IN} <= V _{CC} | 2 | - | - | V | |
| I _{CCDR} | Data Retention Current | HY62256A | V _{CC} = 3.0V /CS >= V _{CC} -0.2V V _{SS} <= V _{IN} <= V _{CC} | L | - | 1 | 50 | uA |
| | | | | LL | - | 1 | 15 ⁽²⁾ | uA |
| | | HY62256A-1 | | L | - | 1 | 50 | uA |
| t _{CDR} | Chip Disable to Data Retention Time | | See Data Retention Timing Diagram | 0 | - | - | ns | |
| t _R | Operating Recovery Time | | Diagram | t _{RC(3)} | - | - | ns | |
| Notes | | | | | | | | |
| 1. Typical values are under the condition of T _A = 25°C | | | | | | | | |
| 2. 3uA max. at T _A = 0°C to 40°C | | | | | | | | |
| 3. t _{RC} is read cycle time. | | | | | | | | |



| RELIABILITY SPEC. | | | TEST SPEC. | |
|---|-----|-----------|-------------------|--|
| TEST MODE | | | | |
| ESD | HBM | >= 2000V | | |
| | MM | >= 250V | | |
| LATCH-UP | | <= -100mA | | |
| | | >= 100mA | | |
| Features Pins Ratings Timing Package Ordering | | | | |

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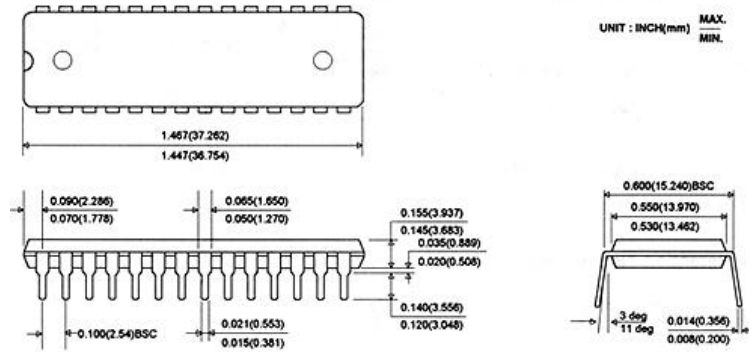
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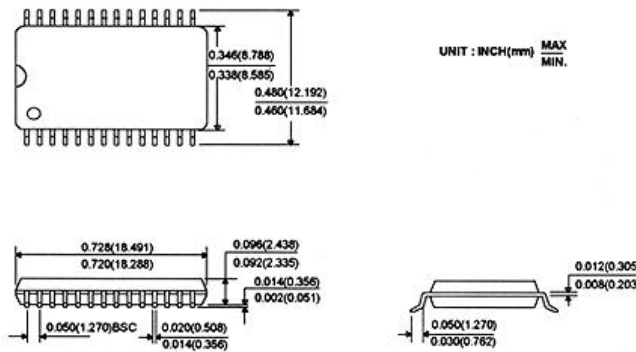


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| HYUNDAI ELECTRONICS AMERICA HY62256A-(I) Series 32Kx8bit CMOS SRAM | PACKAGE INFORMATION |
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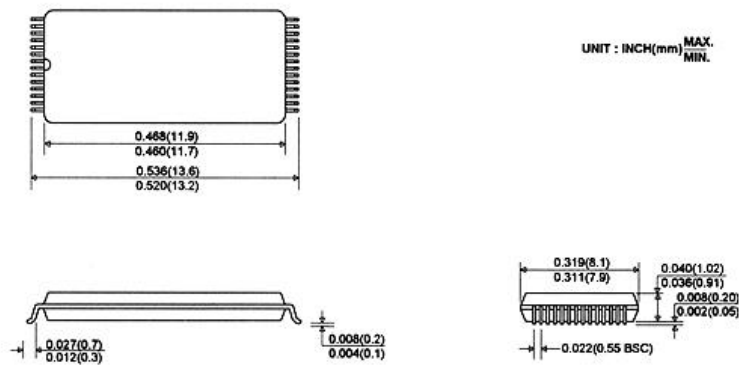
28pin 600mil Dual In-Line Package(P)



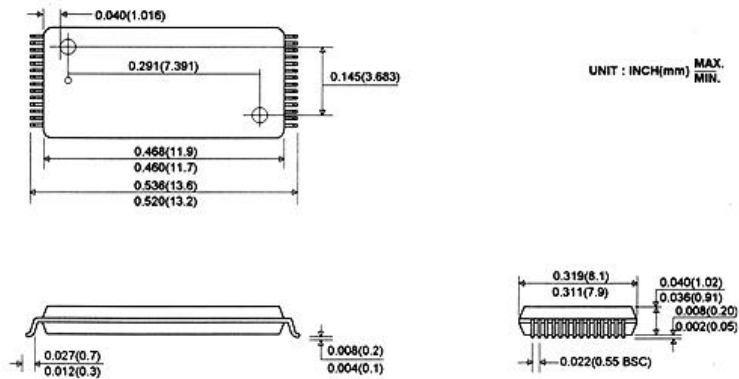
28pin 330mil Small Outline Package(J)



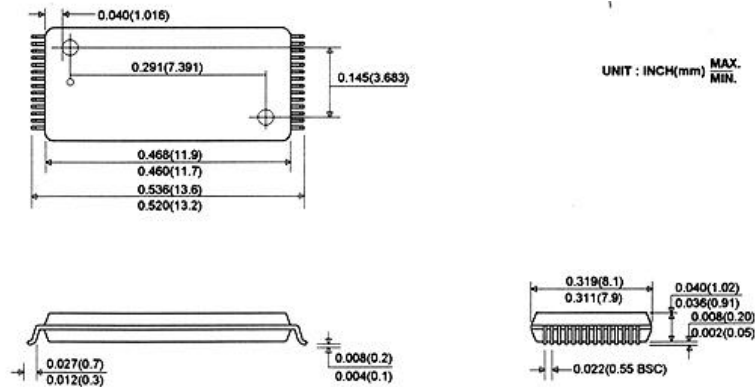
28pin 8X13.4mm Thin Small Outline Package Standard(T1)



28pin 8x13.4mm Thin Small Outline Package Reversed(R1)



28pin 8X13.4mm Thin Small Outline Package SReversed(R1)



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| Part No. | Speed | Power | Temp. | Package |
|---|----------|---------|-------|-----------------|
| HY62256AP | 55/70/85 | | | PDIP |
| HY62256ALP | 55/70/85 | L-part | | PDIP |
| HY62256ALLP | 55/70/85 | LL-part | | PDIP |
| HY62256AJ | 55/70/85 | | | SOP |
| HY62256ALJ | 55/70/85 | L-part | | SOP |
| HY62256ALLJ | 55/70/85 | LL-part | | SOP |
| HY62256AT1 | 55/70/85 | | | TSOP-I Standard |
| HY62256ALT1 | 55/70/85 | L-part | | TSOP-I Standard |
| HY62256ALLT1 | 55/70/85 | LL-part | | TSOP-I Standard |
| HY62256AR1 | 55/70/85 | | | TSOP-I Reversed |
| HY62256ALR1 | 55/70/85 | L-part | | TSOP-I Reversed |
| HY62256ALLR1 | 55/70/85 | LL-part | | TSOP-I Reversed |
| HY62256AP-I | 55/70/85 | | E.T. | PDIP |
| HY62256ALP-I | 55/70/85 | L-part | E.T. | PDIP |
| HY62256AJ-I | 55/70/85 | | E.T. | SOP |
| HY62256ALJ-I | 55/70/85 | L-part | E.T. | SOP |
| HY62256AT1-I | 55/70/85 | | E.T. | TSOP-I |
| HY62256ALT1-I | 55/70/85 | L-part | E.T. | TSOP-I |
| HY62256AR2-I | 55/70/85 | | E.T. | TSOP-I Reversed |
| HY62256ALR2-I | 55/70/85 | L-part | E.T. | TSOP-I Reversed |
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