

Low-Voltage Single SPDT Analog Switch

FEATURES

- Low Voltage Operation (2.25 V to 5.5 V)
- Low On-Resistance - $r_{DS(on)}$: 7 Ω
- Fast Switching - t_{ON} : 9 ns, t_{OFF} : 5 ns
- Low Charge Injection - Q_{INJ} : 5 pC
- Low Power Consumption
- TTL/CMOS Compatible
- 6-Pin SC-70 Package

BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

APPLICATIONS

- Cellular Phones
- Communication Systems
- Portable Test Equipment
- Battery Operated Systems
- Sample and Hold Circuits

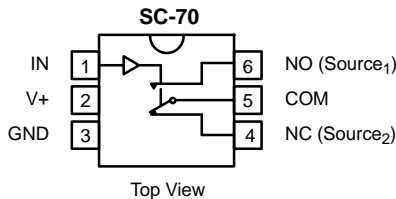
DESCRIPTION

The DG9411 is a single-pole/double-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed (t_{ON} : 9 ns, t_{OFF} : 5 ns), low on-resistance ($r_{DS(on)}$: 7 Ω) and small physical size (SC70), the DG9411 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG9411 is built on Vishay Siliconix's low voltage J12 process. An epitaxial layer prevents latchup. Break-before-make is guaranteed for DG9411.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
Logic	NC	NO
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION		
Temp Range	Package	Part Number
-40 to 85°C	SC70-6	DG9411DL



ABSOLUTE MAXIMUM RATINGS

Reference to GND	
V+	-0.3 to +6 V
IN, COM, NC, NO ^a	-0.3 to (V+ + 0.3 V)
Continuous Current (Any terminal)	± 50 mA
Peak Current	± 200 mA
(Pulsed at 1 ms, 10% duty cycle)	
Storage Temperature (D Suffix)	-65 to 125°C

Power Dissipation (Packages) ^b	
6-Pin SO70°	250 mW

Notes:

- Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6.5 mW/°C above 25°C

SPECIFICATIONS (V+ = 2.5 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 2.5 V, ± 10%, V _{IN} = 0.4 or 2.0 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} , V _{COM}		Full	0		V+	V
Drain-Source On-Resistance	r _{DS(on)}	V+ = 2.25 V, V _D = 1.0 V, I _S = 10 mA	Room Full ^d		26 29	35 40	Ω
r _{DS(on)} Flatness ^d	r _{DS(on)} Flatness	V+ = 2.5 V	Room		10		
Switch Off Leakage Current ^f	I _{S(off)}	V+ = 2.75 V V _S = 0.5 V/1.5 V, V _D = 1.5 V/0.5 V	Room Full ^d	-250 -3.0		250 3.0	pA nA
	I _{D(off)}		Room Full ^d	-250 -3.0		250 3.0	pA nA
Channel-On Leakage Current ^f	I _{D(on)}	V+ = 2.75 V, V _S = V _D = 0.5 V/1.5 V	Room Full ^d	-250 -3.0		250 3.0	pA nA
Digital Control							
Input High Voltage	V _{INH}		Full	2			V
Input Low Voltage	V _{INL}		Full			0.4	
Input Capacitance ^d	C _{in}		Full		3		pF
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	-1		1	μA
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _D or V _S = 1.5 V, R _L = 300 Ω, C _L = 35 pF Figures 1 and 2	Room Full ^d		16	40 45	ns
Turn-Off Time	t _{OFF}		Room Full ^d		7	23 28	
Break-Before-Make Time	t _d		Room	1	12		
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _S = 0 V V _{GEN} = 0 V, R _{GEN} = 0 Ω, Figure 3	Room		5	10	pC
Off-Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		-73		dB
Crosstalk ^d	X _{TALK}		Room		-70		
Source-Off Capacitance ^d	C _{S(off)}	V _{IN} = 0 or V+, f = 1 MHz	Room		7		pF
Channel-On Capacitance ^d	C _{D(on)}		Room		20		
Drain-to-Source Capacitance ^d	C _{DS(off)}		Room		20		
			Room				
Power Supply							
Power Supply Range	V+			2.25		2.75	V
Power Supply Current ^d	I+	V _{IN} = 0 or V+			0.01	1.0	μA
Power Consumption	P _C						0.3



SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, VIN = 0.4 or 2.0 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} , V _{COM}		Full	0		V+	V
Drain-Source On-Resistance ^d	r _{DS(on)}	V+ = 2.7 V, V _D = 1.5 V, I _S = 10 mA	Room Full		15 19	25 30	Ω
r _{DS(on)} Flatness ^d	r _{DS(on)} Flatness	V _S = 0 to V+, I _S = 10 mA	Room		7.5		
Switch Off Leakage Current ^f	I _{S(off)}	V+ = 3.3 V, V _S = 1 V/3 V, V _D = 3 V/1 V	Room Full	-500 -4.0		500 4.0	pA nA
	I _{D(off)}		Room Full	-500 -4.0		500 4.0	pA nA
Channel-On Leakage Current ^f	I _{D(on)}	V+ = 3.3 V, V _S = V _D = 1 V/3 V	Room Full	-500 -4.0		500 4.0	pA nA
Digital Control							
Input High Voltage	V _{INH}		Full	2			V
Input Low Voltage	V _{INL}		Full			0.8	
Input Capacitance ^d	C _{in}		Full		3		pF
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	-1		1	μA
Dynamic Characteristics							
Turn-On Time ^d	t _{ON}	V _D or V _S = 2.0 V, R _L = 300 Ω, C _L = 35 pF Figure 1 and 2	Room Full		12	15 20	ns
Turn-Off Time ^d	t _{OFF}		Room Full		6	8 10	
Break-Before-Make Time ^d	t _d		Room	1	7		
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 0 V, V _S = 0 V R _{GEN} = 0 Ω, Figure 3	Room		5	10	pC
Off-Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		-73		dB
Crosstalk ^d	X _{TALK}		Room		-70		
Source-Off Capacitance ^d	C _{S(off)}	V _{IN} = 0 or V+, f = 1 MHz	Room		7		pF
Channel-On Capacitance ^d	C _{D(on)}		Room		20		
Drain-to-Source Capacitance ^d	C _{DS(off)}		Room		20		
Power Supply							
Power Supply Range	V+			2.7		3.3	V
Power Supply Current	I+	V _{IN} = 0 or V+			0.01	1.0	μA
Power Consumption	P _C						0.4



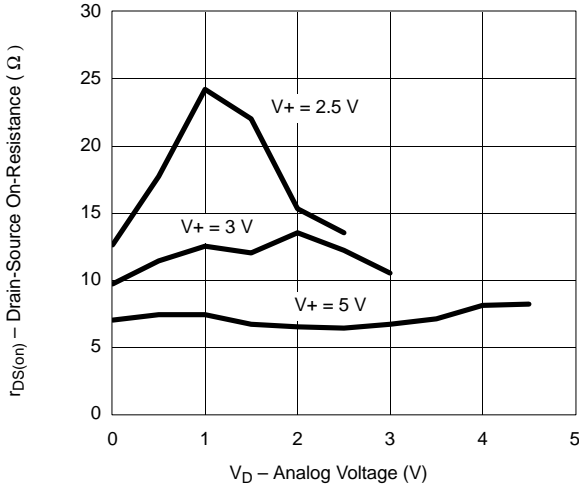
SPECIFICATIONS (V+ = 5 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ±10%, VIN = 0.8 or 2.4 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} , V _{COM}		Full	0		V+	V
Drain-Source On-Resistance	r _{DS(on)}	V+ = 4.5 V, V _D = 3 V, I _S = 10 mA	Room Full		7 10	12 16	Ω
r _{DS(on)} Flatness ^d	r _{DS(on)} Flatness	V+ = 2.5 V	Room		2		
Switch Off Leakage Current	I _{S(off)}	V+ = 5.5 V V _S = 1 V/4.5 V, V _D = 4.5 V/1 V	Room Full	-1.0 -4.0		1.0 4.0	nA
	I _{D(off)}		Room Full	-1.0 -4.0		1.0 4.0	
Channel-On Leakage Current	I _{D(on)}	V+ = 5.5 V, V _S = V _D = 1 V/4.5 V	Room Full	-1.0 -3.0		1.0 4.5	
Digital Control							
Input High Voltage	V _{INH}		Full	2.4			V
Input Low Voltage	V _{INL}		Full			0.8	
Input Capacitance	C _{in}		Full		3		pF
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	-1		1	μA
Dynamic Characteristics							
Turn-On Time ^d	t _{ON}	V _D or V _S = 3 V, R _L = 300 Ω, C _L = 35 pF Figure 1 and 2	Room Full		9	11 15	ns
Turn-Off Time ^d	t _{OFF}		Room Full		5	7 9	
Break-Before-Make Time ^d	t _d		Room	1	4		
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _S = 0 V V _{GEN} = 0 V, R _{GEN} = 0 Ω, Figure 3	Room		5	10	pC
Off-Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		-73		dB
Crosstalk ^d	X _{TALK}		Room		-70		
Source-Off Capacitance ^d	C _{S(off)}	V _{IN} = 0 or V+, f = 1 MHz	Room		7		pF
Channel-On Capacitance ^d	C _{D(on)}		Room		20		
Drain-to-Source Capacitance ^d	C _{DS(off)}		Room		20		
Power Supply							
Power Supply Range	V+			4.5		5.5	V
Power Supply Current	I+	V _{IN} = 0 or V+			0.01	1.0	μA
Power Consumption	P _C						0.6

Notes:

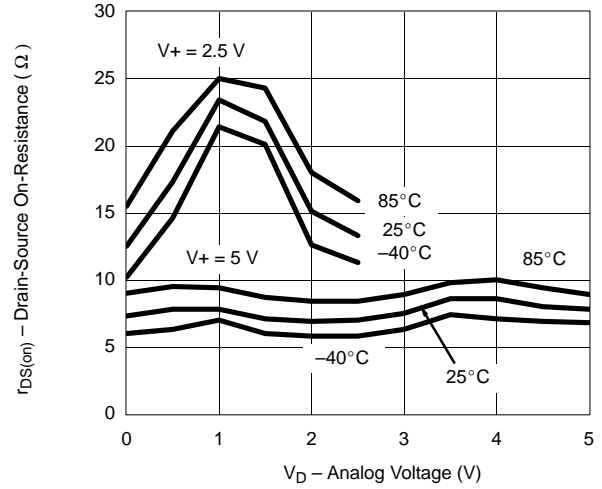
- Room = 25°C, Full = as determined by the operating suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- Guarantee by design, nor subjected to production test.
- V_{IN} = input voltage to perform proper function.
- Guaranteed by 5-V leakage testing, not production tested.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

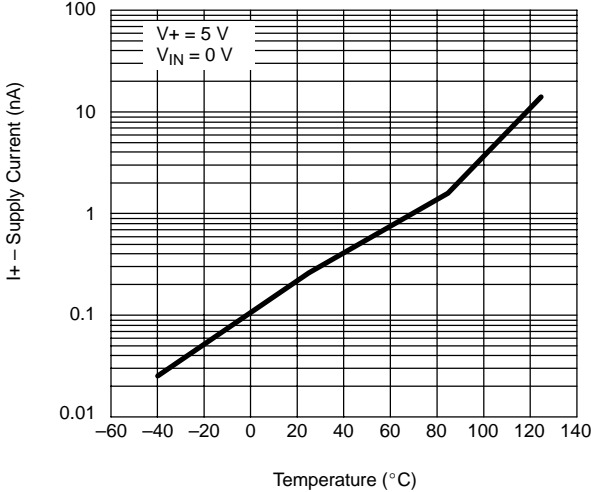
$r_{DS(on)}$ vs. Analog and Power Voltage



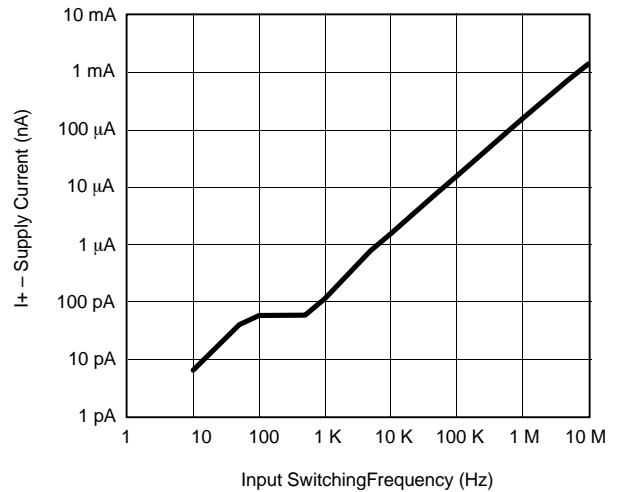
$r_{DS(on)}$ vs. Analog Voltage and Temperature



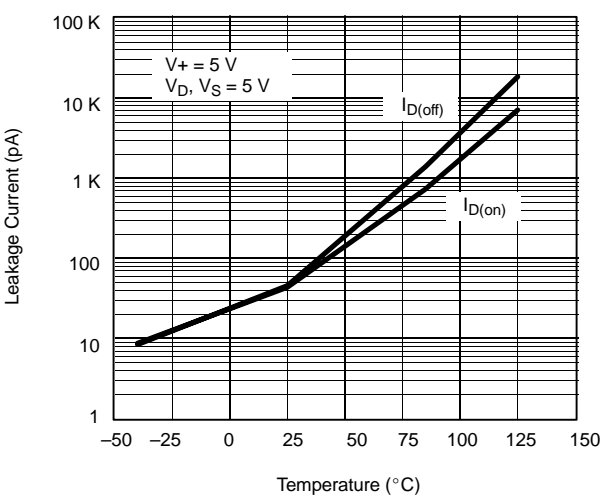
Supply Current vs. Temperature



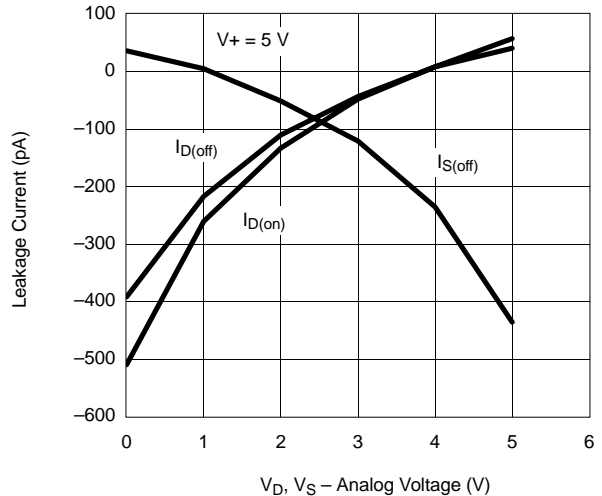
Supply Current vs. Input Switching Frequency



Leakage Current vs. Temperature

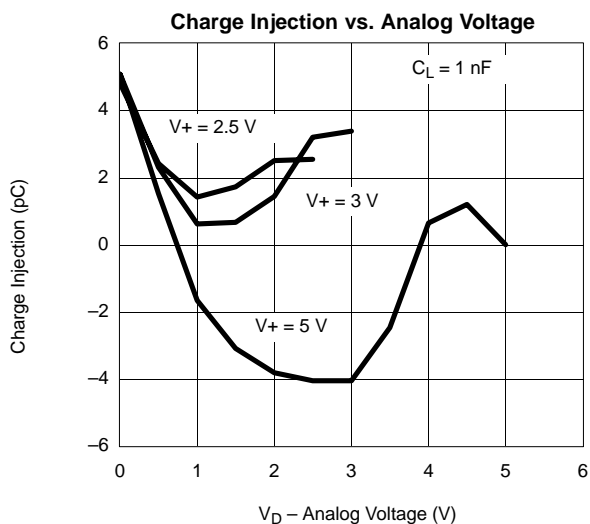
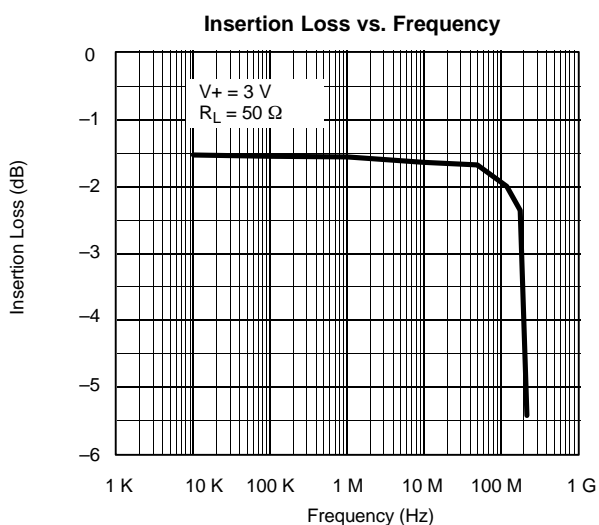
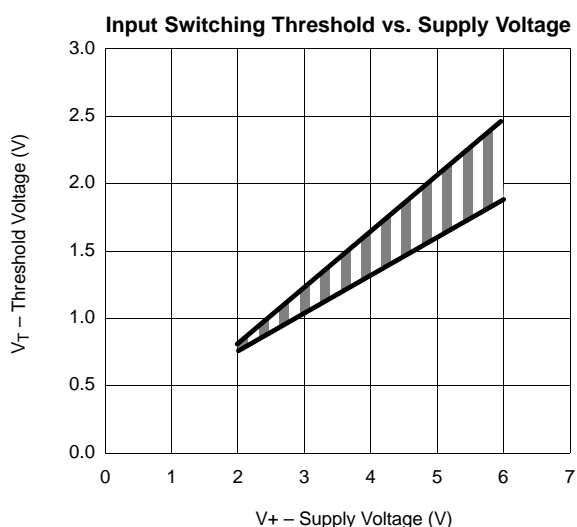
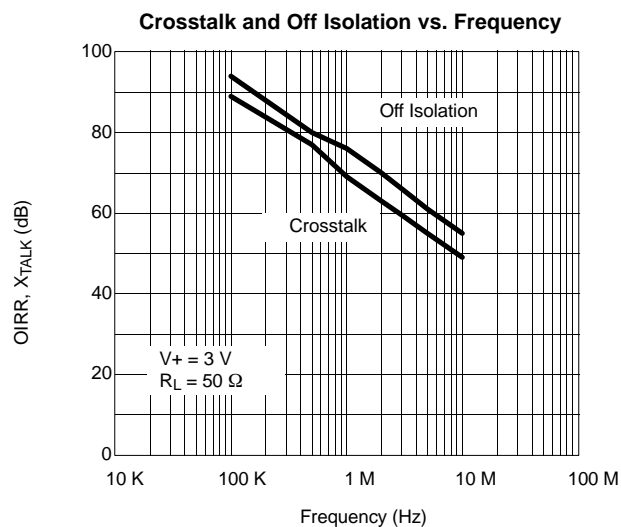
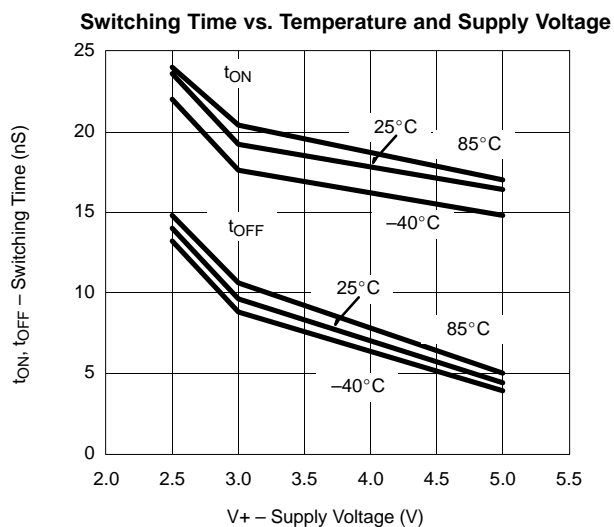


Leakage vs. Analog Voltage

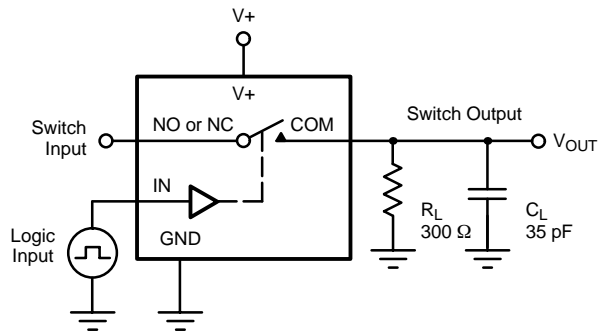




TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

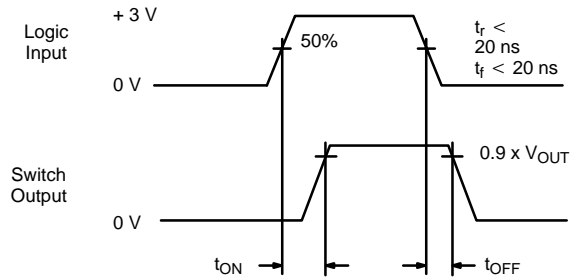


TEST CIRCUITS



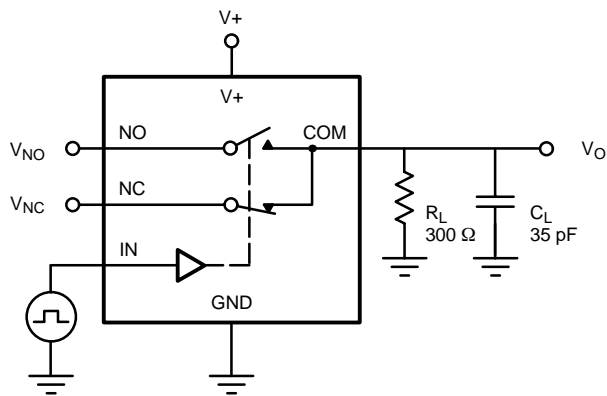
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

FIGURE 1. Switching Time



C_L (includes fixture and stray capacitance)

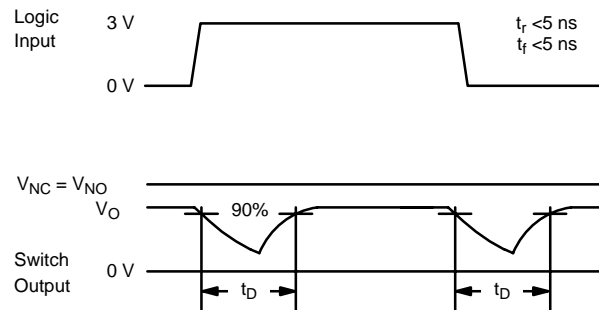
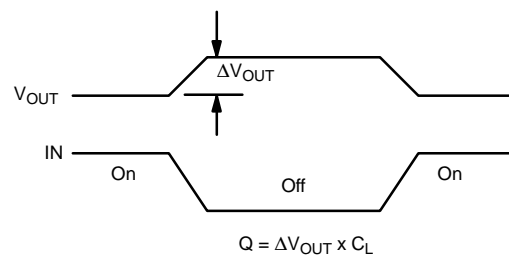
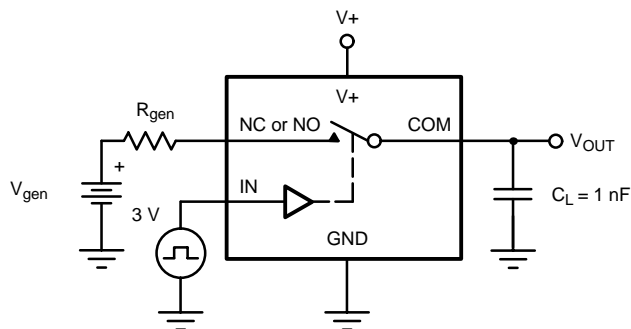


FIGURE 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 3. Charge Injection

TEST CIRCUITS

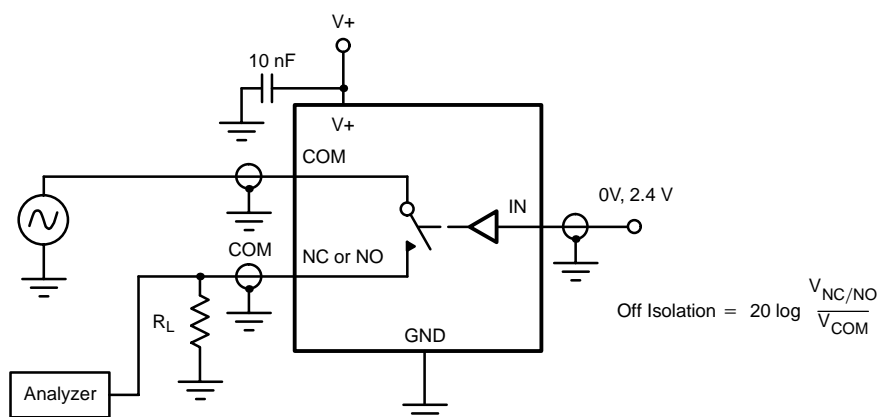


FIGURE 4. Off-Isolation

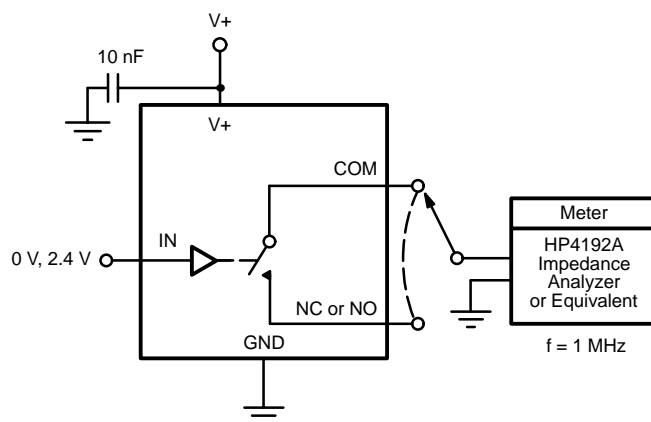


FIGURE 5. Channel Off/On Capacitance