

# DATA SHEET



## **SAA5264; SAA5265** 10 and 1 page intelligent teletext decoders

Preliminary specification  
Supersedes data of 1999 Oct 05  
File under Integrated Circuits, IC02

2000 Jan 27

## 10 and 1 page intelligent teletext decoders

## SAA5264; SAA5265

### FEATURES

The following features apply to both SAA5264 and SAA5265:

- Complete 625 line teletext decoder in one chip reduces printed circuit board area and cost
- Automatic detection of transmitted fasttext links or service information (packet 8/30)
- On-Screen Display (OSD) for user interface menus using teletext and dedicated menu icons
- Video Programming System (VPS) decoding
- Wide Screen Signalling (WSS) decoding
- Pan-European, Cyrillic, Greek/Turkish and French/Arabic character sets in each chip
- High-level command interface via I<sup>2</sup>C-bus gives easy control with a low software overhead
- High-level command interface is backward compatible to Stand-Alone Fasttext And Remote Interface (SAFARI)
- 625 and 525 line display
- RGB interface to standard colour decoder ICs, current source
- Versatile 8-bit open-drain Input/Output (I/O) expander, 5 V tolerant
- Single 12 MHz crystal oscillator
- 3.3 V supply voltage.

### SAA5264 features

- Automatic detection of transmitted pages to be selected by page up and page down
- 8 Page fasttext decoder
- Table Of Pages (TOP) decoder with Basic Top Table (BTT) and Additional Information Tables (AITs)
- 4 Page user-defined list mode.



### GENERAL DESCRIPTION

The SAA5264 is a single-chip ten page 625-line World System Teletext decoder with a high-level command interface, and is SAFARI compatible.

The SAA5265 is a single-chip one page version of the SAA5264.

Both devices are designed to minimize the overall system cost, due to the high-level command interface offering the benefit of a low software overhead in the TV microcontroller.

The SAA5264 has the following functionality:

- 10 page teletext decoder with OSD, Fasttext, TOP, default and list acquisition modes
- Automatic channel installation support
- Closed caption acquisition and display
- Violence Chip (VChip) support.

The SAA5265 has the following functionality:

- 1 Page teletext decoder with OSD, fasttext and default acquisition modes
- Automatic channel installation support
- Closed caption acquisition and display
- VChip support
- No EEPROM fitted (there is no list mode feature).

## 10 and 1 page intelligent teletext decoders

## SAA5264; SAA5265

## ORDERING INFORMATION

TYPE NUMBER <sup>(1)</sup>	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA5264PS/M3/nnnn	SDIP52	plastic shrink dual-in-line package; 52 leads (600 mil)	SOT247-1
SAA5265PS/M4/nnnn	SDIP52	plastic shrink dual-in-line package; 52 leads (600 mil)	SOT247-1

**Note**

1. 'nnnn' is a unique four digit number denoting the software version.

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DDX}$	all supply voltages	referenced to $V_{SS}$	3.0	3.3	3.6	V
$I_{DDP}$	periphery supply current	note 1	1	–	–	mA
$I_{DDC}$	core supply current	normal mode	–	15	18	mA
		idle mode	–	4.6	6	mA
$I_{DDA}$	analog supply current	normal mode	–	45	48	mA
		idle mode	–	0.87	1	mA
$f_{xtal(nom)}$	nominal crystal frequency	fundamental mode	–	12	–	MHz
$T_{amb}$	ambient temperature		–20	–	+70	°C
$T_{stg}$	storage temperature		–55	–	+125	°C

**Note**

1. Periphery supply current is dependent on external components and I/O voltage levels.

10 and 1 page intelligent teletext decoders

SAA5264; SAA5265

**BLOCK DIAGRAM**

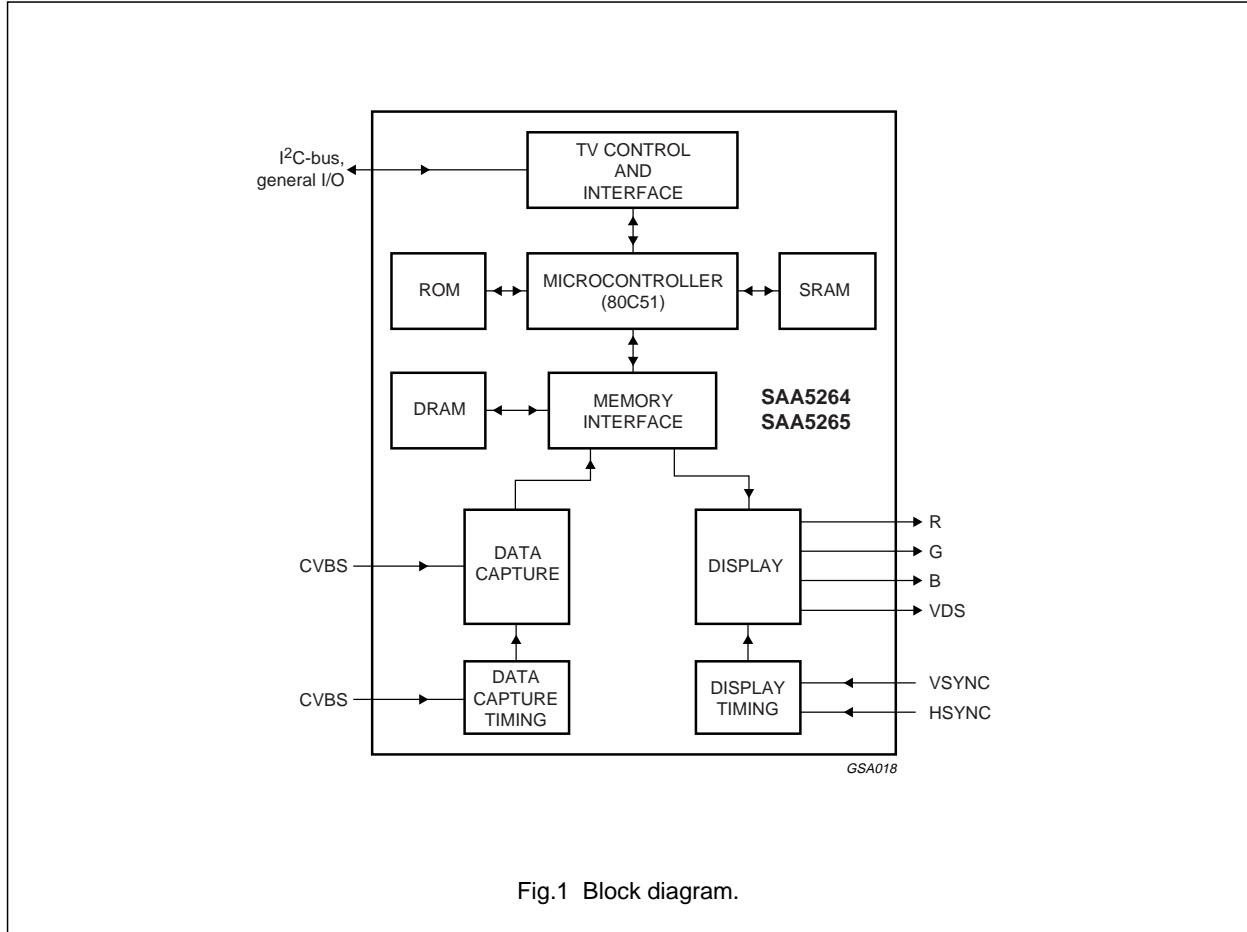


Fig.1 Block diagram.

## 10 and 1 page intelligent teletext decoders

## SAA5264; SAA5265

## PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
<b>Port 2: 8-bit programmable bidirectional port with alternative functions</b>			
P2.0/PWM	1	I/O	output for 14-bit high precision Pulse Width Modulator (PWM)
P2.1/PWM0	2	I/O	outputs for 6-bit PWMs 0 to 6
P2.2/PWM1	3	I/O	
P2.3/PWM2	4	I/O	
P2.4/PWM3	5	I/O	
P2.5/PWM4	6	I/O	
P2.6/PWM5	7	I/O	
P2.7/PWM6	8	I/O	
<b>Port 3: 8-bit programmable bidirectional port with alternative functions</b>			
P3.0/ADC0	9	I/O	inputs for the software Analog-to-Digital-Converter (ADC) facility
P3.1/ADC1	10	I/O	
P3.2/ADC2	11	I/O	
P3.3/ADC3	12	I/O	
P3.4/PWM7	30	I/O	output for 6-bit PWM7
V <sub>SSC</sub>	13	–	core ground
<b>Port 0: 8-bit programmable bidirectional port</b>			
SCL(NVRAM)	14	I	I <sup>2</sup> C-bus Serial Clock input to Non-Volatile RAM
SDA(NVRAM)	15	I/O	I <sup>2</sup> C-bus Serial Data input/output (Non-Volatile RAM)
P0.2	16	I/O	input/output for general use
P0.3	17	I/O	input/output for general use
P0.4	18	I/O	input/output for general use
P0.5	19	I/O	8 mA current sinking capability for direct drive of Light Emitting Diodes (LEDs)
P0.6	20	I/O	
P0.7	21	I/O	input/output for general use
V <sub>SSA</sub>	22	–	analog ground
CVBS0	23	I	Composite Video Baseband Signal (CVBS) input; a positive-going 1 V (peak-to-peak) input is required; connected via a 100 nF capacitor
CVBS1	24	I	
SYNC_FILTER	25	I	sync-pulse-filter input for CVBS; this pin should be connected to V <sub>SSA</sub> via a 100 nF capacitor
IREF	26	I	reference current input for analog circuits; for correct operation a 24 kΩ resistor should be connected to V <sub>SSA</sub>
FRAME	27	O	Frame de-interlace output synchronized with the VSYNC pulse to produce a non-interlaced display by adjustment of the vertical deflection circuits
TEST	28	I	not available; connect this pin to V <sub>SSA</sub>
COR	29	O	contrast reduction: open-drain, active LOW output which allows selective contrast reduction of the TV picture to enhance a mixed mode display
	30	I/O	P3.4/PWM7 (described above)
V <sub>DDA</sub>	31	–	analog supply voltage (3.3 V)
B	32	O	Blue colour information pixel rate output

## 10 and 1 page intelligent teletext decoders

## SAA5264; SAA5265

SYMBOL	PIN	TYPE	DESCRIPTION
G	33	O	Green colour information pixel rate output
R	34	O	Red colour information pixel rate output
VDS	35	O	video/data switch push-pull output for pixel rate fast blanking
HSYNC	36	I	horizontal sync pulse input; Schmitt triggered for a Transistor Transistor Level (TTL) version; the polarity of this pulse is programmable by register bit TXT1.H POLARITY
VSNC	37	I	vertical sync pulse input; Schmitt triggered for a TTL version; the polarity of this pulse is programmable by register bit TXT1.V POLARITY
V <sub>SSP</sub>	38	–	periphery ground
V <sub>DDC</sub>	39	–	core supply voltage (+3.3 V)
OSCGND	40	–	crystal oscillator ground
XTALIN	41	I	12 MHz crystal oscillator input
XTALOUT	42	O	12 MHz crystal oscillator output
RESET	43	I	reset input; if this pin is HIGH for at least 2 machine cycles (24 oscillator periods) while the oscillator is running, the device resets; this pin should be connected to V <sub>DDP</sub> via a capacitor
V <sub>DDP</sub>	44	–	periphery supply voltage (+3.3 V)
<b>Port 1: 8-bit programmable bidirectional port</b>			
P1.0	45	I/O	input/output for general use
P1.1	46	I/O	input/output for general use
P1.2	47	I/O	input/output for general use
P1.3	48	I/O	input/output for general use
SCL	49	I	I <sup>2</sup> C-bus Serial Clock input from application
SDA	50	I/O	I <sup>2</sup> C-bus Serial Data input/output (application)
P1.4	51	I/O	input/output for general use
P1.5	52	I/O	input/output for general use

10 and 1 page intelligent teletext decoders

SAA5264; SAA5265

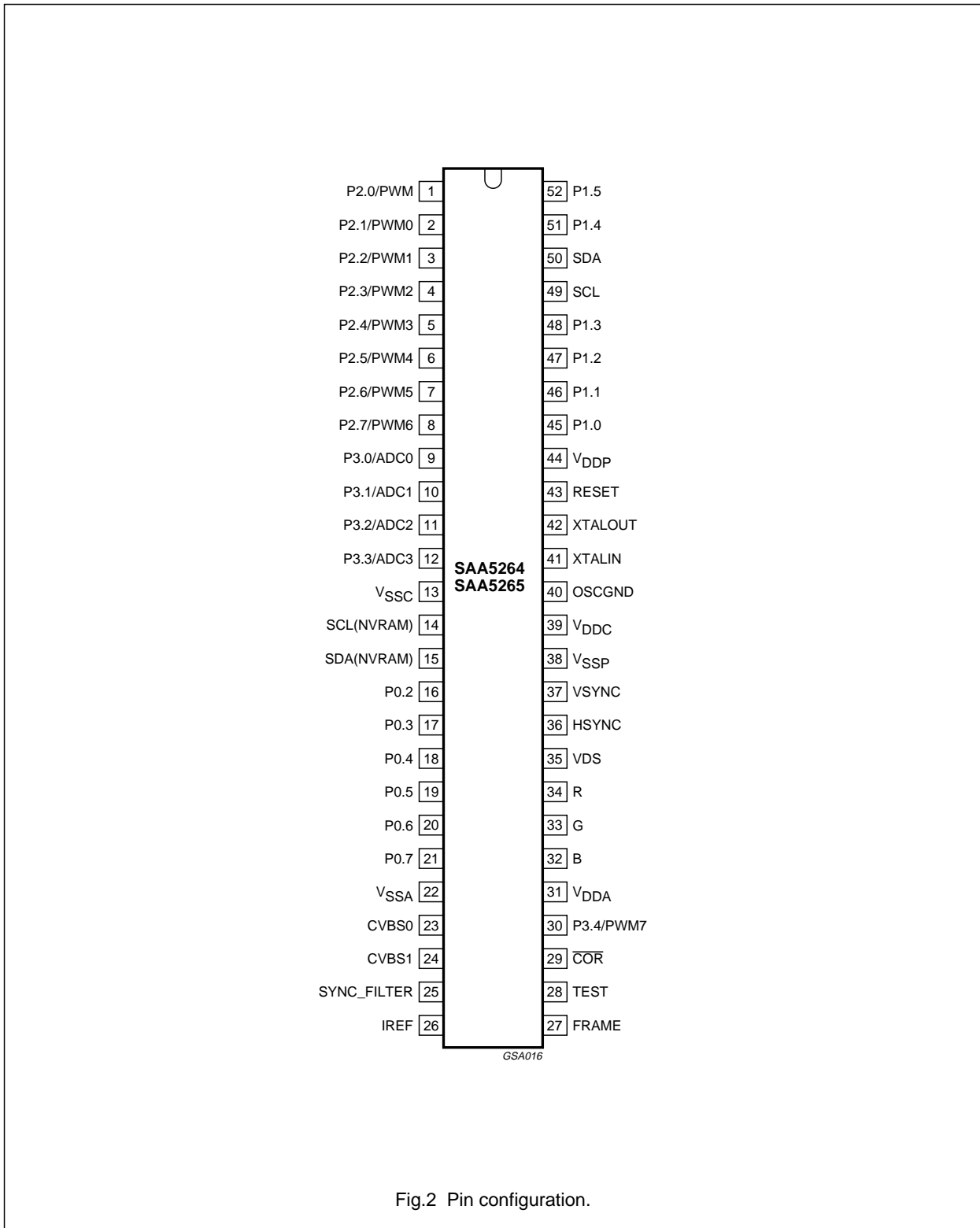


Fig.2 Pin configuration.

## 10 and 1 page intelligent teletext decoders

## SAA5264; SAA5265

**HIGH LEVEL COMMAND INTERFACE**

The I<sup>2</sup>C-bus interface is used to pass control commands and data between the SAA5264/SAA5265 and the television microcontroller. The interface uses high-level commands, which are backward compatible with the SAFARI.

The I<sup>2</sup>C-bus transmission formats are:

**Table 1** User command

START	I <sup>2</sup> C-BUS ADDRESS	WRITE	ACK	COMMAND	ACK	STOP
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**Table 2** System command

START	I <sup>2</sup> C-BUS ADDRESS	WRITE	ACK	COMMAND	ACK	PARAMETER	ACK	STOP
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**Table 3** User read

START	I <sup>2</sup> C-BUS ADDRESS	READ	ACK	DATA	ACK	STOP
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**CHARACTER SETS**

The following standard character sets are included in the SAA5264 and in the SAA5265:

Set 0 = Pan-European

Set 1 = Cyrillic

Set 2 = Greek/Turkish

Set 3 = French/Arabic

If you require any other character sets, please discuss them with your local Regional Sales Office first.

**LIMITING VALUES**

In accordance with Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>DDX</sub>	all supply voltages		-0.5	+4.0	V
V <sub>I</sub>	input voltage (any input)	note 1	-0.5	V <sub>DD</sub> + 0.5 or +4.1	V
V <sub>O</sub>	output voltage (any output)	note 1	-0.5	V <sub>DD</sub> + 0.5	V
I <sub>O</sub>	output current (each output)		-	10	mA
I <sub>IO(d)</sub>	diode DC input or output current		-	20	mA
T <sub>amb</sub>	ambient temperature		-20	+70	°C
T <sub>stg</sub>	storage temperature		-55	+125	°C

**Note**

1. This maximum value refers to 5 V tolerant I/Os and may be 6 V maximum but only when V<sub>DD</sub> is present.



## 10 and 1 page intelligent teletext decoders

## SAA5264; SAA5265

**CHARACTERISTICS**

$V_{DD} = 3.3 \text{ V} \pm 10\%$ ;  $V_{SS} = 0 \text{ V}$ ;  $T_{amb} = -20 \text{ to } +70 \text{ }^\circ\text{C}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
$V_{DDX}$	all supply voltages	referenced to $V_{SS}$	3.0	3.3	3.6	V
$I_{DDP}$	periphery supply current	note 1	1	–	–	mA
$I_{DDC}$	core supply current	normal mode	–	15	18	mA
$I_{DDC(idle)}$	idle mode core supply current		–	4.6	6	mA
$I_{DDA}$	analog supply current		–	45	48	mA
$I_{DDA(idle)}$	idle mode analog supply current	normal mode	–	0.87	1	mA
<b>Digital inputs</b>						
RESET (PIN 43)						
$V_{IL}$	LOW-level input voltage		–	–	1.00	V
$V_{IH}$	HIGH-level input voltage		1.85	–	–	V
$V_{hys}$	Schmitt trigger input hysteresis voltage		0.44	–	0.58	V
$I_{LI}$	input leakage current	$V_I = 0$	–	–	0.17	$\mu\text{A}$
$R_{pd(eq)}$	equivalent pull-down resistance	$V_I = V_{DD}$	55.73	70.71	92.45	$\text{k}\Omega$
HSYNC, VSYNC (PINS 36 AND 37)						
$V_{IL}$	LOW-level input voltage		–	–	0.96	V
$V_{IH}$	HIGH-level input voltage		1.80	–	–	V
$V_{hys}$	Schmitt trigger input hysteresis voltage		0.40	–	0.56	V
$I_{LI}$	Input leakage current	$V_I = 0 \text{ to } V_{DD}$	–	–	0.00	$\mu\text{A}$
<b>Digital outputs</b>						
FRAME, VDS (PINS 27 AND 35)						
$V_{OL}$	LOW-level output voltage	$I_{OL} = 3 \text{ mA}$	–	–	0.13	V
$V_{OH}$	HIGH-level output voltage	$I_{OH} = 3 \text{ mA}$	2.84	–	–	V
$t_{o(r)}$	output rise time	between 10% and 90%; $C_L = 70 \text{ pF}$	7.50	8.85	10.90	ns
$t_{o(f)}$	output fall time	between 10% and 90%; $C_L = 70 \text{ pF}$	6.70	7.97	10.00	ns

## 10 and 1 page intelligent teletext decoders

## SAA5264; SAA5265

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>COR (OPEN-DRAIN OUTPUT, PIN 29)</b>						
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 3 mA	–	–	0.14	V
V <sub>OH(pu)</sub>	HIGH-level pull-up output voltage	I <sub>OL</sub> = –3 mA; push-pull	2.84	–	–	V
V <sub>IL</sub>	LOW-level input voltage		–	–	0.00	V
V <sub>IH</sub>	HIGH-level input voltage		0.00	–	5.50	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 0 to V <sub>DD</sub>	–	–	0.12	μA
t <sub>o(r)</sub>	output rise time	between 10% and 90%; C <sub>L</sub> = 70 pF	7.20	8.64	11.10	ns
t <sub>o(f)</sub>	output fall time	between 10% and 90%; C <sub>L</sub> = 70 pF	4.90	7.34	9.40	ns
<b>Digital input/outputs</b>						
SCL(NVRAM), SDA(NVRAM), P0.4, P0.7, P1.0, P1.1, P2.1 TO P2.7, P3.0 TO P3.4 (PINS 14, 15, 18, 21, 45, 46, 2 TO 12, 30)						
V <sub>IL</sub>	LOW-level input voltage		–	–	0.98	V
V <sub>IH</sub>	HIGH-level input voltage		1.78	–	–	V
V <sub>hys</sub>	Schmitt trigger input hysteresis voltage		0.41	–	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 0 to V <sub>DD</sub>	–	–	0.01	μA
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 4 mA	–	–	0.18	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = –4 mA push-pull	2.81	–	–	V
t <sub>o(r)</sub>	output rise time	between 10% and 90%; C <sub>L</sub> = 70 pF push-pull	6.50	8.47	10.70	ns
t <sub>o(f)</sub>	output fall time	between 10% and 90%; C <sub>L</sub> = 70 pF	5.70	7.56	10.00	ns
<b>P1.2, P1.3, P2.0 (PINS 47, 48, 1)</b>						
V <sub>IL</sub>	LOW-level input voltage		–	–	0.99	V
V <sub>IH</sub>	HIGH-level input voltage		1.80	–	–	V
V <sub>hys</sub>	Schmitt trigger input hysteresis voltage		0.42	–	0.56	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 0 to V <sub>DD</sub>	–	–	0.02	μA

## 10 and 1 page intelligent teletext decoders

## SAA5264; SAA5265

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 4 mA	–	–	0.17	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = –4 mA push-pull	2.81	–	–	V
t <sub>o(r)</sub>	output rise time	between 10% and 90%; C <sub>L</sub> = 70 pF push-pull	7.00	8.47	10.50	ns
t <sub>o(f)</sub>	output fall time	between 10% and 90%; C <sub>L</sub> = 70 pF	5.40	7.36	9.30	ns
P0.5, P0.6 (PINS 19, 20)						
V <sub>IL</sub>	LOW-level input voltage		–	–	0.98	V
V <sub>IH</sub>	HIGH-level input voltage		1.82	–	–	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 0 to V <sub>DD</sub>	–	–	0.11	μA
V <sub>hys</sub>	Schmitt trigger input hysteresis voltage		0.42	–	0.58	V
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 8 mA	–	–	0.20	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = –8 mA push-pull	2.76	–	–	V
t <sub>o(r)</sub>	output rise time	between 10% and 90%; C <sub>L</sub> = 70 pF push-pull	7.40	8.22	8.80	ns
t <sub>o(f)</sub>	output fall time	between 10% and 90%; C <sub>L</sub> = 70 pF	4.20	4.57	5.20	ns
P1.4, P1.5 (OPEN-DRAIN) (PINS 51, 52)						
V <sub>IL</sub>	LOW-level input voltage		–	–	1.08	V
V <sub>IH</sub>	HIGH-level input voltage		1.99	–	–	V
V <sub>hys</sub>	Schmitt trigger input hysteresis voltage		0.49	–	0.60	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 0 to V <sub>DD</sub>	–	–	0.13	μA
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 8 mA	–	–	0.35	V
t <sub>o(f)</sub>	output fall time	between 10% and 90%; C <sub>L</sub> = 70 pF	69.70	83.67	103.30	ns

## 10 and 1 page intelligent teletext decoders

## SAA5264; SAA5265

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Analog inputs</b>						
CVBS0 AND CVBS1 (PINS 23 AND 24)						
$V_{\text{sync}}$	sync voltage amplitude		0.1	0.3	0.6	V
$V_{i(v)(p-p)}$	video input voltage (peak-to-peak value)		0.7	1.0	1.4	V
$Z_{\text{source}}$	source impedance		0	–	250	$\Omega$
$V_{\text{IH}}$	HIGH-level input voltage		3.0	–	$V_{\text{DDA}} + 0.3$	V
$C_i$	input capacitance		–	–	10	pF
IREF (PIN 26)						
$R_{\text{IREF}}$	resistance from IREF to $V_{\text{SSA}}$	resistor tolerance = 2%	–	24	–	k $\Omega$
ADC0 TO ADC3 (PINS 9 TO 12)						
$V_{\text{IH}}$	HIGH-level input voltage		–	–	$V_{\text{DDA}}$	V
$C_i$	input capacitance		–	–	10	pF
<b>Analog outputs</b>						
B, G AND R (PINS 32 TO 34)						
$I_{o(bl)}$	output current (black level)	$V_{\text{DDA}} = 3.3 \text{ V}$	–10	–	+10	$\mu\text{A}$
$I_{o(max)}$	output current (maximum intensity)	$V_{\text{DDA}} = 3.3 \text{ V}$ intensity level code = 15 (Dec)	6.0	6.67	7.3	mA
$I_{o(70\%max)}$	output current (70% of maximum intensity)	$V_{\text{DDA}} = 3.3 \text{ V}$ intensity level code = 0 (Dec)	4.2	4.7	5.1	mA
$R_L$	load resistance (to $V_{\text{SSA}}$ )	resistor tolerance = 5%	–	150	–	$\Omega$
$C_L$	load capacitance		–	–	15	pF
<b>Analog input/output</b>						
SYNC_FILTER (PIN 25)						
$C_{\text{stg}}$	storage capacitor (to $V_{\text{SSA}}$ )		–	100	–	nF
$V_{\text{sync}(nom)}$	sync filter level voltage with nominal sync amplitude		0.35	0.55	0.75	V

## 10 and 1 page intelligent teletext decoders

## SAA5264; SAA5265

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Crystal oscillator</b>						
XTALIN (PIN 41)						
V <sub>IL</sub>	LOW-level input voltage		V <sub>SSA</sub>	–	–	V
V <sub>IH</sub>	HIGH-level input voltage		–	–	V <sub>DDA</sub>	V
C <sub>i</sub>	input capacitance		–	–	10	pF
XTALOUT (PIN 42)						
C <sub>o</sub>	output capacitance		–	–	10	pF
<b>Crystal specification; notes 2 and 3</b>						
f <sub>xtal(nom)</sub>	nominal frequency	fundamental mode	–	12	–	MHz
C <sub>L</sub>	load capacitance		–	–	30	pF
C <sub>mot</sub>	motional capacitance	T <sub>amb</sub> = 25 °C	–	–	20	fF
R <sub>xtal</sub>	crystal resonance resistance	T <sub>amb</sub> = 25 °C	–	–	60	Ω
C <sub>osc</sub>	capacitance at XTALIN, XTALOUT	T <sub>amb</sub> = 25 °C	–	2C <sub>L</sub> – C <sub>chip</sub> – C <sub>stray</sub>	–	pF
C <sub>xtal(hold)</sub>	crystal holder capacitance	T <sub>amb</sub> = 25 °C	–	–	$35 - \frac{C_{osc}}{2} - \frac{C_{chip}}{2} - \frac{C_{stray}}{2}$	pF
T <sub>xtal</sub>	crystal temperature range		–20	+25	+85	°C
X <sub>j</sub>	adjustment tolerance	T <sub>amb</sub> = 25 °C	–	–	±50 × 10 <sup>–6</sup>	
X <sub>d</sub>	drift		–	–	±100 × 10 <sup>–6</sup>	

**Notes**

1. Periphery supply current is dependent on I/O external components and voltage levels.
2. Crystal order number 4322 143 05561. If crystal 4322 143 05561 is not used, then the formulae in the crystal specification should be used.
3. C<sub>osc</sub> may need to be reduced from the initially selected value. C<sub>chip</sub> = 7 pF, the mean of the capacitances due to the chip at XTALIN and at XTALOUT. C<sub>stray</sub> is a value for the mean of the stray capacitances due to the external circuit at XTALIN and XTALOUT. The maximum value for C<sub>xtal(hold)</sub> is to ensure start-up.

## 10 and 1 page intelligent teletext decoders

## SAA5264; SAA5265

**I<sup>2</sup>C-BUS CHARACTERISTICS**

SYMBOL	PARAMETER	FAST-MODE I <sup>2</sup> C-bus		UNIT
		MIN.	MAX.	
f <sub>SCL</sub>	SCL clock frequency	0	400	kHz
t <sub>BUF</sub>	bus free time between a STOP and START condition	1.3	–	μs
t <sub>HD;STA</sub>	hold time START condition; after this period, the first clock pulse is generated	0.6	–	μs
t <sub>LOW</sub>	SCL LOW time	1.3	–	μs
t <sub>HIGH</sub>	SCL HIGH time	0.6	–	μs
t <sub>SU;STA</sub>	set-up time repeated START	0.6	–	μs
t <sub>HD;DAT</sub>	data hold time; notes 1 and 2	0	0.9	μs
t <sub>SU;DAT</sub>	data set-up time; note 3	100	–	ns
t <sub>r</sub>	rise time SDA and SCL; note 4	20	300	ns
t <sub>f</sub>	fall time SDA and SCL; note 4	20	300	ns
t <sub>SU;STO</sub>	set-up time STOP condition	0.6	–	μs
C <sub>b</sub>	capacitive load of each bus line	–	400	pF

**Notes**

1. A device must internally provide a hold time of at least 300 ns for the SDA signal (referenced to the V<sub>IHmin</sub> of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
2. The maximum t<sub>HD;DAT</sub> has only to be met if the device does not stretch the LOW period of the SCL signal (t<sub>LOW(SCL)</sub>).
3. A fast-mode I<sup>2</sup>C-bus device can be used in a standard-mode I<sup>2</sup>C-bus system, but the requirement t<sub>SU;DAT</sub> ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch t<sub>LOW(SCL)</sub>. If such a device does stretch t<sub>LOW(SCL)</sub>, it must output the next data bit to the SDA line t<sub>r(max)</sub> + t<sub>SU;DAT</sub> = 1 000 + 250 = 1 250 ns (according to the standard-mode I<sup>2</sup>C-bus specification) before the SCL line is released.
4. C<sub>b</sub> = total capacitance of one bus line in pF.

## 10 and 1 page intelligent teletext decoders

## SAA5264; SAA5265

**EMC GUIDELINES**

Optimization of circuit return paths and minimization of common mode emission will be assisted by using a double sided Printed Circuit Board (PCB) with low inductance ground plane.

On a single-sided PCB a local ground plane under the whole IC should be present as shown in Fig.3. This should have the widest possible connection between the PCB ground and bulk electrolytic decoupling capacitor. Preferably, the PCB local ground plane connection should not be connected to other grounds on route to the PCB ground. Do not use wire links. Wire links cause ground inductance which increases ground bounce.

The supply pins can be decoupled at the ground pin plane below the IC. This is easily achieved by using surface mount capacitors, which, at high frequency, are more effective than components with leads.

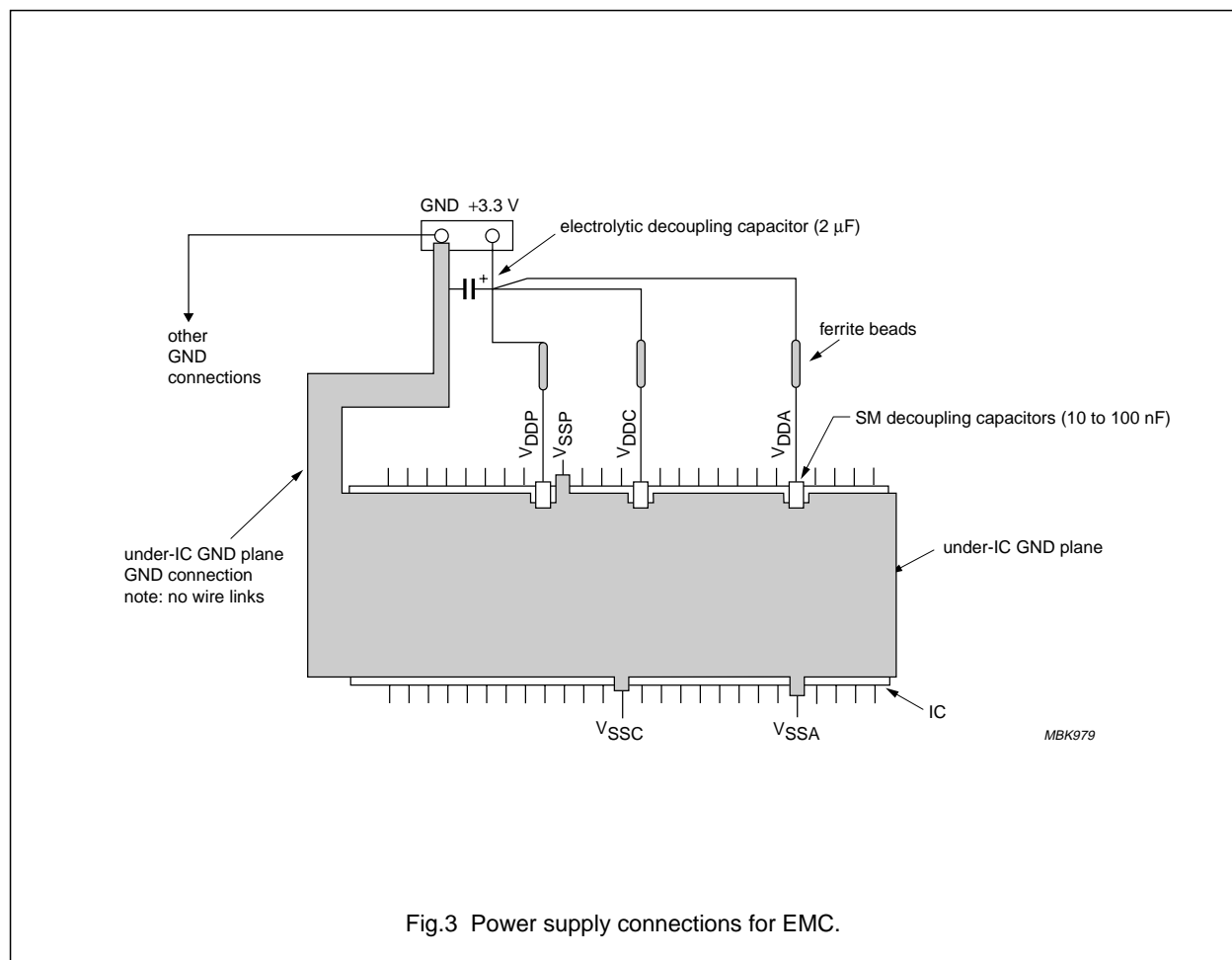
Using a device socket would increase the area and therefore increase the inductance of the external bypass loop.

To provide a high-impedance to any high frequency signals on the  $V_{DD}$  supplies to the IC, a ferrite bead or inductor can be connected in series with the supply line close to the decoupling capacitor. To prevent signal radiation, pull-up resistors of signal outputs should not be connected to the  $V_{DD}$  supply on the IC side of the ferrite bead or inductor.

OSCGND should only be connected to the crystal load capacitors and not to any other ground connection.

Distances to physical connections of associated active devices should be as short as possible.

PCB output tracks should have close proximity, mutually coupled, ground return paths.



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## SAA5264; SAA5265

**QUALITY AND RELIABILITY**

This device will meet Philips Semiconductors general quality specification for business group "Consumer Integrated Circuits SNW-FQ-611-Part E". The principal requirements are shown in Tables 4 to 7.

**Group A****Table 4** Acceptance tests per lot; note 1

TEST	REQUIREMENTS
Mechanical	cumulative target: <80 ppm
Electrical	cumulative target: <100 ppm

**Note**

1. ppm = fraction of defective devices, in parts per million.

**Group B****Table 5** Processability tests (by package family)

TEST	REQUIREMENTS
Solderability	0/16 on all lots
Mechanical	0/15 on all lots
Solder heat resistance	0/15 on all lots

**Group C****Table 6** Reliability tests (by package family); note 1

TEST	CONDITIONS	REQUIREMENTS
Operational life	168 hours at $T_j = 150\text{ }^\circ\text{C}$	<1000 FPM at $T_j = 150\text{ }^\circ\text{C}$
Humidity life	temperature, humidity, bias 1000 hours; $T_{\text{amb}} = 85\text{ }^\circ\text{C}$ , 85% RH (or equivalent test)	<2000 FPM
Temperature cycling performance	$T_{\text{stg}(\text{min})}$ to $T_{\text{stg}(\text{max})}$	<2000 FPM

**Note**

1. FPM = fraction of devices failing at test condition, in Failures Per Million.

**Table 7** Reliability tests (by device type)

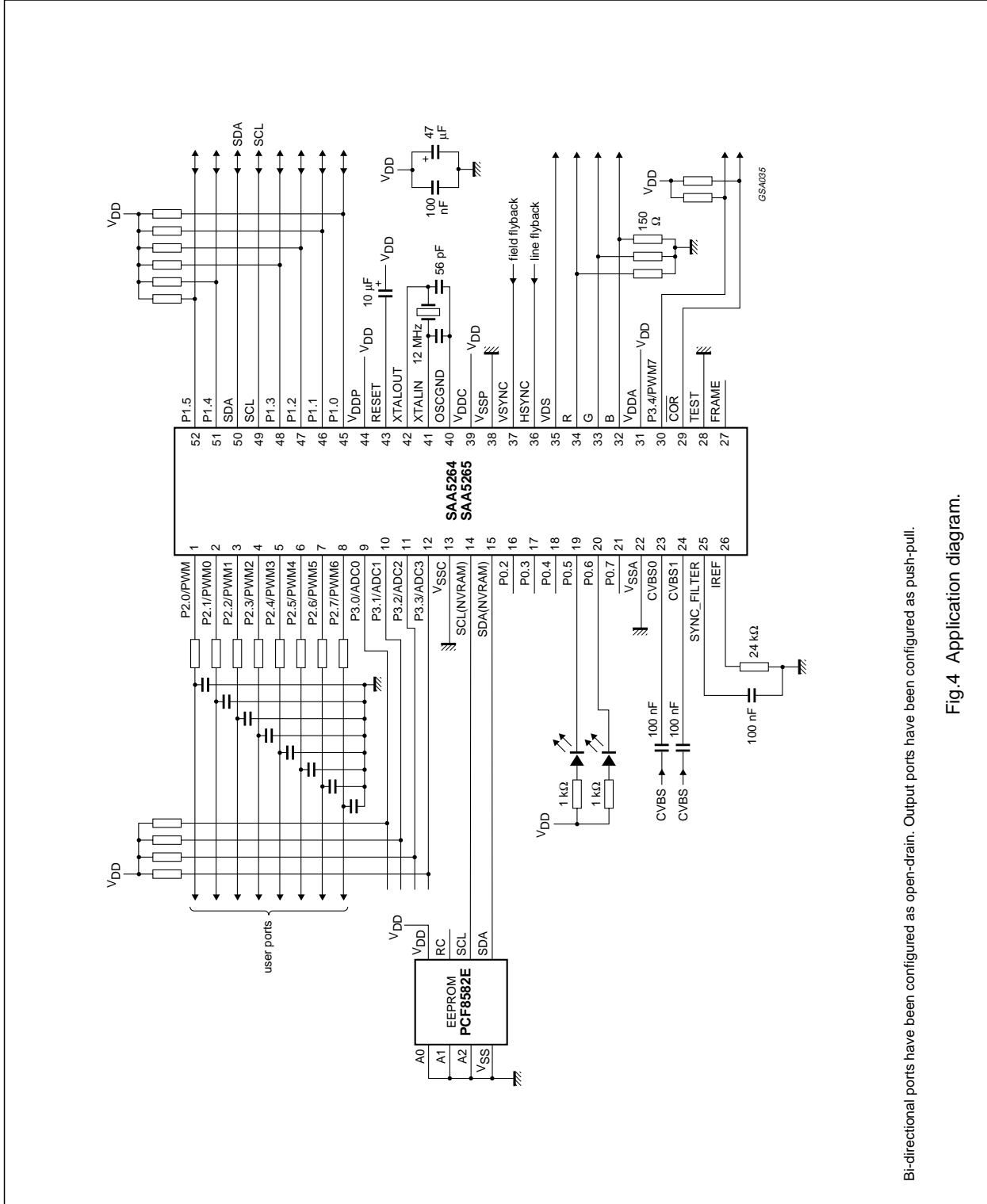
TEST	CONDITIONS	REQUIREMENTS
ESD and latch-up	ESD Human body model 100 pF, 1.5 k $\Omega$	2000 V
	ESD Machine model 200 pF, 0 $\Omega$	200 V
	latch-up	100 mA, $1.5 \times V_{\text{DD}}$ (absolute maximum)



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SAA5264; SAA5265

APPLICATION INFORMATION



Bi-directional ports have been configured as open-drain. Output ports have been configured as push-pull.

Fig.4 Application diagram.

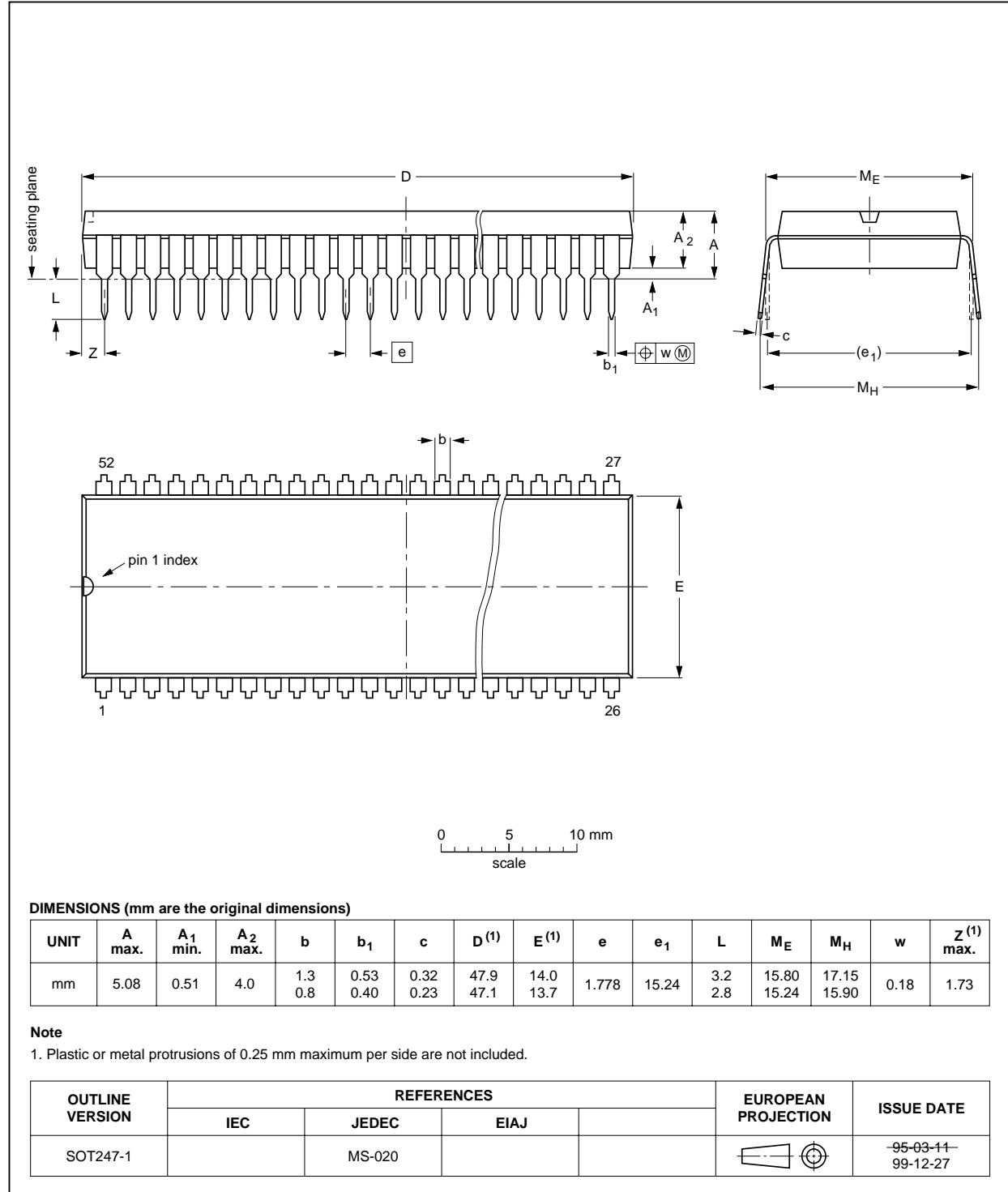
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SAA5264; SAA5265

PACKAGE OUTLINE

SDIP52: plastic shrink dual in-line package; 52 leads (600 mil)

SOT247-1



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## SAA5264; SAA5265

**SOLDERING****Introduction to soldering through-hole mount packages**

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

**Soldering by dipping or by solder wave**

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg(max)}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**Manual soldering**

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

**Suitability of through-hole mount IC packages for dipping and wave soldering methods**

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable <sup>(1)</sup>

**Note**

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

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SAA5264; SAA5265

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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**NOTES**

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**NOTES**

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