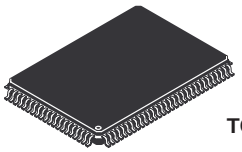
MCM69C233
SCM69C233

4K x 64 CAM



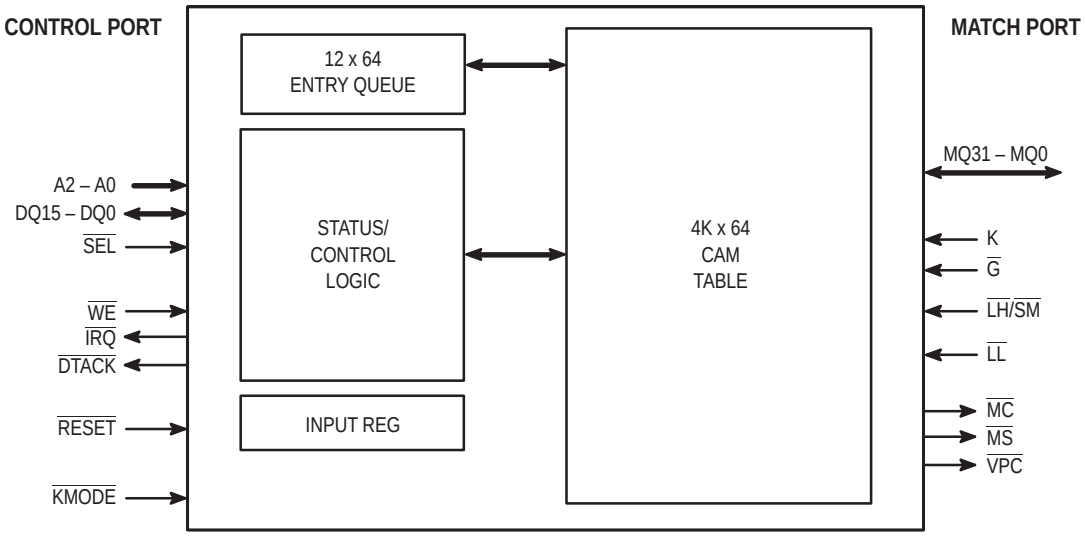
TQ PACKAGE
TQFP
CASE 983A–01

The MCM69C233 is a flexible content–addressable memory (CAM) that can contain 4096 entries of 64 bits each. The widths of the match field and the output field are programmable, and the match time is designed to be 210 ns. As a result, the MCM69C233 is well suited for datacom applications such as Virtual Path Identifier/Virtual Circuit Identifier (VPI/VCI) translation in ATM switches up to OC12 (622 Mbps) data rates and Media Access Control (MAC) address lookup in Ethernet/Fast Ethernet bridges. The match duty cycle of the MCM69C233 is user defined, with a trade–off between the time between the match request rate and the rate of new entries added to the CAM.

- 4096 Entries
- 210 ns Match Time
- Mask Register to “Don’t Care” Selected Bits
- Depth Expansion by Cascading Multiple Devices
- 66 MHz Maximum Clock Rate
- Programmable Match and Output Field Widths
- Concurrent Matching of Virtual Path Circuits and Virtual Connection Circuits in ATM Mode
- Separate Ports for Control and Match Operations
- 300 ns Insertion Time if 1 of 12 Entry Queue Locations is Empty
- 18 ms Initialization Time After Fast Insertion (at Power–Up Only)
- Single 3.3 V ±5% Supply
- IEEE Standard 1149.1 Test Port (JTAG)
- 100–Pin TQFP Package

Related Products

— MCM69C432, MCM69C232, MCM69C433 (CAMs)



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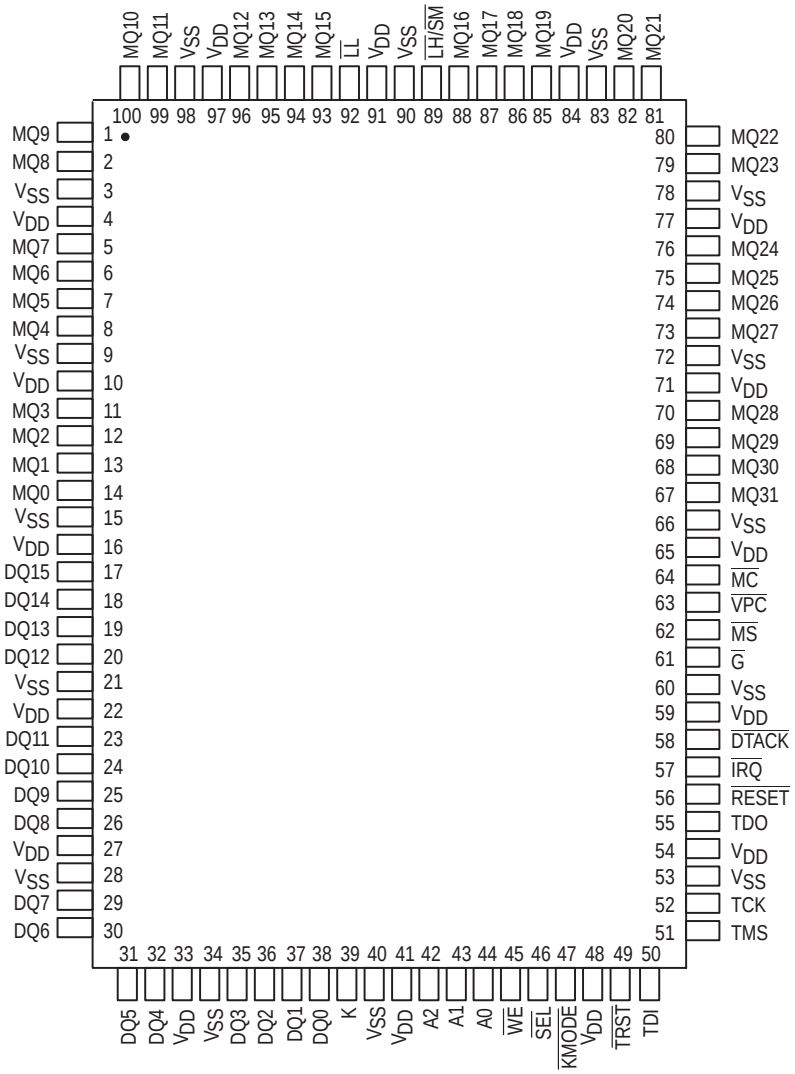
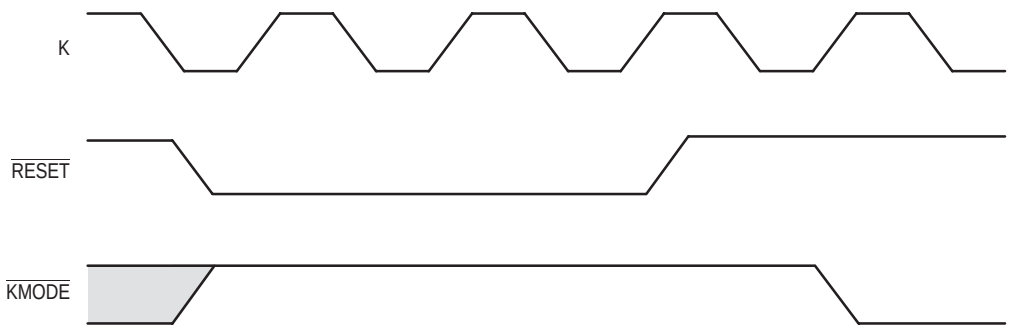
PIN ASSIGNMENT



PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
42 – 44	A2 – A0	Input	3–bit control port address bus.
58	$\overline{\text{DTACK}}$	Output	Control port data transfer acknowledge (Open Drain).
17 – 20, 23 – 26, 29 – 32, 35 – 38	DQ15 – DQ0	I/O	16–bit bidirectional control port data bus.
61	$\overline{\text{G}}$	Input	Asynchronous Output Enable control of MQ31 – MQ0.
57	$\overline{\text{IRQ}}$	Output	Control Port Interrupt (Open Drain).
39	K	Input	Interface Clock, max frequency of 66 MHz.
47	$\overline{\text{KMODE}}$	Input	See Note.
89	$\overline{\text{LH}}/\overline{\text{SM}}$	Input	Latch High/Start Match. Initiates match sequence on match data present on MQ31 – MQ0.
92	$\overline{\text{LL}}$	Input	Latch Low. Latches low order bits if match width is > 32 bits.
64	$\overline{\text{MC}}$	Output	Match Complete (Open Drain).
62	$\overline{\text{MS}}$	Output	Match Successful (Open Drain).
67 – 70, 73 – 76, 79 – 82, 85 – 88, 93 – 96, 99, 100, 1, 2, 5 – 8, 11 – 14	MQ31 – MQ0	I/O	32–bit common I/O CAM data. Used for input of match RAM and data RAM values.
56	$\overline{\text{RESET}}$	Input	Resets chip to a known state.
46	$\overline{\text{SEL}}$	Input	Control Port Chip Select, active low.
52	TCK	Input	Test Clock, part of JTAG interface.
50	TDI	Input	Test Data In, part of JTAG interface.
55	TDO	Output	Test Data Out, part of JTAG interface.
51	TMS	Input	Test Mode Select, part of JTAG interface.
49	$\overline{\text{TRST}}$	Input	TAP Reset part of JTAG interface.
63	$\overline{\text{VPC}}$	Output	Virtual Path Circuit. Used in ATM mode to indicate a virtual path circuit match has occurred (Open Drain).
45	$\overline{\text{WE}}$	Input	Control Port Write Enable.
4, 10, 16, 22, 27, 33, 41, 48, 54, 59, 65, 71, 77, 84, 91, 97	V_{DD}	Supply	Power Supply: 3.3 V ±5%.
3, 9, 15, 21, 28, 34, 40, 53, 60, 66, 72, 78, 83, 90, 98	V_{SS}	Supply	Ground.

NOTE: Assert $\overline{\text{KMODE}}$ 1 clock cycle after $\overline{\text{RESET}}$ is deasserted.



ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Supply Voltage (see Note 2)	V_{DD}	4.6	V
Voltage Relative to V_{SS} (see Note 2)	V_{in}	–0.5 to V_{DD} + 3 V	V
Output Current per Pin	I_{out}	±20	mA
Package Power Dissipation (see Note 3)	P_D	—	W
Temperature Under Bias (see Note 3) Commercial Industrial	T_{bias}	 –10 to 85 –40 to 85	°C
Operating Temperature (see Note 4) Commercial Industrial	T_A	 0 to 70 –40 to 85	°C
Storage Temperature	T_{stg}	–55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. All voltages are referenced to V_{SS}.
3. Power dissipation capability will be dependent upon package characteristics and use environment. See Package Thermal Characteristics.
4. Consult Junction to Ambient Thermal Characteristics table for details and conditions.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ±5%, T_J < 120°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	3.1	3.3	3.5	V
Operating Temperature (Junction)	T_J	—	—	120	°C
Input Low Voltage	V_{IL}	–0.5*	0	0.8	V
Input High Voltage	V_{IH}	2.0	3	5.5	V

* V_{IL} (min) = –3.0 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Active Power Supply Current	I_{DDA}	—	200	mA
Input Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg}(I)$	—	±1	µA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{DD})	$I_{lkg}(O)$	—	±1	µA
Output Low Voltage (I_{OL} = 8 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = –4 mA)	V_{OH}	2.4	—	V

PACKAGE THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance Junction to Ambient (200 lfpm, 4 Layer Board) (Note 2)	$R_{\theta JA}$	27.1	°C/W
Thermal Resistance Junction to Board (Bottom) (Note 3)	$R_{\theta JB}$	17	°C/W
Thermal Resistance Junction to Case (Top) (Note 4)	$R_{\theta JC}$	9	°C/W

NOTES:
1. RAM junction temperature is a function of on–chip power dissipation, package thermal impedance, mounting site temperature, and mounting site thermal impedance.
2. Per SEMI G38–87.
3. Indicates the average thermal impedance between the die and the mounting surface.
4. Indicates the average thermal impedance between the die and the case top surface. Measured via the cold plate method (MIL SPEC–883 Method 1012.1).

CAPACITANCE (Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Max	Unit
Input Capacitance	C_{in}	—	5	pF
I/O Capacitance	$C_{I/O}$	—	8	pF

JUNCTION TO AMBIENT THERMAL CHARACTERISTICS

Board	Air (LFPM)	θ_{JA} (°C/W)	Maximum Ambient Temperature (°C)
1 Layer	0	40.1	55.8
1 Layer	200	34.7	64.4
1 Layer	400	32.1	68.7
4 Layer	0	30.5	71.1
4 Layer	200	27.1	76.6
4 Layer	400	25.6	79.0

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ±5%, T_J < 120°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

Output Timing Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1 Unless Otherwise Noted

CONTROL PORT TIMINGS

(Voltages Referenced to V_{SS} = 0 V, Max's are t_{KHKH} Dependent and Listed Values are for t_{KHKH} = 15 ns)

Parameter	Symbol	Min	Max	Unit	Notes
Address Valid to $\overline{SEL}$ Low	t_{AVSL}	0	—	ns	
$\overline{DTACK}$ Low to Address Invalid	t_{DTLAX}	0	—	ns	
Data Valid to Select Low	t_{DVSL}	0	—	ns	
$\overline{DTACK}$ Low to Data Invalid	t_{DTLDX}	0	—	ns	
Output Valid to $\overline{DTACK}$ Low	t_{QVDTL}	2	—	ns	
$\overline{WE}$ Valid to Select Low	t_{WVSL}	0	—	ns	
$\overline{DTACK}$ Low to $\overline{WE}$ High	t_{DTLWH}	0	—	ns	
$\overline{WE}$ High to Output Active	t_{WHQX}	2	—	ns	
Select Low to $\overline{DTACK}$ Low	t_{SLDTL}	10	—	ns	1
Select High to $\overline{DTACK}$ High	t_{SHDTH}	10	20	ns	
$\overline{DTACK}$ Low to $\overline{IRQ}$ Low	t_{DTLIL}	10	—	ns	
$\overline{IRQ}$ Low to $\overline{IRQ}$ High	t_{ILIH}	20	—	ns	
$\overline{DTACK}$ Low to Select High	t_{DTLSH}	0	—	ns	
$\overline{DTACK}$ High to Select Low	t_{DTHSL}	0	—	ns	
Address Valid to Output Valid	t_{AVQV}	—	8	ns	
Select High to Output High Impedance	t_{SHQZ}	—	8	ns	
$\overline{RESET}$ Low to $\overline{RESET}$ High	t_{RLRH}	2 x t_{KHKH}	—	ns	

NOTE:
1. $\overline{DTACK}$ is delayed when a write is attempted during certain operations. See Functional Description.

MATCH PORT TIMINGS

(Voltages Referenced to V_{SS} = 0 V, Max's are t_{KHKH} Dependent and Listed Values are for t_{KHKH} = 15 ns)

Parameter	Symbol	Min	Max	Unit
Clock Cycle Time	t_{KHKH}	15	250	ns
Clock High Time	t_{KHKL}	6	244	ns
Clock Low Time	t_{KLKH}	6	244	ns
Clock High to $\overline{LHSM}$ or $\overline{LL}$ Low	t_{LLKH}	3	—	ns
Clock High to $\overline{LHSM}$ or $\overline{LL}$ High	t_{KHLH}	1	—	ns
MQ Input Data Setup Time to Clock High	t_{MQVKH}	8	—	ns
Clock High to Match Data Hold Time	t_{KHMQX}	2	—	ns
Clock High to MQ Valid	t_{KHMQV}	—	15	ns
Clock High to $\overline{MC}$ High	t_{KHMCH}	—	10	ns
Clock High to $\overline{MC}$ Low	t_{KHMCL}	—	7	ns
Clock High to $\overline{MS}$ Low	t_{KHMSL}	—	12	ns
Clock High to $\overline{MS}$ High	t_{KHMSH}	—	12	ns
Clock High to $\overline{VPC}$ Low	t_{KHVPL}	—	15	ns
Clock High to $\overline{VPC}$ High	t_{KHVPH}	—	12	ns
$\overline{G}$ Low to MQ Active	t_{GLMQX}	3.8	—	ns
$\overline{G}$ High to MQ High–Z	t_{GHMQZ}	—	7	ns
$\overline{LH}/\overline{SM}$ Low to $\overline{LH}/\overline{SM}$ Low	t_{SMSM}	18	—	cycles

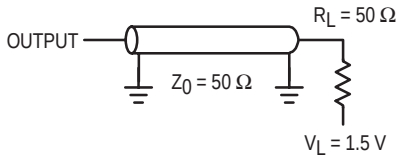
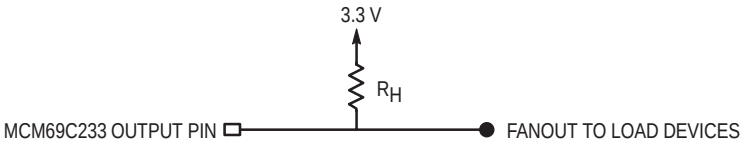


Figure 1. AC Test Loads



NOTES:
1. For $\overline{IRQ}$, $\overline{DTACK}$, $\overline{MS}$, $\overline{MC}$, and $\overline{VPC}$; R_H = 200 Ω.
2. If multiple MCM69C233s are used, R_H should be placed as close to the load devices as possible.

Figure 2. Pullup for Open Drain Outputs

FUNCTIONAL DESCRIPTION

The MCM69C233 is a flexible CAM that can contain 4096 entries of 64 bits each. The widths of the match field and the output field are programmable, and the match time is designed to be 210 ns. As a result, the MCM69C233 is well suited for datacom applications such as VPI/VCI translation in ATM switches up to OC12 (622 Mbps) data rates and MAC address lookup in Ethernet/Fast Ethernet bridges. The match duty cycle of the MCM69C233 is determined by the user, with a trade–off between the match request rate and the rate of entries added to/deleted from the CAM. With the minimum required 60 ns of idle time between matches, a typical value of 1627 insertions or deletions per second can be made. See Figure 3 for a graph of the relationship between insertion/deletion pairs and match duty cycle.

In its basic operating mode, the MCM69C233 reads a data input word through the MQ bus and compares it to all the entries in its CAM table. The $\overline{MC}$ pin is always asserted after the comparisons have been made. If a match is found, the $\overline{MS}$ pin is asserted, and the data associated with the matching entry is output on the MQ bus. If no match is found, the MQ bus remains in a high–impedance state to facilitate depth expansion via the cascading of multiple CAMs.

Before the basic operating mode can be entered, several start–up functions must be performed. First, the output width and match width must be designated by setting the global–mask register. Second, a choice must be made between buffered–entry mode and fast–entry mode. Next, the 64–bit match/output data pairs must be loaded into the table. Depending on the entry mode of choice, the table may have to be initialized. Optionally, the “almost–full” point may be set to provide warning of impending table overflow.

The input bits to be compared are defined by the global–mask register. The mask bits that are 0 correspond to the bits that are used in the match operation.Typically, the bits that are used in matching are the high order bits in the 64–bit CAM table entries, and the bits that are used as outputs are the low order bits. While any of the bits can be defined as match bits, the low order 32 bits of an entry are always driven on the MQ bus as output data.

The choice of entry mode is a trade–off between speed of entry and latency before matching operations can begin. In a typical application, the fast–entry mode will be used to load the initial values into the CAM table. Subsequently, the initialize–table operation, which takes 18 ms, must be executed to establish the required linkages and relationships among the entries. After match operations have begun, the buffered–entry mode should be used to enter new values dynamically; even one addition in fast–entry mode will disable matching until the table is reinitialized. Table insertions using the buffered–entry mode and the fast–entry mode actually take the same amount of time unless the entry queue is full. The capacity of the queue is 12 entries.

After the entry mode choice is made, the table can be loaded. Each 64–bit entry is constructed by writing a 16–bit value to each of the 4 I/O registers in the control port of the MCM69C233. The insertion can then be processed. After all the start–up entries have been loaded into the CAM table, the initialization operation is run if required. Normal matching operations can then begin. A delete operation is provided to remove stale data from the CAM table.

Several error codes are defined in the details of the instruction set. When an error occurs, its corresponding code is written into the error register and the error bit in the flag register is set. The error bit is cleared and the error register is set to $FFFF_{16}$ by the next write to the operation register.

PROGRAMMING MODEL

Three types of registers are accessible through the MCM69C233 control port: I/O registers, an operation register, and result/condition code registers. Each register is 16 bits in length.

REGISTER NAME	BIT NUMBER 15 … 0	ADDRESS OFFSET
I/O REGISTER 0		0
I/O REGISTER 1		1
I/O REGISTER 2		2
I/O REGISTER 3		3
OPERATION REGISTER		4
FLAG REGISTER		5
ERROR CODE REGISTER		6
INTERRUPT REGISTER		7

FLAG BIT DEFINITIONS

Bit 0: 1 = At least one interrupt enabled,
0 = No interrupts enabled
Bit 1: 1 = Last control port match successful,
0 = Last match unsuccessful
Bit 2: 1 = Table initialized, 0 = Table not initialized
Bit 3: 1 = Buffered–entry mode, 0 = Fast–entry mode
Bit 4: 1 = Entry queue empty,
0 = Entry queue not empty
Bit 5: 1 = Entry queue full, 0 = Entry queue not full
Bit 6: 1 = CAM table full, 0 = CAM table not full
Bit 7: 1 = Error condition set, 0 = No error
Bit 8: 1 = Table almost full, 0 = Table not almost full
Bit 9: 1 = ATM mode, 0 = Standard mode
Bit 10: 1 = Last operation complete, 0 = Not yet complete

ERROR CODES

FFFF	No error
FFFD	Invalid instruction
FFFC	Queue not empty for read
FFFB	Table not initialized
FFFA	Queue not empty for write
FFF9	CAM table full
FFF8	Entry queue full

INTERRUPT BIT DEFINITIONS

Bit 0: 1 = Enable interrupt on insert with full entry queue
Bit 1: 1 = Enable interrupt on insert with full table
Bit 2: 1 = Enable interrupt on completion of CHECK–FOR–VALUE instruction
Bit 3: 1 = Enable interrupt on completion of INITIALIZE–TABLE instruction
Bit 4: 1 = Enable interrupt on failed attempt to enter fast–entry mode
Bit 5: 1 = Enable interrupt on CAM table reaching almost–full point
Bit 6: 1 = Enable interrupt on fast read with non–empty queue
Bit 7: 1 = Enable interrupt on illegal instruction

INSTRUCTION SET DETAILS

The MCM69C233 is prepared for match operations by writing data and instructions via the control port. In the general case, required data is loaded into I/O registers 0 – 3, then an instruction is issued by writing an operation code to the operation register. As a result of running an instruction, the CAM table can be modified, bit(s) can be set in the flag register, error codes can be returned in the error code register, and an interrupt can be generated if enabled. For a particular condition to generate an interrupt, the interrupt register bit specific to that condition must be set. The user should verify that the last operation complete bit (bit 10) of the flag register is set before executing the next instruction, if the instruction just executed modifies I/O registers. See the **Simultaneous Port Operations** section for any exceptions.

Table 1. MCM69C233 Operation Summary

Operation	Description	OP Code (Base 16)
INSERT VALUE	Loads a new entry into the CAM table	0000 or 000F
DELETE VALUE	Removes an entry from the CAM table	0001 or 000E
CHECK FOR VALUE	Runs a match cycle via the control port	0006
INITIALIZE TABLE	Prepares CAM table for matching	000B
FAST–ENTRY MODE	Selects entry mode suited for initial CAM table load	0004
BUFFERED–ENTRY MODE	Selects entry mode suited for simultaneous loading and matching	0005
SET ATM MODE	Enter mode that provides concurrent VPC/VCC search	0008
RETURN ENTRY COUNT	Determines number of entries in CAM	0003
SET GLOBAL–MASK REGISTER	Determines match bits to be checked in a match operation	0002 or 000D
SET ALMOST–FULL POINT	Defines CAM almost–full condition	0007
SET FAST–READ REGISTER	Defines table entry that is output by the fast–read operation	0009
FAST READ	Outputs one CAM table entry	000A

INSERT VALUE

This instruction is used to load a new match/output value into the CAM. The contents of I/O registers 0 – 3 are concatenated to create the 64–bit value. Bit 15 of register 3 is the most significant bit, and bit 0 of register 0 is the least significant bit.

If the MCM69C233 is in the buffered–entry mode, the resulting 64–bit value is written to the first available location in the entry queue, and is immediately available for matching. If a buffered insert–value instruction is attempted when the entry queue is full (indicated by bit 5 of the flag register = 1), no value is written, an error code of $FFF8_{16}$ is returned in the error code register, and the error–condition flag (bit 7) is set in the flag register. An interrupt is generated, if enabled by bit 0 of the interrupt register being set.

If the MCM69C233 is running in the fast–entry mode, the concatenated 64–bit value is written directly to the CAM array. If an insert–value instruction is attempted when in fast–entry mode and the table is full, no value is written, an error code of $FFF9_{16}$ is returned in the error code register, and the error–condition flag (bit 7) is set in the flag register. (The table–full condition is indicated by bit 6 of the flag register being set.) An interrupt is generated, if enabled by bit 1 of the interrupt register being set.

Only one entry is allowed for a given match pattern. If an entry is made in the table that duplicates an existing match pattern, it will overwrite the entry already in the CAM table, if the CAM is in buffered–entry mode. The user must ensure that no entries with the same match pattern are inserted in fast–entry mode.

DELETE VALUE

This instruction is used to remove a match/output value from the CAM. The contents of I/O registers 0 – 3 are concatenated, with bit 15 of register 3 as the most significant bit, and bit 0 of register 0 as the least significant bit. The bits that have a 0 in the corresponding bit of the global–mask register are used to find a matching entry in the CAM table. If such an entry is found, it is invalidated. Note that any bit that is not a match bit as defined by the mask register is ignored for this

operation. The operation of the MCM69C233 guarantees that no more than one matching entry can exist in the table, unless they were accidently loaded using fast–entry mode. This must be avoided by the user, as the results of subsequent matches and deletes will be undefined.

Example: I/O Register 0 = 3020_{16}
I/O Register 1 = 0000_{16}
I/O Register 2 = $543A_{16}$
I/O Register 3 = $FE55_{16}$
Concatenated value = $FE55543A00003020_{16}$
Global–Mask Register = $C0000000FFFFFFFF_{16}$

Of the high–order 32 bits, the rightmost 30 bits are cared by the global–mask register. Therefore, the MCM69C233 will delete an entry, if it exists, which has a value of $3E55543A_{16}$ in bits 61 – 32.

CHECK FOR VALUE

This instruction checks for a matching value in the CAM table via the control port. The contents of I/O registers 0 – 3 are concatenated, with bit 15 of register 3 as the most significant bit, and bit 0 of register 0 as the least significant bit. The bits that have a 0 in the corresponding bit of the global–mask register are used to find a matching entry in the CAM table. If such an entry is found, the last–match–successful bit of the flag register is set. In addition, the matching entry is written to I/O registers 0 – 3, with bit 15 of register 3 as the most significant bit, and bit 0 of register 0 as the least significant bit

If no match is found, the last–match–successful bit is cleared. An interrupt is generated regardless of the result, if enabled by bit 2 of the interrupt register, when the operation has been completed. The operation of the MCM69C233 guarantees that no more than one matching entry can exist in the table. If uninterrupted by match port activity, the check for value instruction will finish in 16 clock cycles. NOTE: If both the control port and matching port are utilized simultaneously, see the **Simultaneous Port Operations** section.

INITIALIZE TABLE

If fast–entry mode has been used to load the CAM table, the initialize–table operation must be used to establish the needed relationships and linkages between the entries in the table before matching can proceed. Upon completion, this operation sets the table–initialized bit in the flag register, and generates an interrupt if enabled by bit 3 of the interrupt register. It also sets the buffered–entry mode bit in the flag register. This operation makes the programming model's registers read–only for up to 18 ms after the acknowledgment of the op code write cycle.

FAST–ENTRY MODE

This instruction is used to enter the fast–entry mode. When the MCM69C233 is in this mode, insert–value operations bypass the entry queue and write new table entries directly to the CAM table. The fast–entry mode can only be entered while the entry queue is empty, as reflected by the queue–empty flag being set (bit 4 of the flag register). If this operation is attempted while the entry queue is not empty, the value $FFFA_{16}$ is written to the error code register, the error–condition flag (bit 7) is set in the flag register, and an interrupt is generated if enabled by bit 4 of the interrupt register.

If this mode is used to enter data, the initialize–table operation must be executed before matching operations can begin. The entry–mode bit and the table–initialized bit of the flag register (bit 3) are cleared by this operation.

BUFFERED–ENTRY MODE

This instruction is used to enter the buffered–entry mode. When the MCM69C233 is in this mode, insert–value and delete–value operations utilize the entry queue. This mode can be entered at any time. Table entries are available for match operations immediately, without running the initialize–table operation, if all entries are made in this mode. Note that if both the buffered–entry and fast–entry modes have been used to input data, none of the entries are available for matching until the initialize–table operation is executed. Conflicting table and queue values are resolved in favor of the latest entry in the queue. For example, if there is an entry in the CAM, a corresponding delete–entry in the queue, and a later insert–entry in the queue (all with the same match data), the queued insert–entry will return a match value.

RETURN ENTRY COUNT

This operation is used to determine the number of valid entries in the MCM69C233. The value is returned in I/O register 0, and reflects the sum of the number of valid entries in the CAM table and the inserts in the entry queue.

SET GLOBAL–MASK REGISTER

This operation is used to indicate the bits to be used in performing matches. A 1 indicates that a bit should be ignored in the match operation, while a 0 indicates that a bit should be used in the match operation.

When this operation is executed, the contents of I/O registers 0 – 3 are concatenated, with bit 15 of register 3 as the most significant bit, and bit 0 of register 0 as the least significant bit. The resulting 64–bit value is written to the global–mask register.

This operation should be executed before entering required values into the CAM table. Otherwise, the initialize–table instruction must be executed if the global–mask register is changed after data is loaded into the CAM.

SET ALMOST–FULL POINT

This operation is used to define the "almost–full" condition in the CAM table. The 12 low–order bits of I/O register 0 are copied to the almost–full–point register. If an entry is added to the MCM69C233 (via the insert–value operation) that causes the valid–entry count to equal the almost–full point, then bit 8 of the flag register is set, and an interrupt is generated if enabled by bit 5 of the interrupt register. The value of the almost–full register can be changed dynamically during match operations. For example, it could first be set to 2048 to generate an interrupt when the table is half full. When that point is reached, the register could be reprogrammed to 3072 to provide warning that the table has become three–quarters full. The almost–full interrupt is generated, if enabled, based on the number of entries in the CAM table. Entries in the queue are not included in the count.

SET FAST–READ REGISTER VALUE

This operation defines the table address that is output by the fast–read operation. The least significant 12 bits of I/O register 0 are copied to the fast–read register. The queue must be empty when this instruction is executed.

The fast–read instruction can only be executed while the entry queue is empty, as reflected by the queue–empty flag being set (bit 4 of the flag register). If this operation is attempted while the entry queue is not empty, the value $FFFC_{16}$ is written to the error code register, the error–condition flag (bit 7) is set in the flag register, and an interrupt is generated if enabled by bit 7 of the interrupt register.

FAST READ

This operation is used to output the contents of one entry in the CAM table. The fast–read register is used to specify the appropriate entry, and is then auto–incremented. As a result, successive execution of multiple fast–read operations will provide access to contiguous entries in the CAM table.

The CAM entry is copied to I/O registers 0 – 3, with bit 15 of register 3 as the most significant bit, and bit 0 of register 0 as the least significant bit.

The fast–read instruction can only be executed while the entry queue is empty, as reflected by the queue–empty flag being set (bit 4 of the flag register.) If this operation is attempted while the entry queue is not empty, the value $FFFC_{16}$ is written to the error code register, the error–condition flag (bit 7) is set in the flag register, and an interrupt is generated if enabled by bit 7 of the interrupt register.

SET ATM MODE

When the MCM69C233 is placed in ATM mode, it provides simultaneous searching for virtual path circuits (VPCs) and virtual connection circuits (VCCs). A VCC is detected when both the VPI and the VCI of an incoming cell match an entry in the CAM. A VPC match occurs when the VPI of an incoming cell matches the VPI field of a CAM entry that has all 1s as its VCI. A VPC match is signaled by the assertion of the $\overline{VPC}$ pin along with the $\overline{MS}$ pin. At 66 MHz, a match is completed in 210 ns, whether the applied VPI/VCI belongs to a VCC or a VPC.

The VCI match field must be defined as bits 32 – 47 of each entry, and the VPI match data must occupy bits 48 – 59. The VPI can be limited to bits 48 – 55, if the switch handles only User–Network Interface (UNI) protocols. The mask register should be used to “don’t care” any unused bits beyond the VPI field. Entering ATM mode will set bit 9 of the flag register.

To load a VPC into the CAM table, the desired VPI value is written (right justified) to I/O register 3, $FFFF_{16}$ is written to I/O register 2 as the VCI field, the upper half of the desired output word is written to I/O register 1, and the lower half of the desired output word is written to I/O register 0. Then, the “INSERT VALUE” instruction is written to the operation register.

When performing a match operation, the VCI must be placed in bits 0 – 15 of the MQ port. The VPI is expected on bits 16 – 27, or bits 16 – 23 in the UNI case.

buffered–entry mode insertions and deletions are modified in the following way when the MCM69C233 is in ATM mode. If you try to add a VCC with the same VPI as an existing VPC, you overwrite the VPC. If you try to delete a VCC when the VCC is not in the table, but a VPC with that VPI is in the table, the VPC will be deleted.

The CAM table should never contain, simultaneously, a VCC entry and VPC entry with matching VPIs. Violation of this requirement may lead to unpredictable behavior.

Bits 60 – 63 may be used for matching in ATM mode if the application requires extra bits. The use of bits 0 – 31 for matching is not supported in ATM mode.

MATCH DUTY CYCLE

At 66 MHz, the MCM69C233 completes a match 210 ns, or 14 clock cycles, after assertion of the $\overline{SM}$ signal. However, if entries need to be added to or deleted from the CAM, idle time is needed between match output and match requests for control port insertions and deletions. At 66 MHz, the match duty cycle should be defined at least at 18 clock cycles (270 ns), leaving 2 clock cycles for insertions/deletions. The additional clock cycles are used for holding the match data on the MQ bus. Therefore, every 18 clock cycles, when a match operation and data output are completed, $\overline{SM}$ can be asserted.

Entries are stored from least value at the top of the table to the highest value at the bottom. If an entry with a match data value smaller than any other entry is continually added or dropped from the table, worst–case scenario occurs causing shifting of all other entries. The idle time, in terms of the number cycles, needed to perform a worst–case insertion and/or deletion is given by the formula 8192 x MDC / (MDC – 16) cycles, where MDC is the match duty cycles. For example, if match requests are occurring every 18 clock cycles:

$$\frac{8192 \times 18 \text{ clock cycles}}{18 \text{ clock cycles} - 16} = 73{,}728 \text{ clock cycles}$$

At 66 MHz (15 ns per cycle)

= 0.00110592 sec per insert or deletion.

If both insertions and deletions are occurring

= 452 insertion/deletion pairs per sec (worst–case).

More typical cases consist of insertions occurring at one end of the table and deletions occurring at the other end, or when insertions and/or deletions take place toward the middle of the table. The latter scenario would consist of approximately half the total entries being shifted. The idle time, in terms of the number of cycles, needed to perform a typical insertion and/or deletion is given by the formula 2048 x MDC / (MDC – 9) cycles, where MDC is the match duty cycles. For example, if match requests are occurring every 18 clock cycles:

$$\frac{4096 \times 18 \text{ clock cycles}}{18 \text{ clock cycles} - 16} = 36{,}864 \text{ clock cycles}$$

At 66 MHz (15 ns per cycle)

= 0.00055296 sec per insert or deletion.

If both insertions and deletions are occurring

= 904 insertion/deletion pairs per sec (worst–case).

The number of insertion/deletion pairs for both cases are depicted in Figure 3. In general, the time for an insertion or deletion is proportional to its distance from the end of the CAM table. That is, entries with the largest match value take

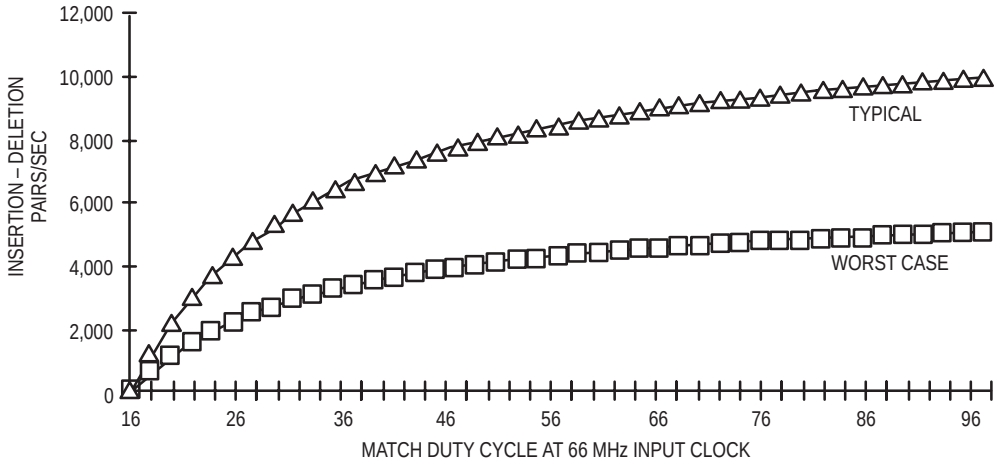


Figure 3. Connections per Second vs Match Cycle Time

the least time to insert or delete, while entries with the smallest values take the most time.

Therefore, the effective rate of insertion and deletion is maximized if the longest–lived entries are placed near the beginning of the table and the shortest–lived entries are placed near the end of the table. For an ATM application, this would correspond to the assignment of small VPI values to permanent virtual circuits and large VPI values to switched virtual circuits.

Note that at start–up, when entries are loaded into the CAM via the fast–entry mode, the process is dominated by the time it takes to execute the initialization instruction that follows. The resulting effective rate of loading the CAM at start–up is approximately 227,500 entries per second.

$\overline{\text{RESET}}$

$\overline{\text{RESET}}$ is synchronous to the rising edge of the clock with 0 ns setup and hold. Asserting $\overline{\text{RESET}}$ for two clock cycles removes all entries from the CAM table and entry queue. The flag register is set to $1C_{16}$ (setting the queue empty, buffered–entry mode, and table initialized bits). The error register is set to $FFFF_{16}$, indicating no errors. The interrupt mask is cleared, and the almost–full register is set to FFF_{16}.

TIMING OVERVIEW

CONTROL PORT

The control port of the MCM69C233 is asynchronous. Data transfers, both read and write, are initiated by the assertion of the $\overline{\text{SEL}}$ signal. Address values should be valid and $\overline{\text{WE}}$ should be high, when $\overline{\text{SEL}}$ is asserted to begin a read cycle. All values (address, $\overline{\text{WE}}$, and $\overline{\text{SEL}}$) should be held until the MCM69C233 asserts $\overline{\text{DTACK}}$ to signal the end of the read cycle.

Address and data values should be valid and $\overline{\text{WE}}$ should be low, when $\overline{\text{SEL}}$ is asserted to begin a write cycle. Address, data, $\overline{\text{WE}}$, and $\overline{\text{SEL}}$ values should be held until the MCM69C233 asserts $\overline{\text{DTACK}}$ to signal the end of the write cycle.

MATCH PORT

The MCM69C233 match port is synchronous in operation. When the match width is ≤32 bits, a match cycle can be initiated by presenting the match data on MQ31 – MQ0 and asserting the $\overline{\text{LH}}/\overline{\text{SM}}$ signal with the appropriate setup time relative to the rising edge of the clock. The assertion of the $\overline{\text{MC}}$ output signifies the completion of the match cycle. If a match has been found, the $\overline{\text{MS}}$ output is also asserted. If the match is a virtual path circuit match in ATM mode, the $\overline{\text{VPC}}$ output will be asserted with the $\overline{\text{MS}}$ output. Output data, if any, is enabled by the assertion of the $\overline{\text{G}}$ input.

If the match width is greater than 32 bits, the lower bits are first latched into the MCM69C233 by the $\overline{\text{LL}}$ input. The match cycle is then initiated as specified in the previous paragraph.

Two alternative timing diagrams are presented to describe the Match Port timing. In the first, $\overline{\text{LH}}/\overline{\text{SM}}$ must meet setup and hold specs across two consecutive clock cycles, while the MQ bus need only be valid for a single cycle. In the second diagram, $\overline{\text{LH}}/\overline{\text{SM}}$ need only be asserted for a single clock cycle, while the MQ bus must be held valid with constant data across two clock cycles.

SIMULTANEOUS PORT OPERATIONS

When the control and match ports are utilized simultaneously, certain procedures must be followed. If a CHECK FOR VALUE command is issued, both the last operation complete bit (bit 10) and the entry queue empty bit (bit 4) in the flag register should be set prior to executing the CHECK FOR VALUE command in order to receive valid results. However, matching on the match port can be done directly after the last operation complete flag is set.

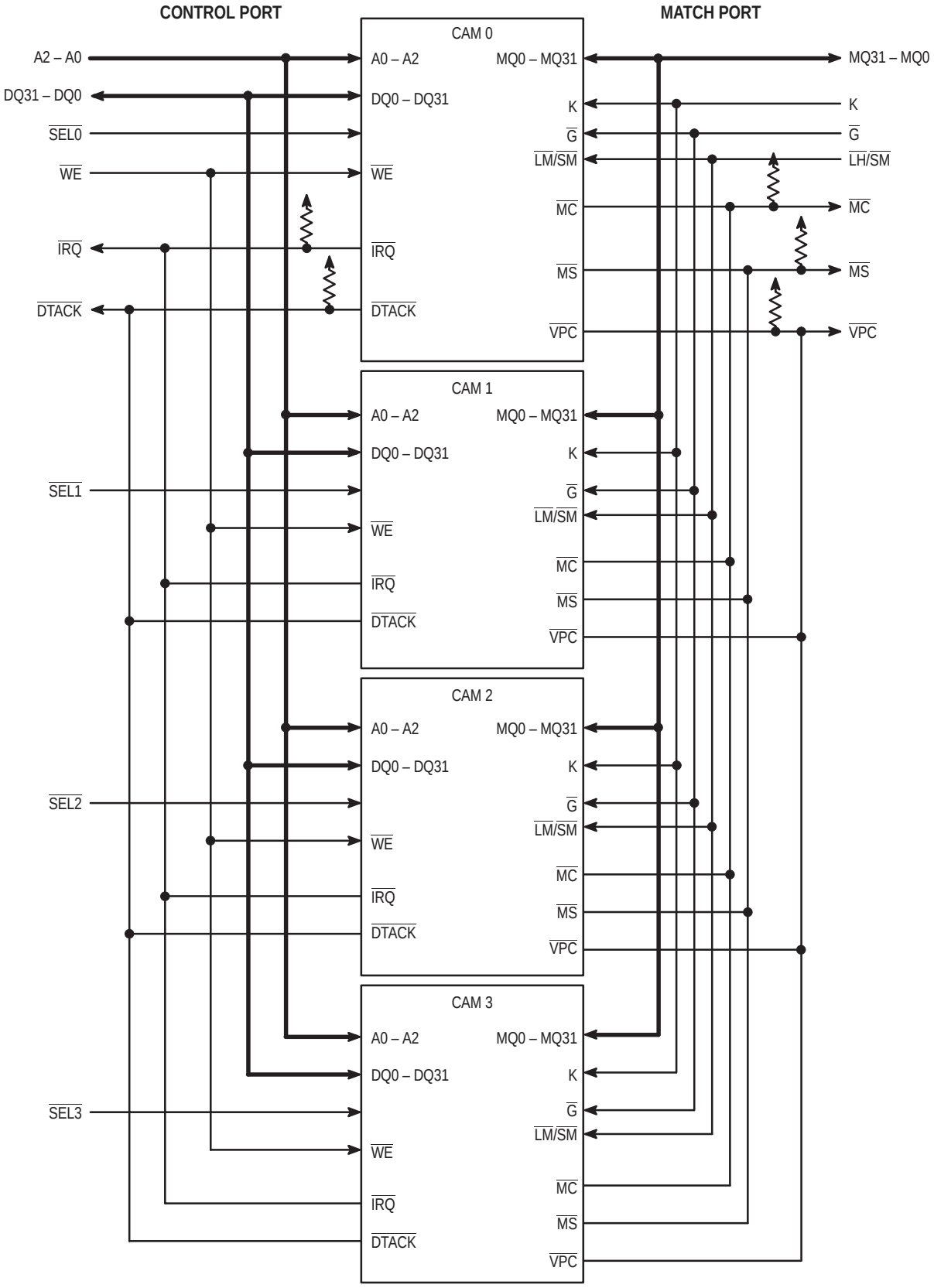
The match port has priority over the control port during simultaneous operations.

DEPTH EXPANSION

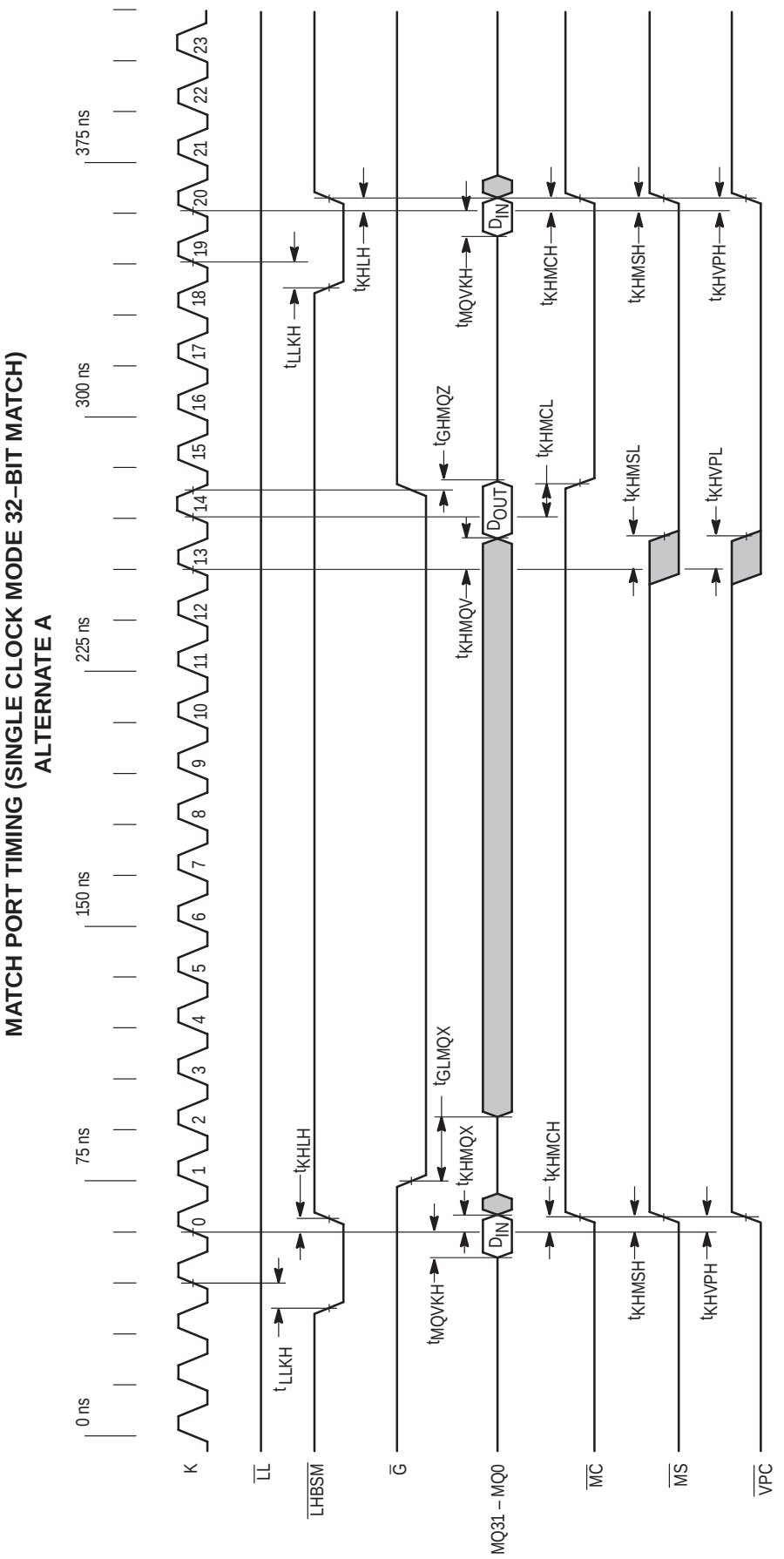
Multiple CAMs can be cascaded to increase the depth of the match table. The hardware requirements are very straightforward, as the following pins on each device are simply wired in parallel: A2 – A0, DQ15 – DQ0, $\overline{\text{WE}}$, $\overline{\text{IRQ}}$, $\overline{\text{DTACK}}$, MQ31 – MQ0, K, $\overline{\text{G}}$, $\overline{\text{LH}}/\overline{\text{SM}}$, $\overline{\text{MC}}$, $\overline{\text{MS}}$, and $\overline{\text{VPC}}$. Four CAMs can be easily cascaded. Simulations show that eight devices can be cascaded if care is taken to minimize the length of the PC board traces connecting the CAMs.

The buffered–entry mode prevents multiple matching entries in a single CAM. The check for value instruction should be used to verify that multiple matching entries will not result from a potential new entry. If a match is found in CAM 1, for example, the new value should be placed in CAM 1, where it will replace the existing entry.

DEPTH EXPANSION EXAMPLE
CASCADING FOUR MCM69C233s FOR A 16K WORD TABLE

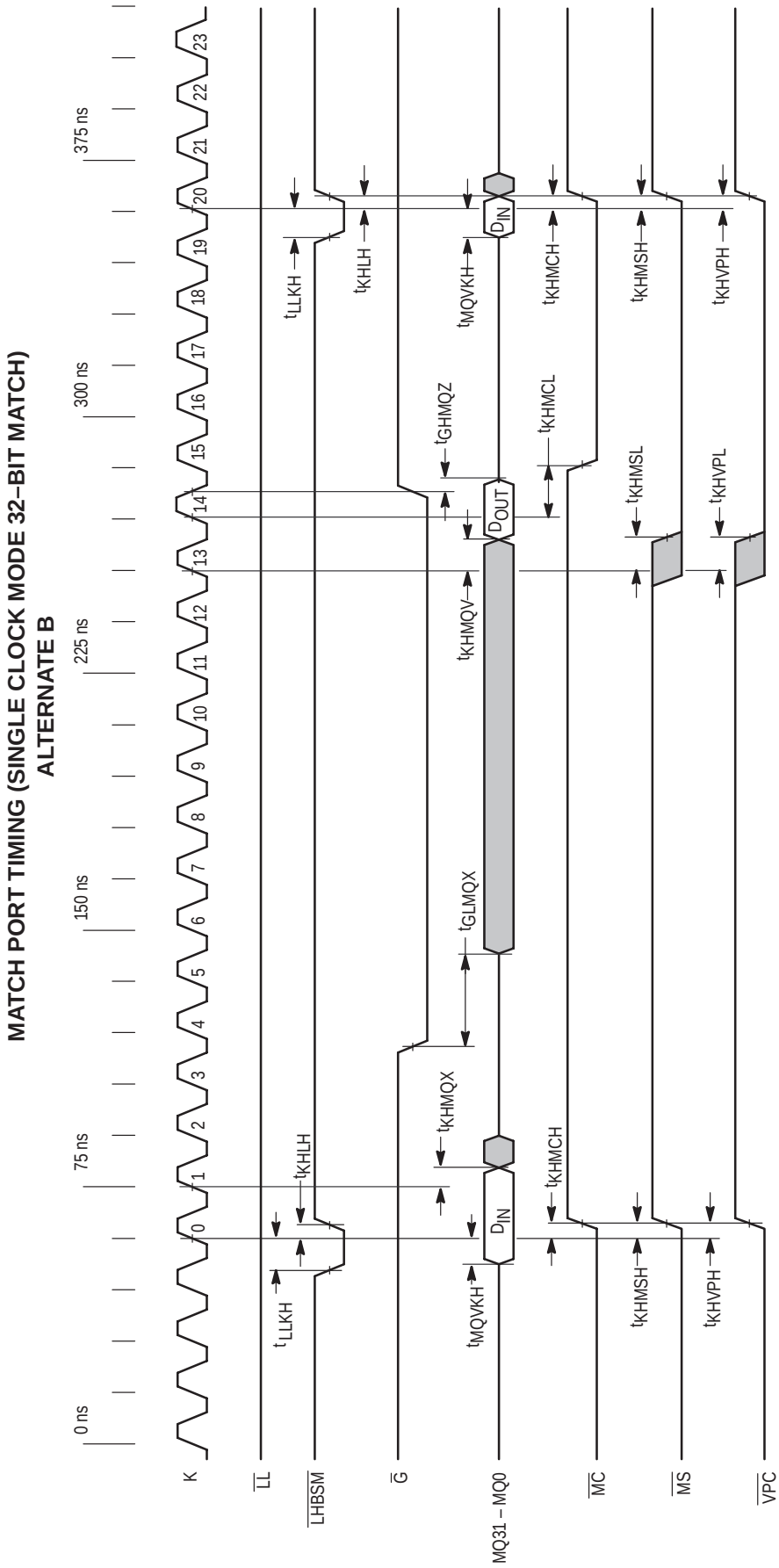


MATCH PORT TIMING (SINGLE CLOCK MODE 32–BIT MATCH) ALTERNATE A



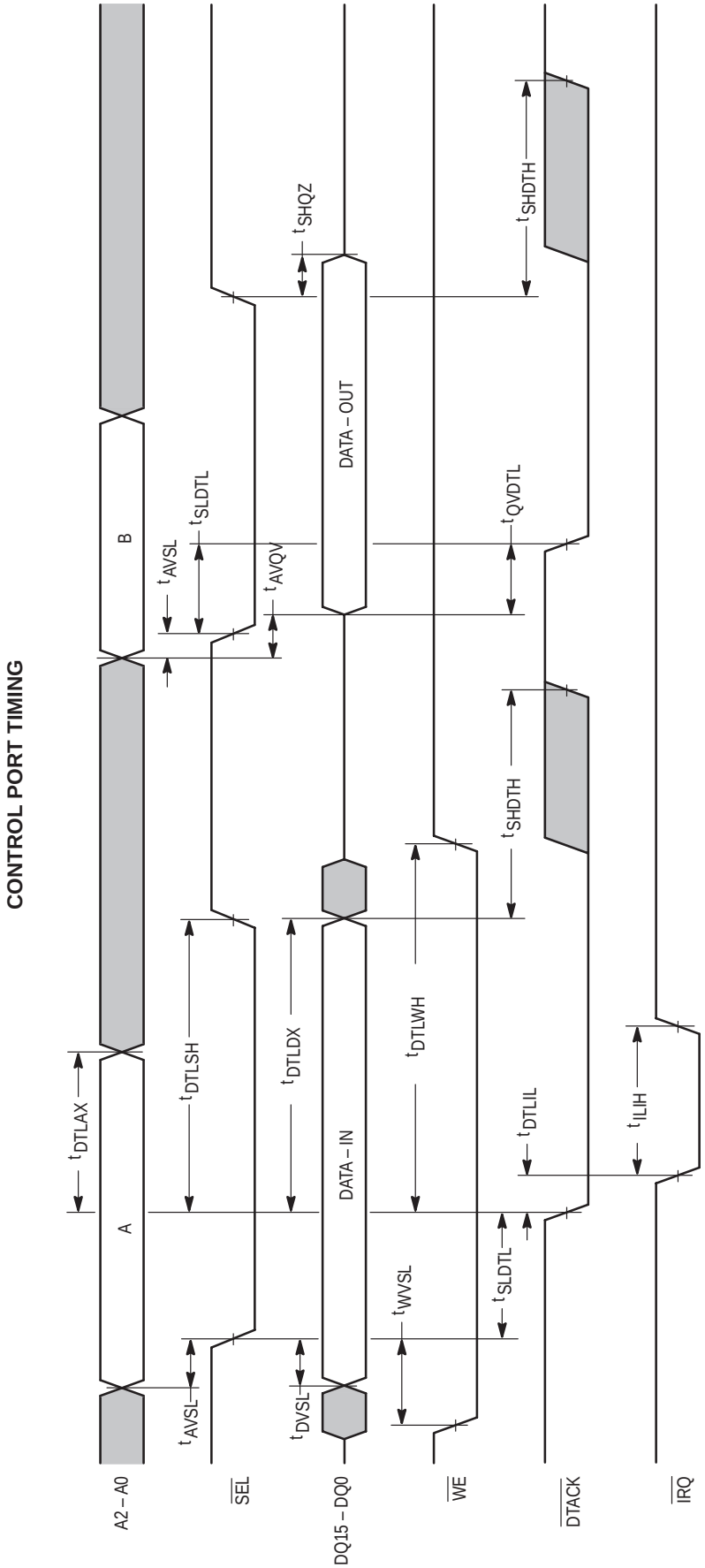
NOTE: See description of Match Port Timing.

MATCH PORT TIMING (SINGLE CLOCK MODE 32–BIT MATCH) ALTERNATE B



NOTE: See description of Match Port Timing.

CONTROL PORT TIMING



JTAG

AC OPERATING CONDITIONS AND CHARACTERISTICS FOR THE TEST ACCESS PORT (IEEE 1149.1)

(T_J < 120°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 3 ns

Output Measurement Timing Level . . . . . 1.5 V
Output Load . . . . . 50 Ω Termination to 1.5 V

TAP CONTROLLER TIMING

Parameter		Symbol	Min	Max	Unit	Notes
Cycle Time		t_{CK}	30	—	ns	
Clock High Time		t_{CKH}	12	—	ns	
Clock Low Time		t_{CKL}	12	—	ns	
Clock Low to Output Valid		t_A	5	9	ns	
Clock Low to Output High–Z		t_{CKZ}	0	9	ns	1
Clock Low to Output Active		t_{CKX}	0	9	ns	2, 3
Setup Times:	TMS TDI $\overline{TRST}$	t_S t_{SD} t_{SR}	2 2 2	—	ns	
Hold Times:	TMS TDI $\overline{TRST}$	t_H t_{HD} t_{HR}	2 2 10	—	ns	

NOTES:
1. TDO will High–Z from a clock low edge depending on the current state of the TAP state machine.
2. TDO is active only in the SHIFT–IR and SHIFT–DR state of the TAP state machine.
3. Transition is measured ±500 mV from steady–state voltage. This parameter is sampled and not 100% tested.

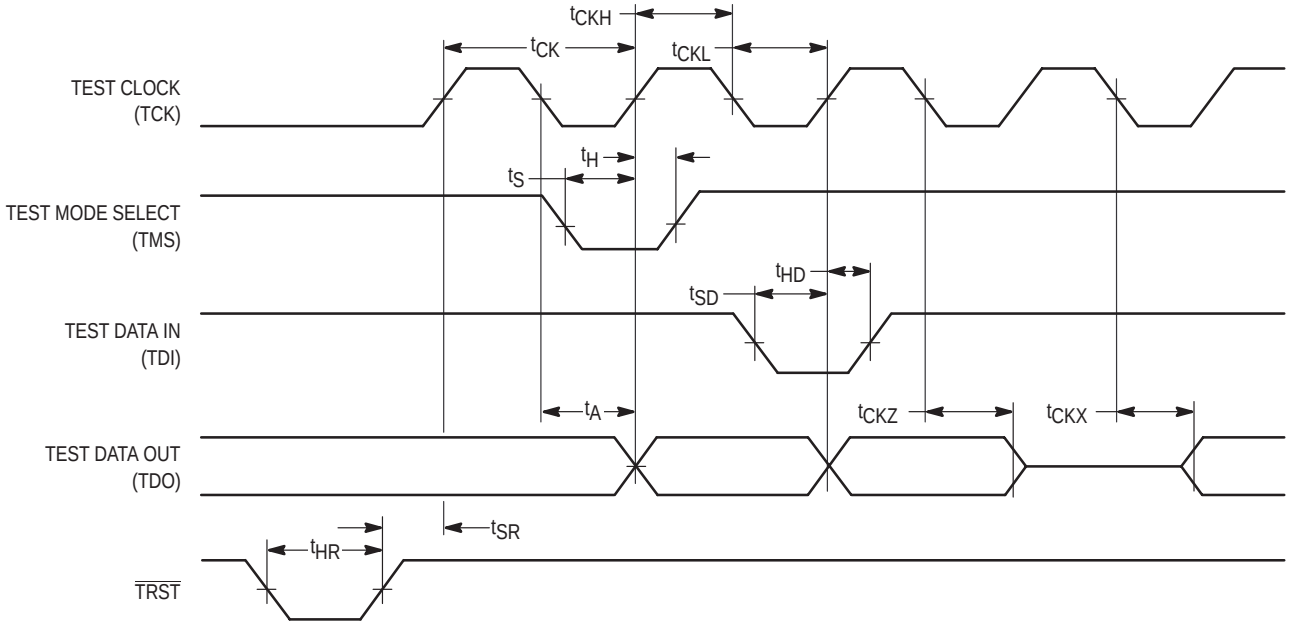


Figure 4. TAP Controller Timing

TEST ACCESS PORT DESCRIPTION

INSTRUCTION SET

A 5–pin IEEE Standard 1149.1 Test Port (JTAG) is included on this device. When the TAP (Test Access Port) controller is in the SHIFT–IR state, the instruction register is placed between TDI and TDO. In this state, the desired instruction would be serially loaded through the TDI input. $\overline{TRST}$ resets the TAP controller to the test–logic reset state. The TAP instruction set for this device are as follows.

STANDARD INSTRUCTIONS

Instruction	Code (Binary)	Description
BYPASS	1111*	Bypass instruction
SAMPLE/PRELOAD	0010	Sample and/or preload instruction
EXTEST	0000	Extest instruction
HIGH–Z	1001	High–Z all output pins while the bypass register is between TDI and TDO
CLAMP	1100	Clamp output pins while the bypass register is between TDI and TDO

* Default state at power–up.

SAMPLE/PRELOAD TAP INSTRUCTION

The SAMPLE/PRELOAD TAP instruction is used to allow scanning of the boundary scan register without causing interference to the normal operation of the chip logic. The 62–bit boundary scan register contains bits for all device signal and clock pins and associated control signals. This register is accessible when the SAMPLE/PRELOAD TAP instruction is loaded into the TAP instruction register in the SHIFT–IR state. When the TAP controller is then moved to the SHIFT–DR state, the boundary scan register is placed between TDI and TDO. This scan register can then be used prior to the EXTEST instruction to preload the output pins with desired values so that these pins will drive the desired state when the EXTEST instruction is loaded. As data is written into TDI, data also streams out of TDO, which can be used to pre–sample the inputs and outputs.

SAMPLE/PRELOAD would also be used prior to the CLAMP instruction to preload the values on the output pins that will be driven out when the CLAMP instruction is loaded.

EXTEST TAP INSTRUCTION

The EXTEST instruction is intended to be used in conjunction with the SAMPLE/PRELOAD instruction to assist in testing board level connectivity. Normally, the SAMPLE/PRELOAD instruction would be used to preload all output pins. The EXTEST instruction would then be loaded. During EXTEST, the boundary scan register is placed between TDI and TDO in the SHIFT–DR state of the TAP controller. Once the EXTEST instruction is loaded, the TAP controller would then be moved to the run–test/idle state. In this state, one cycle of TCK would cause the preloaded data on the output pins to be driven while the values on the input pins would be sampled. Note the TCK, not the clock pin (CLK), is used as the clock input while CLK is only sampled during EXTEST. After one clock cycle of TCK, the TAP controller would then be moved to the SHIFT–DR state where the sampled values would be shifted out of TDO (and new values would be shifted in TDI). These values would normally be compared to expected values to test for board connectivity.

CLAMP TAP INSTRUCTION

The CLAMP instruction is provided to allow the state of the signals driven from the output pins to be determined from the boundary scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the output pins will not change while the CLAMP instruction is selected. EXTEST could also be used for this purpose, but CLAMP shortens the board scan path by inserting only the bypass register between TDI and TDO. To use CLAMP, the SAMPLE/PRELOAD instruction would be used first to scan in the values that will be driven on the output pins when the CLAMP instruction is active.

HIGH–Z TAP INSTRUCTION

The HIGH–Z instruction is provided to allow all the outputs to be placed in an inactive drive state (high–Z). During the HIGH–Z instruction the bypass register is connected between TDI and TDO.

BYPASS TAP INSTRUCTION

The BYPASS instruction is the default instruction loaded at power–up. This instruction will place a single shift register between TDI and TDO during the SHIFT–DR state of the TAP controller. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

BOUNDARY SCAN REGISTER

The boundary scan register is identical in length to the number of active input, output, and I/O connections on the device (not counting the TAP pins). The boundary scan register, under the control of the TAP controller, is loaded with the contents of the RAM I/O ring when the controller is in capture–DR state and then is placed between the TDI and TDO pins when the controller is moved to shift–DR state. Several TAP instructions can be used to activate the boundary scan register.

The Bit Scan Order table (Table 2) describes which device pin connects to each boundary scan register location. The first column defines the bit's position in the boundary scan register. The shift register bit at $\overline{G}$ (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the pin, the third column is the pin number, and the fourth column is the pin type (input, output, or I/O).

DISABLING THE TEST ACCESS PORT AND BOUNDARY SCAN

It is possible to use this device without utilizing the four pins used for the test access port. To circuit disable the device, TCK must be tied to V_{SS} to preclude mid–level inputs. Although TDI and TMS are designed in such a way that an undriven input will produce a response equivalent to the application of a logic 1, it is still advisable to tie these inputs to V_{DD} through a 1K resistor. TDO should remain unconnected.

Table 2. Sample/Preload Boundary Scan Register Bit Definitions

Bit No.	Bit Pin Name	Bit Pin No.
1	$\overline{G}$	61
2	$\overline{MS}$	62
3	$\overline{VPC}$	63
4	$\overline{MC}$	64
5	MQ31	67
6	MQ30	68
7	MQ29	69
8	MQ28	70
9	MQ27	73
10	MQ26	74
11	MQ25	75
12	MQ24	76
13	MQ23	79
14	MQ22	80
15	MQ21	81
16	MQ20	82
17	MQ19	85
18	MQ18	86
19	MQ17	87
20	MQ16	88
21	$\overline{LH}/\overline{SM}$	89
22	$\overline{LL}$	92
23	MQ15	93
24	MQ14	94
25	MQ13	95
26	MQ12	96
27	MQ11	99
28	MQ10	100
29	MQ9	1
30	MQ8	2
31	MQ7	5

Bit No.	Bit Pin Name	Bit Pin No.
32	MQ6	6
33	MQ5	7
34	MQ4	8
35	MQ3	11
36	MQ2	12
37	MQ1	13
38	MQ0	14
39	DQ15	17
40	DQ14	18
41	DQ13	19
42	DQ12	20
43	DQ11	23
44	DQ10	24
45	DQ9	25
46	DQ8	26
47	DQ7	29
48	DQ6	30
49	DQ5	31
50	DQ4	32
51	DQ3	35
52	DQ2	36
53	DQ1	37
54	DQ0	38
55	K	39
56	A2	42
57	A1	43
58	A0	44
59	$\overline{WE}$	45
60	$\overline{SEL}$	46
61	$\overline{RESET}$	56
62	$\overline{IRQ}$	57
63	$\overline{DTACK}$	58

TEST ACCESS PORT PINS

TCK — TEST CLOCK (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

TMS — TEST MODE SELECT (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic 1 input level.

TDI — TEST DATA IN (INPUT)

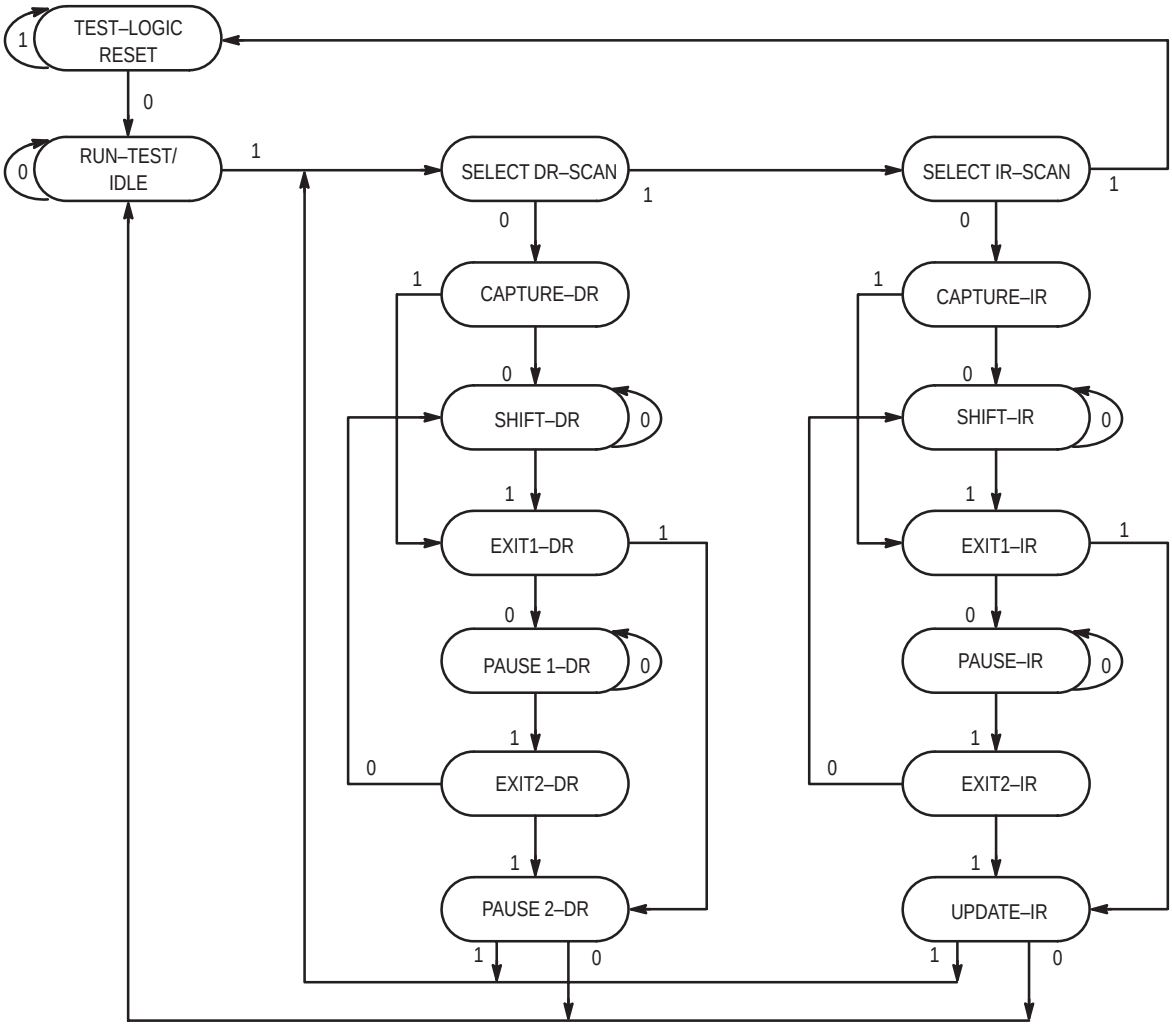
The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (see Figure 5). An undriven TDI pin will produce the same result as a logic 1 input level.

TDO — TEST DATA OUT (OUTPUT)

Output that is active depending on the state of the TAP state machine (see Figure 5). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

$\overline{\text{TRST}}$ — TAP RESET

This device has a $\overline{\text{TRST}}$ pin. $\overline{\text{TRST}}$ is optional in IEEE 1149.1. Asserting the asynchronous $\overline{\text{TRST}}$ places the TAP controller in test–logic reset state. Test–logic reset state can also be entered by holding TMS high for five rising edges of TCK. This type of reset does not affect the operation of the system logic.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 5. TAP Controller State Diagram

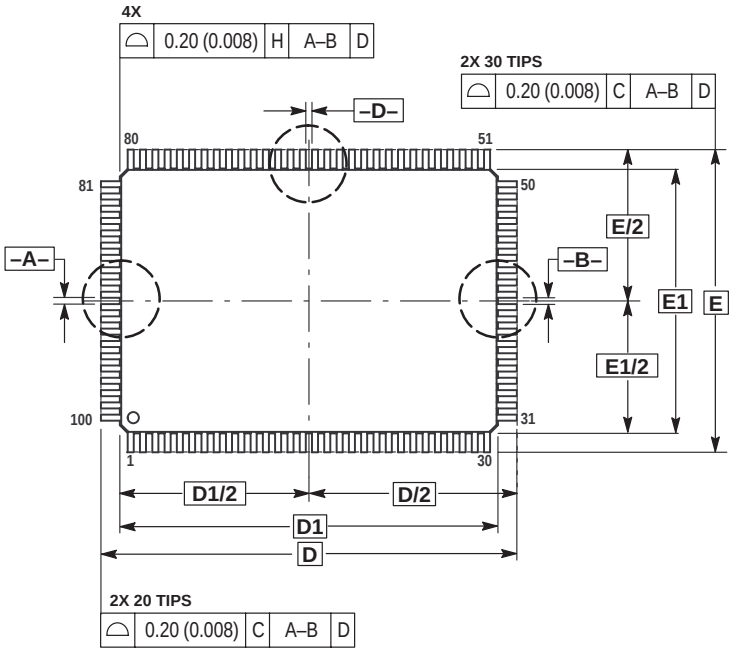
ORDERING INFORMATION
(Order by Full Part Number)

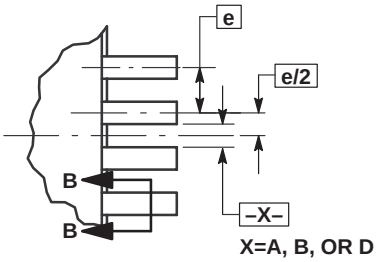
Full Commercial Part Numbers — MCM69C233TQ15 MCM69C233TQ15R

Full Industrial Part Numbers — SCM69C233TQ15 SCM69C233TQ15R

PACKAGE DIMENSIONS

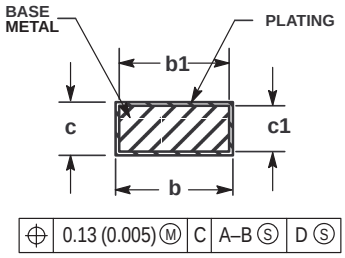
TQ PACKAGE
TQFP
CASE 983A–01



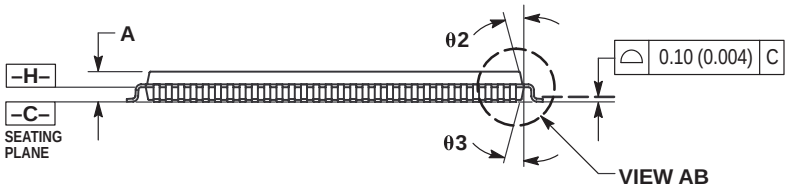


X=A, B, OR D

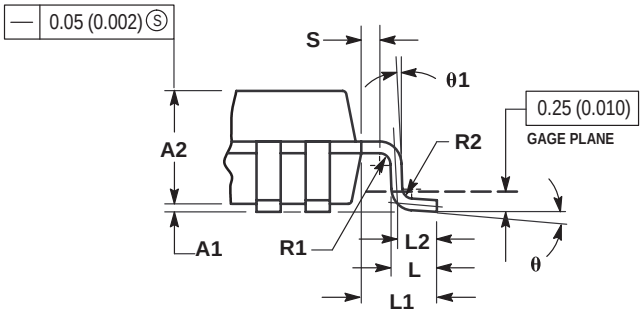
VIEW Y



SECTION B–B



VIEW AB



VIEW AB

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
3. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE –C–.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS D1 AND B1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.45 (0.018).

	MILLIMETERS	
DIM	MIN	MAX
A	—	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.22	0.38
b1	0.22	0.33
c	0.09	0.20
c1	0.09	0.16
D	22.00 BSC	
D1	20.00 BSC	
E	16.00 BSC	
E1	14.00 BSC	
e	0.65 BSC	
L	0.45	0.75
L1	1.00 REF	
L2	0.50 REF	
S	0.20	—
R1	0.08	—
R2	0.08	0.20
θ	0 °	7 °
θ1	0 °	—
θ2	11 °	13 °
θ3	11 °	13 °

NOTES

NOTES

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