

2Kx8 Dual-Port Static RAM

Features

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- 2K x 8 organization
- 0.65-micron CMOS for optimum speed/power
- High-speed access: 15 ns
- Low operating power: $I_{CC} = 110$ mA (max.)
- Fully asynchronous operation
- Automatic power-down
- Master CY7C132/CY7C136 easily expands data bus width to 16 or more bits using slave CY7C142/CY7C146
- **BUSY** output flag on CY7C132/CY7C136; **BUSY** input on CY7C142/CY7C146
- **INT** flag for port-to-port communication (52-pin PLCC/PQFP versions)
- Available in 48-pin DIP (CY7C132/142), 52-pin PLCC and 52-pin TQFP (CY7C136/146)
- Pin-compatible and functionally equivalent to IDT7132/IDT7142

Functional Description

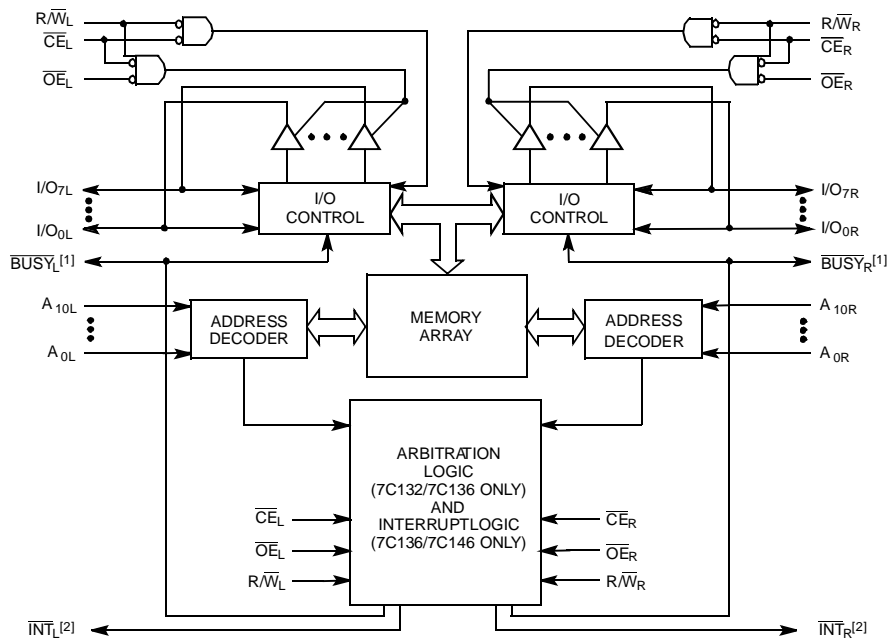
The CY7C132/CY7C136/CY7C142 and CY7C146 are high-speed CMOS 2K by 8 dual-port static RAMs. Two ports are provided to permit independent access to any location in memory. The CY7C132/ CY7C136 can be utilized as either a standalone 8-bit dual-port static RAM or as a MASTER dual-port RAM in conjunction with the CY7C142/CY7C146 SLAVE dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable (\overline{CE}), write enable (R/\overline{W}), and output enable (\overline{OE}). **BUSY** flags are provided on each port. In addition, an interrupt flag (**INT**) is provided on each port of the 52-pin PLCC version. **BUSY** signals that the port is trying to access the same location currently being accessed by the other port. On the PLCC version, **INT** is an interrupt flag indicating that data has been placed in a unique location (7FF for the left port and 7FE for the right port).

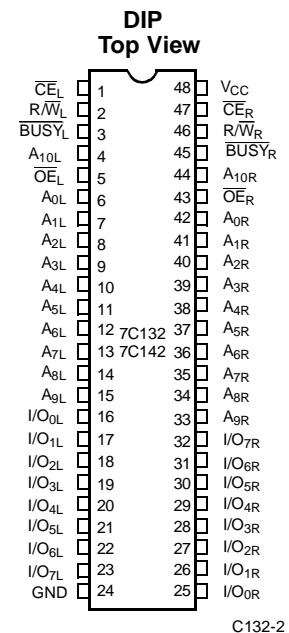
An automatic power-down feature is controlled independently on each port by the chip enable (\overline{CE}) pins.

The CY7C132/CY7C142 are available in 48-pin DIP. The CY7C136/CY7C146 are available in 52-pin PLCC and PQFP.

Logic Block Diagram



Pin Configuration



Notes:

1. CY7C132/CY7C136 (Master): **BUSY** is open drain output and requires pull-up resistor. CY7C142/CY7C146 (Slave): **BUSY** is input.
2. Open drain outputs; pull-up resistor required.

Electrical Characteristics Over the Operating Range^[5]

Parameter	Description	Test Conditions	7C136-15 ^[3] 7C146-15		7C132-30 ^[3] 7C136-25,30 7C142-30 7C146-25,30		7C132-35,45 7C136-35,45 7C142-35,45 7C146-35,45		7C132-55 7C136-55 7C142-55 7C146-55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	I _{OL} = 4.0 mA		0.4		0.4		0.4		0.4	V
		I _{OL} = 16.0 mA ^[6]		0.5		0.5		0.5		0.5	
V _{IH}	Input HIGH Voltage		2.2		2.2		2.2		2.2		V
V _{IL}	Input LOW Voltage			0.8		0.8		0.8		0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	-5	+5	-5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} = Max., V _{OUT} = GND		-350		-350		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	$\overline{CE} = V_{IL}$, Outputs Open, f = f _{MAX} ^[8]	Com'l	190		170		120		110	mA
			Mil					170		120	
I _{SB1}	Standby Current Both Ports, TTL Inputs	\overline{CE}_L and $\overline{CE}_R \geq V_{IH}$, f = f _{MAX} ^[8]	Com'l	75		65		45		35	mA
			Mil					65		45	
I _{SB2}	Standby Current One Port, TTL Inputs	\overline{CE}_L or $\overline{CE}_R \geq V_{IH}$, Active Port Outputs Open, f = f _{MAX} ^[8]	Com'l	135		115		90		75	mA
			Mil					115		90	
I _{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0	Com'l	15		15		15		15	mA
			Mil					15		15	
I _{SB4}	Standby Current One Port, CMOS Inputs	One Port \overline{CE}_L or $\overline{CE}_R \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, Active Port Outputs Open, f = f _{MAX} ^[8]	Com'l	125		105		85		70	mA
			Mil					105		85	

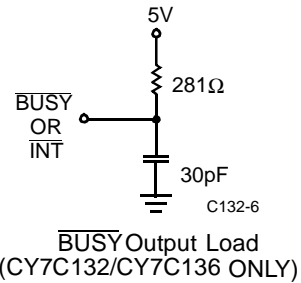
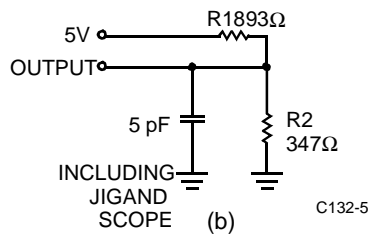
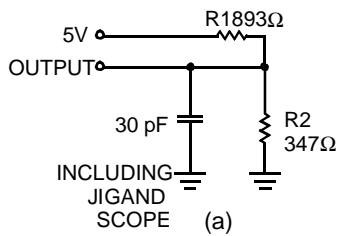
Shaded area contains preliminary information.

Capacitance^[9]

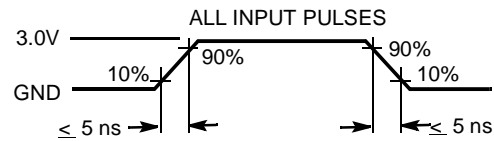
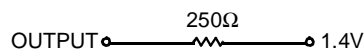
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz,	15	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.0V	10	pF

Notes:

- See the last page of this specification for Group A subgroup testing information.
- BUSY and INT pins only.
- Duration of the short circuit should not exceed 30 seconds.
- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of 1/t_{rc} and using AC Test Waveforms input levels of GND to 3V.
- This parameter is guaranteed but not tested.

AC Test Loads and Waveforms


Equivalent to: THÉVENIN EQUIVALENT


Switching Characteristics Over the Operating Range^[5, 10]

Parameter	Description	7C136-15 ^[3] 7C146-15		7C132-25 ^[3] 7C136-25 7C142-25 7C146-25		7C132-30 7C136-30 7C142-30 7C146-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	15		25		30		ns
t _{AA}	Address to Data Valid ^[11]		15		25		30	ns
t _{OHA}	Data Hold from Address Change	0		0		0		ns
t _{ACE}	\overline{CE} LOW to Data Valid ^[11]		15		25		30	ns
t _{DOE}	\overline{OE} LOW to Data Valid ^[11]		10		15		20	ns
t _{LZOE}	\overline{OE} LOW to Low Z ^[9, 12]	3		3		3		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[9, 12, 13]		10		15		15	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[9, 12]	3		5		5		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[9, 12, 13]		10		15		15	ns
t _{PU}	\overline{CE} LOW to Power-Up ^[9]	0		0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down ^[9]		15		25		25	ns
WRITE CYCLE^[14]								
t _{WC}	Write Cycle Time	15		25		30		ns
t _{SCE}	\overline{CE} LOW to Write End	12		20		25		ns
t _{AW}	Address Set-Up to Write End	12		20		25		ns
t _{HA}	Address Hold from Write End	2		2		2		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	R/ \overline{W} Pulse Width	12		15		25		ns
t _{SD}	Data Set-Up to Write End	10		15		15		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{HZWE}	R/ \overline{W} LOW to High Z ^[9]		10		15		15	ns
t _{LZWE}	R/ \overline{W} HIGH to Low Z ^[9]	0		0		0		ns

Switching Characteristics Over the Operating Range^[5, 10] (continued)

Parameter	Description	7C136-15 ^[3] 7C146-15		7C132-25 ^[3] 7C136-25 7C142-25 7C146-25		7C132-30 7C136-30 7C142-30 7C146-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING								
t _{BLA}	BUS \bar{Y} LOW from Address Match		15		20		20	ns
t _{BHA}	BUS \bar{Y} HIGH from Address Mismatch ^[15]		15		20		20	ns
t _{BLC}	BUS \bar{Y} LOW from $\bar{C}\bar{E}$ LOW		15		20		20	ns
t _{BHC}	BUS \bar{Y} HIGH from $\bar{C}\bar{E}$ HIGH ^[15]		15		20		20	ns
t _{PS}	Port Set Up for Priority	5		5		5		ns
t _{WB}	R/ \bar{W} LOW after BUS \bar{Y} LOW ^[16]	0		0		0		ns
t _{WH}	R/ \bar{W} HIGH after BUS \bar{Y} HIGH	13		20		30		ns
t _{BDD}	BUS \bar{Y} HIGH to Valid Data		15		25		30	ns
t _{DDD}	Write Data Valid to Read Data Valid		Note 17		Note 17		Note 17	ns
t _{WDD}	Write Pulse to Data Delay		Note 17		Note 17		Note 17	ns
INTERRUPT TIMING^[18]								
t _{WINS}	R/ \bar{W} to $\bar{I}\bar{N}\bar{T}\bar{E}\bar{R}\bar{R}\bar{U}\bar{P}\bar{T}$ Set Time		15		25		25	ns
t _{EINS}	$\bar{C}\bar{E}$ to $\bar{I}\bar{N}\bar{T}\bar{E}\bar{R}\bar{R}\bar{U}\bar{P}\bar{T}$ Set Time		15		25		25	ns
t _{INS}	Address to $\bar{I}\bar{N}\bar{T}\bar{E}\bar{R}\bar{R}\bar{U}\bar{P}\bar{T}$ Set Time		15		25		25	ns
t _{OINR}	$\bar{O}\bar{E}$ to $\bar{I}\bar{N}\bar{T}\bar{E}\bar{R}\bar{R}\bar{U}\bar{P}\bar{T}$ Reset Time ^[15]		15		25		25	ns
t _{EINR}	$\bar{C}\bar{E}$ to $\bar{I}\bar{N}\bar{T}\bar{E}\bar{R}\bar{R}\bar{U}\bar{P}\bar{T}$ Reset Time ^[15]		15		25		25	ns
t _{INR}	Address to $\bar{I}\bar{N}\bar{T}\bar{E}\bar{R}\bar{R}\bar{U}\bar{P}\bar{T}$ Reset Time ^[15]		15		25		25	ns

Shaded area contains preliminary information.

Switching Characteristics Over the Operating Range^[5, 10]

Parameter	Description	7C132-35 7C136-35 7C142-35 7C146-35		7C132-45 7C136-45 7C142-45 7C146-45		7C132-55 7C136-55 7C142-55 7C146-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	35		45		55		ns
t _{AA}	Address to Data Valid ^[11]		35		45		55	ns
t _{OHA}	Data Hold from Address Change	0		0		0		ns
t _{ACE}	$\bar{C}\bar{E}$ LOW to Data Valid ^[11]		35		45		55	ns
t _{DOE}	$\bar{O}\bar{E}$ LOW to Data Valid ^[11]		20		25		25	ns
t _{LZOE}	$\bar{O}\bar{E}$ LOW to Low Z ^[9, 12]	3		3		3		ns
t _{HZOE}	$\bar{O}\bar{E}$ HIGH to High Z ^[9, 12, 13]		20		20		25	ns
t _{LZCE}	$\bar{C}\bar{E}$ LOW to Low Z ^[9, 12]	5		5		5		ns
t _{HZCE}	$\bar{C}\bar{E}$ HIGH to High Z ^[9, 12, 13]		20		20		25	ns
t _{PU}	$\bar{C}\bar{E}$ LOW to Power-Up ^[9]	0		0		0		ns
t _{PD}	$\bar{C}\bar{E}$ HIGH to Power-Down ^[9]		35		35		35	ns

Switching Characteristics Over the Operating Range^[5, 10] (continued)

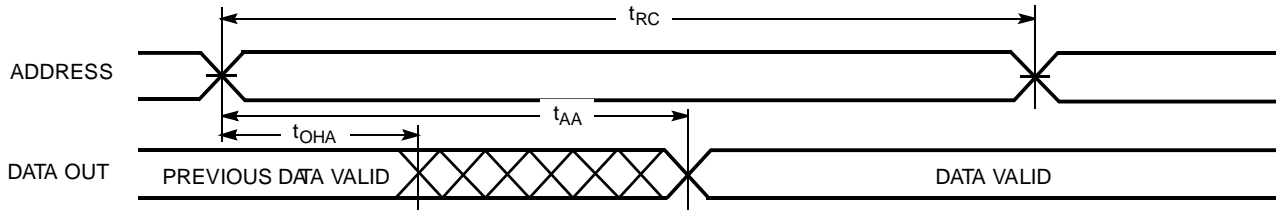
		7C132-35 7C136-35 7C142-35 7C146-35	7C132-45 7C136-45 7C142-45 7C146-45	7C132-55 7C136-55 7C142-55 7C146-55		
WRITE CYCLE^[14]						
t _{WC}	Write Cycle Time	35	45	55		ns
t _{SCE}	\overline{CE} LOW to Write End	30	35	40		ns
t _{AW}	Address Set-Up to Write End	30	35	40		ns
t _{HA}	Address Hold from Write End	2	2	2		ns
t _{SA}	Address Set-Up to Write Start	0	0	0		ns
t _{PWE}	R/ \overline{W} Pulse Width	25	30	30		ns
t _{SD}	Data Set-Up to Write End	15	20	20		ns
t _{HD}	Data Hold from Write End	0	0	0		ns
t _{HZWE}	R/ \overline{W} LOW to High Z ^[9]		20	20		25 ns
t _{LZWE}	R/ \overline{W} HIGH to Low Z ^[9]	0	0	0		ns
BUSY/INTERRUPT TIMING						
t _{BLA}	\overline{BUSY} LOW from Address Match		20	25		30 ns
t _{BHA}	\overline{BUSY} HIGH from Address Mismatch ^[15]		20	25		30 ns
t _{BLC}	\overline{BUSY} LOW from \overline{CE} LOW		20	25		30 ns
t _{BHC}	\overline{BUSY} HIGH from \overline{CE} HIGH ^[15]		20	25		30 ns
t _{PS}	Port Set Up for Priority	5	5	5		ns
t _{WB}	R/ \overline{W} LOW after \overline{BUSY} LOW ^[16]	0	0	0		ns
t _{WH}	R/ \overline{W} HIGH after \overline{BUSY} HIGH	30	35	35		ns
t _{BDD}	\overline{BUSY} HIGH to Valid Data		35	45		45 ns
t _{DDD}	Write Data Valid to Read Data Valid		Note 17	Note 17		Note 17 ns
t _{WDD}	Write Pulse to Data Delay		Note 17	Note 17		Note 17 ns
INTERRUPT TIMING^[18]						
t _{WINS}	R/ \overline{W} to $\overline{INTERRUPT}$ Set Time		25	35		45 ns
t _{EINS}	\overline{CE} to $\overline{INTERRUPT}$ Set Time		25	35		45 ns
t _{INS}	Address to $\overline{INTERRUPT}$ Set Time		25	35		45 ns
t _{OINR}	\overline{OE} to $\overline{INTERRUPT}$ Reset Time ^[15]		25	35		45 ns
t _{EINR}	\overline{CE} to $\overline{INTERRUPT}$ Reset Time ^[15]		25	35		45 ns
t _{INR}	Address to $\overline{INTERRUPT}$ Reset Time ^[15]		25	35		45 ns

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- AC test conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
- At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
- t_{LZCE}, t_{LZOE}, t_{HZCE}, t_{HZOE}, and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and R/ \overline{W} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
- CY7C142/CY7C146 only.
- A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
 BUSY on Port B goes HIGH.
 Port B's address toggled.
 \overline{CE} for Port B is toggled.
 R/ \overline{W} for Port B is toggled during valid read.
- 52-pin PLCC and PQFP versions only.

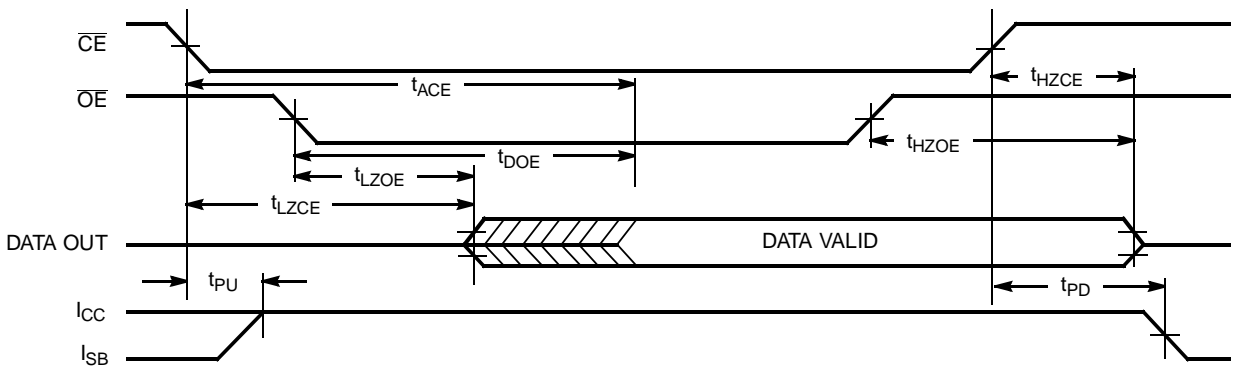
Switching Waveforms

Read Cycle No. 1 (Either Port-Address Access)^[19, 20]



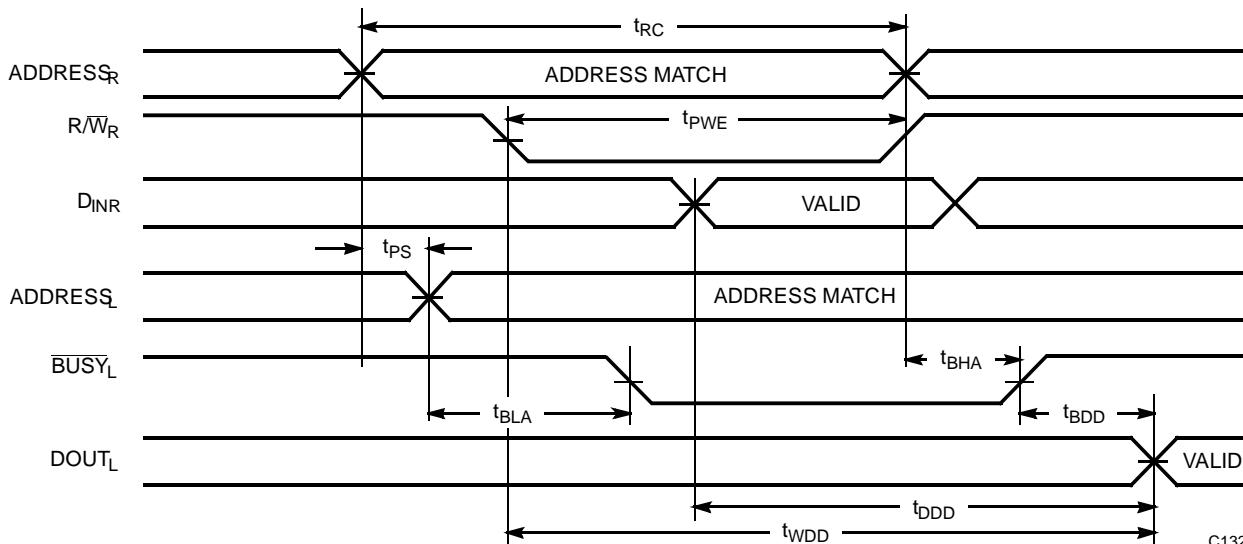
C132-7

Read Cycle No. 2 (Either Port- $\overline{CE}/\overline{OE}$)^[19, 21]



C132-8

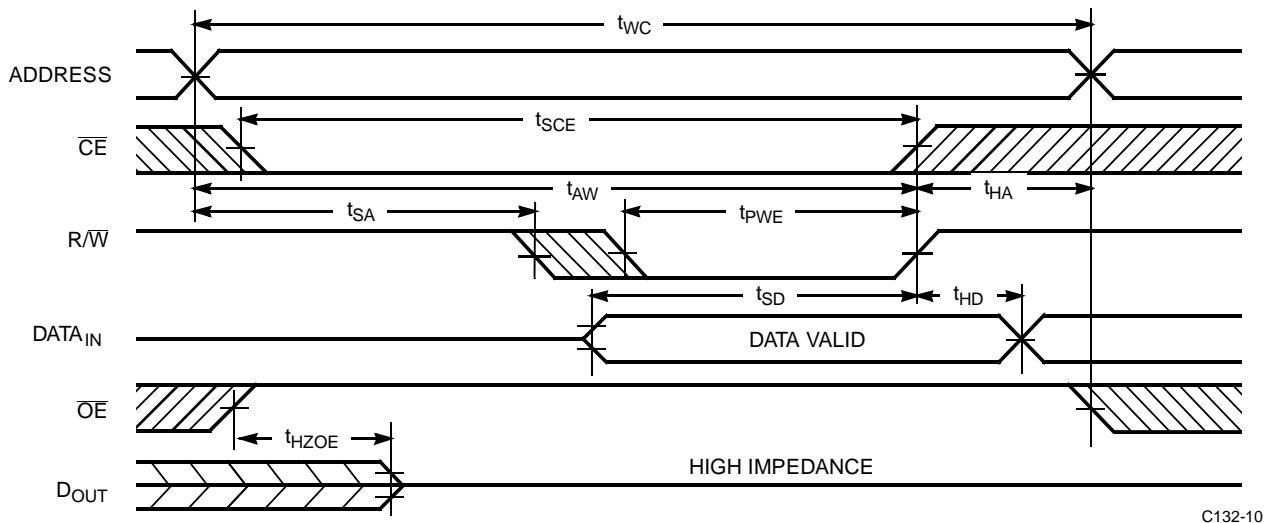
Read Cycle No. 3 (Read with BUSY Master: CY7C132 and CY7C136)



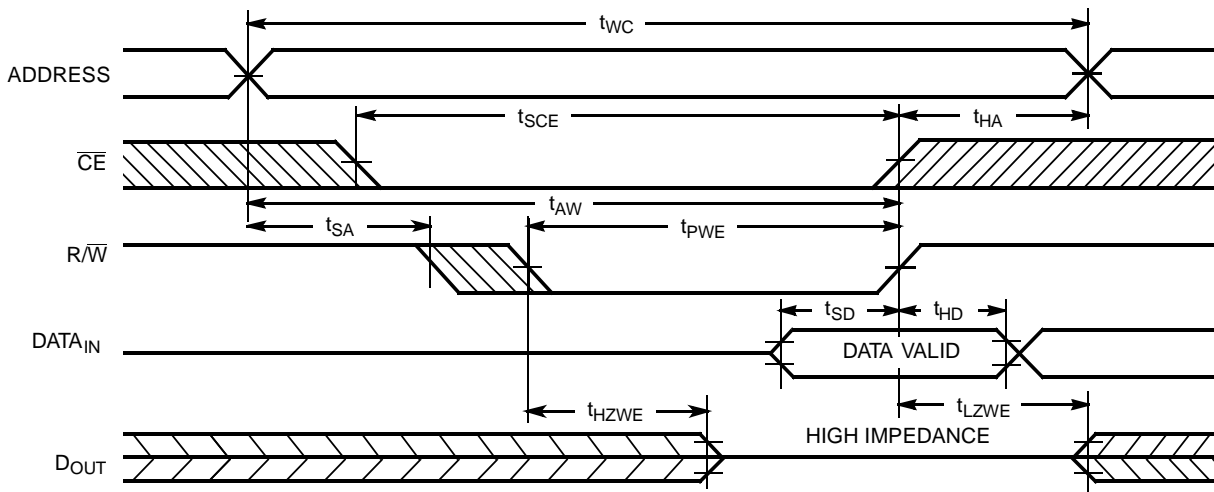
C132-9

Notes:

19. R/ \overline{W} is HIGH for read cycle.
20. Device is continuously selected, $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IL}$.
21. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)
Write Cycle No.1 (\overline{OE} Three-States Data I/Os—Either Port)^[14, 22]


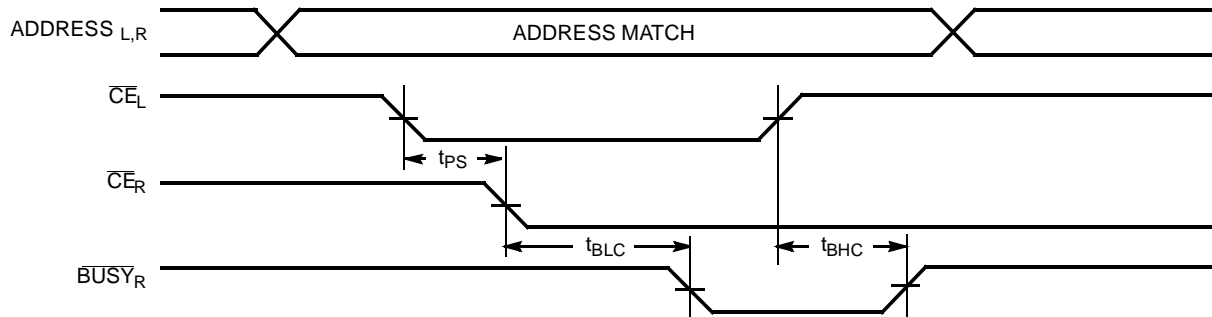
C132-10

Write Cycle No. 2 (R/\overline{W} Three-States Data I/Os—Either Port)^[14, 23]


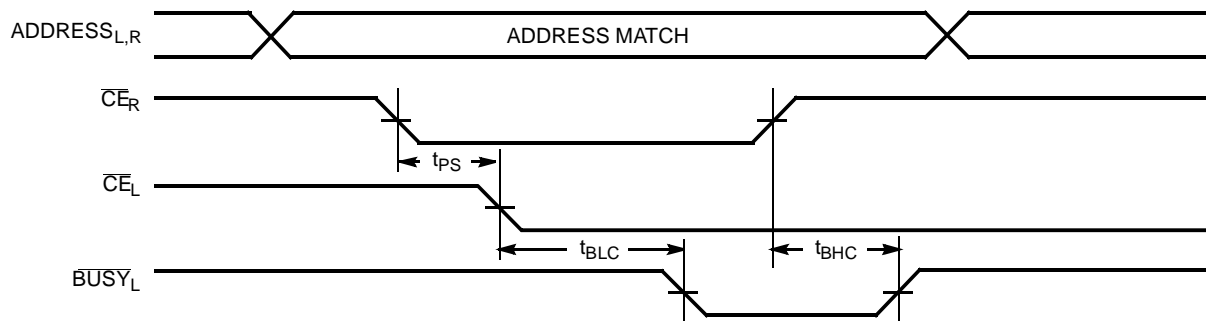
C132-11

Notes:

22. If \overline{OE} is LOW during a R/\overline{W} controlled write cycle, the write pulse width must be the larger of t_{PWE} or $t_{HZWE} + t_{SD}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD} .
23. If the \overline{CE} LOW transition occurs simultaneously with or after the R/\overline{W} LOW transition, the outputs remain in a high-impedance state.

Switching Waveforms (continued)
Busy Timing Diagram No. 1 (\overline{CE} Arbitration)
 \overline{CE}_L Valid First:


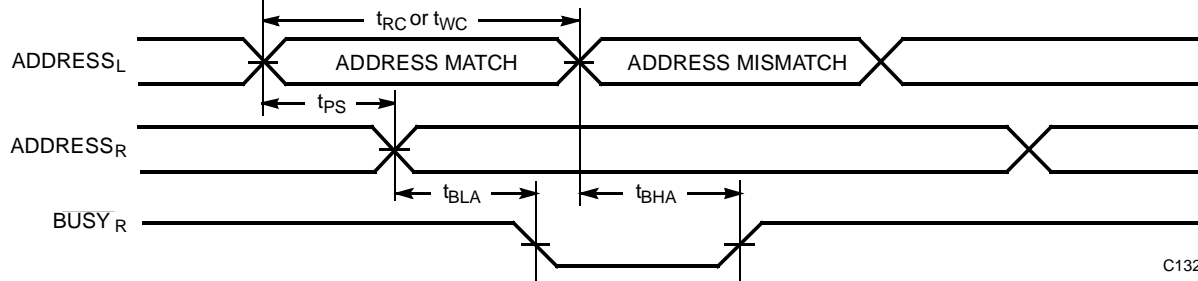
C132-12

 \overline{CE}_R Valid First:


C132-13

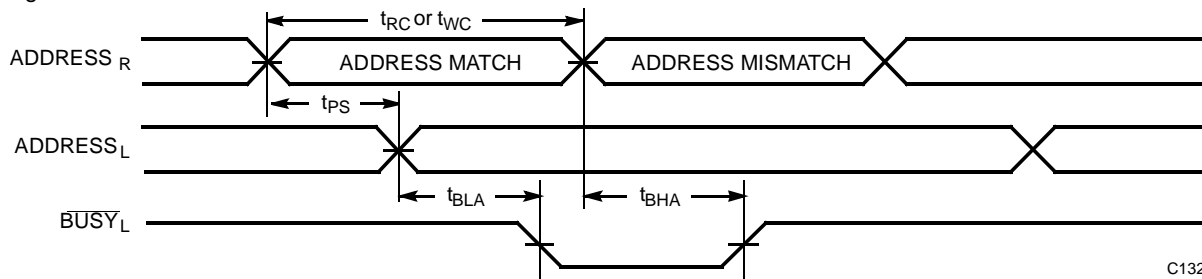
Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:



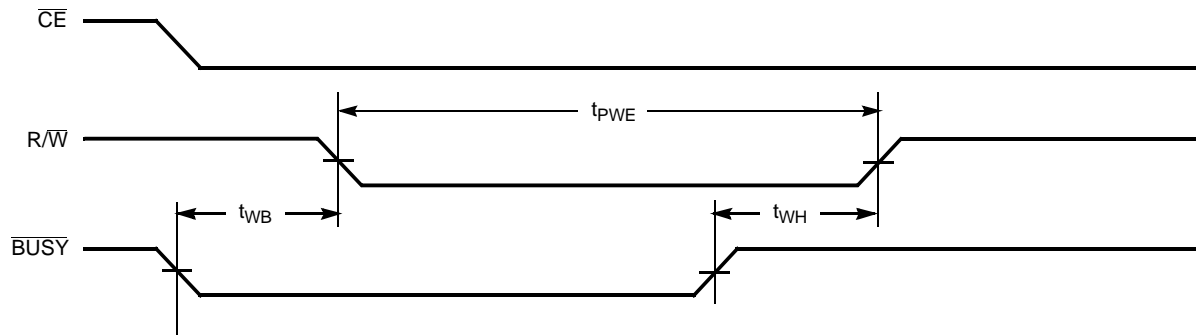
C132-14

Right Address Valid First:

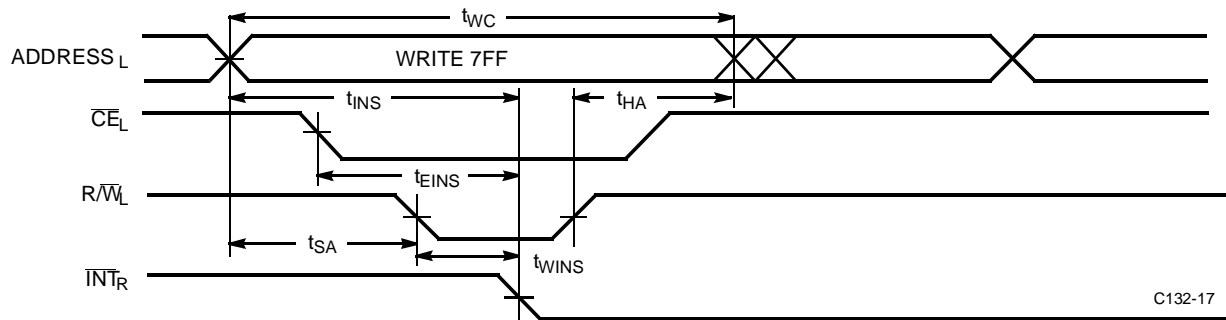


C132-15

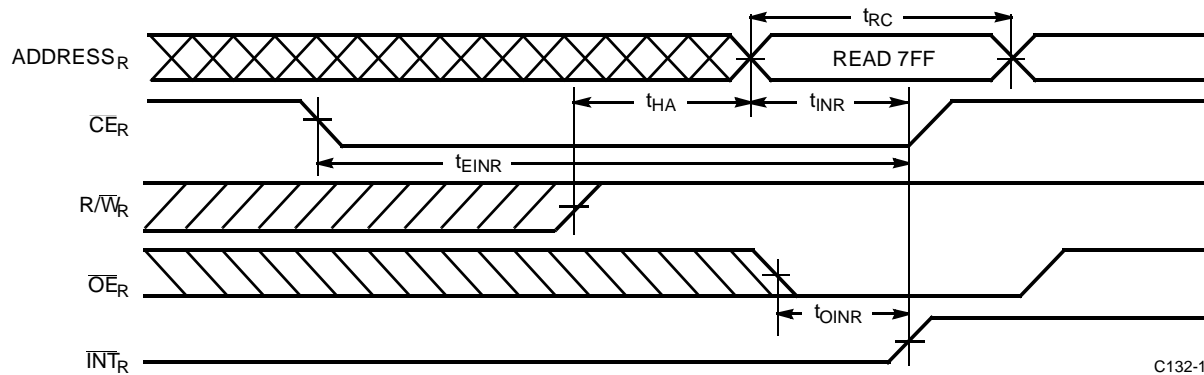
Switching Waveforms (continued)

Busy Timing Diagram No. 3 (Write with $\overline{\text{BUSY}}$, Slave: CY7C142/CY7C146)


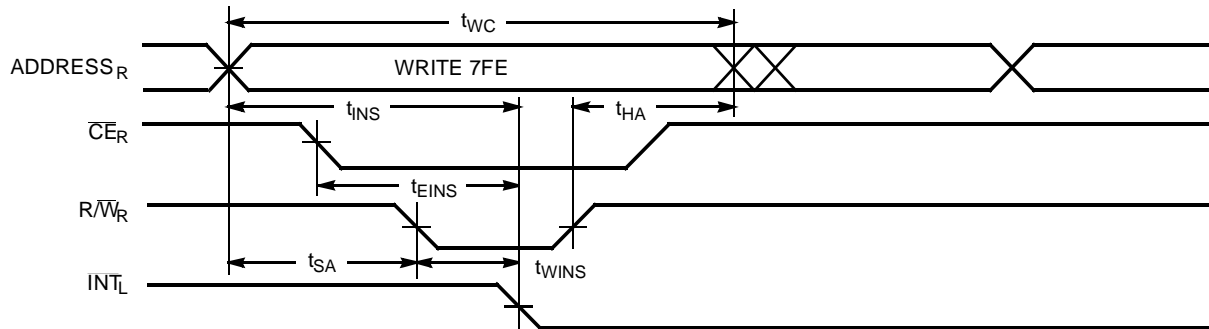
C132-16

Interrupt Timing Diagrams^[18]
Left Side Sets $\overline{\text{INT}}_R$:


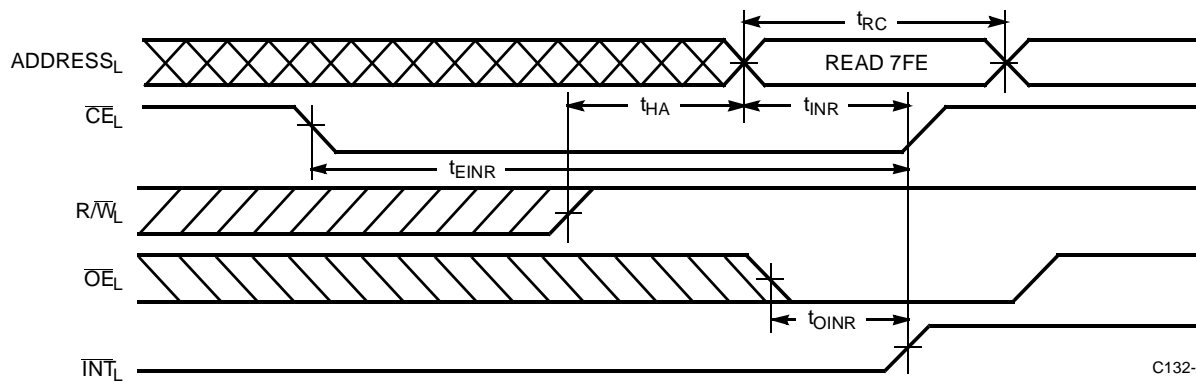
C132-17

Right Side Clears $\overline{\text{INT}}_R$:


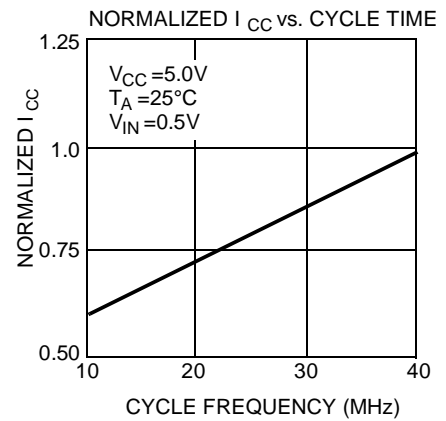
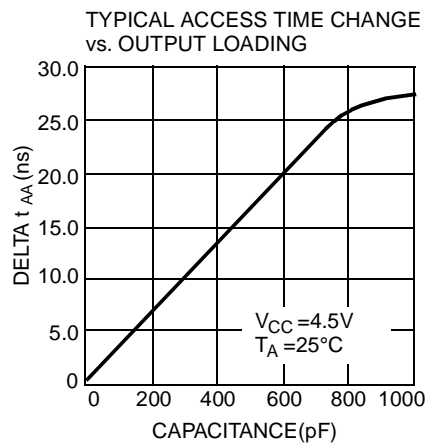
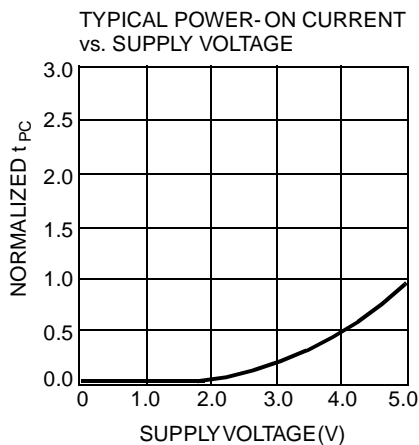
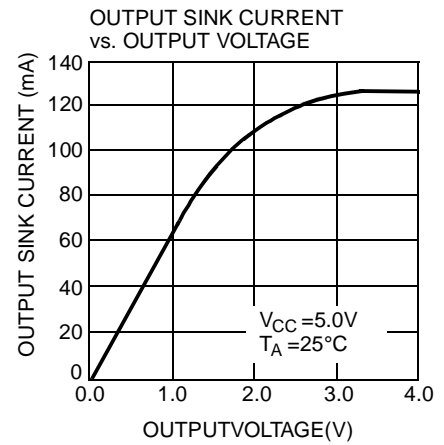
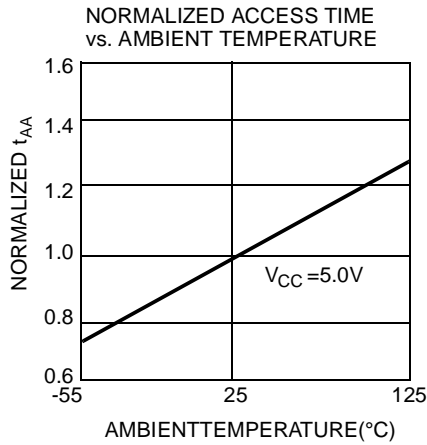
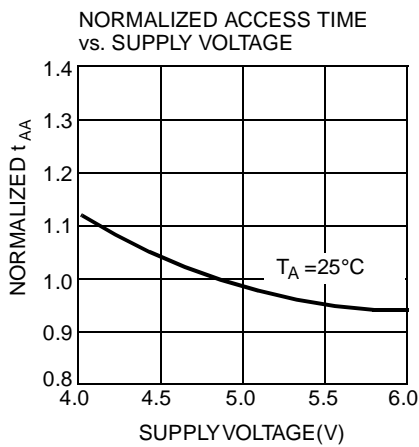
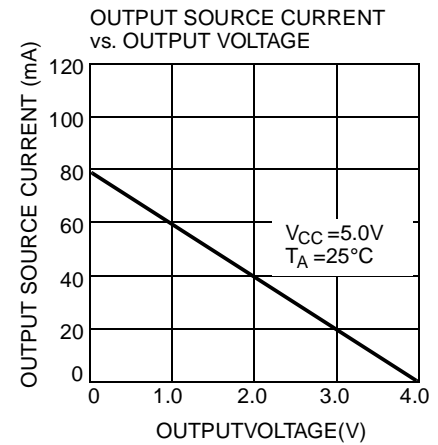
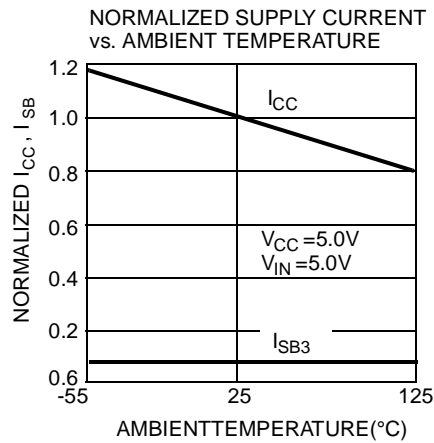
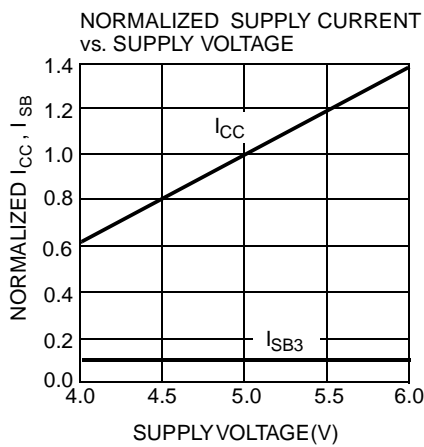
C132-18

Interrupt Timing Diagrams^[18] (continued)
Right Side Sets \overline{INT}_L :


C132-19

Right Side Clears \overline{INT}_L :


C132-20

Typical DC and AC Characteristics


Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C132-30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132-30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C132-35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132-35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132-35DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
45	CY7C132-45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132-45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132-45DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
55	CY7C132-55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132-55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132-55DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C136-15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-15NC	N52	52-Pin Plastic Quad Flatpack	
25	CY7C136-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-25NC	N52	52-Pin Plastic Quad Flatpack	
30	CY7C136-30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136-30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C136-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136-35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C136-45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136-45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136-45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C136-55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C136-55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136-55LMB	L69	52-Square Leadless Chip Carrier	Military

Shaded area contains preliminary information.

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C142-30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142-30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C142-35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142-35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142-35DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
45	CY7C142-45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142-45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142-45DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
55	CY7C142-55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142-55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142-55DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C136-15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-15NC	N52	52-Pin Plastic Quad Flatpack	
25	CY7C146-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146-25NC	N52	52-Pin Plastic Quad Flatpack	
30	CY7C146-30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146-30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C146-30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C146-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146-35NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C146-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146-35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C146-45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146-45NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C146-45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146-45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C146-55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146-55NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C146-55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146-55LMB	L69	52-Square Leadless Chip Carrier	Military

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{WINS}	7, 8, 9, 10, 11
t_{EINS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{OINR}	7, 8, 9, 10, 11
t_{EINR}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
$t_{WB}^{[24]}$	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11

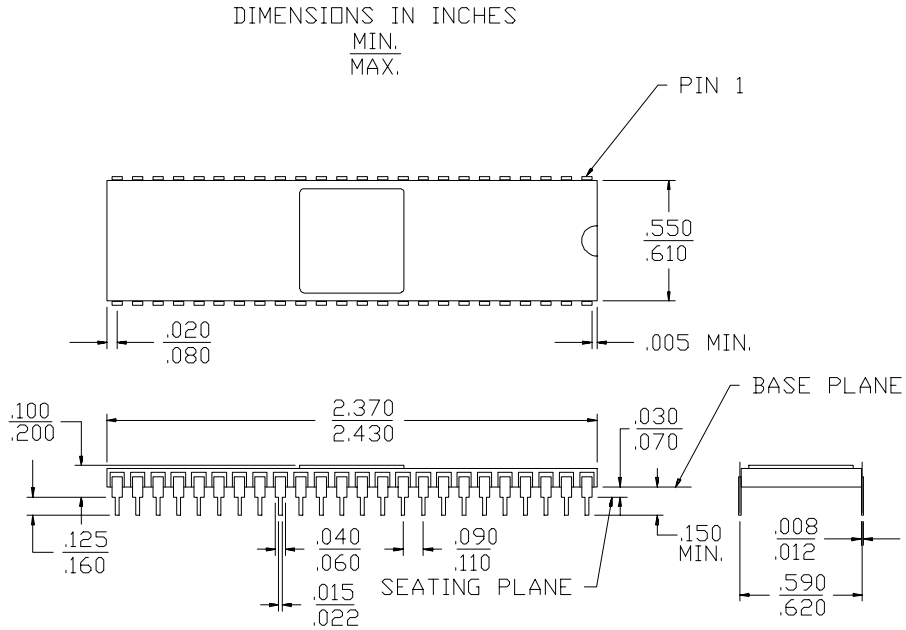
Note:

24. CY7C142/CY7C146 only.

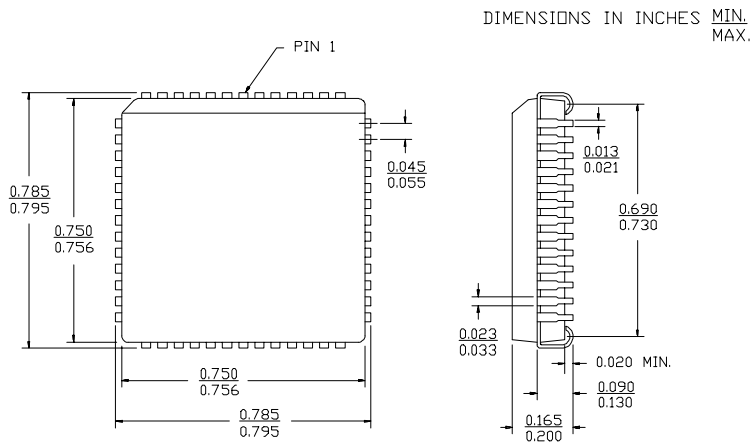
Document #: 38-00061-L

Package Diagrams

48-Lead (600-Mil) Sidebrazed DIP D26

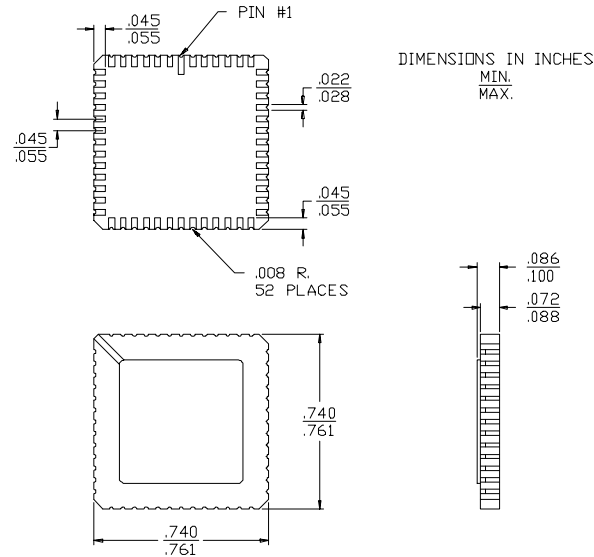


52-Lead Plastic Leaded Chip Carrier J69



Package Diagrams (continued)

52-Square Leadless Chip Carrier L69



52-Lead Plastic Quad Flatpack N52

