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12-OUTPUT BiCMOS PLL CLOCK GENERATOR S4406

FEATURES

- Generates outputs from 10 MHz to 66 MHz
- Four groups of three outputs (12 outputs total)
- Eight user-selectable output functions for each group
- TTL compatible outputs, with <1.5-ns edge rates
- Performs clock doubling, dividing, invert, lead/lag placement
- Internal VCO running between 160 to 266 MHz
- 1.0µ BiCMOS technology
- Output skew less than 500 ps
- 52 PQFP package

APPLICATIONS

- High-performance microprocessor systems
- CMOS ASIC systems
- Backplane clock deskew and distribution
- Compatible with Intel's Pentium™ processor

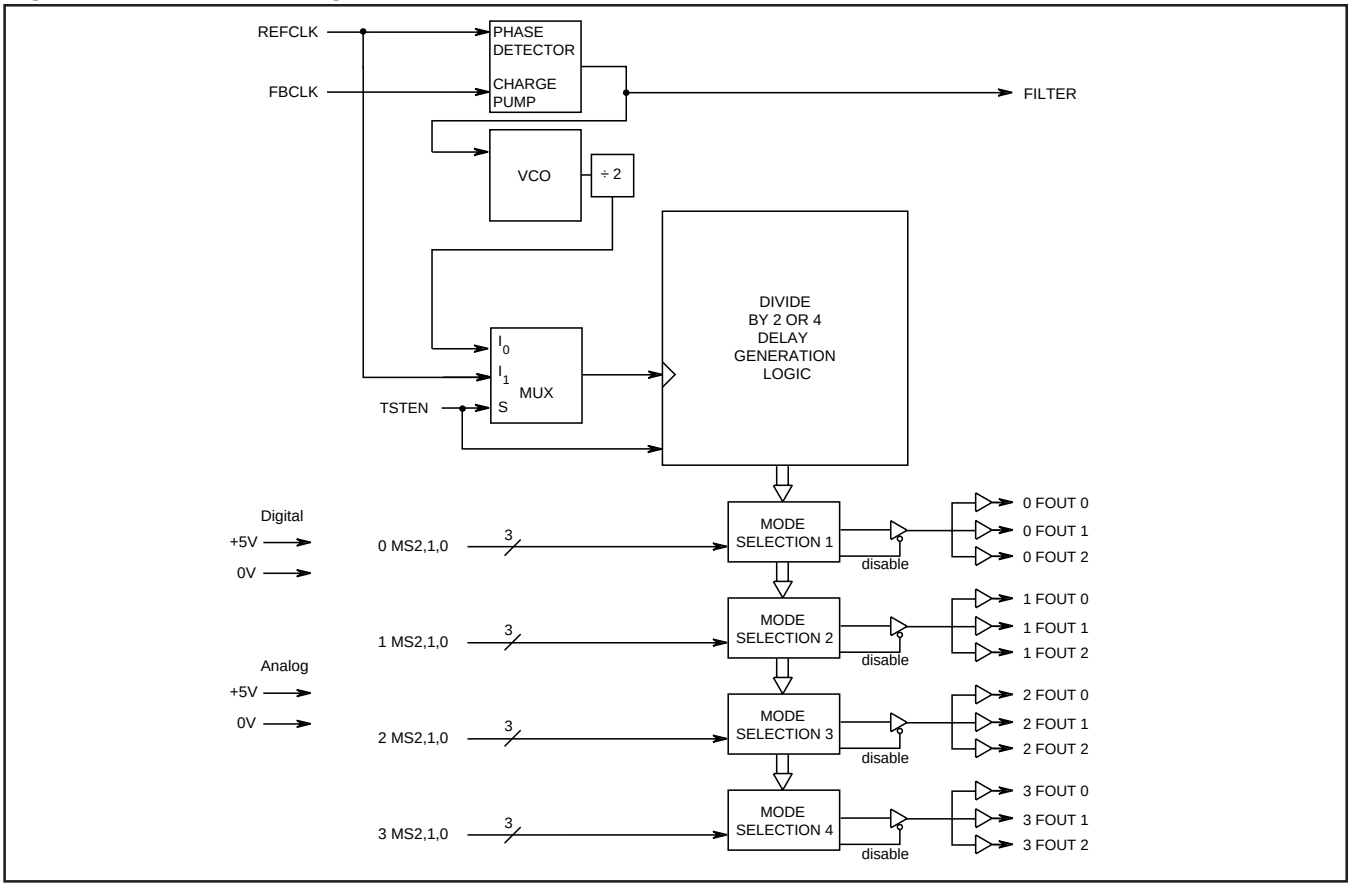
GENERAL DESCRIPTION

The S4406 BiCMOS clock generator provides 12 TTL outputs with less than 500 ps of skew. Implemented in AMCC's 1.0µ BiCMOS technology, the internal PLL and divider/delay selector logic allow the user to individually tailor the (4) TTL output groups to the system's needs. The internal VCO can operate between 160 to 266 MHz, and the programmability allows the user to generate output clocks in the 20–66 MHz range.

The S4406 offers the user the ability to select the appropriate phase and frequency relationship for each of the four groups of three TTL clock outputs.

In addition to clock doubling and inversion functions, the S4406 allows any output groups to lead or lag the others by the minimum phase delay of 3.75–6.25 ns.

Figure 1. S4406 Block Diagram



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FUNCTIONAL DESCRIPTION

The 12 xFOUT0–2 outputs are the main TTL output clocks that the generator supplies. The mode selection choices are shown in Table 1 and waveform definitions are given in Figure 2. The "x" represents the output group number (1–4). The frequency of these outputs is determined by the REFCLK clock frequency and the output clock that is tied to the FBCLK input (xFOUT0–2 can be equal to REFCLK, half of REFCLK, or twice the frequency of REFCLK).

Example:

In order to meet bus timing specifications for a typical system, designers may need three outputs at 66 MHz for the system clock and processor, a 33-MHz output for the cache controller, and a 33-MHz delayed output for a memory management unit. This system requirement can be met using the S4406 by setting the mode select pins for the first group of outputs (0MS2,1,0) to 111, the second group (1MS2,1,0) to 110, and the third group (2MS2,1,0) to 101. In this configuration, one of the 33-MHz outputs should be fed back to the FBCLK input. This example makes use of only three of the four output banks, leaving the fourth available for any other clock signals needed.

Table 1. Mode Selection Options

xMS2,1,0	MODE DESCRIPTION	xFOUT0,1,2
000	Disabled.	Logical Hi
001	All three outputs at the fundamental output frequency, but early by a minimum phase delay.	f – t
010	All three outputs at half the fundamental output frequency and inverted.	I /2
011	All three outputs at the fundamental output frequency and inverted.	I
100	All three outputs at half the fundamental output frequency, but delayed by a minimum phase delay.	f/2 + t
101	All three outputs at the fundamental output frequency, but delayed by a minimum phase delay.	f + t
110	All three outputs at half the fundamental output frequency.	f/2
111	All three outputs at the fundamental output frequency.	f

Note: If f is fed back, the fundamental frequency is equal to REFCLK.
If f/2 is fed back, the fundamental frequency is twice REFCLK.

Filter

FILTER is the analog signal from the phase detector going into the VCO. This pin is provided so a simple external filter (a single capacitor and resistor) can be included in the phase locked loop of the clock generator. See Figure 3.

Phase Delay

The minimum phase delay between xFOUT0–2 signals is a function of the VCO frequency. The VCO frequency can be determined by multiplying the fundamental output frequency by four, or half the fundamental frequency by eight. The minimum phase delay is equal to the period of the VCO frequency: t = 1/(VCO freq). Since the VCO can operate in the 160-MHz to 266-MHz range, the range of minimum phase delay values is 6.25 ns to 3.75 ns (See Table 2).

Figure 2. Waveform Definitions

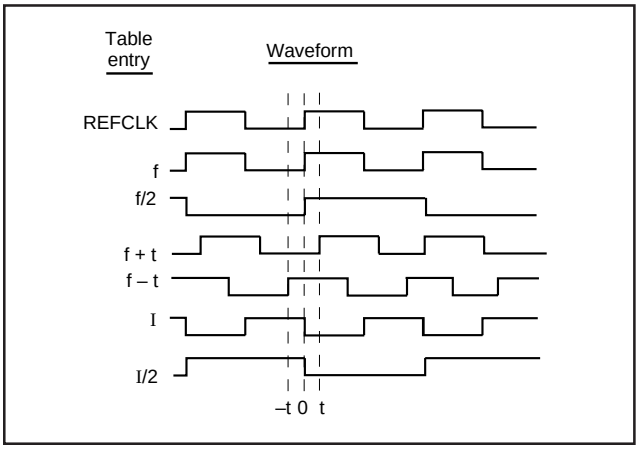
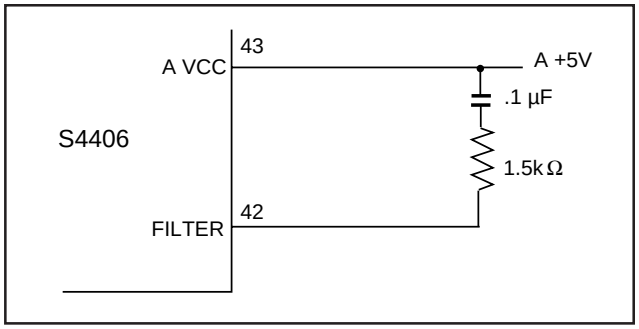


Figure 3. External PLL Filter



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Test Capabilities

TESTEN allows the chip to use the REFCLK input instead of the VCO output to clock the chip. This is used during chip test to allow the counters and control logic to be tested independently of the VCO. In addition, when TESTEN is brought High, an internal RESET pulse is generated. This initializes the internal counter flip-flops to zeros, and at the end of the next clock cycle, the outputs go to a zero state. TESTEN can also be used for board testing to allow the user to control the output clocks from the S4406 by inputting the board clock to the REFCLK input.

Table 2. VCO Operating Frequencies

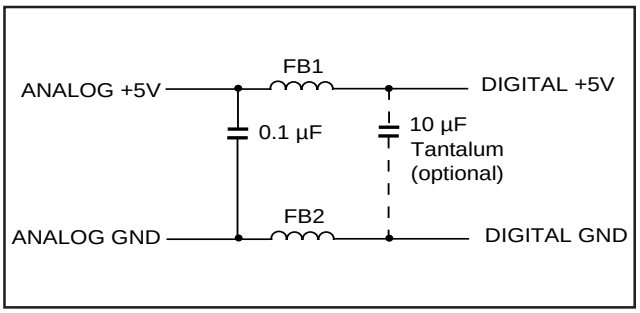
xFOUT0–2	VCO FREQ	MIN PHASE DELAY
66.6 MHz	266 MHz	3.750 ns
50 MHz	200 MHz	5.000 ns
40 MHz	160 MHz	6.250 ns
33.3 MHz	266 MHz	3.750 ns
25 MHz	200 MHz	5.000 ns
20 MHz	160 MHz	6.250 ns

The bank containing the output used as feedback must be in one of the f/2 modes to ensure the VCO is operating within its 160-266 MHz range.

Power Supply Considerations

Power for the analog portion of the S4406 chips must be isolated from the digital power supplies to minimize noise on the analog power supply pins. This isolation between the analog and digital power supplies can be accomplished with a simple external power supply filter (Figure 4). The analog power planes are connected to the digital power planes through single ferrite beads (FB1 and FB2) or inductors capable of handling 25 mA. The recommended value for the inductors is in the range from 5 to 100µH, and depends upon the frequency spectrum of the digital power supply noise.

Figure 4. External Power Supply Filter



Decoupling capacitors are also very important to minimize noise. The decoupling capacitors must have low lead inductance to be effective, so ceramic chip capacitors are recommended. Decoupling capacitors should be located as close to the power pins as physically possible. And the decoupling should be placed on the top surface of the board between the part and its connections to the power and ground planes.

BOARD LAYOUT CONSIDERATIONS

• The S4406 chips are sensitive to noise on the Analog +5 V and Filter pins. Care should be taken during board layout for optimum results.

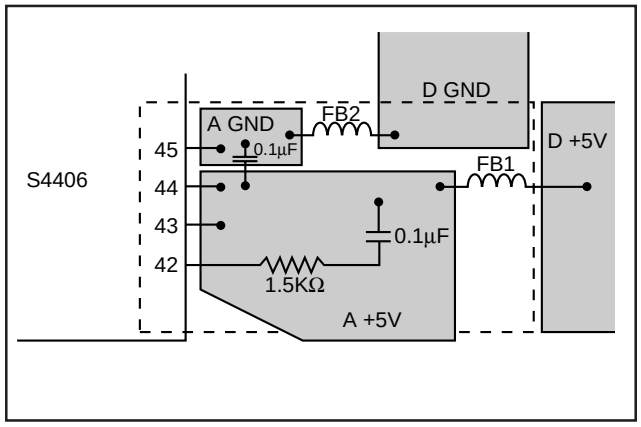
• All decoupling capacitors (C1–C4 = 0.1 µF) should be bypassed between VCC and GND, and placed as close to the chip as possible (preferably using ceramic chip caps) and placed on top of board between S4406 and the power and ground plane connections.

• No dynamic signal lines should pass through or beneath the filter circuitry area (enclosed by dashed lines in Figure 5) to avoid the possibility of noise due to crosstalk.

• The analog VCC supply can be a filtered digital VCC supply as shown below. The ferrite beads or inductors, FB1 and FB2, should be placed within three inches of the chip.

• The analog VCC plane should be separated from the digital VCC and ground planes by at least 1/8 inch.

Figure 5. Board Layout



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PIN DESCRIPTIONS

Input Signals

REFCLK. Frequency reference supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the outputs. Also replaces the VCO output when TSTEN is high (after first divide-by-two stage in divider phase control logic). See TSTEN.

FBCLK. Feedback clock that, along with the REFCLK input, determines the frequency of the outputs. One output is selected to feed back to this input.

TSTEN. Active High. Allows REFCLK to drive the divider phase adjust circuitry, after the first divide-by-two stage. Also, when brought High, generates an internal Reset pulse that initializes the internal counter flip-flops to zero.

xMS2,1,0. Mode selection inputs that allow selection of the phase and frequency relationship of each of the four banks of three clock outputs. The “x” represents the output group number (0–3). Refer to Table 1 for mode selection options.

Output Signals

FILTER. A tap between the analog output of the phase detector and the VCO input. Allows a simple external filter (a single resistor and one capacitor) to be included in the PLL.

xFOUT0–2. Clock signal outputs. Refer to Table 1 and Figure 4 for a description of output options.

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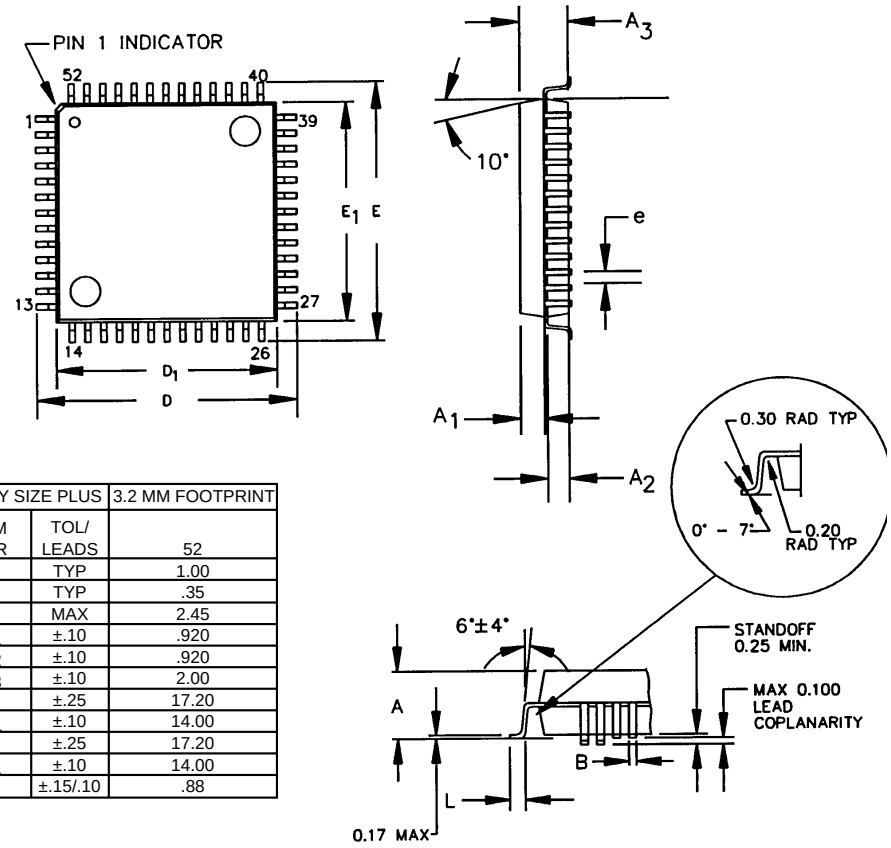
Figure 6. 52–pin PQFP Package



BODY SIZE PLUS	3.2 MM FOOTPRINT	
DIM LTR	TOL/ LEADS	52
e	TYP	1.00
B	TYP	.35
A	MAX	2.45
A_1	±.10	.920
A_2	±.10	.920
A_3	±.10	2.00
D	±.25	17.20
D_1	±.10	14.00
E	±.25	17.20
E_1	±.10	14.00
L	±.15/.10	.88

All dimensions in mm.

DC CHARACTERISTICS

Symbol	Parameter	DC Test Conditions		Min	Typ[1]	Max	Units
V_{IH}[2]	Input HIGH Voltage	Guaranteed input HIGH voltage for all inputs		2.0			V
V_{IL}[2]	Input LOW Voltage	Guaranteed input LOW voltage for all inputs				0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = -18 mA			-0.8	-1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min	I_{OH} = -12 mA[3]	2.4			V
			I_{OH} = -24 mA[3]	2.0			V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 24 mA[3]				0.5	V
I_{IH}	Input HIGH Current	V_{CC} = Min, V_{IN} = 2.4V	4MS2,3MS2,1,0			-200	µA
			Other			50	µA
I_I	Input HIGH Current at Max	V_{CC} = Max, V_{IN} = V_{CC}				1.0	mA
I_{IL}	Input LOW Current	V_{CC} = Min, V_{IN} = 0.5V	4MS2,3MS2,1,0			-500	µA
			Other			-50	µA
I_{OS}[4]	Output short circuit current	V_{CC} = Max, V_{OUT} = 0V		-25		-100	mA
I_{CC}	Static	V_{CC} = Max				70	mA
I_{CCT}	Total I_{CC} (Dynamic and Static)	C_{LOAD} = 25 pF at 50 MHz				200	mA

1. Typical limits are at 25°C, V_{CC} = 5.0V.
2. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.
3. I_{OH}/I_{OL} values indicated are for DC test correlation. Actual dynamic currents are significantly higher.
4. Maximum test duration one second.

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ABSOLUTE MAXIMUM RATINGS

TTL Supply Voltage VCC (VEE = 0)	7.0 V
TTL Input Voltage (VEE = 0)	5.5 V
Operating Temperature	0°C to 70°C ambient
Operating Junction Temperature TJ	+ 130°C
Storage Temperature	–65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Nom	Max	Units
TTL Supply Voltage (VCC)	4.75	5.0	5.25	V
Operating Temperature	0 (ambient)	—	70 (ambient)	°C
Junction Temperature	—	—	130	°C

Table 3. AC Specifications

Symbol	Description	Min	Max	Units
f_{VCO}	VCO Frequency	160	266	MHz
f_{REF}	REFCLK Frequency	10	66	MHz
t_{IRF}	Input Rise/Fall Time	1	3	ns
MPW_{REF}	REFCLK Minimum Pulse Width	5.0		ns
t_{PE}	Phase Error between REFCLK and FBCLK	-1.0	0	ns
t_{PED}	Phase Error Difference from Part to Part[1]	0	750	ps
t_{SKEW}	Output Skew[2] across all outputs	0	500	ps
t_{SKEWA}	Output Skew[2] within any bank	0	250	ps
t_{DC}	Output Duty Cycle[3]	45	55	%
f_{FOUT}	FOUT Frequency[4]	10	66	MHz
t_{PS}	Nominal Phase Shift Increment[5]	3.75	6.25	ns
t_j	Clock Stability[6]		500	ps
t_{ORF}	FOUT Rise/Fall Time[7]	0.5	1.5	ns
t_{LOCK}	Loop Acquisition Time[8]		5	ms
t_{PSV}	Phase Shift Variation[5]	-250	+250	ps

1. Difference in phase error between two parts at the same voltage, temperature and frequency.
2. Output skew guaranteed for equal loading at each output.
3. Outputs loaded with 35 pF, measured at 1.5 V.
4. C_{LOAD} = 35 pF.
5. All phase shift increments and variation are measured relative to 0FOUT0 at 1.5 V.
6. Clock period jitter with all FOUT outputs operating at 66MHz loaded with 25 pF using loop filter shown. Parameter guaranteed, but not tested.
7. With 35 pF output loading (0.8 V to 2.0 V transition).
8. Depends on loop filter chosen. (Number given is for example filter.)

Figure 7. Timing Waveforms

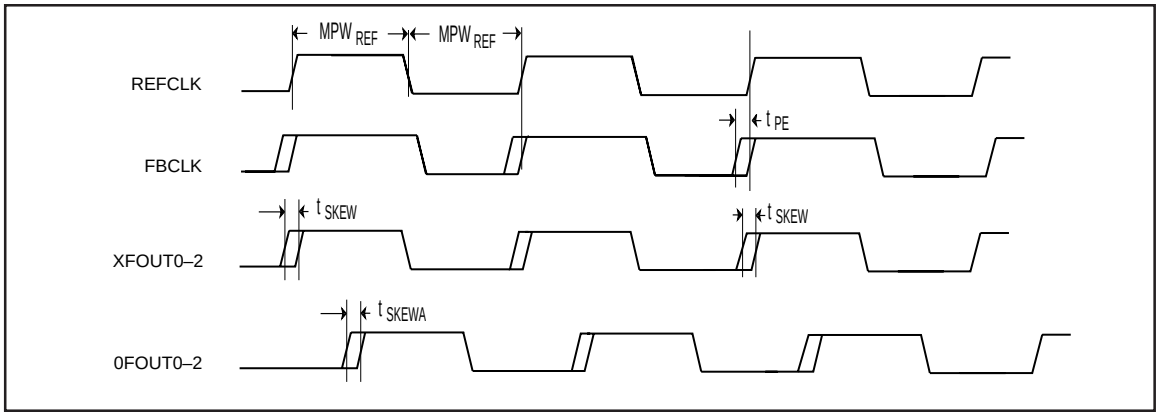

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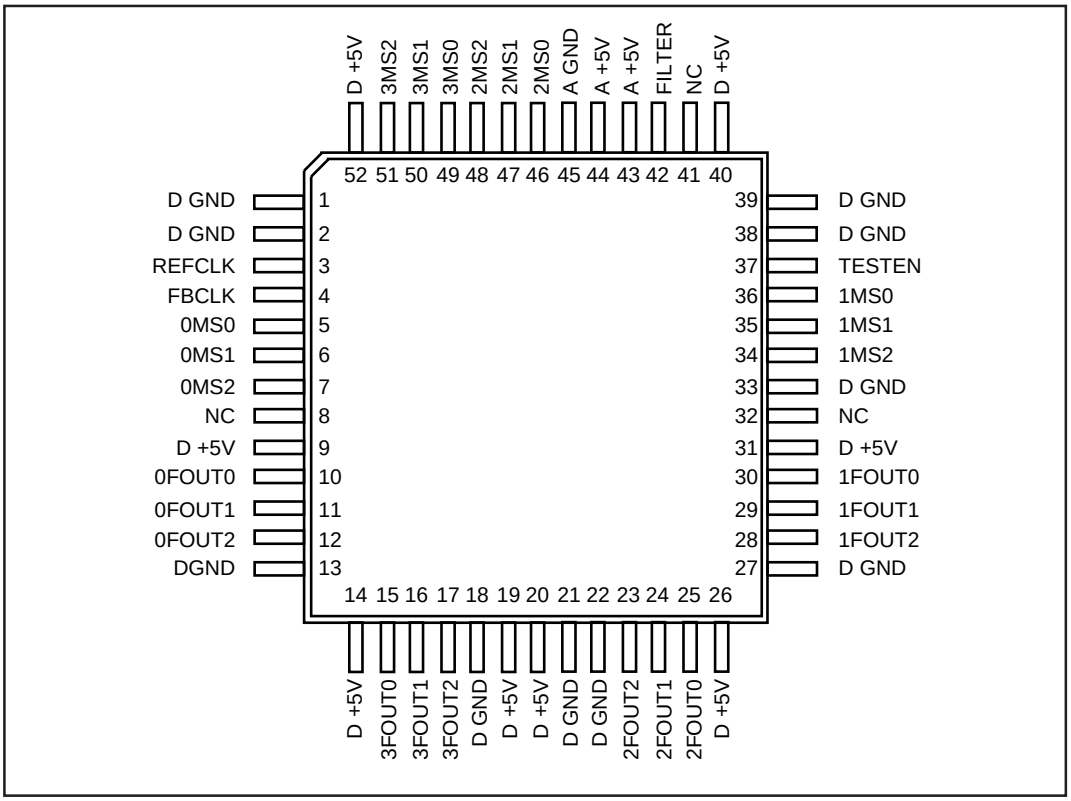
Figure 8. S4406 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Speed Option (if applicable)**
- **Optional Shipping Configuration**

S4406 **Q** **– 66** **/TD**

Optional Shipping Configuration
Blank = 84-unit matrix tray
/D = dry pack
/TD = tape, reel and dry pack

Speed Option
– 66 = 66 MHz

Package Option
Q = 52-pin Plastic Quad Flat Pack (PQFP)

Device Number

Example: S4406Q–66/D
52-pin PQFP package, 66 MHz, shipped dry packed in the standard matrix tray.

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