MB8868A

MOS Universal Asynchronous Receiver/Transmitter (UART)

October 1986
Edition 2.0

Description

The Fujitsu MB8868/A is a programmable Universal Asynchronous Receiver/Transmitter (UART), fabricated with an N-channel silicon gate MOS technology. All control pins, input pins and output pins are TTL compatible. The UART interfaces asynchronous serial data channels from terminals or other peripherals to the parallel data of a microprocessor, computer, or other terminal. Parallel data is converted by the transmitter section of the UART into a serial word consisting of the data as well as start, parity, and stop bit(s). Serial data is converted by the receiver section of the UART into parallel data. The receiver section verifies correct code transmission by parity checking and active reception of a valid stop bit. The UART can be programmed to accept word lengths of 5, 6, 7, or 8 bits. Even or odd parity can be set. Parity generation and checking can be inhibited.

One, one and one-half, or two stop bits can be set when transmitting a 5-bit code.

Features

- Full or Half Duplex Operation
- Completely Programmable
- Start Bit Generated Automatically
- Data and Clock Synchronization Performed Automatically
- Data Received/Transmitted Status Automatically Generated
- Complete Static Circuitry
- TTL Compatible I/O
- Three-State Output Capability
- Single Power Supply: +5V
- Standard 40-Pin Dual In-Line Package
- Functionally Compatible with Western Digital TR1863 and AMI S1602

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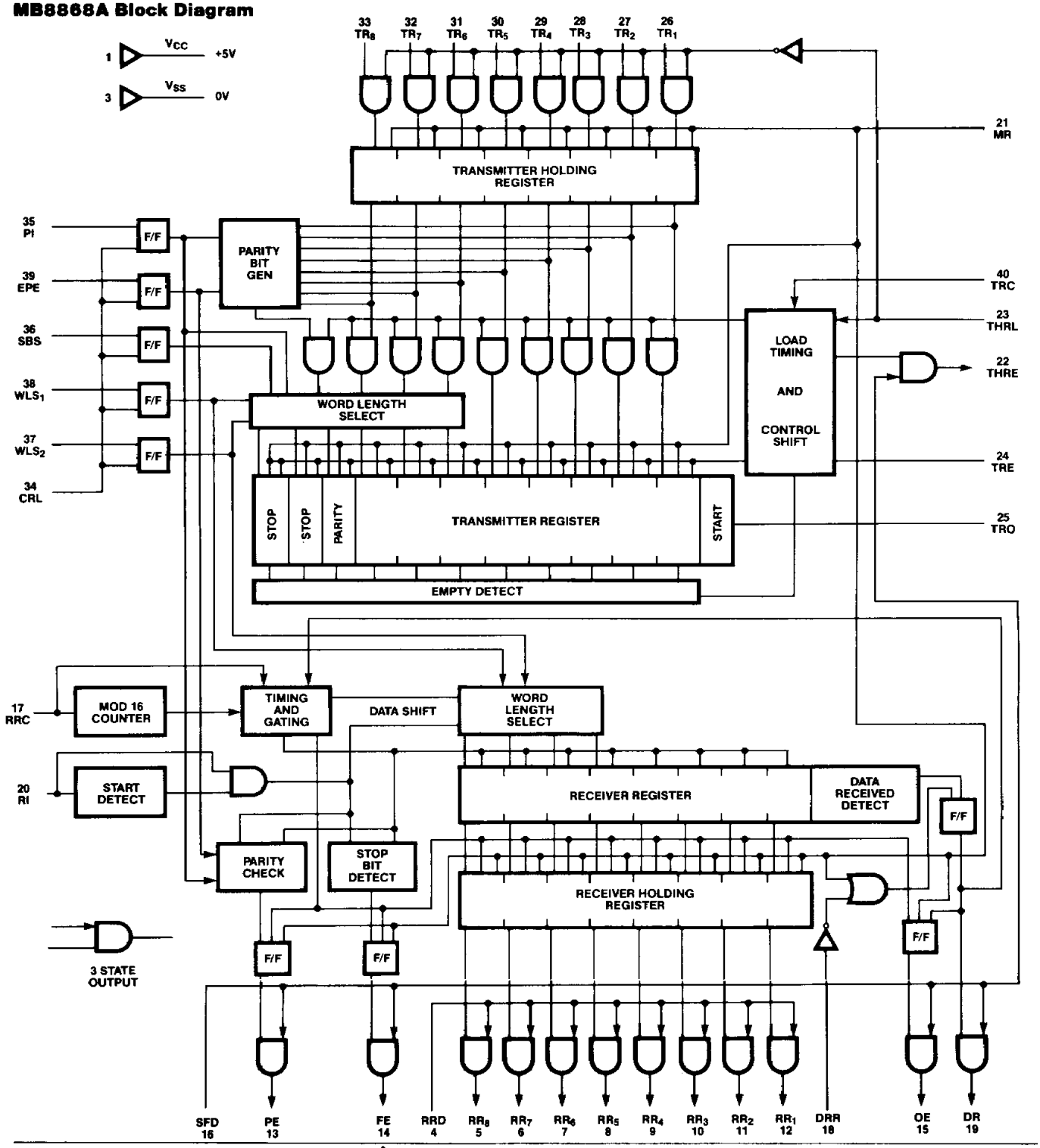
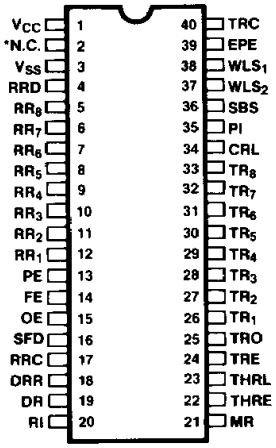
MB8868A Block Diagram



Capacitance
(T_A = 25° C, f = 1MHz, V_{IN} = 0V)

Parameter	Symbol	Value Typ.	Value Max.	Unit
Input Capacitance for all inputs	C_{IN}	10	—	pF

Pin Assignment



* N.C. (no connection)

Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
V_{CC} Pin Potential to V_{SS} Pin	V_{CC}	-0.3 to +7.0	V_{DC}
Input Voltage	V_{IN}	-0.3 to +7.0	V_{DC}
Output Voltage	V_O	-0.3 to +7.0	V_{DC}
Operating Temperature	T_{OP}	0 to +70	°C
Storate Temperature	T_{stg}	-55 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. **Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This** device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid applications of any voltages higher than maximum rated voltages to this high impedance circuit.

Recommended Operating Conditions

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Operating Temperature
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	O°C to +70°C
	V_{SS}	0.0	0.0	0.0	V	
Logic Input High Voltage	V_{IH}	2.2	—	V_{CC}	V	
Logic Input Low Voltage	V_{IL}	-0.3	—	+0.8	V	

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DC Characteristics

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value Min.	Typ.	Max.	Units
Input Leakage Current (V_{IN} = 0 to 5.25V, V_{CC} = 5.25V)	I_{LI}	—	—	350	μA
Output Leakage Current for 3-State (V_{OUT} = 0V to V_{CC}, SFD = RRD = V_{IH})	I_{LZ}	-20	—	+20	μA
Output Low Voltage (I_{OL} = 1.8mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OL} = -200μA)	V_{OH}	2.4	—	—	V
V_{CC} Supply Current	I_{CC}	—	70	—	mA

AC Characteristics

(Recommended operating ranges unless otherwise noted)

Parameter	Symbol	Value Min.	Typ.	Max.	Units
Clock Frequency for RRC and TRC (Duty Cycle = 50%)	f_C	DC	—	800	kHz
CRL Pulse Width, High	t_{PWC}	200	—	—	ns
THRL Pulse Width, Low	t_{PWT}	180	—	—	ns
DRR Pulse Width, Low	t_{PWR}	180	—	—	ns
MR Pulse Width, High	t_{PWM}	150	—	—	ns
Coincidence Time (Fig. 4 and Fig. 8)	t_C	180	—	—	ns
Hold Time (Fig. 4 and Fig. 8)	t_H	20	—	—	ns
Setup Time (Fig. 4 and Fig. 8)	t_{SET}	0	—	—	ns
Propagation Delay Time, High to Low, Output (C_L = 130 pF + 1 TTL)	t_{pd0}	—	—	350	ns
Propagation Delay Time, Low to High, Output (C_L = 130 pF + 1 TTL)	t_{pd1}	—	—	350	ns

Pin Descriptions

Pin Name	Pin Number	Description
RRD	4	**Receiver Register Disconnect** A high logic level, V_{IH}, on this pin disconnects the Receiver Holding Register outputs from the data outputs RR_8–RR_1 on pins 5–12.
RR_8 thru RR_1	5, 6, 7, 8, 9, 10, 11, 12	**Receiver Holding Register Data** These are the parallel outputs from the Receiver Holding Register if the RRD input is an input low level, V_{IL}. Data is right justified for character formats of less than eight bits, with RR_1 being the least significant bit. Unused MSB's are forced to a low logic output level, V_{OL}.
PE	13	**Parity Error** This output pin goes to a high level, V_{OH}, if the received parity does not agree with that programmed by the Even Parity Enable input (pin 39). With each character transferred to the Receiver Holding Register, this output is updated. The status Flag Disconnect input (pin 16) allows additional PE lines to be tied together by providing an output disconnect capability.

Pin Descriptions
(Continued)

Pin Name	Pin Number	Description
FE	14	**Framing Error** This output pin goes to a high level, V_{OH}, if the received character has no valid Stop bit. With each character transferred to the Receiver Holding Register, this output is updated. The Status Flag Disconnect input (pin 16) allows additional FE lines to be tied together by providing an output disconnect capability.
OE	15	**Overrun Error** This output pin goes to a high level, V_{OH}, if the Data Received Flag (pin 19) is not reset before the next character is transferred to the Receiver Holding Register. The Status Flag Disconnect input (pin 16) allows additional OE lines to be tied together by providing an output disconnect capability.
SFD	16	**Status Flag Disconnect** When this input goes to a high level, V_{IH}, PEE, FE, OE, DR, and THRE outputs are disconnected allowing bus sharing capability.
RRC	17	**Receiver Register Clock** This clock input is sixteen times the desired receiver shift rate.
DRR	18	**Data Received Reset (DRR)** A low level input, V_{IL}, resets the data Received (DR) line.
DR	19	**Data Received** This output goes to a high level, V_{OH}, when an entire character has been received and transferred to the Receiver Holding Register.
RI	20	**Receiver Input** Serial input data enters on this line. It is transferred to the Receiver Register as determined by the character length, parity, and number of Stop bits. When data is not being received, this input must be at high level, V_{IH}
MR	21	**Master Reset** A high level pulse, V_{IH}, on this input will clear the internal logic. The Transmitter and Receiver Registers, the Receiver Holding Register, FE, OE, PE, and DRR are reset. In addition, the serial output line is set to a high level, V_{OH}.
THRE	22	**Transmitter Holding Register Empty** This output goes to a high level, V_{OH}, when the Transmitter Holding Register has completed transfer of its contents to the Transmitter Register. The high level indicates that a new character may be loaded into the transmitter Holding Register.
THRL	23	**Transmitter Holding Register Load** When a low level, V_{IL}, is applied to this input, a character is loaded into the Transmitter Holding Register. This character is transferred to the Transmitter Register on a low to high level transition, as long as the Transmitter Register is not currently in the process of transmitting a character. If a character is being transmitted, the transfer from the Transmitter Holding Register is delayed until character transmission has been completed. Then, the new character is transferred simultaneously with the start of the serial transmission of the new character.
TRE	24	**Transmitter Register Empty** This output is at a high level , V_{OH}, when the Transmitter Register has completed the serial transmission of a full character including the required number of Stop bits. A high level will be maintained until the start of transmission of the next character.

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Pin Descriptions
(Continued)

Pin Name	Pin Number	Description
TRO	25	**Transmitter Register Output** This output line transmits the Transmitter Register contents [Start bit, Data bits, Parity bit, and Stop bit(s)] serially. This output remains at a high level, V_{OH}, when no data is being transmitted. Therefore, the start of transmission is determined by the transition of the Start bit from a high level to a low level voltage, V_{OL}.
TR_1 thru TR_8	26, 27, 28, 29, 30, 31, 32, 33	**Transmitter Register Data Inputs** The THRL strobe loads each character on these lines into the Transmitter Holding Register. If WLS_1 and WLS_2 have selected a character of less than 8 bits, the character is then right-justified to the least significant bit, TR_1, with the excess bits not used. A high input level, V_{IH}, will cause a high output level, V_{OH}, to be transmitted.
CRL	34	**Control Register Load** When this input is at a high level, V_{IH}, the control bits (WLS_1, WLS_2, EPE, PI, SBS), are loaded into the Control Register. This input may be either strobed or hard wired to a high level.
PI	35	**Parity Inhibit** When this input is at a high level, V_{IH}, parity generation and verification circuitry are inhibited and the PE output will be held to a low level, V_{OL}. In the inhibit condition, the Stop bit(s) will follow the last data bit on transmission.
SBS	36	**Stop Bit(s) Select** A high level, V_{IH}, on this input will select two Stop bits, and a low level, V_{IL}, will select one Stop bit. If 5-bit long words are selected, a high level, V_{IH}, will generate one and one-half Stop bits.
WLS_1, WLS_2, EPE, TRC		**Word Length Select (WLS_1, WLS_2)** The state of these two inputs determines the character length (exclusive of parity) as follows:

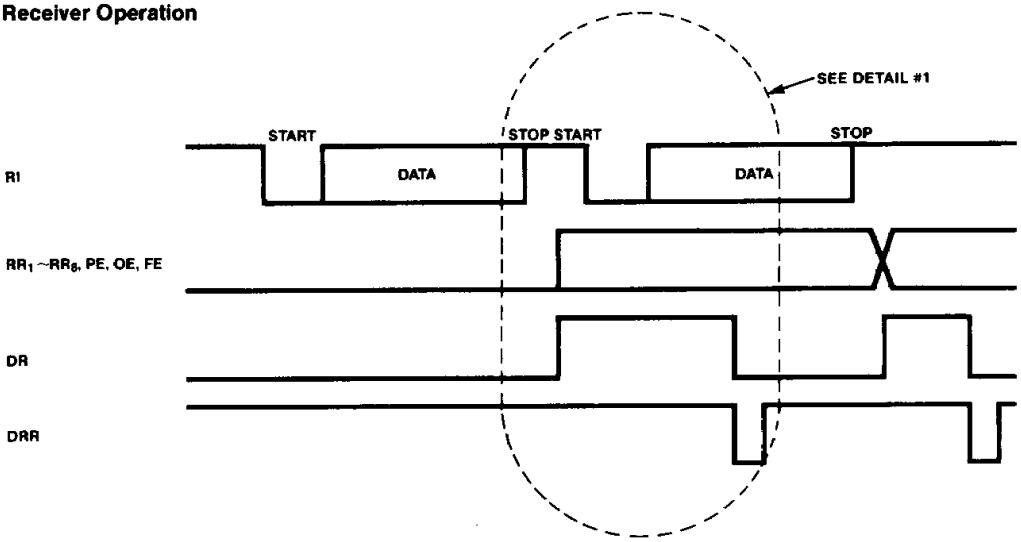
WLS_2	WLS_1	Word Length
V_{IH}	V_{IH}	8 bits
V_{IH}	V_{IL}	7 bits
V_{IL}	V_{IH}	6 bits
V_{IL}	V_{IL}	5 bits

Even Parity Enable (EPE)
A high level, V_{IH}, on this input will select even Parity, while a low level, V_{IL}, selects odd Parity.

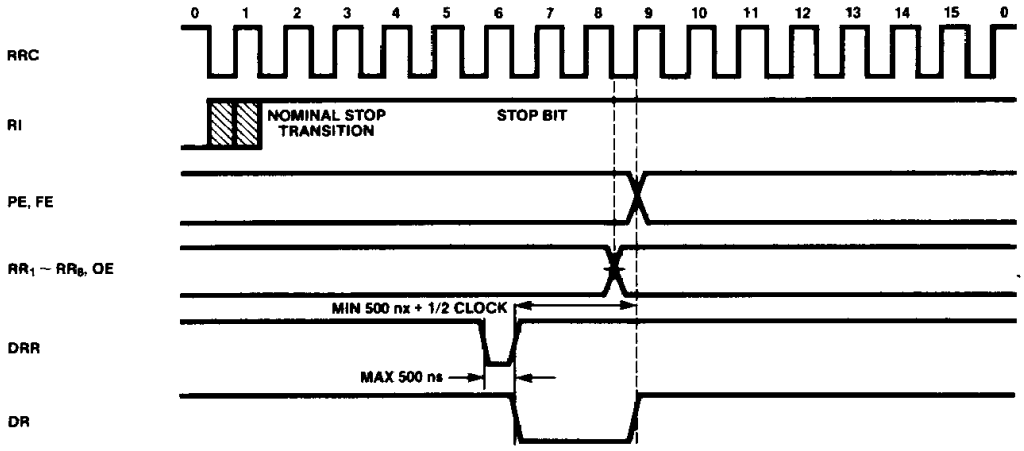
Transmitter Register Clock (TRC)
The frequency of this clock is 16 times the desired transmitter shift rate.

Timing Diagrams

Receiver Operation



Timing for Status Flag, RR_1, thru RR_8 and DR (Detail #1)



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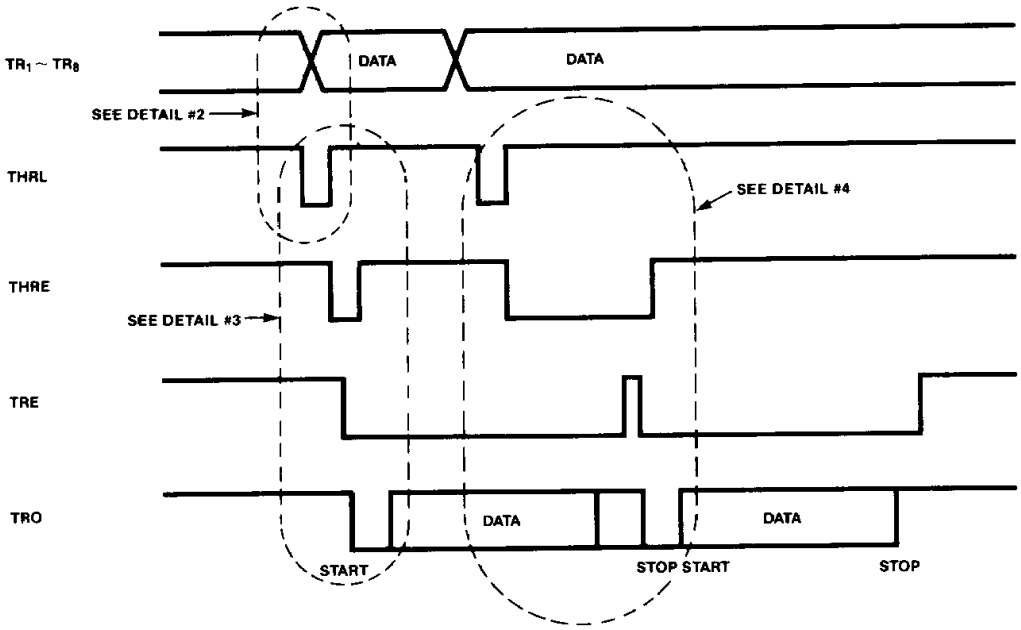
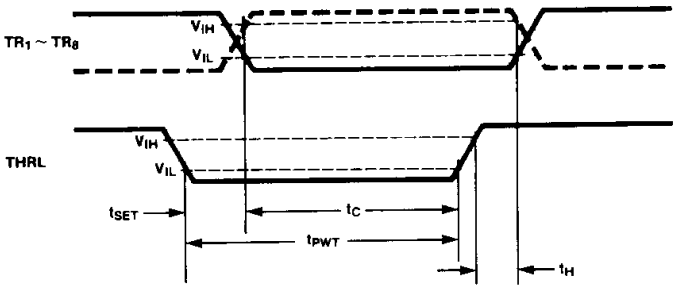
Timing Diagrams
(Continued)

Transmitter Operation

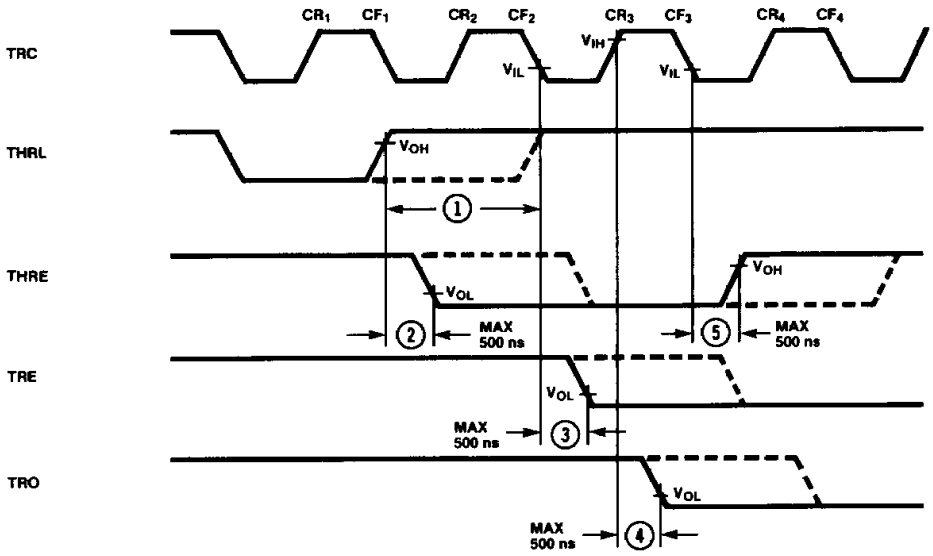


Data Input Load Cycle (Detail #2)



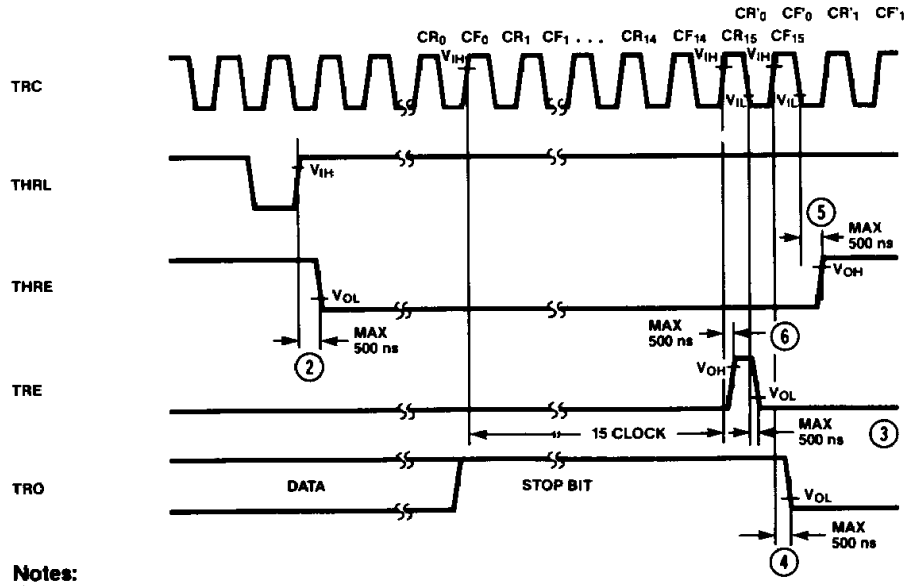
Timing Diagrams
(Continued)

Transmitter Output Timing (1) (Detail #3)



Notes:
① When the positive transition of THRL is ≥ 500 ns before the falling edge of TRC (CF2 in the figure), then TRE is enabled at CF2. But when 500 ns >①> 0 ns, then TRE is invalid between CF2 and CF3.
② THRE goes low during 500 ns Max. from the postive transition of THRL.
③ TRE goes low during 500 ns Max. from the first falling edge of TRC after THRE goes low with TRE high.
④ TRO goes low (START BIT) during 500 ns Max. from the first rising edge of TRC after TRE goes low.
⑤ THRE goes high during 500 ns Max. from the falling edge of TRC after Start bit is enabled.

Transmitter Output Timing (2) (Detail #4)



Notes:
② ~ ⑤ Refer to Notes in Detail #3
⑥ TRE goes high during 500 ns Max. from the 15th rising edge of TRC after Stop bit is enabled.

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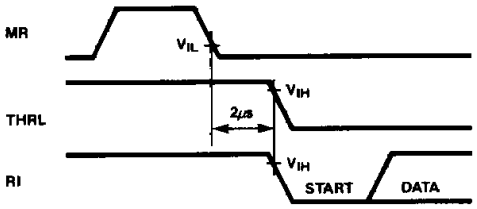
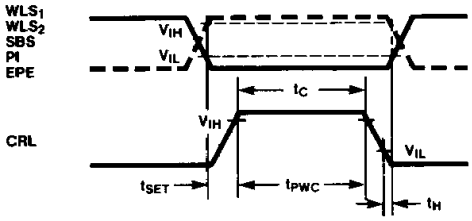
Timing Diagrams
(Continued)

Other Timing Diagrams

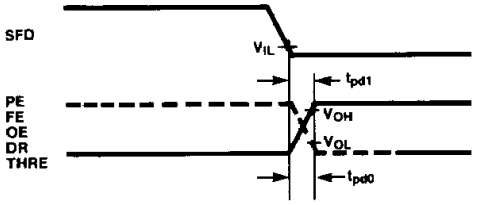
Input After Master Reset



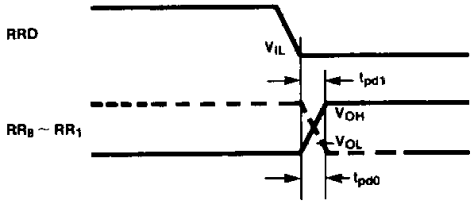
Control Register Load Cycle



Status Flag Output



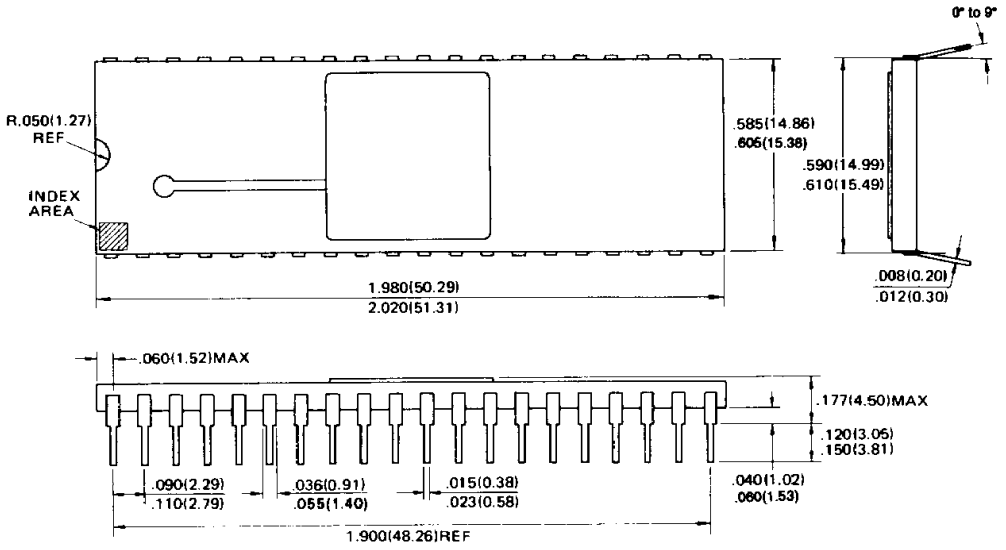
Data Output



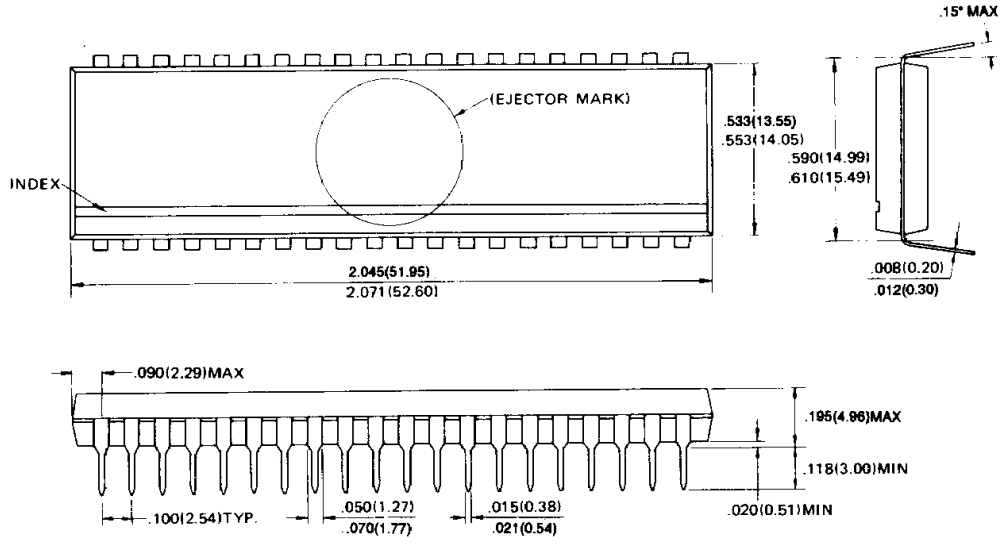
Package Dimensions

(Dimensions in millimeters)

40-Lead Ceramic (Metal Seal) Dual In-Line Package DIP-40C-A01



40-Lead Plastic Dual In-Line Package DIP-40P-M01



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