

TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS  
131,072-WORD BY 16-BIT STATIC RAM

**DESCRIPTION**

The TC55V2161FT is a 2,097,152-bit static random access memory (SRAM) organized as 131,072 words by 16 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.7 to 3.6V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz and a minimum cycle time of 85 ns. It is automatically placed in low-power mode at 1μA standby current (for the L-Version V<sub>DD</sub>=3V, Ta=25°C) when chip enable ( $\overline{CE}$ ) is asserted high or chip select (CS) is asserted low. There are three control inputs.  $\overline{CE}$  is used to select the device and for data retention control, CS is used for data retention control, and output enable ( $\overline{OE}$ ) provides fast memory access. Data byte control pin ( $\overline{LB}$ ,  $\overline{UB}$ ) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. The TC55V2161FT is available in a plastic 44-pin thin-small-outline package (TSOP).

**FEATURES**

- Low-power dissipation  
Operating: 10.8 mW/MHz (typical)
- Single power supply voltage of 2.7 to 3.6V
- Power down features using  $\overline{CE}$  and CS
- Data retention supply voltage of 2 to 3.6V
- Direct TTL compatibility for all inputs and outputs
- Standby current (maximum)

	TC55V2161FT	
	-85, -10	-85L, -10L
3.6V	35 μA	25 μA
3.0V	25 μA	15 μA

- Access Times (maximum):

	TC55V2161FT	
	-85, -85L	-10, -10L
Access Time	85 ns	100 ns
$\overline{CE}$ Access Time	85 ns	100 ns
$\overline{OE}$ Access Time	45 ns	50 ns

- Package:  
TSOP II 44-P-400-0.80 (FT)

**PIN ASSIGNMENT (TOP VIEW)**

A4 □ 1 ○	44 □ A5
A3 □ 2	43 □ A6
A2 □ 3	42 □ A7
A1 □ 4	41 □ $\overline{OE}$
A0 □ 5	40 □ $\overline{UB}$
$\overline{CE}$ □ 6	39 □ $\overline{LB}$
I/O1 □ 7	38 □ I/O16
I/O2 □ 8	37 □ I/O15
I/O3 □ 9	36 □ I/O14
I/O4 □ 10	35 □ I/O13
V <sub>DD</sub> □ 11	34 □ GND
GND □ 12	33 □ V <sub>DD</sub>
I/O5 □ 13	32 □ I/O12
I/O6 □ 14	31 □ I/O11
I/O7 □ 15	30 □ I/O10
I/O8 □ 16	29 □ I/O9
R/W □ 17	28 □ CS
A15 □ 18	27 □ A8
A14 □ 19	26 □ A9
A13 □ 20	25 □ A10
A12 □ 21	24 □ A11
A16 □ 22	23 □ NC

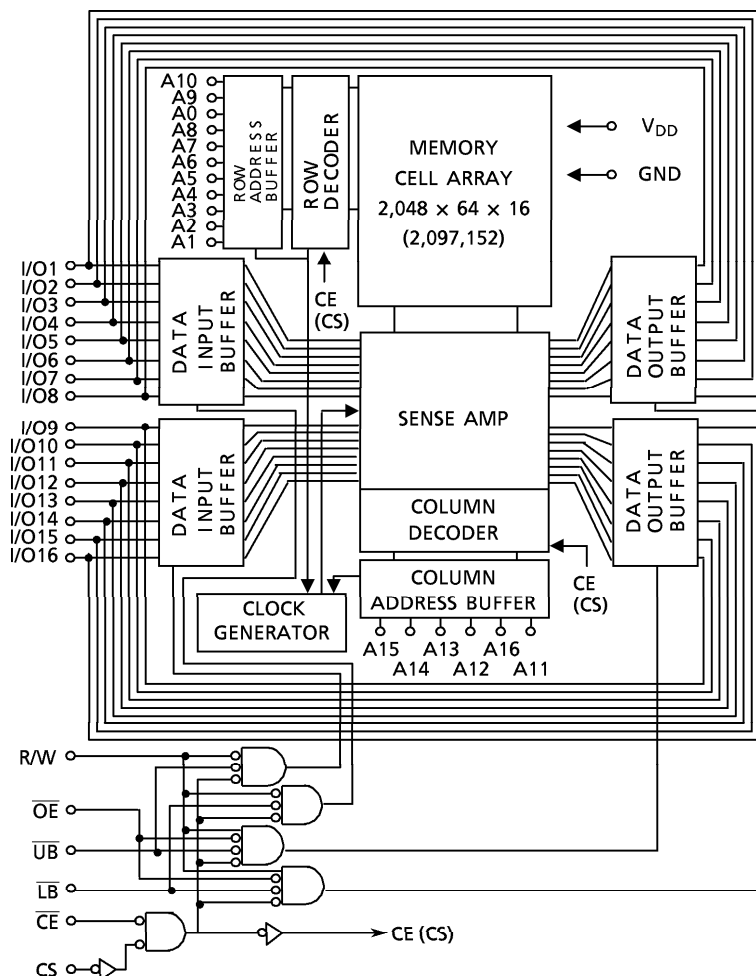
**PIN NAMES**

A0 to A16	Address Inputs
$\overline{CE}$	Chip Enable Input
CS	Chip Select Input
R/W	Read / Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$ , $\overline{UB}$	Data Byte Control Inputs
I/O1 to I/O16	Data Inputs / Outputs
V <sub>DD</sub>	Power
GND	Ground
NC	No Connection

961001EBA1

- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to foreign exchange and foreign trade control laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

BLOCK DIAGRAM



OPERATING MODE

MODE	$\overline{CE}$	CS	$\overline{OE}$	R/W	$\overline{LB}$	$\overline{UB}$	I/O1 to I/O8	I/O9 to I/O16	POWER
Read	L	H	L	H	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	I <sub>DDO</sub>
					H	L	High-Z	D <sub>OUT</sub>	I <sub>DDO</sub>
					L	H	D <sub>OUT</sub>	High-Z	I <sub>DDO</sub>
Write	L	H	x	L	L	L	D <sub>IN</sub>	D <sub>IN</sub>	I <sub>DDO</sub>
					H	L	High-Z	D <sub>IN</sub>	I <sub>DDO</sub>
					L	H	D <sub>IN</sub>	High-Z	I <sub>DDO</sub>
Output Deselect	L	H	H	H	x	x	High-Z	High-Z	I <sub>DDO</sub>
			x	x	L	L			
CS Standby	x	L	x	x	x	x	High-Z	High-Z	I <sub>DDS</sub>
Standby	H	x	x	x	x	x	High-Z	High-Z	I <sub>DDS</sub>

Note: x = don't care. H = logic high. L = logic low

**MAXIMUM RATINGS**

SYMBOL	RATING	VALUE	UNIT
V <sub>DD</sub>	Power Supply Voltage	- 0.3 to 4.6	V
V <sub>IN</sub>	Input Voltage	- 0.3 * to 4.6	V
V <sub>I/O</sub>	Input/Output Voltage	- 0.5 to V <sub>DD</sub> + 0.5	V
P <sub>D</sub>	Power Dissipation	0.8	W
T <sub>solder</sub>	Soldering Temperature (10 s)	260	°C
T <sub>strg</sub>	Storage Temperature	- 55 to 150	°C
T <sub>opr</sub>	Operating Temperature	0 to 70	°C

\* - 3.0 V when measured at a pulse width of 30 ns

**DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V <sub>DD</sub>	Power Supply Voltage	2.7	-	3.6	V
V <sub>IH</sub>	Input High Voltage	2.0	-	V <sub>DD</sub> + 3.6	V
V <sub>IL</sub>	Input Low Voltage	- 0.3 *	-	0.8	V
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	-	3.6	V

\* - 3.0 V when measured at a pulse width of 30 ns

**DC CHARACTERISTICS (Ta = 0° to 70°C, V<sub>DD</sub> = 2.7 to 3.6V)**

SYMBOL	PARAMETER	TEST CONDITION				MIN	TYP	MAX	UNIT		
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0 V to V <sub>DD</sub>				-	-	± 1.0	μA		
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> - 0.5 V				-0.5	-	-	mA		
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4 V				2.1	-	-	mA		
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IL}$ or $CS = V_{IH}$ or $RW = V_{IL}$ V <sub>OUT</sub> = 0 V to V <sub>DD</sub>				-	-	± 1.0	μA		
I <sub>DDO1</sub>	Operating Current	$\overline{CE} = V_{IL}$ and $CS = V_{IH}$ and $RW = V_{IH}$ and I <sub>OUT</sub> = 0 mA Other Input = V <sub>IH</sub> /V <sub>IL</sub>	V <sub>DD</sub> = 3 V ± 10%	T <sub>cycle</sub>	min	-	-	55	mA		
				1 μs	-	-	10				
			V <sub>DD</sub> = 3.3 V ± 0.3 V	T <sub>cycle</sub>	min	-	-	60			
				1 μs	-	-	12				
I <sub>DDO2</sub>	Operating Current	$\overline{CE} = 0.2$ V and $CS = V_{DD} - 0.2$ V and $RW = V_{DD} - 0.2$ V, I <sub>OUT</sub> = 0 mA Other Inputs = V <sub>DD</sub> - 0.2 V/0.2 V	V <sub>DD</sub> = 3 V ± 10%	T <sub>cycle</sub>	min	-	-	45	mA		
				1 μs	-	-	5				
			V <sub>DD</sub> = 3.3 V ± 0.3 V	T <sub>cycle</sub>	min	-	-	50			
				1 μs	-	-	6				
I <sub>DDS1</sub>	Standby Current	$\overline{CE} = V_{IH}$ or $CS = V_{IL}$  $\overline{CE} = V_{DD} - 0.2$ V or $CS = 0.2$ V V <sub>DD</sub> = 2.0 to 3.6 V	V <sub>DD</sub> = 3 V ± 10%	Ta = 25°C	-85, -10	-	1	2.5	μA		
					-85L, -10L	-	0.5	1.2			
				Ta = 0° to 70°C		-85, -10	-	-		30	
							-85L, -10L	-		-	20
			V <sub>DD</sub> = 3.3 V ± 0.3 V	Ta = 25°C	-85, -10	-	1.5	3			
					-85L, -10L	-	0.7	1.4			
				Ta = 0° to 70°C		-85, -10	-	-		35	
						-85L, -10L	-	-		25	
				V <sub>DD</sub> = 3 V	Ta = 25°C	-85, -10	-	1		2	
						-85L, -10L	-	0.5		1	
			Ta = 0° to 40°C		-85, -10	-	-	5			
					-85L, -10L	-	-	3			
				Ta = 0° to 70°C		-85, -10	-	-		25	
			-85L, -10L	-	-	15					

Note: In standby mode with  $\overline{CE} \geq V_{DD} - 0.2$  V, these limits are assured for the condition  $CS \geq V_{DD} - 0.2$  V or  $CS \leq 0.2$  V.

**CAPACITANCE** ( $T_a = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = \text{GND}$	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

**AC CHARACTERISTICS AND OPERATING CONDITIONS** (Ta = 0° to 70°C, VDD = 2.7 to 3.6V)

**READ CYCLE**

SYMBOL	PARAMETER	TC55V2161FT				UNIT
		-85, -85L		-10, -10L		
		MIN	MAX	MIN	MAX	
t <sub>RC</sub>	Read Cycle Time	85	–	100	–	ns
t <sub>ACC</sub>	Address Access Time	–	85	–	100	
t <sub>CO</sub>	Chip Enable Access Time	–	85	–	100	
t <sub>OE</sub>	Output Enable Access Time	–	45	–	50	
t <sub>BA</sub>	Data Byte Control Access Time	–	45	–	50	
t <sub>COE</sub>	Chip Enable Low to Output Active	10	–	10	–	
t <sub>OEE</sub>	Output Enable Low to Output Active	5	–	5	–	
t <sub>BE</sub>	Data Byte Control Low to Output Active	5	–	5	–	
t <sub>OD</sub>	Chip Enable High to Output High-Z	–	30	–	35	
t <sub>ODO</sub>	Output Enable High to Output High-Z	–	30	–	35	
t <sub>BDO</sub>	Data Byte Control High to Output High-Z	–	30	–	35	
t <sub>OH</sub>	Output Data Hold Time	10	–	10	–	

**WRITE CYCLE**

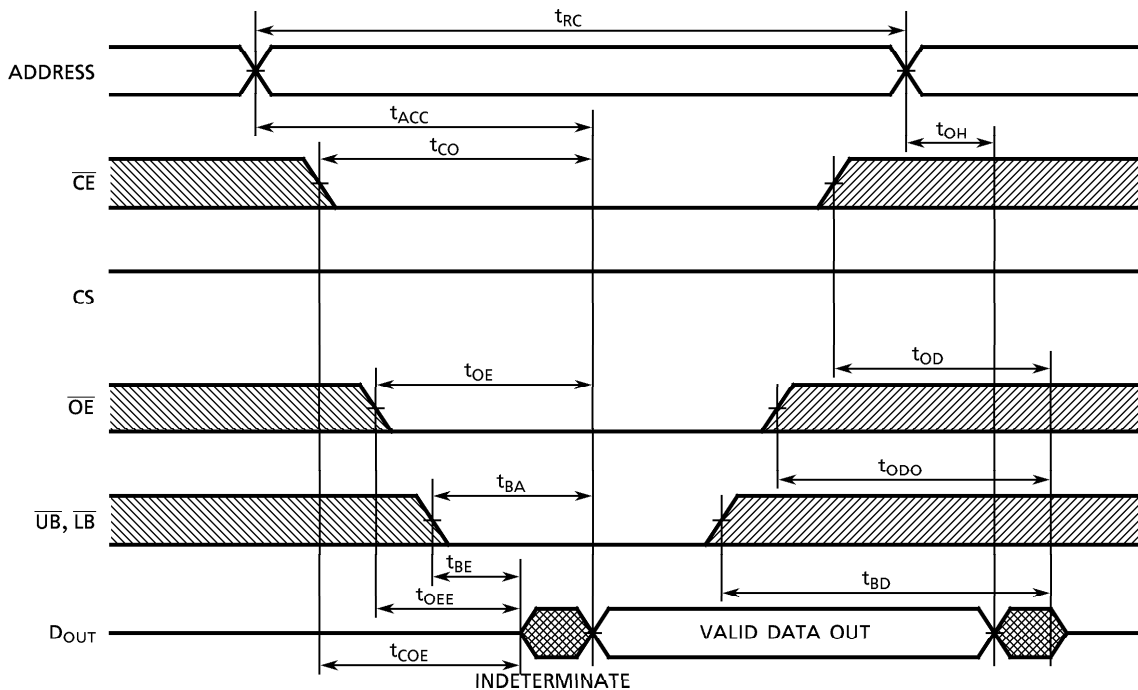
SYMBOL	PARAMETER	TC55V2161FT				UNIT
		-85, -85L		-10, -10L		
		MIN	MAX	MIN	MAX	
t <sub>WC</sub>	Write Cycle Time	85	–	100	–	ns
t <sub>WP</sub>	Write Pulse Width	60	–	60	–	
t <sub>CW</sub>	Chip Enable to End of Write	75	–	80	–	
t <sub>BW</sub>	Data Byte Control to End of Write	60	–	60	–	
t <sub>AS</sub>	Address Setup Time	0	–	0	–	
t <sub>WR</sub>	Write Recovery Time	0	–	0	–	
t <sub>ODW</sub>	R/W Low to Output High-Z	–	30	–	35	
t <sub>OEW</sub>	R/W High to Output Active	5	–	5	–	
t <sub>DS</sub>	Data Setup Time	35	–	40	–	
t <sub>DH</sub>	Data Hold Time	0	–	0	–	

**AC TEST CONDITIONS**

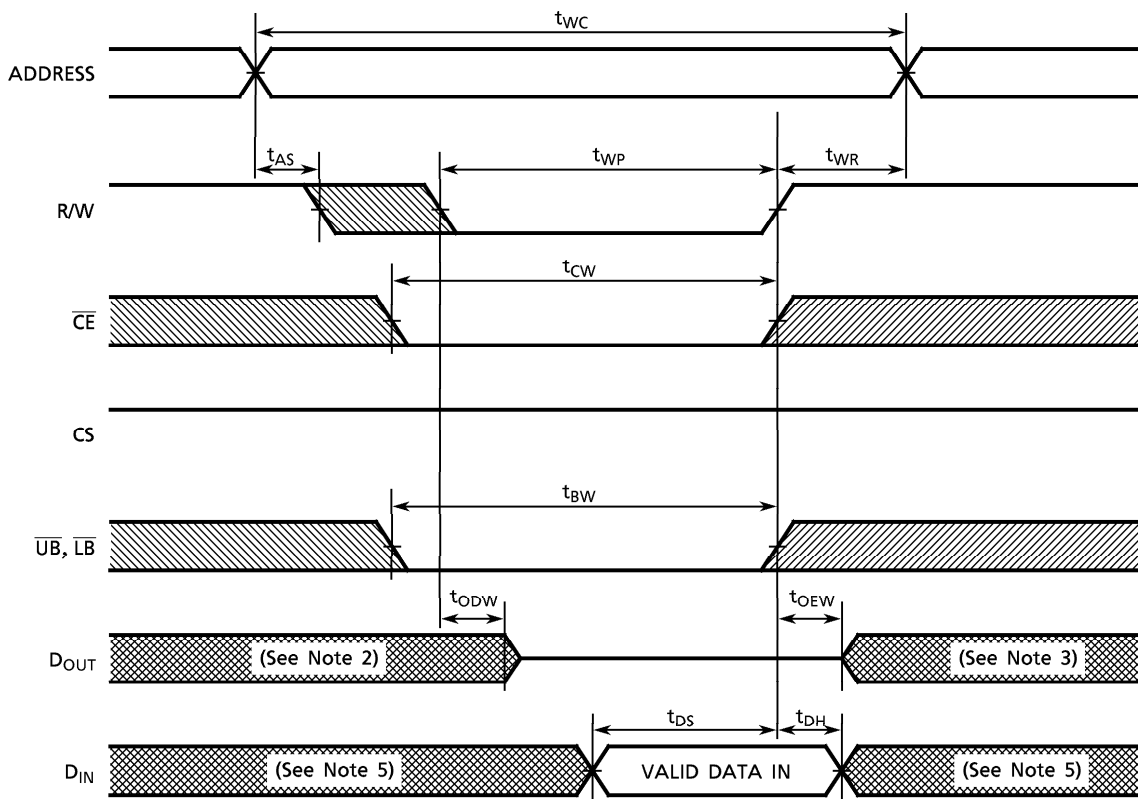
Output load: 100 pF + one TTL gate  
 Input pulse level: 0.6 V, 2.2 V  
 Timing measurements: 1.5 V  
 Reference level: 1.5 V  
 t<sub>R</sub>, t<sub>F</sub>: 5 ns

**TIMING DIAGRAMS**

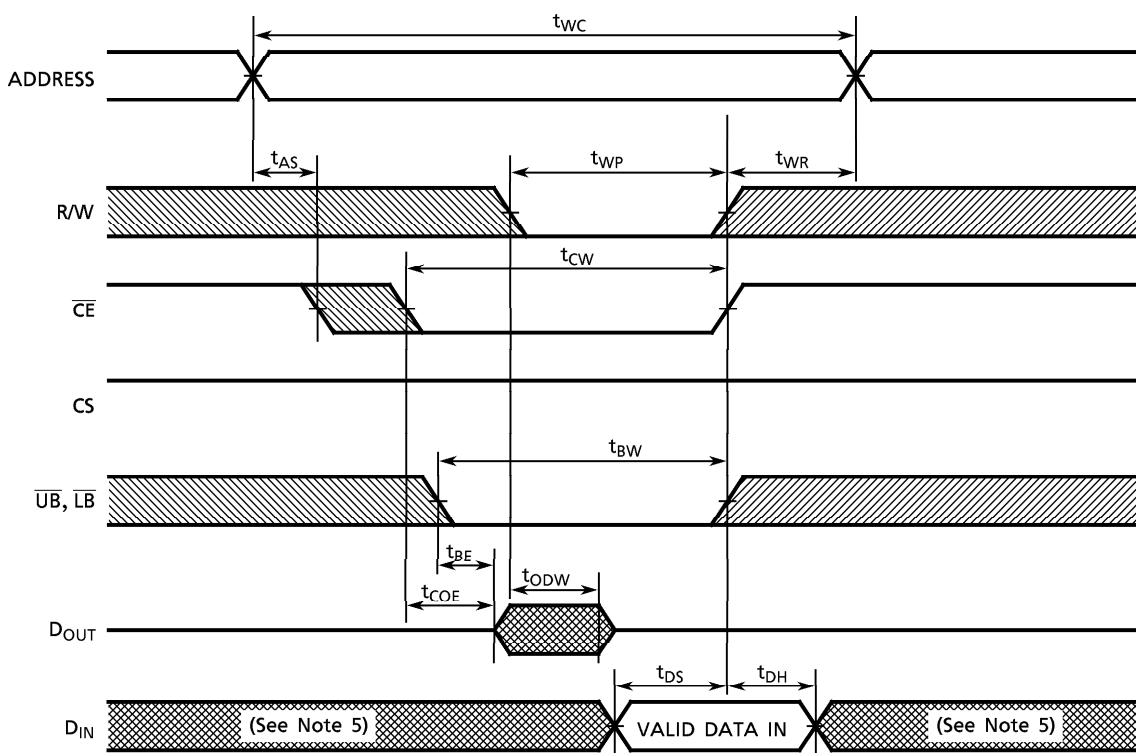
**READ CYCLE (See Note 1)**



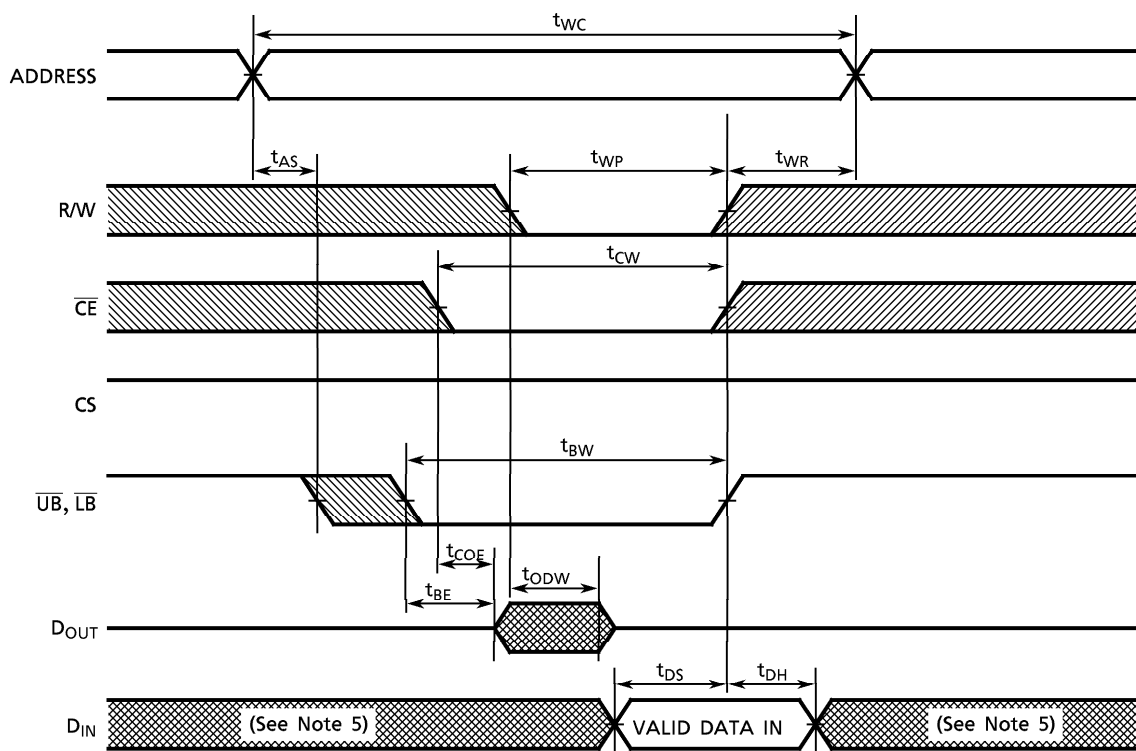
**WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)**



WRITE CYCLE 2 ( $\overline{CE}$  CONTROLLED) (See Note 4)



WRITE CYCLE 3 ( $\overline{UB}, \overline{LB}$  CONTROLLED) (See Note 4)

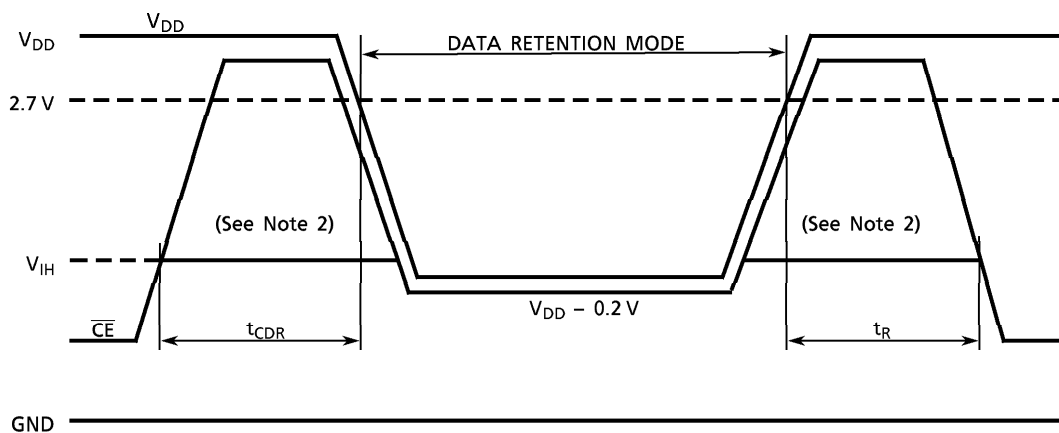


- Note:
- (1) R/W remains HIGH for the read cycle.
  - (2) If  $\overline{CE}$  goes LOW (or CS goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.
  - (3) If  $\overline{CE}$  goes HIGH (or CS goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.
  - (4) If  $\overline{OE}$  is HIGH during the write cycle, the outputs will remain at high impedance.
  - (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

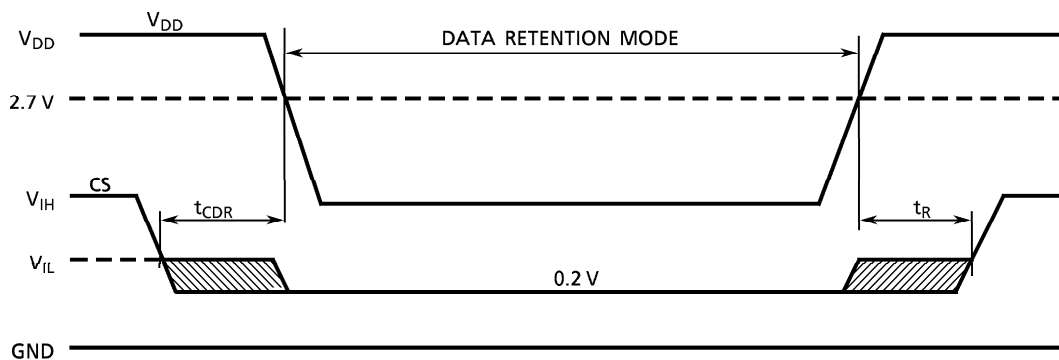
**DATA RETENTION CHARACTERISTICS (Ta = 0° to 70°C)**

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT		
V <sub>DH</sub>	Data Retention Supply Voltage		2.0	-	3.6	V		
I <sub>DSD2</sub>	Standby Current	V <sub>DD</sub> = 3.0 V	Ta = 0° to 40°C	-85, -10	-	5	μA	
			-85L, -10L	-	-	3		
		V <sub>DD</sub> = 3.0 V	Ta = 0° to 70°C	-85, -10	-	-		25
				-85L, -10L	-	-		15
			Ta = 0° to 70°C	-85, -10	-	-		35
-85L, -10L	-	-	25					
t <sub>CDR</sub>	Chip Deselect to Data Retention Mode Time		0	-	-	nS		
t <sub>R</sub>	Recovery Time		5	-	-	mS		

**CE CONTROLLED DATA RETENTION MODE (See Note 1)**



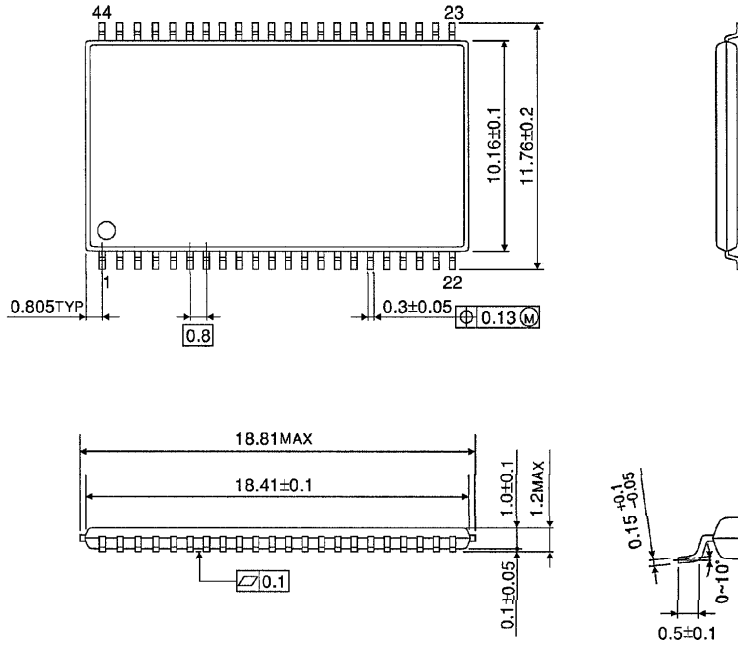


CE CONTROLLED DATA RETENTION MODE (See Note 3)

- Note: (1) In  $\overline{CE}$  controlled data retention mode, minimum standby current mode is entered when  $CS \leq 0.2 \text{ V}$  or  $CS \geq V_{DD} - 0.2 \text{ V}$ .
- (2) When  $\overline{CE}$  is operating at the  $V_{IH}$  level (2.0 V), the operating current is given by  $I_{DDSI}$  during the transition of  $V_{DD}$  from 3.6 to 2.2 V.
- (3) In CS controlled data retention mode, minimum standby current mode is entered when  $CS \leq 0.2 \text{ V}$ .

PACKAGE DIMENSIONS (TSOPII 44-P-400-0.80)

Units in mm



Weight: (typ)