
HA19211BP/BNT/BMP

High-Speed, Low-Power 8-bit A/D Flash Converter

HITACHI

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Description

The HA19211BP/BNT/BMP high-speed, low-power 8-bit A/D flash converters require no sampling and holding circuits. The digital outputs and clock inputs of these monolithic bipolar ICs are fully TTL/CMOS compatible.

These devices are suitable for high-speed image processing applications such as video signal digitization.

Features

- 8-bit resolution (with overflow)
- Low power consumption (250 mW Typ)
- High conversion rate (20 Msps Min)
- Single power supply operation: +5 V
- Built-in output latch circuit
- TTL/CMOS compatible digital outputs and clock inputs

Applications

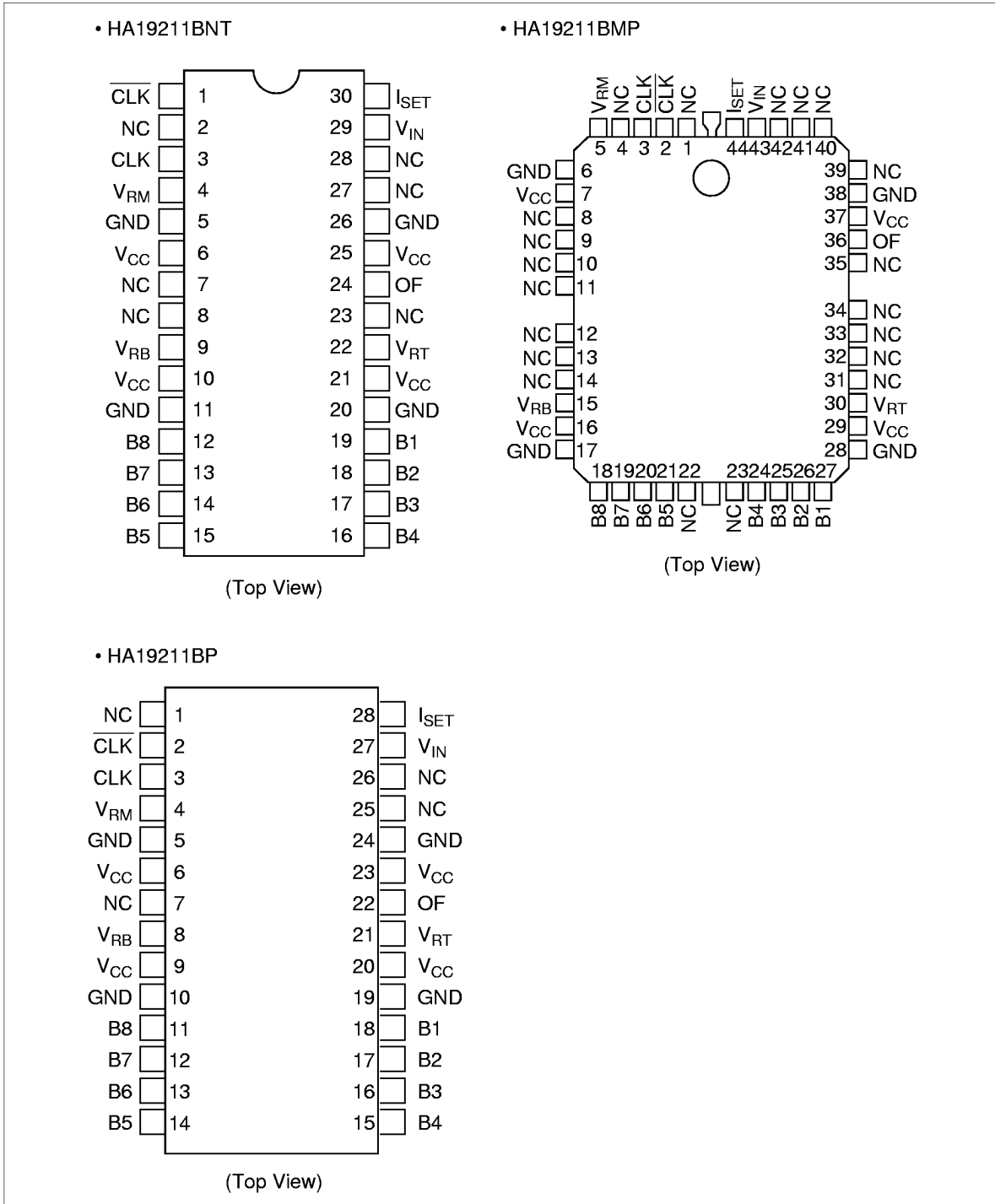
- Digital TV/VCR
- Industrial pattern recognition equipment
- High-speed measuring devices

Ordering Information

Type No.	Package
HA19211BP	600mil 28-pin plastic DIP (DP-28)
HA19211BNT	400mil 30-pin plastic shrink DIP (DP-30S)
HA19211BMP	44-pin plastic QFI (MP-44)

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Pin Arrangement



Pin Descriptions**HA19211BP, HA19211BMP**

Pin No.	Symbol	Function
1 (1)	NC	No Connected
2 (2)	$\overline{\text{CLK}}$	Inverted clock input
3 (3)	CLK	Clock input
4 (5)	V_{RM}	Reference voltage compensation input
5 (6)	GND	Ground
6 (7)	V_{CC}	Power supply (+5 V)
7 (8)	NC	No Connected
8 (15)	V_{RB}	Low-level reference voltage input
9 (16)	V_{CC}	Power supply (+5 V)
10 (17)	GND	Ground
11 (18)	B8	Digital output (MSB)
12 (19)	B7	Digital output
13 (20)	B6	Digital output
14 (21)	B5	Digital output
15 (24)	B4	Digital output
16 (25)	B3	Digital output
17 (26)	B2	Digital output
18 (27)	B1	Digital output (LSB)
19 (28)	GND	Ground
20 (29)	V_{CC}	Power Supply (+5 V)
21 (30)	V_{RT}	High-level reference voltage input
22 (36)	OF	Overflow output
23 (37)	V_{CC}	Power supply (+5 V)
24 (38)	GND	Ground
25 (39)	NC	No connected
26 (40)	NC	No connected
27 (43)	V_{IN}	Analog input
28 (44)	I_{SET}	Output current setting input

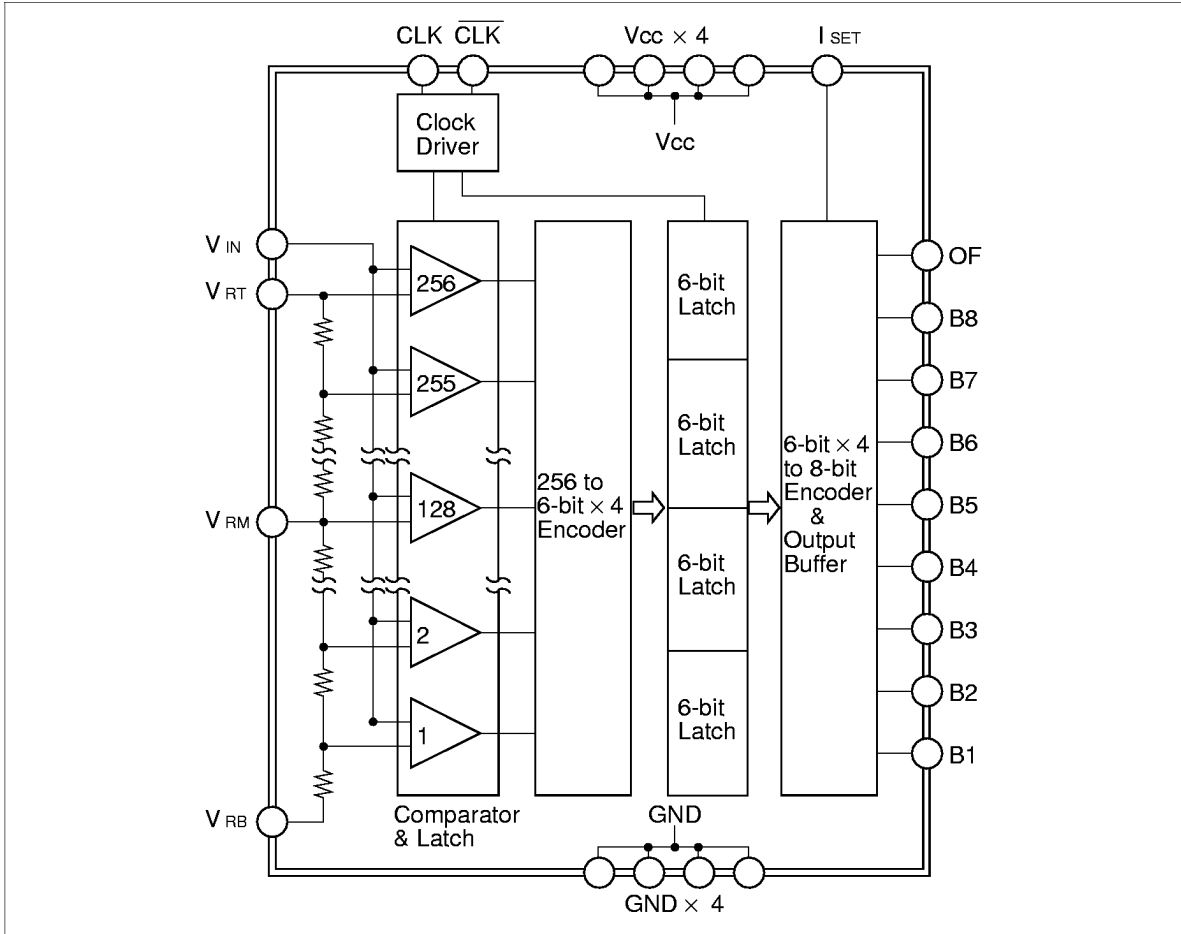
Note: Pin numbers in parentheses are for the HA19211BMP. For this chip pins 4, 9 to 14, 22, 23, 31 to 35, 41 and 42 are no connected.

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HA19211BNT

Pin No.	Symbol	Function
1	$\overline{\text{CLK}}$	Inverted clock input
2	NC	No connected
3	CLK	Clock input
4	V_{RM}	Reference voltage compensation input
5	GND	Ground
6	V_{CC}	Power supply (+5 V)
7	NC	No connected
8	NC	No connected
9	V_{RB}	Low-level reference voltage input
10	V_{CC}	Power supply (+5 V)
11	GND	Ground
12	B8	Digital output (MSB)
13	B7	Digital output
14	B6	Digital output
15	B5	Digital output
16	B4	Digital output
17	B3	Digital output
18	B2	Digital output
19	B1	Digital output (LSB)
20	GND	Ground
21	V_{CC}	Power supply (+5 V)
22	V_{RT}	High-level reference voltage input
23	NC	No connected
24	OF	Digital output (overflow)
25	V_{CC}	Power supply (+5 V)
26	GND	Ground
27	NC	No connected
28	NC	No connected
29	V_{IN}	Analog input
30	I_{SET}	Output current setting input

Block Diagram



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Absolute Maximum Ratings (Ta = 25°C unless otherwise specified)

Parameter	Symbol	Rating	Unit
Power supply voltage	V _{CC}	+7.0	V
Analog Input voltage* ¹	V _{IN}	0 to V _{CC} - 0.9	V
Reference voltage* ¹	V _R	0 to V _{CC} - 0.9	V
Clock input voltage* ²	V _{CLK}	0 to V _{CC}	V
Power dissipation	P _T	800	mW
Operating temperature	Topr	-20 to +85	°C
Storage temperature	Tstg	-55 to +125	°C
Reference voltage difference	V _{RT} - V _{RB}	2.1	V
Output current setting	I _{SET(max)}	5	mA
Reference center tap voltage	V _{RM}	Open state voltage ±0.1	V

Notes: 1. V_{IN} and V_R should never be below 1.2 V at the same time.
2. V_{CLK} and V_{CLK} should never be below 1.5 V at the same time.

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Electrical Characteristics ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{RT} = 3.5\text{ V}$, $V_{RB} = 1.5\text{ V}$, unless otherwise specified)

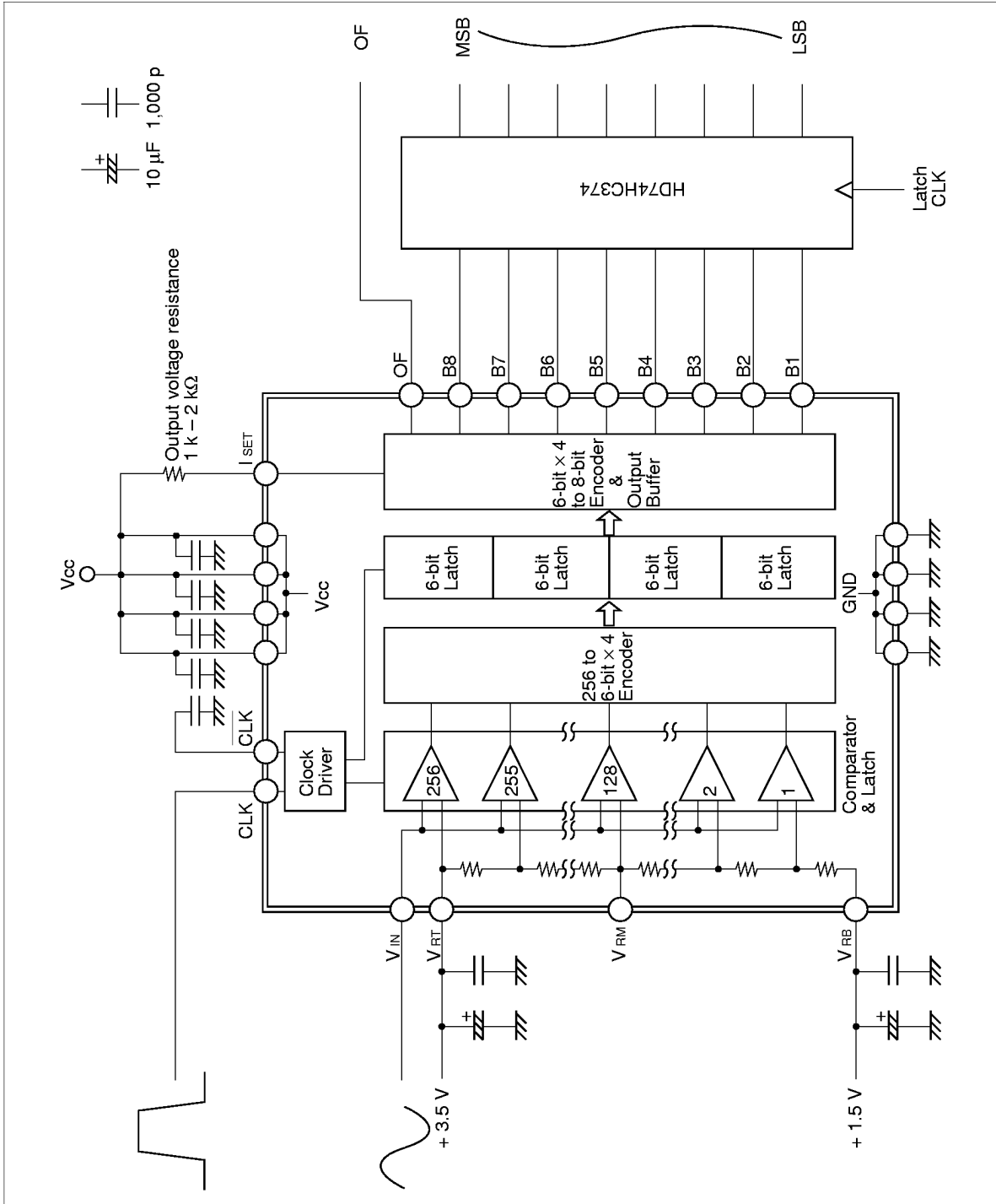
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Resolution		8	8	8	bits	
Power supply voltage	V_{CC}	4.75	5.0	5.25	V	
Power supply current	I_{CC}	—	50	75	mA	$V_{CC} = 5.0\text{ V}$, $f_{CLK} = 20\text{ Msps}$, $I_{SET} = 0\text{ mA}$
Reference current (+)	I_{RT}	—	11	14.5	mA	
Reference current (–)	I_{RB}	–14.5	–11	—	mA	
Input current	I_{IN}	—	70	200	μA	$V_{IN} = 4.1\text{ V}$
Input capacitance	C_{IN}	—	40	—	pF	$f_{IN} = 1\text{ MHz}$, $V_{RB} < V_{IN} < V_{RT}$
Digital output high voltage	V_{OH1}	4.0	4.2	—	V	$I_{OH} = -400\ \mu\text{A}$, $I_{SET} = 0\text{ mA}$
	V_{OH2}	3.5	3.8	—	V	$I_{OH} = -5\text{ mA}$, $I_{SET} = 0\text{ mA}$
Digital output low voltage	V_{OL}	—	0.6	0.70	V	$I_{OL} = 400\ \mu\text{A}$, $I_{SET} = 2\text{ mA}$
Clock input current	I_I	–400	—	400	μA	V_{CLK} : 0.4 V to 2.7 V
Clock input high voltage	V_{IH}	2.0	—	V_{CC}	V	
Clock input low voltage	V_{IL}	0	—	0.8	V	
Static linearity	Differential	D.N.L	–0.5	—	0.5	LSB
Error	Integral	I.N.L	—	—	2.0	LSB _{P-P}
Maximum conversion rate	f_{CLK}	20	—	—	Msps	$f_{IN} = 3.58\text{ MHz}$
Differential gain	DG	—	1.0	—	%	$f_{CLK} = 20\text{ Msps}$, NTSC,
Differential phase	DP	—	0.5	—	deg	40 IRE UNLOCKED
Clock pulse width	t_{WH}	25	30	—	ns	$f_{CLK} = 20\text{ Msps}$
	t_{WL}	15	20	—	ns	$I_{SET} = 5\text{ mA}$
Digital output delay time	t_{PD}	—	35	46	ns	
Digital output hold time	t_{HOLD}	5	10	—	ns	

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Output Code Table

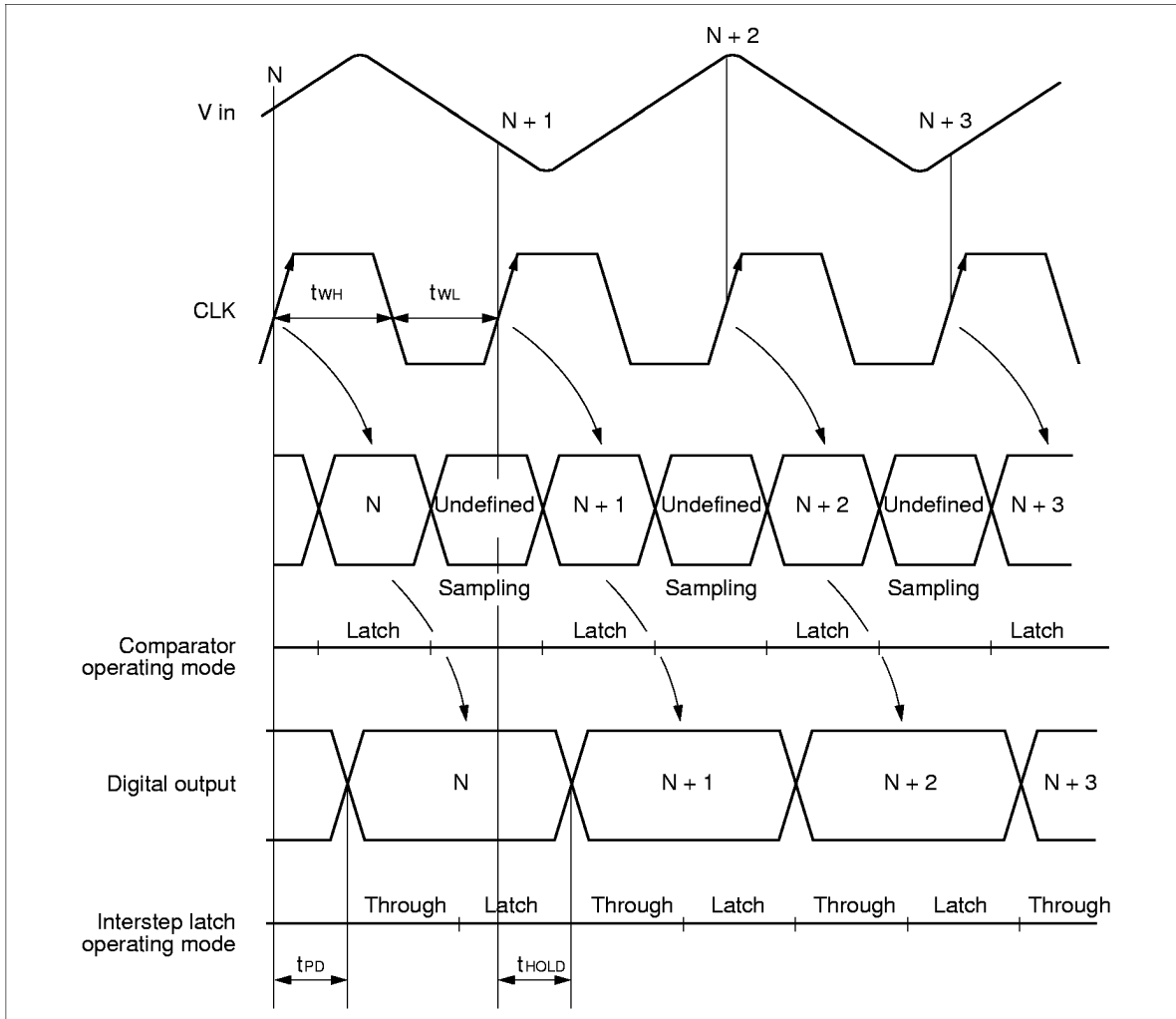
Input voltage	OF	B8	B7	...	B2	B1
V_{RB}	0	0	0		0	0
$V_{RB} + 1\text{LSB}$	0	0	0		0	1
$V_{RB} + 2\text{LSB}$	0	0	0		1	0
$V_{RB} + 127\text{LSB}$	0	0	1		1	1
$V_{RB} + 128\text{LSB}$	0	1	0		0	0
$V_{RT} - 2\text{LSB}$	0	1	1		1	0
$V_{RT} - 1\text{LSB}$	0	1	1		1	1
V_{RT}	1	1	1		1	1

Application Example



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Timing Chart



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