

**MOTOROLA**  
**SEMICONDUCTOR**  
**TECHNICAL DATA**

2

**HIGH SLEW RATE, WIDE BANDWIDTH,  
JFET INPUT OPERATIONAL AMPLIFIERS**

These devices are a new generation of high speed JFET input monolithic operational amplifiers. Innovative design concepts along with JFET technology provide wide gain bandwidth product and high slew rate. Well matched JFET input devices and advanced trim techniques ensure low input offset errors and bias currents. The all NPN output stage features large output voltage swing, no deadband crossover distortion, high capacitive drive capability, excellent phase and gain margins, low open-loop output impedance, and symmetrical source/sink ac frequency response.

This series of devices are available in standard or prime performance (A suffix) grades, fully compensated or decompensated ( $A_{VCL} \geq 2$ ) and are specified over commercial or Military temperature ranges. They are pin compatible with existing Industry standard operational amplifiers, and allow the designer to easily upgrade the performance of existing designs.

- Wide Gain Bandwidth: 8.0 MHz for Fully Compensated Devices  
16 MHz for Decompensated Devices
- High Slew Rate: 25 V/ $\mu$ s for Fully Compensated Devices  
50 V/ $\mu$ s for Decompensated Devices
- High Input Impedance:  $10^{12} \Omega$
- Input Offset Voltage: 0.5 mV Maximum (Single Amplifier)
- Large Output Voltage Swing:  $-14.7 \text{ V to } +14 \text{ V}$  for  
 $V_{CC}/V_{EE} = \pm 15 \text{ V}$
- Low Open-Loop Output Impedance:  $30 \Omega @ 1.0 \text{ MHz}$
- Low THD Distortion: 0.01%
- Excellent Phase/Gain Margins: 55°/7.6 dB for Fully Compensated Devices

**ORDERING INFORMATION**

Op Amp Function	Fully Compensated	$A_{VCL} \geq 2$ Decompensated	Temperature Range	Package
Single	MC35081U,AU	MC35080U,AU	-55 to +125°C	Ceramic DIP
	MC34081D,AD MC34081P,AP	MC34080D,AD MC34080P,AP		0 to +70°C
Dual	MC34082P,AP	MC34083P,AP		Plastic DIP
Quad	MC35084L,AL	MC35085L,AL	-55 to +125	Ceramic DIP
	MC34084DW,ADW MC34084P,AP	MC34085DW,ADW MC34085P,AP		0 to +70°C

**MC34080/MC35080**  
**thru**  
**MC34085/MC35085**

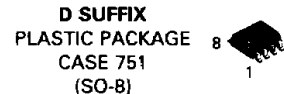
**HIGH PERFORMANCE**  
**JFET INPUT**  
**OPERATIONAL AMPLIFIERS**



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626

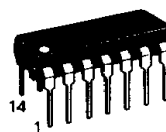
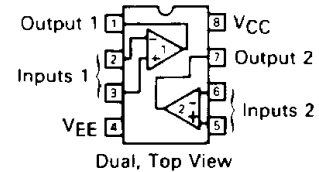
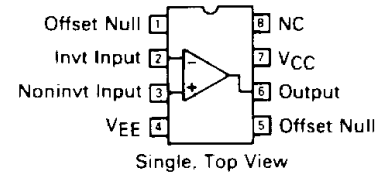


**U SUFFIX**  
CERAMIC PACKAGE  
CASE 693

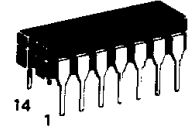


**D SUFFIX**  
PLASTIC PACKAGE  
CASE 751  
(SO-8)

**PIN ASSIGNMENTS**

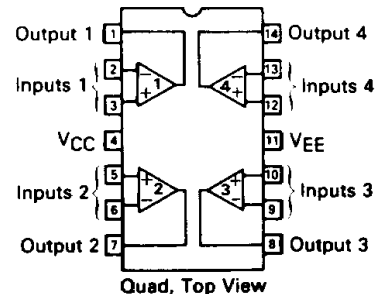


**P SUFFIX**  
PLASTIC PACKAGE  
CASE 646

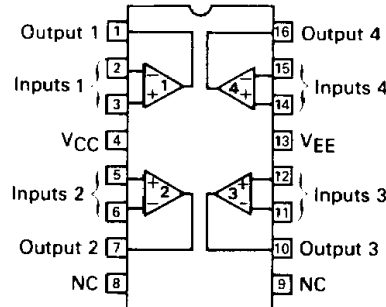


**L SUFFIX**  
CERAMIC PACKAGE  
CASE 632

**PIN ASSIGNMENTS**



**DW SUFFIX**  
PLASTIC PACKAGE  
CASE 751G  
(SO-16L)



# MC34080, MC35080 Series

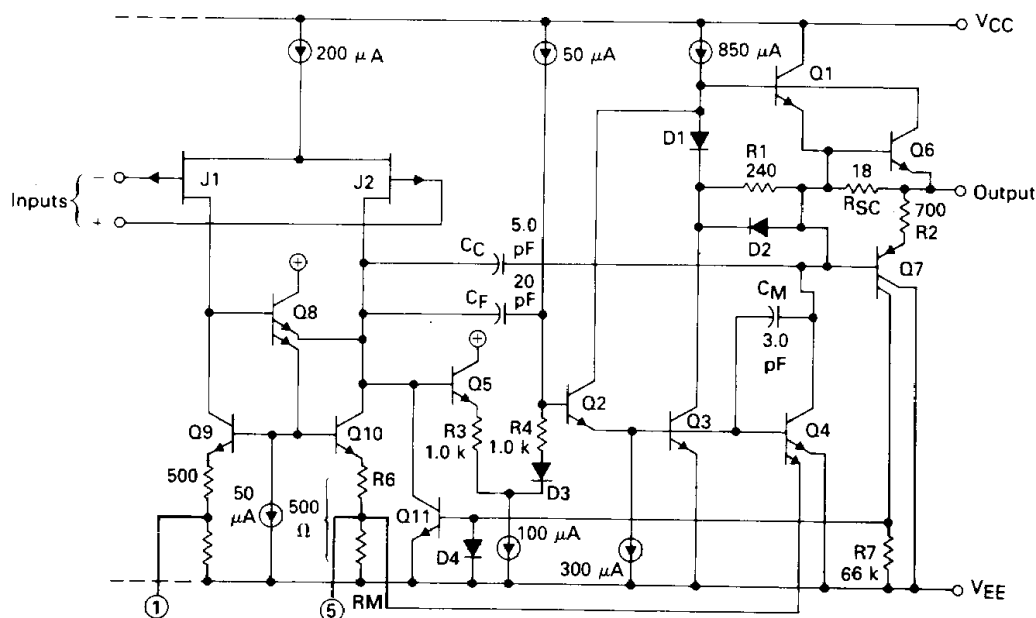
## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from $V_{CC}$ to $V_{EE}$ )	$V_S$	+44	V
Input Differential Voltage Range	$V_{IDR}$	(Note 1)	V
Input Voltage Range	$V_{IR}$	(Note 1)	V
Output Short-Circuit Duration (Note 2)	$t_S$	Indefinite	Seconds
Operating Ambient Temperature Range MC35XXX MC34XXX	$T_A$	-55 to +125 0 to +70	°C
Operating Junction Temperature Ceramic Package Plastic Package	$T_J$	+165 +125	°C
Storage Temperature Range Ceramic Package Plastic Package	$T_{stg}$	-65 to +165 -55 to +125	°C

### NOTES:

1. Either or both input voltages must not exceed the magnitude of  $V_{CC}$  or  $V_{EE}$ .
2. Power dissipation must be considered to ensure maximum junction temperature ( $T_J$ ) is not exceeded.

## EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)



Null Adjust  
(MC34080, 081)\*

\*Pins 1 & 5 (MC34080,081) should *not* be directly grounded or connected to  $V_{CC}$ .

# MC34080, MC35080 Series

## DC ELECTRICAL CHARACTERISTICS ( $V_{CC} = +15\text{ V}$ , $V_{EE} = -15\text{ V}$ , $T_A = T_{\text{low}}$ to $T_{\text{high}}$ [Note 3], unless otherwise noted)

Characteristic	Symbol	A Suffix			Non-Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	$V_{IO}$							mV
Single								
$T_A = +25^\circ\text{C}$		—	0.3	0.5	—	0.5	1.0	
$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ (MC34080, MC34081)		—	—	2.5	—	—	3.0	
$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ (MC35080, MC35081)		—	—	3.5	—	—	4.0	
Dual								
$T_A = +25^\circ\text{C}$		—	0.6	1.0	—	1.0	3.0	
$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ (MC34082, MC34083)		—	—	3.0	—	—	5.0	
$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ (MC35082, MC35083)		—	—	4.0	—	—	6.0	
Quad								
$T_A = +25^\circ\text{C}$	—	3.0	6.0	—	6.0	12		
$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ (MC34084, MC34085)	—	—	8.0	—	—	14		
$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ (MC35084, MC35085)	—	—	9.0	—	—	15		
Average Temperature Coefficient of Offset Voltage	$\Delta V_{IO}/\Delta T$	—	10	—	10	—	$\mu\text{V}/^\circ\text{C}$	
Input Bias Current ( $V_{CM} = 0$ Note 5)	$I_{IB}$							nA
$T_A = +25^\circ\text{C}$		—	0.06	0.2	—	0.06	0.2	
$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$		—	—	4.0	—	—	4.0	
$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$	—	—	50	—	—	50		
Input Offset Current ( $V_{CM} = 0$ Note 5)	$I_{IO}$							nA
$T_A = +25^\circ\text{C}$		—	0.02	0.1	—	0.02	0.1	
$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$		—	—	2.0	—	—	2.0	
$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$	—	—	25	—	—	25		
Large Signal Voltage Gain ( $V_O = \pm 10\text{ V}$ , $R_L = 2.0\text{ k}$ )	$A_{VOL}$							V/mV
$T_A = +25^\circ\text{C}$		50	80	—	25	80	—	
$T_A = T_{\text{low}}$ to $T_{\text{high}}$		25	—	—	15	—	—	
Output Voltage Swing	$V_{OH}$							V
$R_L = 2.0\text{ k}$ , $T_A = +25^\circ\text{C}$		13.2	13.7	—	13.2	13.7	—	
$R_L = 10\text{ k}$ , $T_A = +25^\circ\text{C}$		13.4	13.9	—	13.4	13.9	—	
$R_L = 10\text{ k}$ , $T_A = T_{\text{low}}$ to $T_{\text{high}}$		13.4	—	—	13.4	—	—	
$R_L = 2.0\text{ k}$ , $T_A = +25^\circ\text{C}$		—	-14.1	-13.5	—	-14.1	-13.5	
$R_L = 10\text{ k}$ , $T_A = +25^\circ\text{C}$		—	-14.7	-14.1	—	-14.7	-14.1	
$R_L = 10\text{ k}$ , $T_A = T_{\text{low}}$ to $T_{\text{high}}$	—	—	-14.0	—	—	-14.0		
Output Short-Circuit Current ( $T_A = +25^\circ\text{C}$ )	$I_{SC}$							mA
Input Overdrive = 1.0 V, Output to Ground								
Source		20	31	—	20	31	—	
Sink	20	28	—	20	28	—		
Input Common Mode Voltage Range	$V_{ICR}$							V
$T_A = +25^\circ\text{C}$		(V <sub>EE</sub> + 4.0) to (V <sub>CC</sub> - 2.0)			(V <sub>EE</sub> + 4.0) to (V <sub>CC</sub> - 2.0)			
Common Mode Rejection Ratio ( $R_S \leq 10\text{ k}$ , $T_A = +25^\circ\text{C}$ )	CMRR	75	90	—	70	90	—	dB
Power Supply Rejection Ratio ( $R_S = 100\ \Omega$ , $T_A = 25^\circ\text{C}$ )	PSRR	75	86	—	70	86	—	dB
Power Supply Current	$I_D$							mA
Single								
$T_A = +25^\circ\text{C}$		—	2.5	3.4	—	2.5	3.4	
$T_A = T_{\text{low}}$ to $T_{\text{high}}$		—	—	4.2	—	—	4.2	
Dual								
$T_A = +25^\circ\text{C}$		—	4.9	6.0	—	4.9	6.0	
$T_A = T_{\text{low}}$ to $T_{\text{high}}$		—	—	7.5	—	—	7.5	
Quad								
$T_A = +25^\circ\text{C}$	—	9.7	11	—	9.7	11		
$T_A = T_{\text{low}}$ to $T_{\text{high}}$	—	—	13	—	—	13		

### NOTES: (CONTINUED)

3.  $T_{\text{low}} = -55^\circ\text{C}$  for MC35080,A, MC35081,A, MC35082,A, MC35083,A, MC35084,A, MC35085,A  
 $T_{\text{low}} = 0^\circ\text{C}$  for MC34080,A, MC34081,A, MC34082,A, MC34083,A, MC34084,A, MC34085,A  
 $T_{\text{high}} = +125^\circ\text{C}$  for MC35080,A, MC35081,A, MC35082,A, MC35083,A, MC35084,A, MC35085,A  
 $T_{\text{high}} = +70^\circ\text{C}$  for MC34080,A, MC34081,A, MC34082,A, MC34083,A, MC34084,A, MC34085,A

4. See application information for typical changes in input offset voltage due to solderability and temperature cycling.  
 5. Limits at  $T_A = +25^\circ\text{C}$  are guaranteed by high temperature ( $T_{\text{high}}$ ) testing.

# MC34080, MC35080 Series

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## AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = +15\text{ V}$ , $V_{EE} = -15\text{ V}$ , $T_A = +25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	A Suffix			Non-Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Slew Rate ( $V_{in} = -10\text{ V to }+10\text{ V}$ , $R_L = 2.0\text{ k}$ , $C_L = 100\text{ pF}$ ) Compensated $A_V = +1.0$ $A_V = -1.0$ Decompensated $A_V = +2.0$ $A_V = -1.0$	SR	20	25	—	20	25	—	$\text{V}/\mu\text{s}$
Settling Time (10 V Step, $A_V = -1.0$ ) To 0.10% ( $\pm 1/2$ LSB of 9-Bits) To 0.01% ( $\pm 1/2$ LSB of 12-Bits)	$t_s$	—	0.72	—	—	0.72	—	$\mu\text{s}$
Gain Bandwidth Product ( $f = 200\text{ kHz}$ ) Compensated Decompensated	GBW	6.0	8.0	—	6.0	8.0	—	MHz
Power Bandwidth ( $R_L = 2.0\text{ k}$ , $V_O = 20\text{ V}_{p-p}$ , THD = 5.0%) Compensated $A_V = +1.0$ Decompensated $A_V = -1.0$	BWp	—	400	—	—	400	—	kHz
Phase Margin (Compensated) $R_L = 2.0\text{ k}$ $R_L = 2.0\text{ k}$ , $C_L = 100\text{ pF}$	$\phi_m$	—	55	—	—	55	—	Degrees
Gain Margin (Compensated) $R_L = 2.0\text{ k}$ $R_L = 2.0\text{ k}$ , $C_L = 100\text{ pF}$	$A_m$	—	7.6	—	—	7.6	—	dB
Equivalent Input Noise Voltage $R_S = 100\ \Omega$ , $f = 1.0\text{ kHz}$	$e_n$	—	30	—	—	30	—	$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current ( $f = 1.0\text{ kHz}$ )	$i_n$	—	0.01	—	—	0.01	—	$\text{pA}/\sqrt{\text{Hz}}$
Input Capacitance	$C_i$	—	5.0	—	—	5.0	—	pF
Input Resistance	$r_i$	—	1012	—	—	1012	—	$\Omega$
Total Harmonic Distortion $A_V = +10$ , $R_L = 2.0\text{ k}$ , $2.0 \leq V_O \leq 20\text{ V}_{p-p}$ , $f = 10\text{ kHz}$	THD	—	0.05	—	—	0.05	—	%
Channel Separation ( $f = 10\text{ kHz}$ )	—	—	120	—	—	120	—	dB
Open-Loop Output Impedance ( $f = 1.0\text{ MHz}$ )	$z_o$	—	35	—	—	35	—	$\Omega$

## TYPICAL PERFORMANCE CURVES

FIGURE 1 — INPUT COMMON MODE VOLTAGE RANGE versus TEMPERATURE

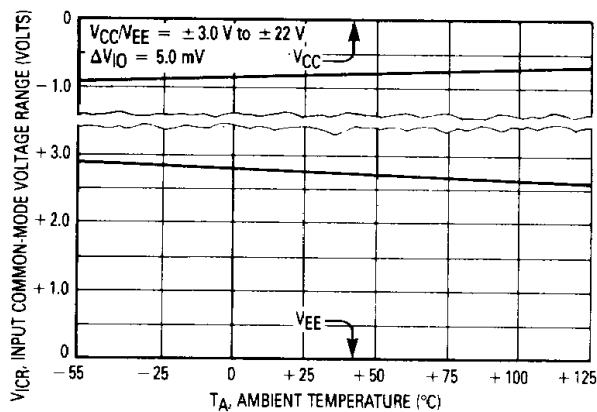
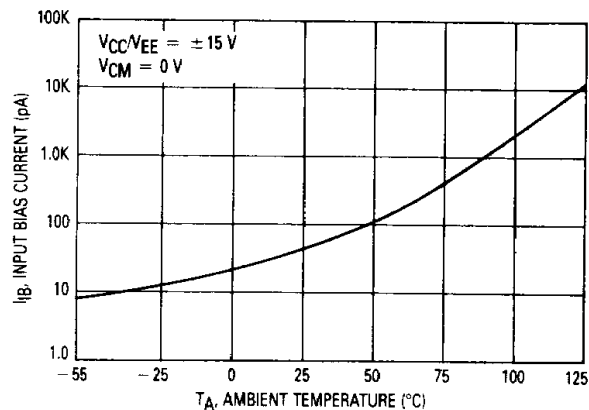


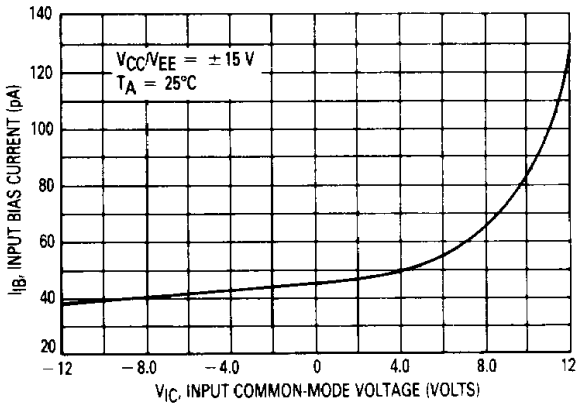
FIGURE 2 — INPUT BIAS CURRENT versus TEMPERATURE



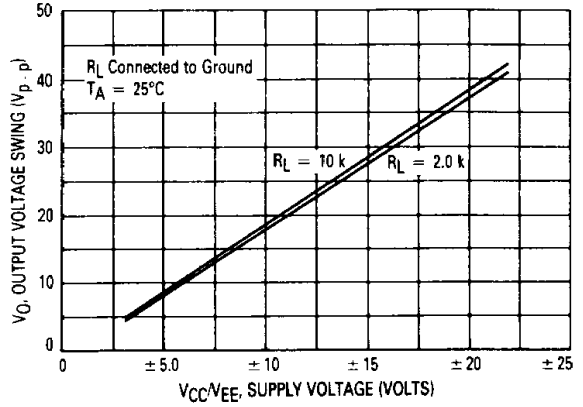
# MC34080, MC35080 Series

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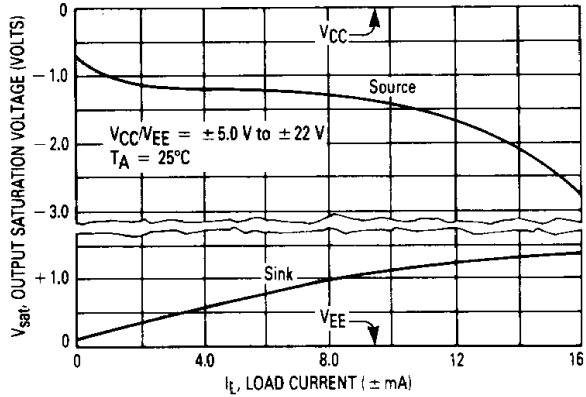
**FIGURE 3 — INPUT BIAS CURRENT versus INPUT COMMON-MODE VOLTAGE**



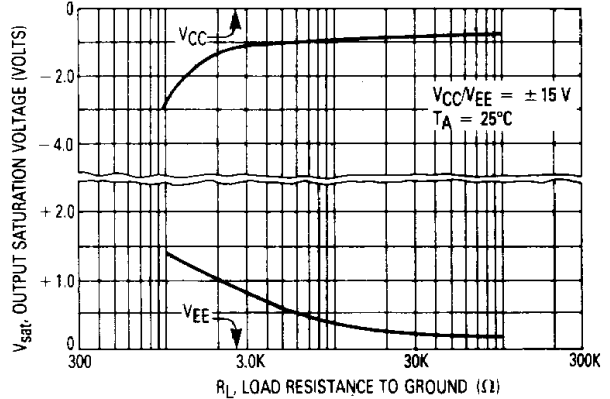
**FIGURE 4 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE**



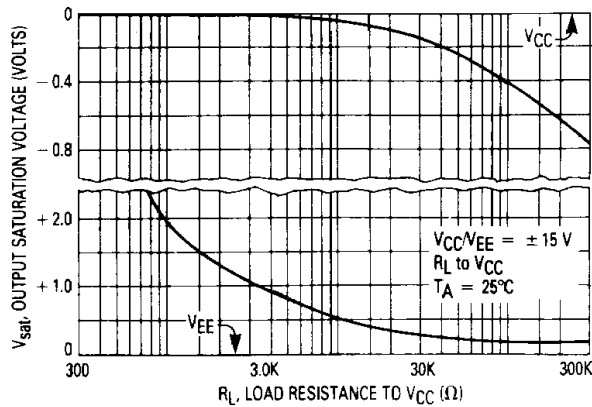
**FIGURE 5 — OUTPUT SATURATION versus LOAD CURRENT**



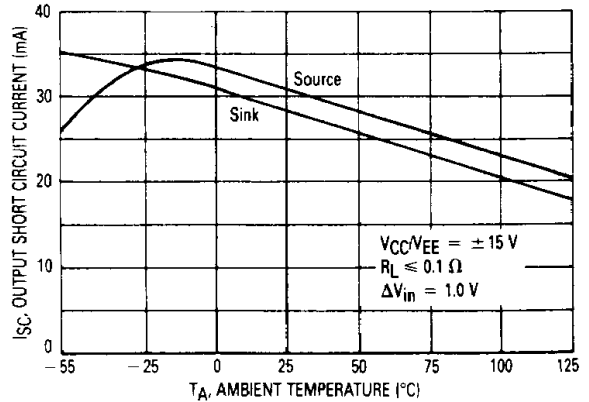
**FIGURE 6 — OUTPUT SATURATION versus LOAD RESISTANCE TO GROUND**



**FIGURE 7 — OUTPUT SATURATION versus LOAD RESISTANCE TO  $V_{CC}$**



**FIGURE 8 — OUTPUT SHORT CIRCUIT CURRENT versus TEMPERATURE**



# MC34080, MC35080 Series

FIGURE 9 — OUTPUT IMPEDANCE versus FREQUENCY

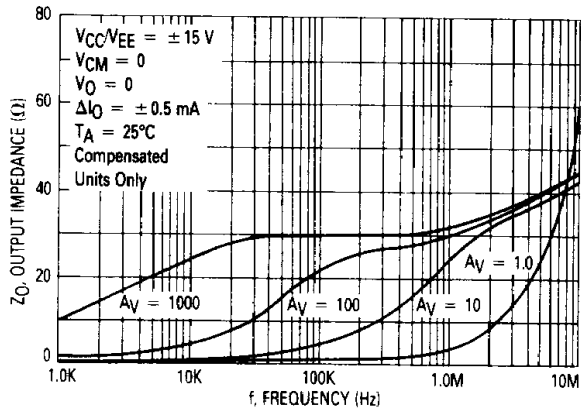


FIGURE 10 — OUTPUT IMPEDANCE versus FREQUENCY

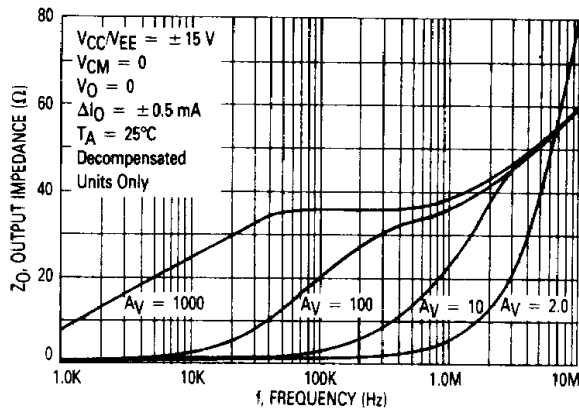


FIGURE 11 — OUTPUT VOLTAGE SWING versus FREQUENCY

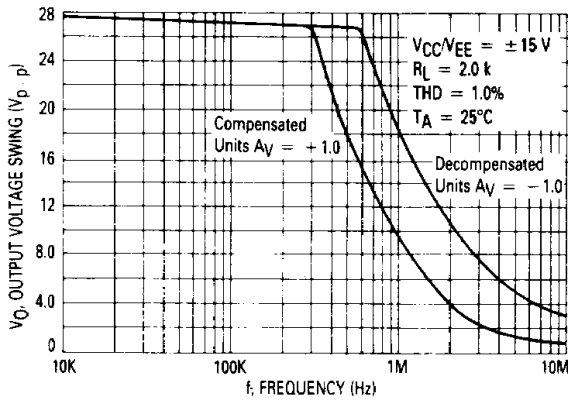


FIGURE 12 — OUTPUT DISTORTION versus FREQUENCY

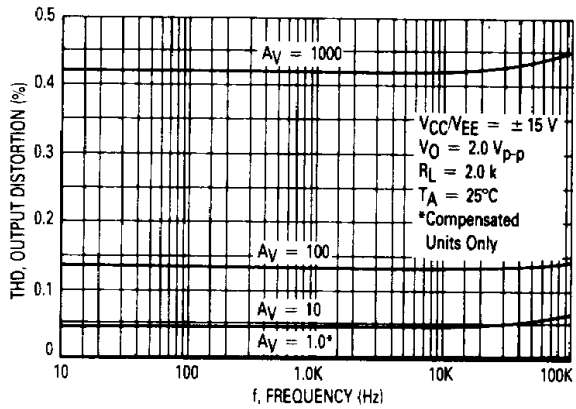
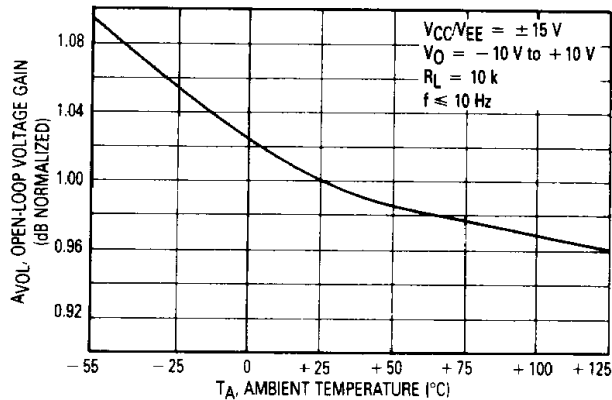
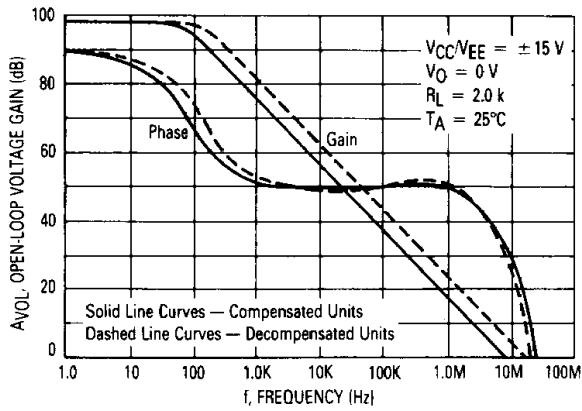


FIGURE 13 — OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

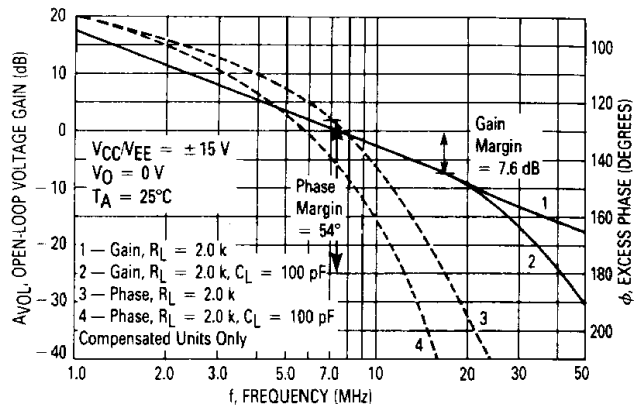


# MC34080, MC35080 Series

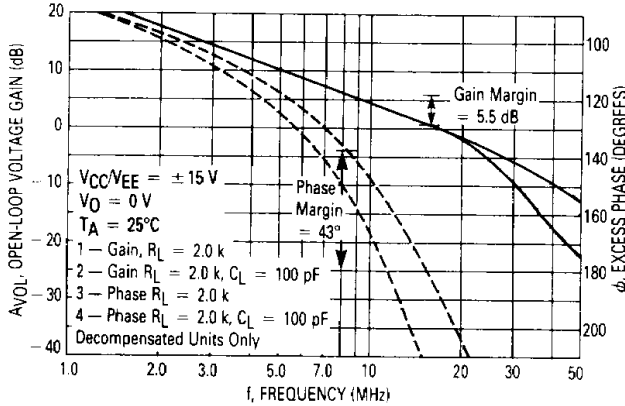
**FIGURE 14 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY**



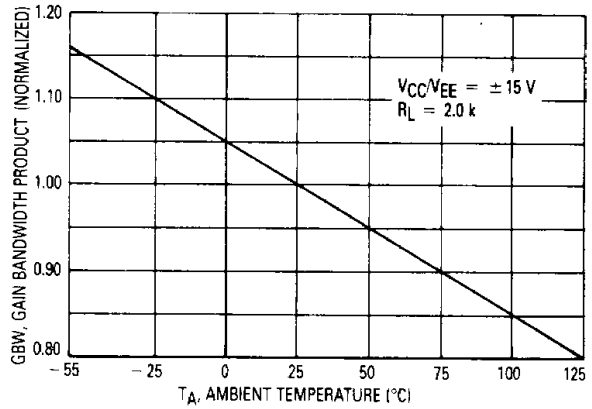
**FIGURE 15 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY**



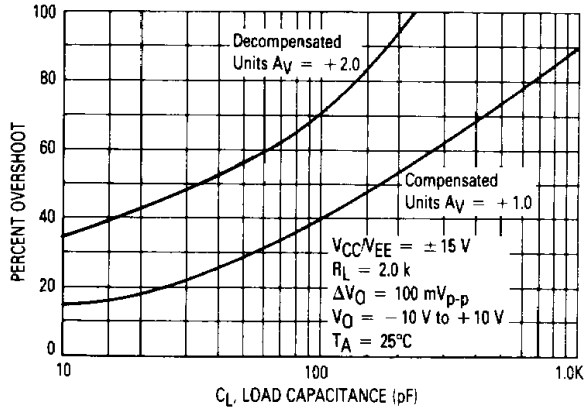
**FIGURE 16 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY**



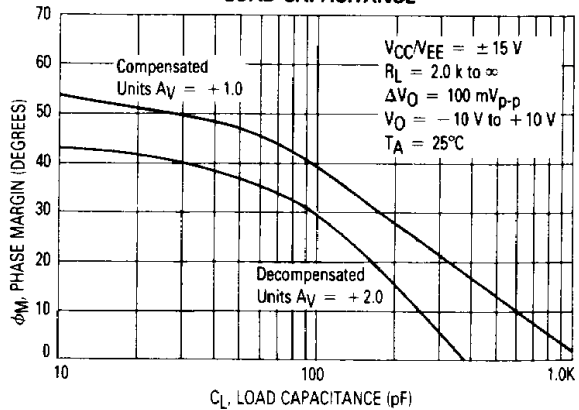
**FIGURE 17 — NORMALIZED GAIN BANDWIDTH PRODUCT versus TEMPERATURE**



**FIGURE 18 — PERCENT OVERSHOOT versus LOAD CAPACITANCE**



**FIGURE 19 — PHASE MARGIN versus LOAD CAPACITANCE**



# MC34080, MC35080 Series

FIGURE 20 — GAIN MARGIN versus LOAD CAPACITANCE

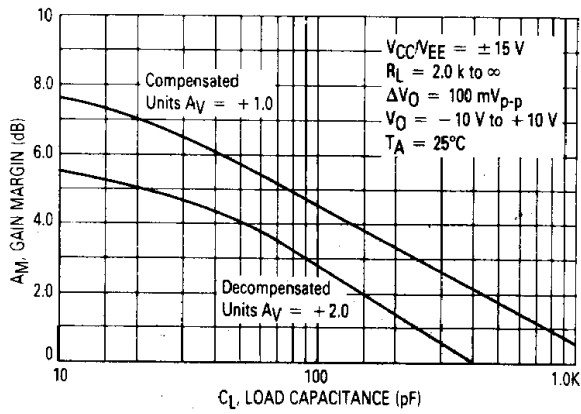


FIGURE 21 — PHASE MARGIN versus TEMPERATURE

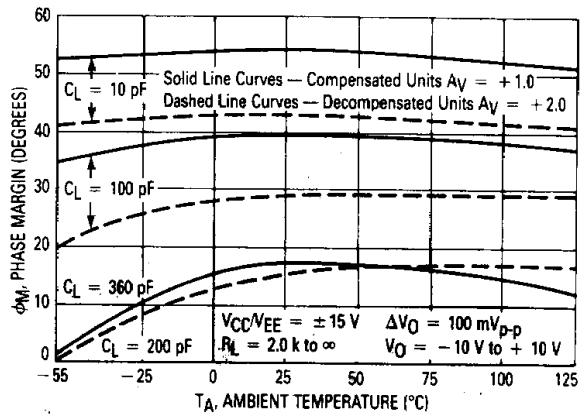


FIGURE 22 — GAIN MARGIN versus TEMPERATURE

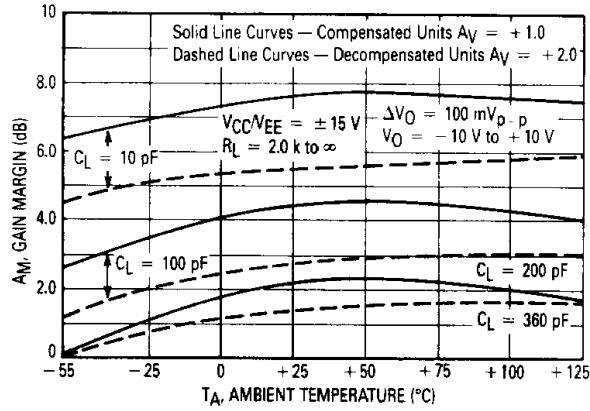
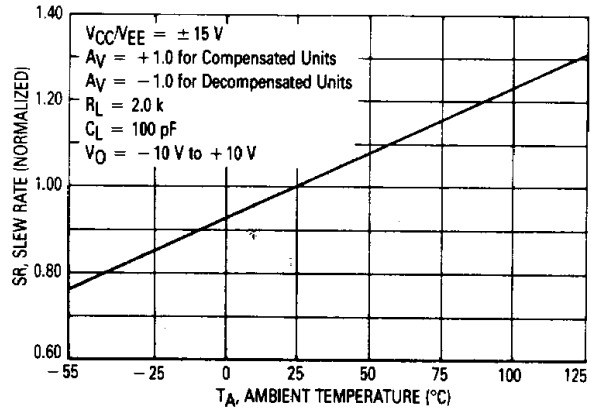


FIGURE 23 — NORMALIZED SLEW RATE versus TEMPERATURE





# MC34080, MC35080 Series

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## MC34084 TRANSIENT RESPONSE

$A_V = +1.0$ ,  $R_L = 2.0 \text{ k}$ ,  $V_{CC}/V_{EE} = \pm 15 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

FIGURE 24 — SMALL-SIGNAL

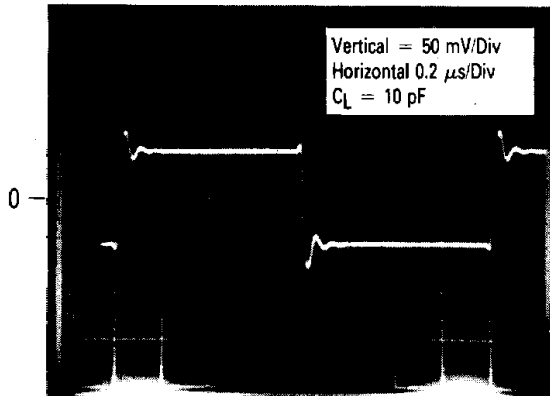
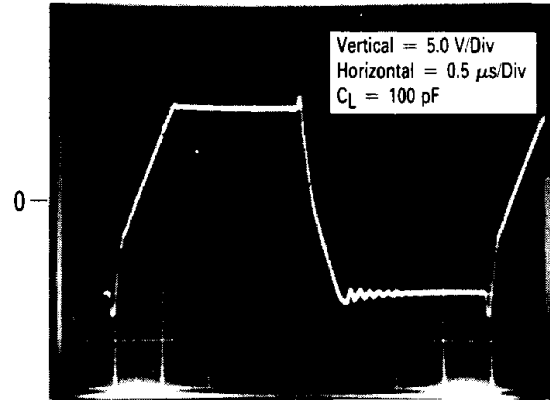


FIGURE 25 — LARGE-SIGNAL



## MC34085 TRANSIENT RESPONSE

$A_V = +2.0$ ,  $R_L = 2.0 \text{ k}$ ,  $V_{CC}/V_{EE} = \pm 15 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

FIGURE 26 — SMALL-SIGNAL

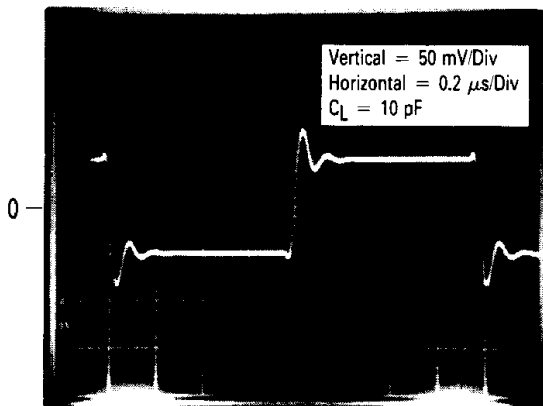
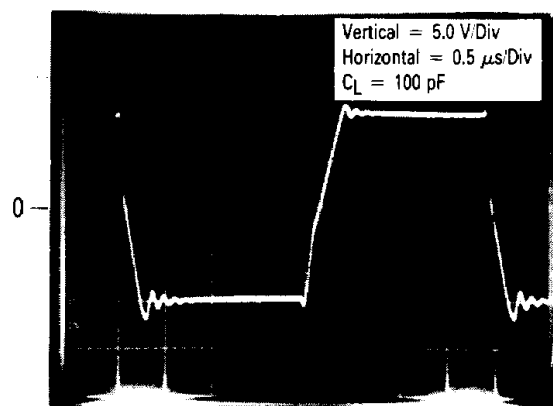


FIGURE 27 — LARGE-SIGNAL



# MC34080, MC35080 Series

FIGURE 28 — COMMON-MODE REJECTION RATIO versus FREQUENCY

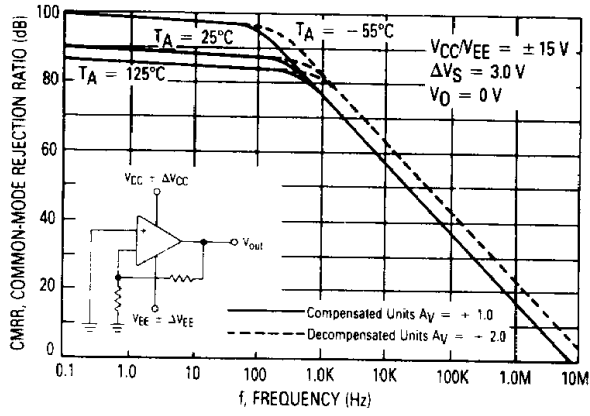


FIGURE 29 — POWER SUPPLY REJECTION RATIO versus FREQUENCY

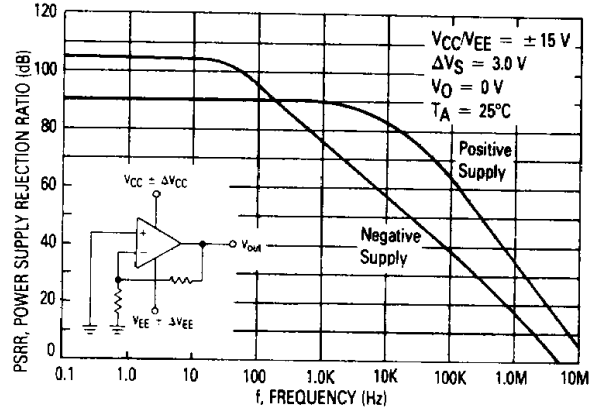
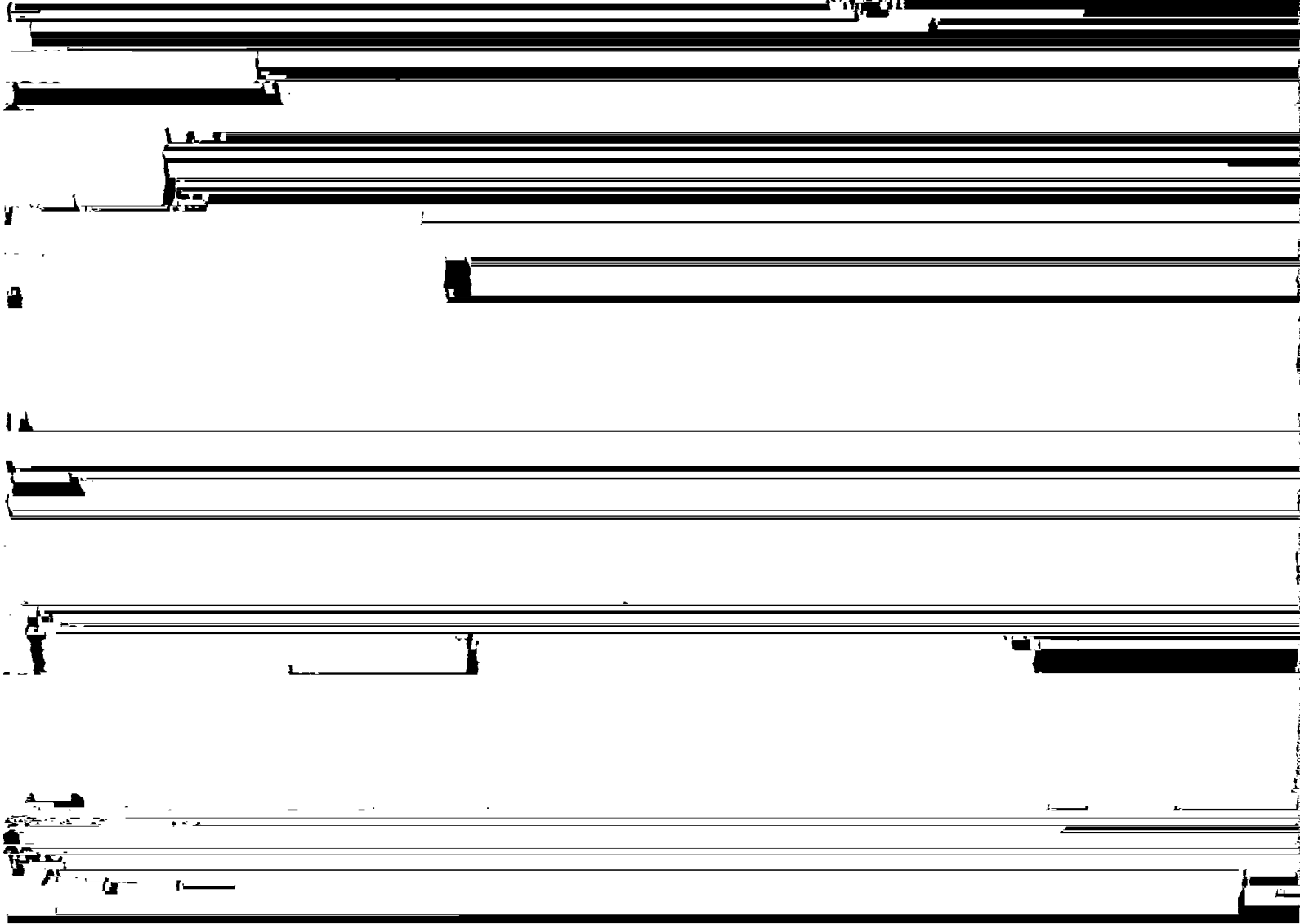


FIGURE 30 — POWER SUPPLY REJECTION RATIO versus TEMPERATURE

FIGURE 31 — NORMALIZED SUPPLY CURRENT versus SUPPLY VOLTAGE



### APPLICATIONS INFORMATION

The bandwidth and slew rate of the MC34080 series is nearly double that of currently available general purpose JFET op-amps. This improvement in ac performance is due to the P-channel JFET differential input stage driving a compensated miller integration amplifier in conjunction with an all NPN output stage.

The all NPN output stage offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. With a 10 k load resistance, the op-amp can typically swing within 1.0 V of the positive rail ( $V_{CC}$ ), and within 0.3 volts of the negative rail ( $V_{EE}$ ), providing a 28.7 Vp-p swing from  $\pm 15$  volt supplies. This large output swing becomes most noticeable at lower supply voltages. If the load resistance is referenced to  $V_{CC}$  instead of ground, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to  $V_{CC}$  during the positive swing and the NPN output transistor will pull the output very near  $V_{EE}$  during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull-up capability.

The all NPN transistor output stage is also inherently fast, contributing to the operational amplifier's high gain-bandwidth product and fast settling time. The associated high frequency output impedance is 50 ohms (typical) at 8.0 MHz. This allows driving capacitive loads from 0 to 300 pF without oscillations over the military temperature range, and over the full range of output swing. The 55° phase margin and 7.6 dB gain margin as well as the general gain and phase characteristics are virtually independent of the sink/source output swing conditions. The high frequency characteristics of the MC34080 series is especially useful for active filter applications.

The common mode input range is from 2.0 volts below the positive rail ( $V_{CC}$ ) to 4.0 volts above the neg-

ative rail ( $V_{EE}$ ). The amplifier remains active if the inputs are biased at the positive rail. This may be useful for some applications in that single supply operation is possible with a single negative supply. However, a degradation of offset voltage and voltage gain may result.

Phase reversal does not occur if either the inverting or noninverting input (or both) exceeds the positive common mode limit. If either input (or both) exceeds the negative common mode limit, the output will be in the high state. The input stage also allows a differential up to  $\pm 44$  volts, provided the maximum input voltage range is not exceeded. The supply voltage operating range is from  $\pm 5.0$  V to  $\pm 22$  V.

For optimum frequency performance and stability careful component placement and printed circuit board layout should be exercised. For example, long unshielded input or output leads may result in unwanted input-output coupling. In order to reduce the input capacitance, resistors connected to the input pins should be physically close to these pins. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pickup" at this node.

Supply decoupling with adequate capacitance close to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit large impedance changes over temperature.

Primarily due to the JFET inputs of the op amp, the input offset voltage may change due to temperature cycling and board soldering. After 20 temperature cycles ( $-55^{\circ}\text{C}$  to  $165^{\circ}\text{C}$ ), the typical standard deviation for input offset voltage is 559  $\mu\text{V}$  and 473  $\mu\text{V}$  in the plastic and ceramic packages respectively. With respect to board soldering ( $260^{\circ}\text{C}$ , 10 seconds) the typical standard deviation for input offset voltage is 525  $\mu\text{V}$  and 227  $\mu\text{V}$  in the plastic and ceramic package respectively. Socketed plastic or ceramic packaged devices should be used over a minimal temperature range for optimum input offset voltage performance.

FIGURE 34 — OFFSET NULLING CIRCUIT

