

Document Title
4Bank x 512K x 32bits Synchronous DRAM

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Draft	May. 2004	Preliminary
0.2	Removed Preliminary	July 2004	
0.3	1. Updated Output Load Capacitance for Access Time Measurement CL = 30pF in AC OPERATING TEST CONDITION 2. Updated the tolerance zone of the leads and the description of the package type in PACKAGE DIMENSION	Sep. 2004	

This document is a general product description and is subject to change without notice. Hynix does not assume any responsibility for use of circuits described. No patent licenses are implied.

Rev. 0.3 / Sep. 2004

1

DESCRIPTION

The Hynix HY57V643220D(L/S)T(P) series is a 67,108,864bit CMOS Synchronous DRAM, ideally suited for the memory applications which require wide data I/O and high bandwidth. HY57V643220D(L/S)T(P) is organized as 4banks of 524,228x32.

HY57V643220D(L/S)T(P) is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTTL.

Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a '2N' rule)

FEATURES

- Voltage : VDD, VDDQ 3.3V supply voltage
- All device pins are compatible with LVTTTL interface
- JEDEC standard 400mil 86pin TSOP-II with 0.5mm of pin pitch
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by DQM 0, 1, 2 and DQM 3
- Internal four banks operation
- Auto refresh and self refresh
- 4096 Refresh cycles / 64ms
- Programmable Burst Length and Burst Type
 - 1, 2, 4, 8 or full page for Sequential Burst
 - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{\text{CAS}}$ Latency ; 2, 3 Clocks
- Burst Read Single Write operation

ORDERING INFORMATION

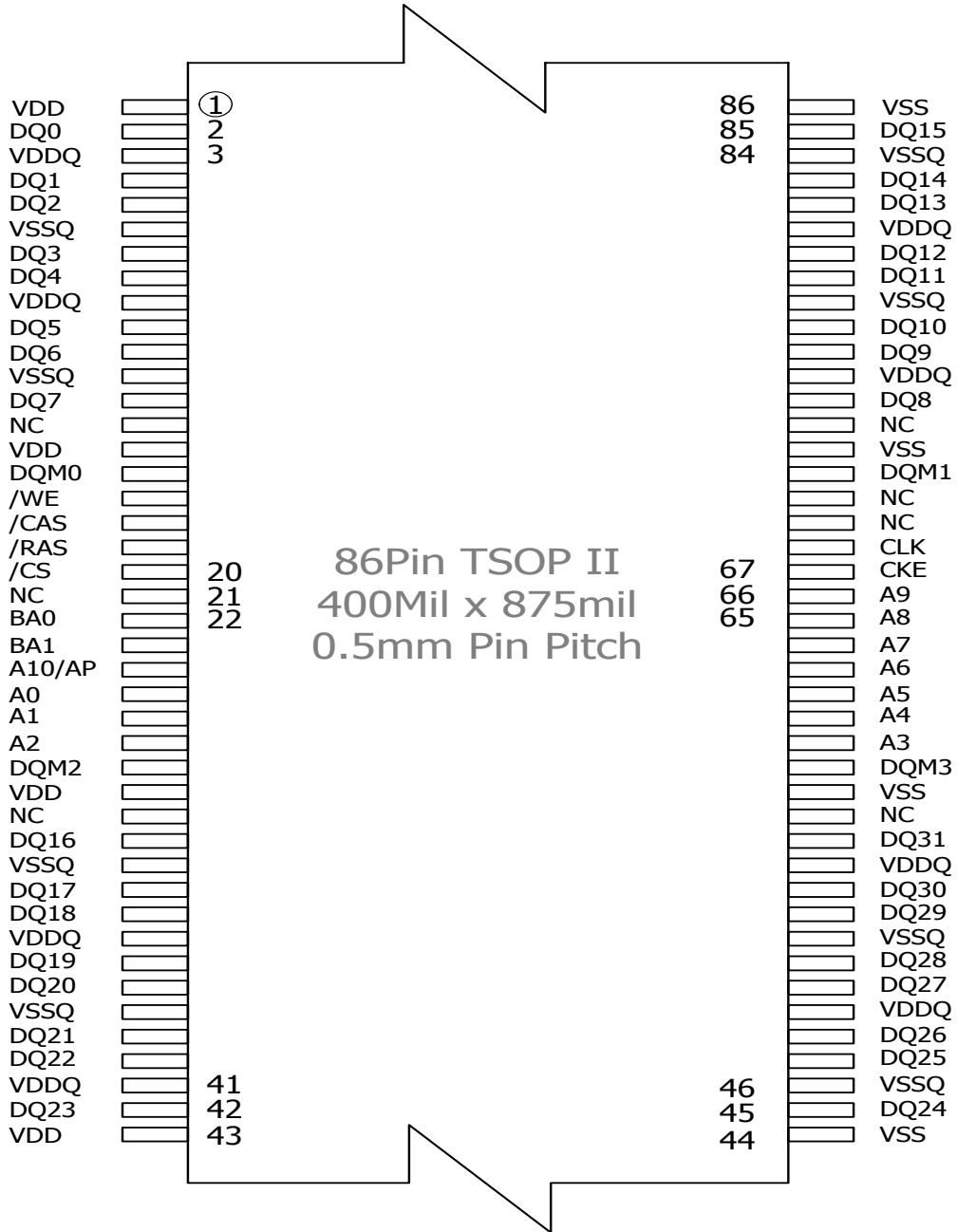
Part No.	Clock Frequency	Organization	Interface	Package
HY57V643220D(L/S)T(P)-45	222MHz	4Banks x 512Kbits x32	LVTTTL	86pin TSOP-II (Lead Free)
HY57V643220D(L/S)T(P)-5	200MHz			
HY57V643220D(L/S)T(P)-55	183MHz			
HY57V643220D(L/S)T(P)-6	166MHz			
HY57V643220D(L/S)T(P)-7	143MHz			

Note

1. HY57V643220DT(P) Series : Normal Power
2. HY57V643220DLT(P) Series : Low Power
3. HY57V643220DST(P) Series : Super Low Power
4. HY57V643220D(L/S)T Series : Leaded
5. HY57V643220D(L/S)TP Series : Lead Free

This document is a general product description and is subject to change without notice. Hynix does not assume any responsibility for use of circuits described. No patent licenses are implied.

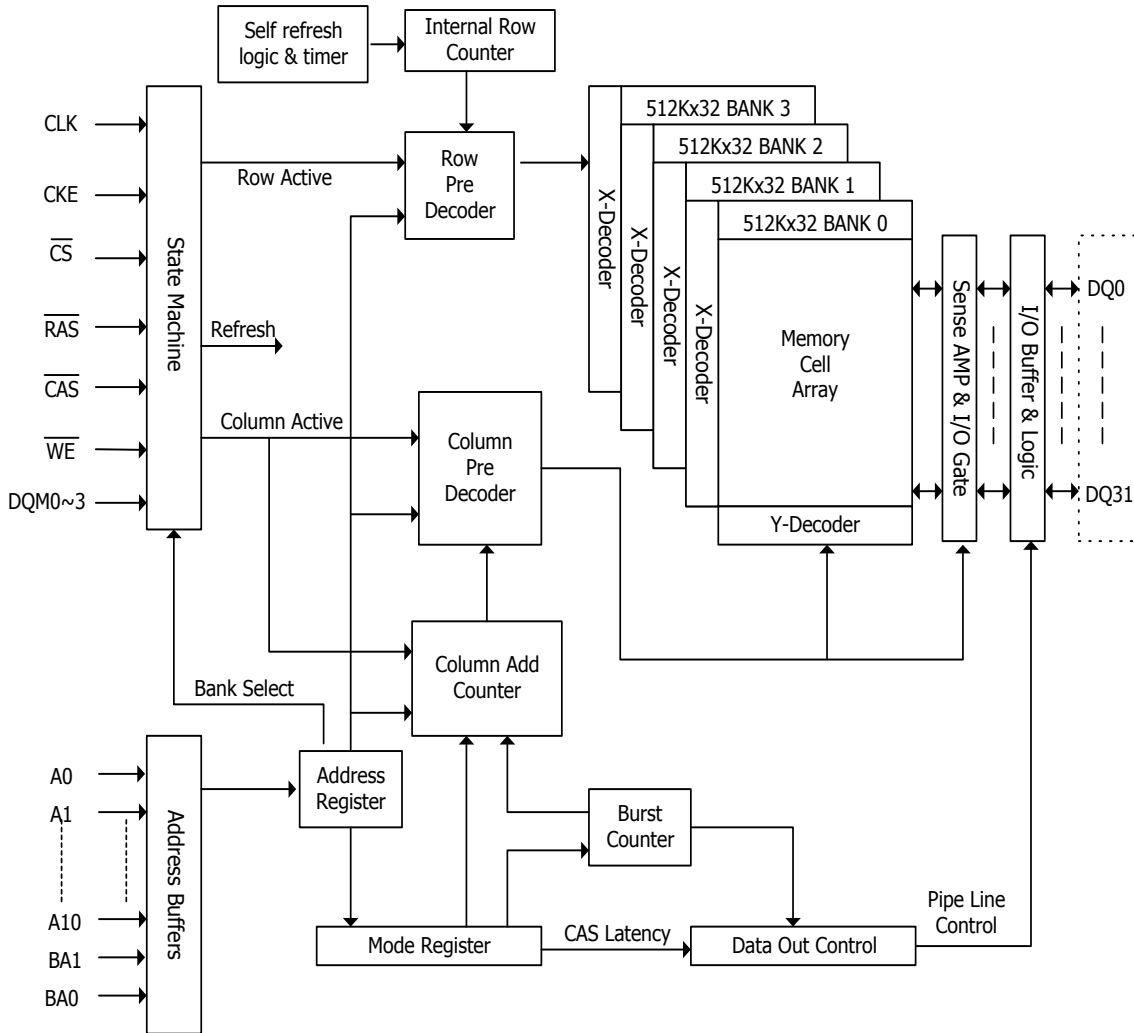
86PIN TSOP II CONFIGURATION



Pin FUNCTION DESCRIPTIONS

Pin	Pin Name	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK.
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
\overline{CS}	Chip Select	Enables or disables all inputs except CLK, CKE and DQM
BA0, BA1	Bank Address	Selects bank to be activated during \overline{RAS} activity Selects bank to be read/written during \overline{CAS} activity
A0 ~ A10	Address	Row Address : RA0 ~ RA10, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
\overline{RAS} , \overline{CAS} , \overline{WE}	Row Address Strobe, Column Address Strobe, Write Enable	\overline{RAS} , \overline{CAS} and \overline{WE} define the operation Refer function truth table for details
DQM0~3	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ31	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	Power Supply/Ground	Power supply for internal circuits and input buffers
VDDQ/VSSQ	Data Output Power/ Ground	Power supply for output buffers
NC	No Connection	No connection

FUNCTIONAL BLOCK DIAGRAM
512Kbit x 4banks x 32 I/O Low Power Synchronous DRAM



BASIC FUNCTIONAL DESCRIPTION

Mode Register

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	OP Code	0	0	CAS Latency			BT	Burst Length		

OP Code

A9	Write Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

Burst Type

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Length	
			A3 = 0	A3 = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	-40 ~ 85	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD relative to VSS	VDD	-1.0 ~ 4.6	V
Voltage on VDDQ relative to VSS	VDDQ	-1.0 ~ 4.6	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	1	W
Soldering Temperature · Time	TSOLDER	260 · 10	°C · Sec

DC OPERATING CONDITION (TA= -40 to 85°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	VDD, VDDQ	3.0	3.3	3.6	V	1
Input High Voltage	VIH	2.0	3.3	VDDQ+0.3	V	1, 2
Input Low Voltage	VIL	-0.3	-	0.8	V	1, 3

- Note : 1. All voltages are referenced to VSS = 0V
 2. VIH(max) is acceptable 5.6V AC pulse width with <=3ns of duration.
 3. VIL(min) is acceptable -2.0V AC pulse width with <=3ns of duration

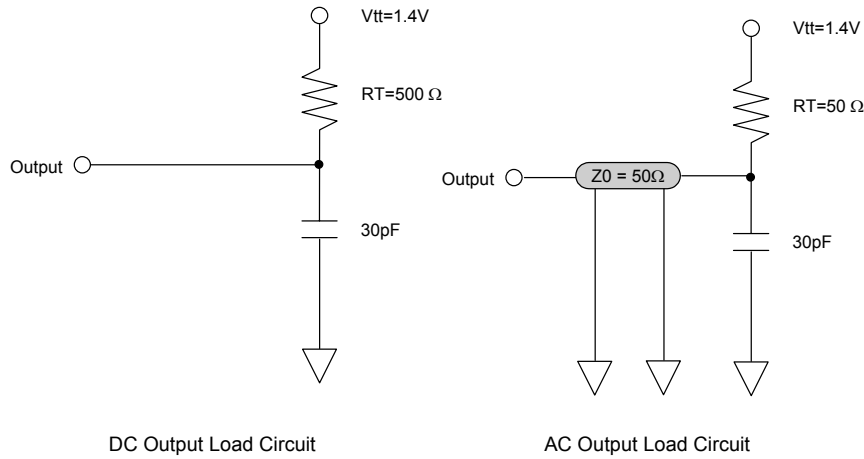
AC OPERATING TEST CONDITION (TA= -40 to 85 °C, VDD=3.3±0.3V, VSS=0V)

Parameter	Symbol	Value	Unit	Note
AC Input High/Low Level Voltage	VIH / VIL	2.4/0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise/Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	CL	30	pF	

CAPACITANCE (TA= -40 to 85 °C, f=1MHz, VDD=3.3V)

Parameter	Pin	Symbol	Min	Max	Unit
Input capacitance	CLK	CI1	2.5	3.5	pF
	A0 ~ A10, BA0, BA1, CE, CS, RAS, CAS, WE, DQM 0~3	CI2	2.5	3.8	pF
Data input / output capacitance	DQ0 ~ DQ31	CI/O	4	6.5	pF

Note 1.



DC CHARACTERISTICS I (TA= 0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Input Leakage Current	ILI	-1	1	uA	1
Output Leakage Current	ILO	-1	1	uA	2
Output High Voltage	VOH	2.4	-	V	IOH = -2mA
Output Low Voltage	VOL	-	0.4	V	IOL = +2mA

Note :

- VIN = 0 to 3.6V, All other balls are not tested under VIN =0V
- DOUT is disabled, VOUT=0 to 3.6

DC CHARACTERISTICS II (TA= 0 to 70°C)

Parameter	Symbol	Test Condition	Speed					Unit	Note	
			45	5	55	6	7			
Operating Current	IDD1	Burst length=1, One bank active tRC ≥ tRC(min), IOL=0mA	220	200	190	180	170	mA	1	
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ VIL(max), tCK = 15ns	2					mA		
	IDD2PS	CKE ≤ VIL(max), tCK = ∞	2					mA		
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$, tCK = 15ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V	17					mA		
	IDD2NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.	12							
Active Standby Current in Power Down Mode	IDD3P	CKE ≤ VIL(max), tCK = 15ns	3					mA		
	IDD3PS	CKE ≤ VIL(max), tCK = ∞	3							
Active Standby Current in Non Power Down Mode	IDD3N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$, tCK = 15ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V	40					mA		
	IDD3NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.	30							
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), IOL=0mA All banks active	CL=3	290	280	260	240	210	mA	1
Auto Refresh Current	IDD5	tRC ≥ tRC(min), All banks active	260	250	235	220	210	mA	2	
Self Refresh Current	IDD6	CKE ≤ 0.2V	Normal	2					mA	3
			Low Power	0.8					mA	4
			Super Low Power	450					uA	5

Note :

1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open
2. Min. of tRC (Refresh \overline{RAS} cycle time) is shown at AC CHARACTERISTICS II
3. HY57V643220DT(P) Series
4. HY57V643220DLT(P) Series
5. HY57V643220DST(P) Series

AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

Parameter		Symbol	45		5		55		6		7		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
System Clock Cycle Time	CAS Latency=3	tCK3	4.5	1000	5.0	1000	5.5	1000	6.0	1000	7.0	1000	ns	
	CAS Latency=2	tCK2	10		10		10		10		ns			
Clock High Pulse Width		tCHW	1.75	-	2.0	-	2.25	-	2.5	-	3.0	-	ns	1
Clock Low Pulse Width		tCLW	1.75	-	2.0	-	2.25	-	2.5	-	3.0	-	ns	1
Access Time From Clock	CAS Latency=3	tAC3	-	4.5	-	4.5	-	5.0	-	5.5	-	5.5	ns	2
	CAS Latency=2	tAC2	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	ns	
Data-out Hold Time		tOH	1.5	-	1.5	-	2.0	-	2.0	-	2.0	-	ns	
Data-Input Setup Time		tDS	1.3	-	1.5	-	1.5	-	1.5	-	1.75	-	ns	1
Data-Input Hold Time		tDH	0.8	-	1.0	-	1.0	-	1.0	-	1.0	-	ns	1
Address Setup Time		tAS	1.3	-	1.5	-	1.5	-	1.5	-	1.75	-	ns	1
Address Hold Time		tAH	0.8	-	1.0	-	1.0	-	1.0	-	1.0	-	ns	1
CKE Setup Time		tCKS	1.3	-	1.5	-	1.5	-	1.5	-	1.75	-	ns	1
CKE Hold Time		tCKH	0.8	-	1.0	-	1.0	-	1.0	-	1.0	-	ns	1
Command Setup Time		tCS	1.3	-	1.5	-	1.5	-	1.5	-	1.75	-	ns	1
Command Hold Time		tCH	0.8	-	1.0	-	1.0	-	1.0	-	1.0	-	ns	1
CLK to Data Output in Low-Z Time		tOLZ	1.0	-	1.0	-	1.0	-	1.0	-	1.0	-	ns	
CLK to Data Output in High-Z Time	CAS Latency=3	tOHZ3	-	4.0	-	4.5	-	5.0	-	5.5	-	5.5	ns	
	CAS Latency=2	tOHZ2	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	ns	

Note :

1. Assume t_R / t_F (input rise and fall time) is 1ns. If t_R & $t_F > 1ns$, then $[(t_R+t_F)/2-1]ns$ should be added to the parameter.
2. Access time to be measured with input signals of 1V/ns edge rate, from 0.8V to 2.0V. If $t_R > 1ns$, then $(t_R/2-0.5)ns$ should be added to the parameter.

AC CHARACTERISTICS II (AC operating conditions unless otherwise noted)

Parameter		Sym- bol	45		5		55		6		7		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
RAS Cycle Time	Operation	tRC	58.5	-	55	-	55	-	60	-	63	-	ns	
RAS Cycle Time	Auto Refresh	tRRC	58.5	-	55	-	55	-	60	-	63	-	ns	
RAS to CAS Delay		tRCD	18	-	15	-	16.5	-	18	-	20	-	ns	
RAS Active Time		tRAS	40.5	100K	38.7	100K	38.7	100K	42	100K	42	100K	ns	
RAS Precharge Time		tRP	18	-	15	-	16.5	-	18	-	20	-	ns	
RAS to RAS Bank Active Delay		tRRD	9	-	10	-	11	-	12	-	14	-	ns	
CAS to CAS Delay		tCCD	1	-	1	-	1	-	1	-	1	-	CLK	
Write Command to Data-In Delay		tWTL	0	-	0	-	0	-	0	-	0	-	CLK	
Data-in to Precharge Command		tDPL	TBD	-	TBD	-	TBD	-	1	-	1	-	CLK	
Data-In to Active Command		tDAL	tDPL + tRP											
DQM to Data-Out Hi-Z		tDQZ	2	-	2	-	2	-	2	-	2	-	CLK	
DQM to Data-In Mask		tDQM	0	-	0	-	0	-	0	-	0	-	CLK	
MRS to New Command		tMRD	2	-	2	-	2	-	2	-	2	-	CLK	
Precharge to Data Output High-Z	CAS Latency=3	tPROZ3	3	-	3	-	3	-	3	-	3	-	CLK	
	CAS Latency=2	tPROZ2	-	-	2	-	2	-	2	-	2	-	CLK	
Power Down Exit Time		tDPE	1	-	1	-	1	-	1	-	1	-	CLK	
Self Refresh Exit Time		tSRE	1	-	1	-	1	-	1	-	1	-	CLK	1
Refresh Time		tREF	-	64	-	64	-	64	-	64	-	64	ms	

Note :

1. A new command can be given tRC after self refresh exit.

COMMAND TRUTH TABLE

Command	CKEn-1	CKEn	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	DQM	ADDR	A10/AP	BA	Note	
Mode Register Set	H	X	L	L	L	L	X	OP code				
No Operation	H	X	H	X	X	X	X	X				
			L	H	H	H						
Bank Active	H	X	L	L	H	H	X	RA		V		
Read	H	X	L	H	L	H	X	CA	L	V		
Read with Autoprecharge									H			
Write	H	X	L	H	L	L	X	CA	L	V		
Write with Autoprecharge									H			
Precharge All Banks	H	X	L	L	H	L	X	X	H	X		
Precharge selected Bank									L	V		
Burst Stop	H	X	L	H	H	L	X	X				
DQM	H	X					V	X				
Auto Refresh	H	H	L	L	L	H	X	X				
Burst-Read-Single-WRITE	H	X	L	L	L	L	X	A9 ball High (Other balls OP code)		MRS Mode		
Self Refresh ¹	Entry	H	L	L	L	L	H	X	X			
	Exit	L	H	H	X	X	X	X				
Precharge power down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X				X				

PACKAGE INFORMATION

JEDEC STANDARD 400mil 86pin TSOP-II with 0.5mm pin pitch

