

4496203 HITACHI/ LOGIC/ARRAYS/MEM

04E 12622 D

HM6264 Series

Maintenance Only
(Substitute HM6264A)

T-46-23-12

B192-word x 8-bit High Speed CMOS Static RAM

■ **FEATURES**

- Fast access Time 100ns/120ns/150ns (max.)
- Low Power Standby Standby: 0.1mW (typ.)
10μW (typ.) L-/LL-version
- Low Power Operation Operating: 200mW/MHz (typ.)
- Single +5V Supply
- Completely Static Memory. . . . No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764
- Capability of Battery Back Up Operation (L-/LL-version)

■ **ORDERING INFORMATION**

Type No.	Access Time	Package
HM6264P-10	100ns	600 mil 28 pin Plastic DIP
HM6264P-12	120ns	
HM6264P-15	150ns	
HM6264LP-10	100ns	600 mil 28 pin Plastic DIP
HM6264LP-12	120ns	
HM6264LP-15	150ns	
HM6264LP-10L	100ns	600 mil 28 pin Plastic DIP
HM6264LP-12L	120ns	
HM6264LP-15L	150ns	
HM6264FP-10	100ns	28 pin Plastic SOP (Note)
HM6264FP-12	120ns	
HM6264FP-15	150ns	
HM6264LFP-10	100ns	28 pin Plastic SOP (Note)
HM6264LFP-12	120ns	
HM6264LFP-15	150ns	
HM6264LFP-10L	100ns	28 pin Plastic SOP (Note)
HM6264LFP-12L	120ns	
HM6264LFP-15L	150ns	

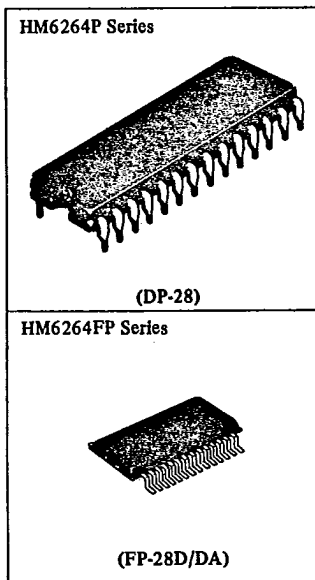
Note) A character T is added to the end of type No. for SOP of 3.00 mm (max.) thickness.

■ **ABSOLUTE MAXIMUM RATINGS**

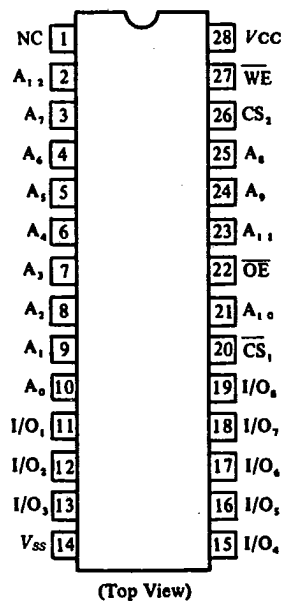
Item	Symbol	Rating	Unit
Terminal Voltage *1	V _T	-0.5*2 to +7.0	V
Power Dissipation	P _T	1.0	W
Operating Temperature	T _{opr}	0 to +70	°C
Storage Temperature	T _{stg}	-55 to +125	°C
Storage Temperature Under Bias	T _{bias}	-10 to +85	°C

Notes) *1. With respect to V_{SS}
*2. -3.0V for pulse width ≤ 50ns

Note) This device is not available for new application.



■ **PIN ARRANGEMENT**



(Top View)



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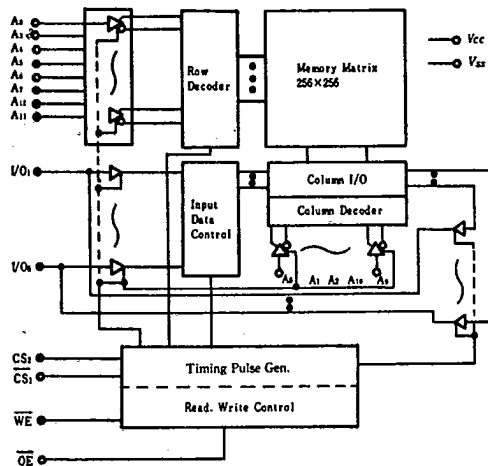
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■ BLOCK DIAGRAM



■ TRUTH TABLE

WE	CS ₁	CS ₂	OE	Mode	I/O Pin	V _{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I _{SB} , I _{SB1}	
X	X	L	X	Output Disabled	High Z	I _{SB} , I _{SB2}	
H	L	H	H	Output Disabled	High Z	I _{CC} , I _{CC1}	
H	L	H	L	Read	Dout	I _{CC} , I _{CC1}	
L	L	H	H	Write	Din	I _{CC} , I _{CC1}	Write Cycle (1)
L	L	H	L		Din	I _{CC} , I _{CC1}	Write Cycle (2)

X : H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input Voltage	V _{IH}	2.2	-	6.0	V
	V _{IL}	-0.3*1	-	0.8	V

Note) *1. -3.0V for pulse width ≤ 50ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current	I _{LI} †	V _{in} =V _{SS} to V _{CC}	-	-	2	μA
Output Leakage Current	I _{LO} †	CS ₁ =V _{IH} or CS ₂ =V _{IL} or OE=V _{IH} or WE=V _{IL} , V _{I/O} =V _{SS} to V _{CC}	-	-	2	μA
Operating Power Supply Current	I _{CC}	CS ₁ =V _{IL} , CS ₂ =V _{IH} , I _{I/O} =0mA	-	40	80	mA
Average Operating Current	I _{CC1}	Min. cycle, duty=100%, I _{I/O} =0mA	-	60	110	mA
	I _{SB}	CS ₁ =V _{IH} or CS ₂ =V _{IL}	-	1	3	mA
Standby Power Supply Current	I _{SB1} *2	CS ₁ ≥ V _{CC} -0.2V, CS ₂ ≥ V _{CC} -0.2V or CS ₂ ≤ 0.2V	-	0.02	2	mA
			-	2*3	100*3	μA
	I _{SB2} *2	CS ₂ ≤ 0.2V	-	0.02	2	mA
			-	2*3	100*3	μA
Output Voltage	V _{OL}	I _{OL} = 2.1mA	-	-	0.4	V
	V _{OH}	I _{OH} = -1.0 mA	2.4	-	-	V

Notes) *1. Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.

*2. V_{IL} min=-0.3V

*3. This characteristics is guaranteed only for L-version.

*4. This characteristics is guaranteed only for LL-version.



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■ CAPACITANCE ($f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0\text{V}$	-	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($V_{CC} = 5\text{V} \pm 10\%$, $T_a = 0$ to $+70^\circ\text{C}$)

● AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10ns

Input and Output Timing Reference Level: 1.5V

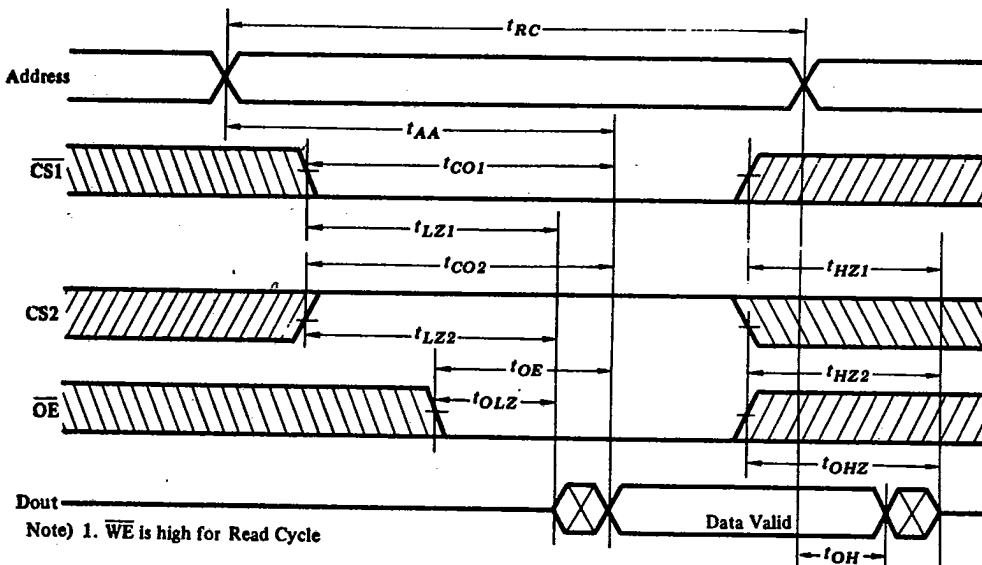
Output Load: 1TTL Gate and C_L (100pF) (Including scope and jig)

● READ CYCLE

Item	Symbol	HM6264-10		HM6264-12		HM6264-15		Unit	
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	100	-	120	-	150	-	ns	
Address Access Time	t_{AA}	-	100	-	120	-	150	ns	
Chip Selection to Output	CS1	t_{CO1}	-	100	-	120	-	150	ns
	CS2	t_{CO2}	-	100	-	120	-	150	ns
Output Enable to Output Valid	t_{OE}	-	50	-	60	-	70	ns	
Chip Selection to Output in Low Z	CS1	t_{LZ1}	10	-	10	-	15	-	ns
	CS2	t_{LZ2}	10	-	10	-	15	-	ns
Output Enable to Output in Low Z	t_{OLZ}	5	-	5	-	5	-	ns	
Chip Deselection to Output in High Z	CS1	t_{HZ1}	0	35	0	40	0	50	ns
	CS2	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns	
Output Hold from Address Change	t_{OH}	10	-	10	-	15	-	ns	

Notes) 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

● READ CYCLE



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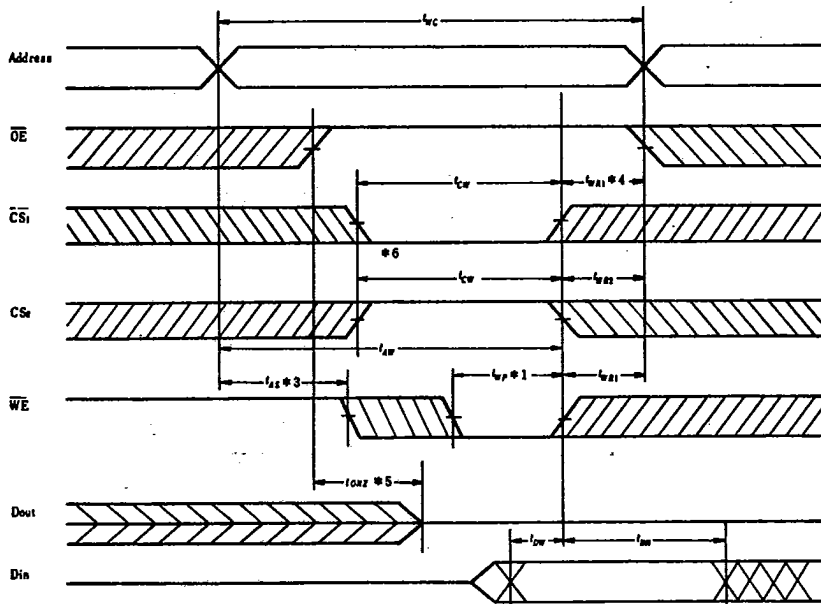
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• WRITE CYCLE

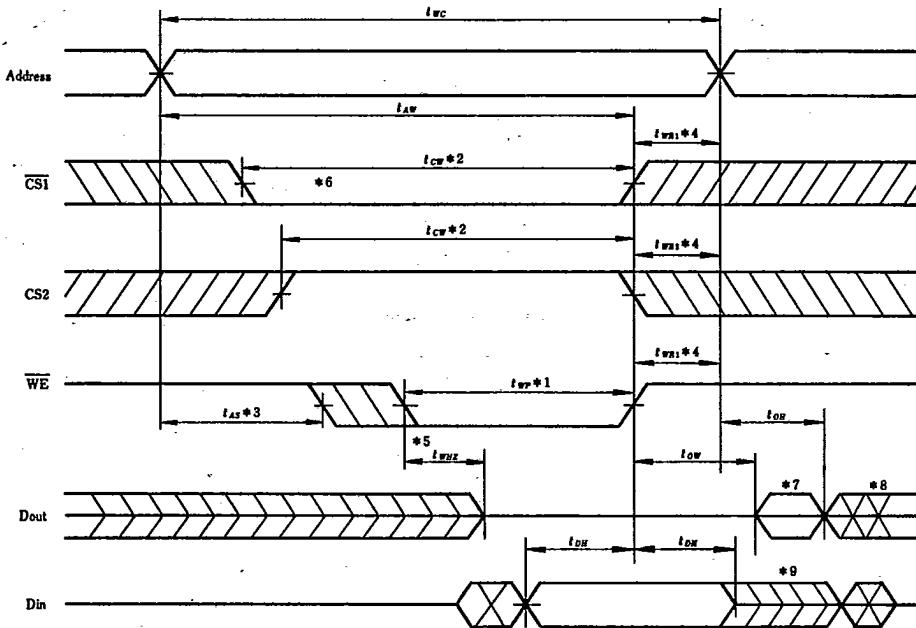
Item	Symbol	HM6264-10		HM6264-12		HM6264-15		Unit	
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	100	-	120	-	150	-	ns	
Chip Selection to End of Write	t_{CW}	80	-	85	-	100	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns	
Address Valid to End of Write	t_{AW}	80	-	85	-	100	-	ns	
Write Pulse Width	t_{WP}	60	-	70	-	90	-	ns	
Write Recovery Time	CS1, WE	t_{WR1}	5	-	5	-	10	-	ns
	CS2	t_{WR2}	15	-	15	-	15	-	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns	
Data to Write Time Overlap	t_{DW}	40	-	50	-	60	-	ns	
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns	
\overline{OE} to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns	
Output Active from End of Write	t_{OW}	5	-	5	-	10	-	ns	

• WRITE CYCLE (1) (\overline{OE} clock)



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• WRITE CYCLE (2) (\overline{OE} Low Fix)



- Notes)
1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low \overline{WE} . A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and \overline{WE} going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and \overline{WE} going high. t_{wp} is measured from the beginning of write to the end of write.
 2. t_{cw} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
 3. t_{as} is measured from the address valid to the beginning of write.
 4. t_{wr} is measured from the end of write to the address change.
 t_{wr1} applies in case a write ends at $\overline{CS1}$ or \overline{WE} going high.
 t_{wr2} applies in case a write ends at CS2 going low.
 5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
 6. If $\overline{CS1}$ goes low simultaneously with \overline{WE} going low or after \overline{WE} going low, the outputs remain in high impedance state.
 7. Dout is the same phase of the latest written data in this write cycle.
 8. Dout is the read data of next address.
 9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.



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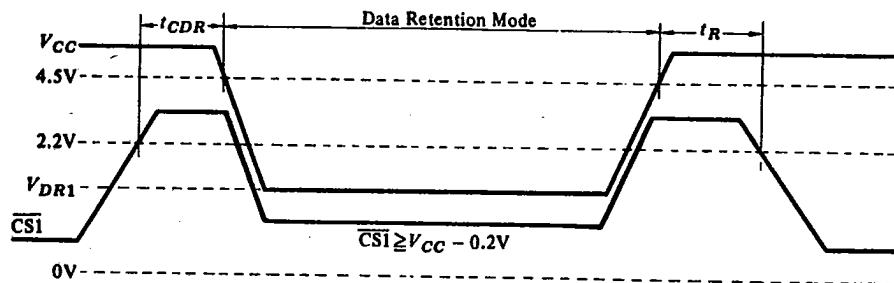
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■ **LOW V_{CC} DATA RETENTION CHARACTERISTICS** ($T_a = 0$ to $+70^\circ\text{C}$)
This characteristics is guaranteed only for L/LL-version.

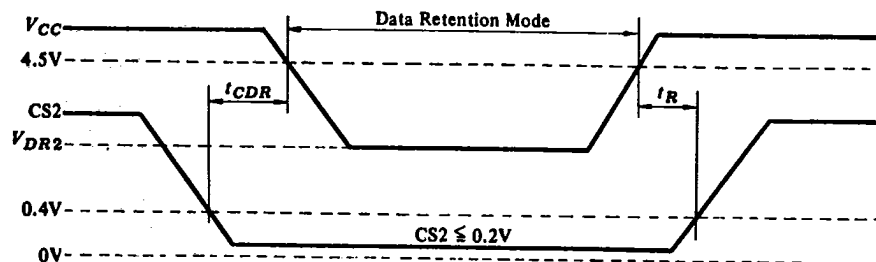
Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$CS1 \geq V_{CC} - 0.2V$, $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$	2.0	-	-	V
	V_{DR2}	$CS2 \leq 0.2V$	2.0	-	-	V
Data Retention Current	I_{CCDR1}	$V_{CC} = 3.0V$, $CS1 \geq V_{CC} - 0.2V$	-	1*1	50*1	μA
		$CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$	-	1*2	25*2	
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	-	1*1	50*1	μA
			-	1*2	25*2	
Operation Recovery Time	t_R		0	-	-	ns
			t_{RC}^{*3}	-	-	ns

Notes) *1. V_{IL} min = $-0.3V$, $20\mu\text{A}$ max at $T_a = 0$ to 40°C . This characteristics is guaranteed only for L-version.
*2. V_{IL} min = $-0.3V$, $10\mu\text{A}$ max at $T_a = 0$ to 40°C . This characteristics is guaranteed only for LL-version.
*3. t_{RC} = Read Cycle Time

● **LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)**



● **LOW V_{CC} DATA RETENTION WAVEFORM (2) ($CS2$ Controlled)**



NOTE: In Data Retention Mode, $CS2$ controls the Address, \overline{WE} , $\overline{CS1}$, \overline{OE} and Din buffer. If $CS2$ controls data retention mode, V_{in} for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, $CS2$ must satisfy either $CS2 > V_{CC} - 0.2V$ or $CS2 \leq 0.2V$. The other input levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.



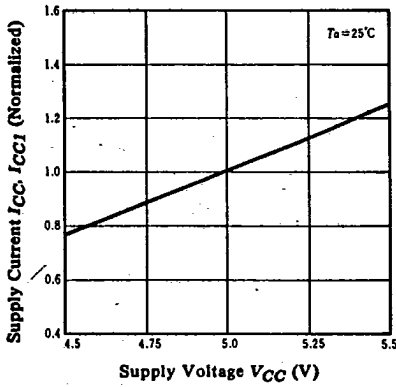
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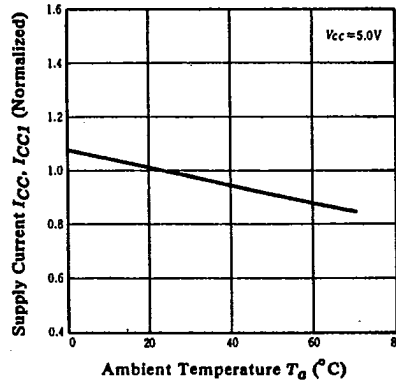
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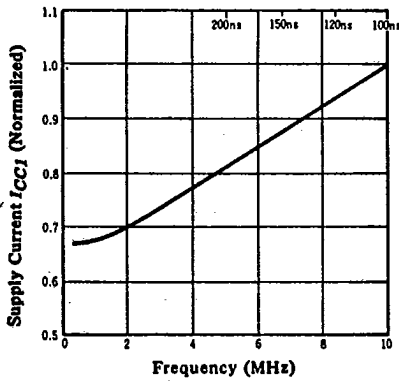
SUPPLY CURRENT vs. SUPPLY VOLTAGE



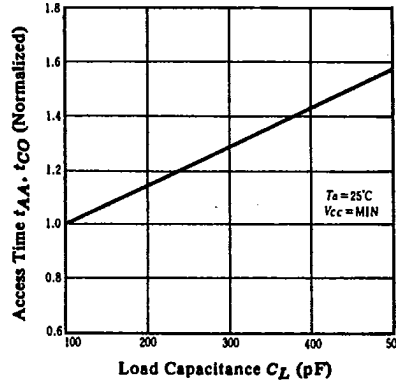
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



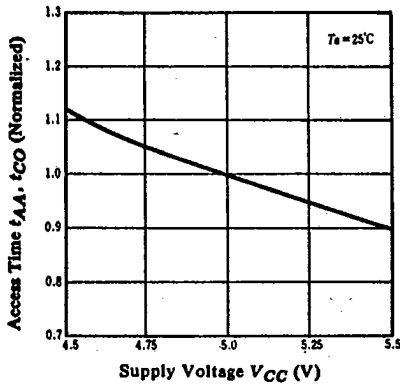
SUPPLY CURRENT vs. FREQUENCY



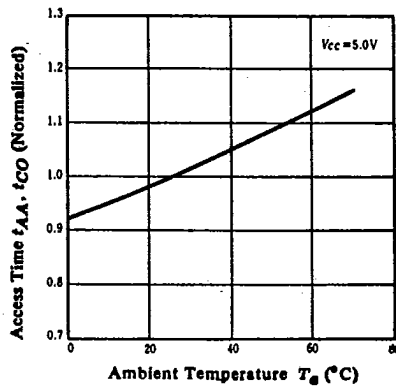
ACCESS TIME vs. LOAD CAPACITANCE



ACCESS TIME vs. SUPPLY VOLTAGE



ACCESS TIME vs. AMBIENT TEMPERATURE

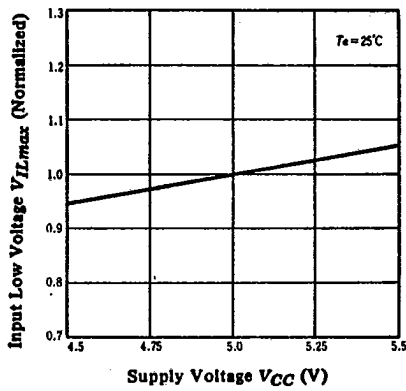


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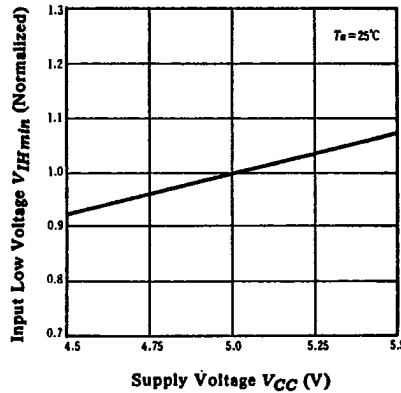
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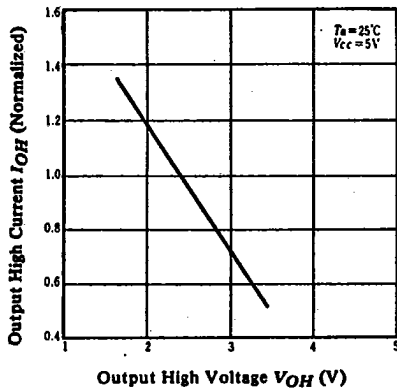
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



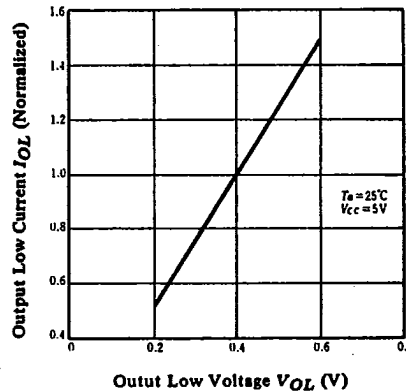
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



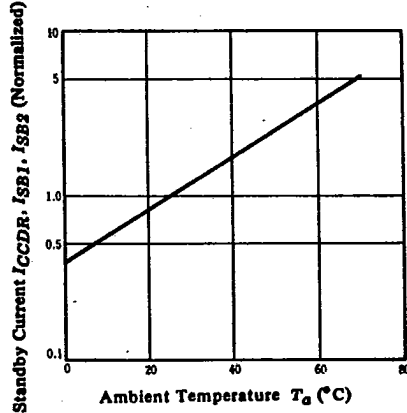
OUTPUT CURRENT vs. OUTPUT VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE



STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE

