Integrated Device Technology, Inc.

HIGH-SPEED 4K x 9 DUAL-PORT STATIC RAM

IDT7014S

FEATURES:

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- High-speed access
  - — Military: 20/25/35ns (max.)
  - — Commercial: 12/15/20/25ns (max.)
- Low-power operation
  - — IDT7014S
    Active: 900mW (typ.)
- Fully asynchronous operation from either port
- TTL-compatible; single 5V (±10%) power supply
- Available in 52-pin PLCC and a 64-pin TQFP
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

The IDT7014 is an extremely high-speed 4K x 9 Dual-Port Static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to high-speed applications which do not need on-chip arbitration to manage simultaneous access.

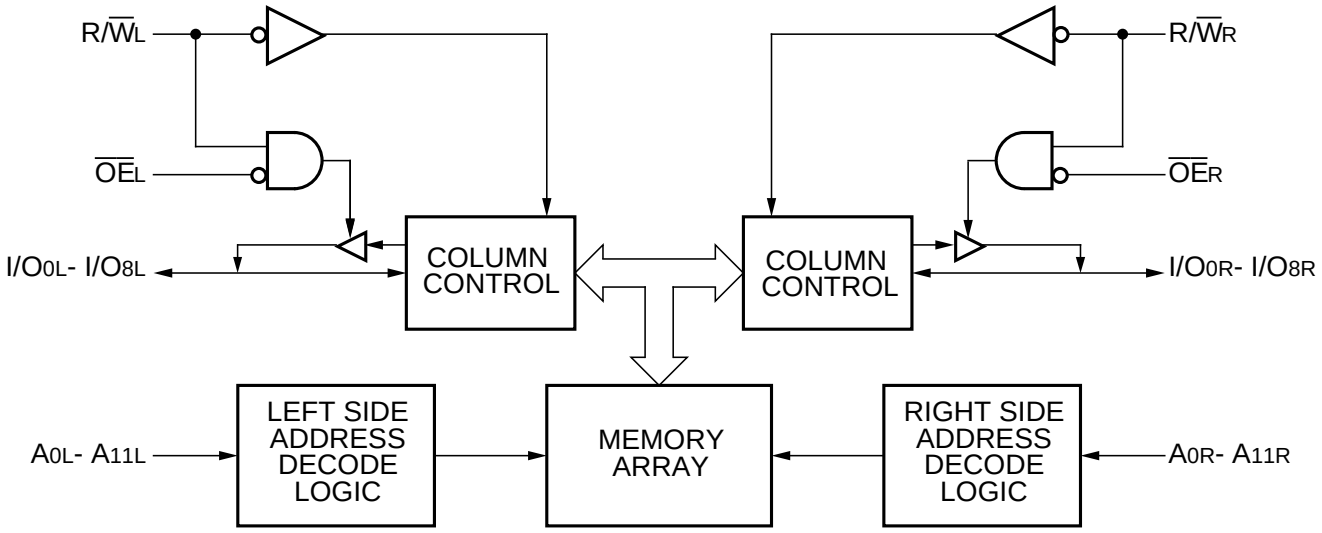
The IDT7014 provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. See functional description.

The IDT7014 utilitizes a 9-bit wide data path to allow for parity at the user's option. This feature is especially useful in data communication applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's high-performance technology, the IDT7014 Dual-Ports typically operate on only 900mW of power at maximum access times as fast as 12ns.

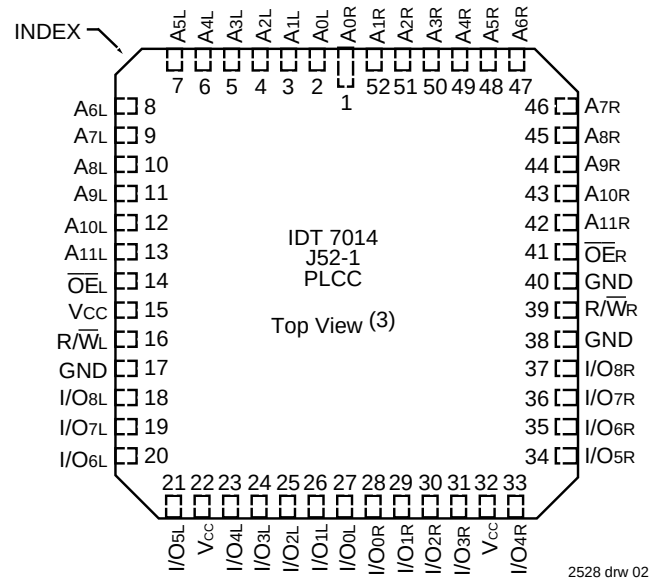
The IDT7014 is packaged in a 52-pin PLCC and a 64-pin thin plastic quad flatpack (TQFP).

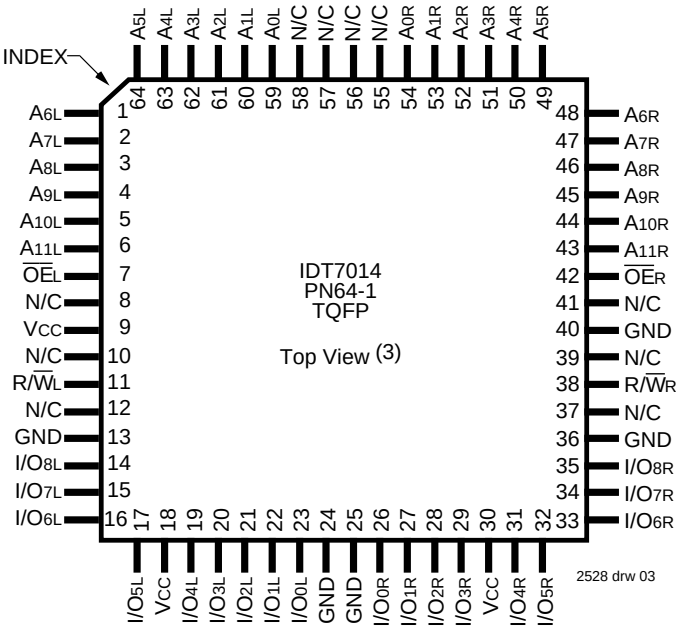
FUNCTIONAL BLOCK DIAGRAM



2528 drw 01

PIN CONFIGURATIONS[1,2]





NOTES:
1. All VCC pins must be connected to power supply.
2. All ground pins must be connected to ground supply.
3. This text does not indicate the orientation of the actual part-marking

ABSOLUTE MAXIMUM RATINGS [1]

Symbol	Rating	Commercial	Military	Unit
VTERM[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
VTERM[3]	Terminal Voltage	–0.5 to Vcc	–0.5 to Vcc	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTES: 2528 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2528 tbl 02

RECOMMENDED DC OPERATING CONDTIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0[2]	V
VIL	Input Low Voltage	–0.5[1]	—	0.8	V

NOTES: 2528 tbl 03
1. VIL ≥ -1.5V for pulse width less than 10ns.
2. VTERM must not exceed Vcc + 0.5V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	IDT7014S Min.	IDT7014S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	—	V

2528 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version	IDT7014S12 Com'l. Only Typ.	IDT7014S12 Com'l. Only Max.	IDT7014S15 Com'l. Only Typ.	IDT7014S15 Com'l. Only Max.	IDT7014S20 Typ.	IDT7014S20 Max.	IDT7014S25 Typ.	IDT7014S25 Max.	IDT7014S35 Mil. Only Typ.	IDT7014S35 Mil. Only Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	Outputs Open f = f_{MAX}(1)	Mil.	—	—	160	260	155	260	150	255	150	250	mA
			Com'l.	160	250	160	250	155	245	150	240	—	—	

NOTE:
1. At f = fmax, address inputs are cycling at the maximum read cycle of 1/t_{RC} using the "AC Test Conditions" input levels of GND to 3V.

2528 tbl 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1, 2, and 3

2528 tbl 06

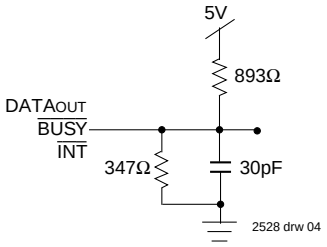


Figure 1. AC Output Test Load.

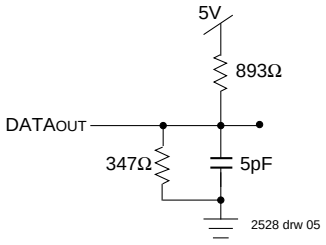


Figure 2. Output Test Load (for t_{HZ}, t_{WZ}, and t_{OW})
Including scope and jig.

CAPACITANCE(1)

(T_A = +25°C, f = 1.0MHz) TQFP Package Only

Symbol	Parameter	Condition(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

2528 tbl 07

NOTES:
1. This parameter is determined by device characteristics but is not tested.
2. 3dv references the interperlated capacitance when the input and output signals swith from 0V to 3V or from 3V to 0V.

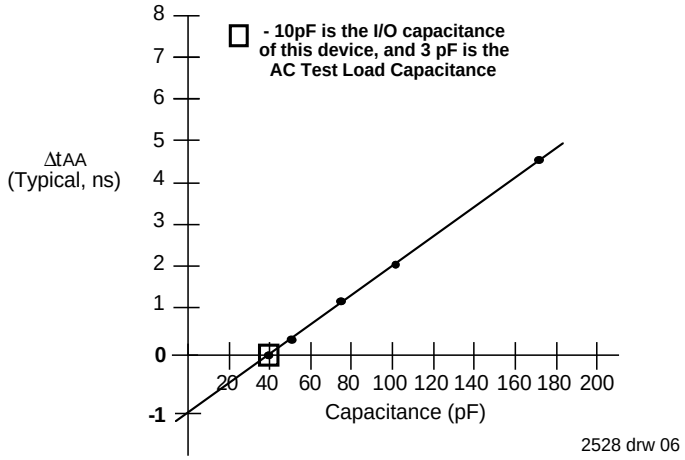


Figure 3. Typical Output Derating (Lumped Capacitive Load).

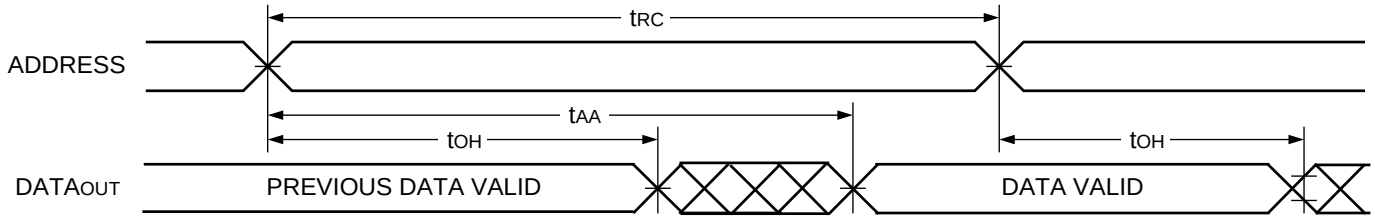
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	7014S12 Com'l. Only		7014S15 Com'l. Only		7014S20		7014S25		7014S35 Mil. Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	12	—	15	—	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	—	25	—	35	ns
t_{AOE}	Output Enable Access Time	—	8	—	8	—	10	—	12	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1, 2]	3	—	3	—	3	—	3	—	3	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	7	—	7	—	9	—	11	—	15	ns

NOTES:
2528 tbl 08

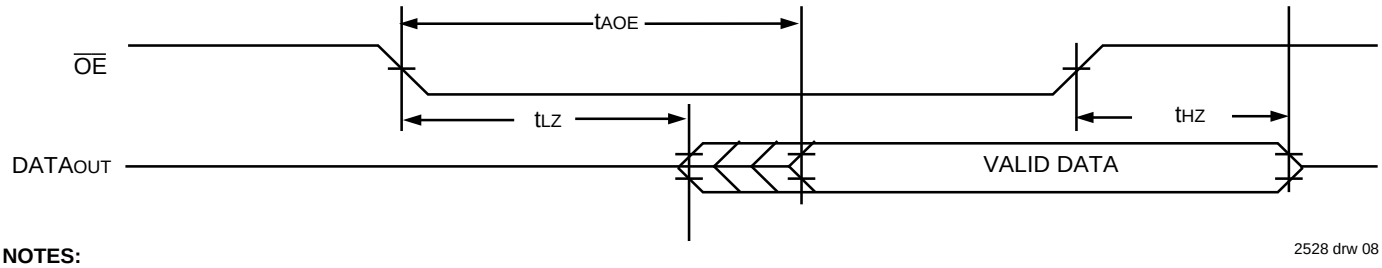
1. Transition is measured ±200mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is determined by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1,2]



2528 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]



2528 drw 08

NOTES:

1. R/$\overline{W}$ = V_{IH} for Read Cycles.
2. $\overline{OE}$ = V_{IL}.
3. Addresses valid prior to $\overline{OE}$ transition LOW.

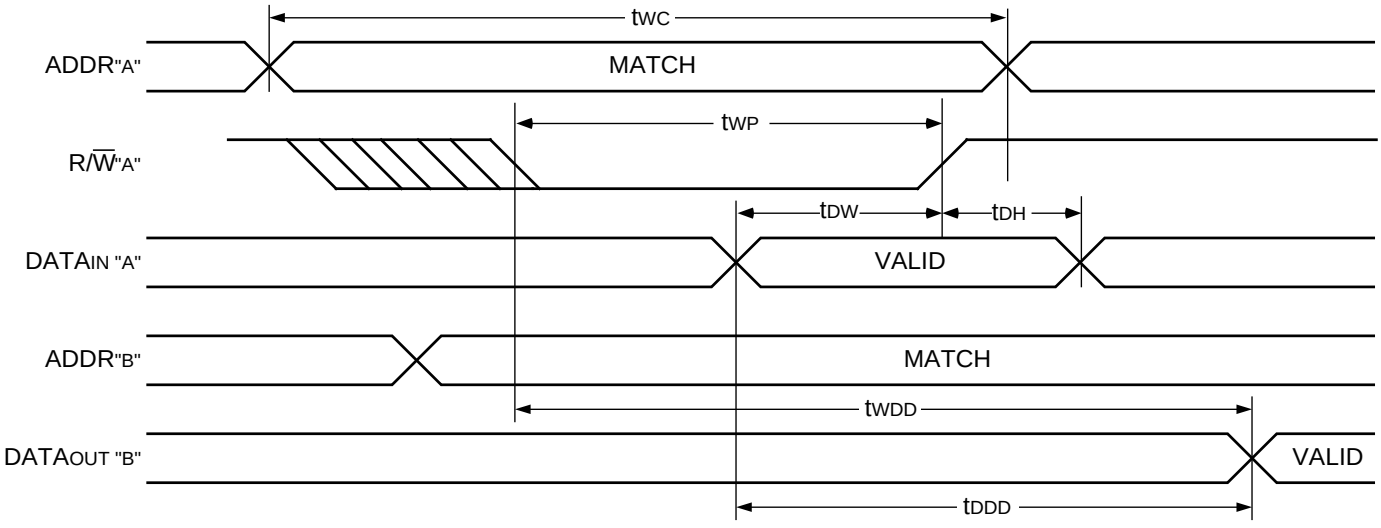
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	7014S12 Com'l. Only		7014S15 Com'l. Only		7014S20		7014S25		7014S35 Mil. Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE												
t_{WC}	Write Cycle Time	12	—	15	—	20	—	25	—	35	—	ns
t_{AW}	Address Valid to End-of-Write	10	—	14	—	15	—	20	—	30	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	10	—	12	—	15	—	20	—	30	—	ns
t_{WR}	Write Recovery Time	1	—	1	—	2	—	2	—	2	—	ns
t_{DW}	Data Valid to End-of-Write	8	—	10	—	12	—	15	—	25	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	7	—	7	—	9	—	11	—	15	ns
t_{DH}	Data Hold Time[3]	0	—	0	—	0	—	0	—	0	—	ns
t_{WZ}	Write Enabled to Output in High-Z[1, 2]	—	7	—	7	—	9	—	11	—	15	ns
t_{OW}	Output Active from End-of-Write[1, 2, 3]	0	—	0	—	0	—	0	—	0	—	ns
t_{WDD}	Write Pulse to Data Delay[4]	—	25	—	30	—	40	—	45	—	55	ns
t_{DDD}	Write Data Valid to Read Data Delay[4]	—	22	—	25	—	30	—	35	—	45	ns

NOTES: 2528 tbl 09

1. Transition is measured ±200mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
4. Port-to-port delay through RAM cells from writing port to reading port, refer to “Timing Waveform of Write With Port-to-Port Read”.

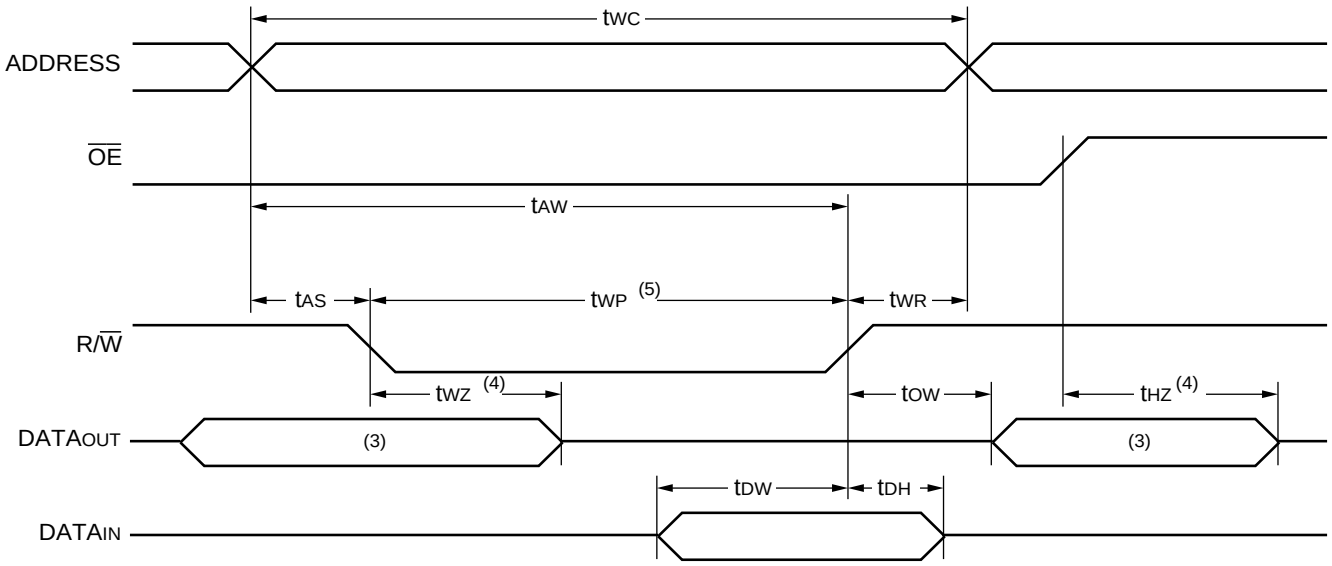
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ [1,2]



NOTES:

1. $R/\overline{W}_{"B"} = V_{IH}$, Read cycle pass through. 2528 drw 09
2. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is opposite from port "A".

TIMING WAVEFORM OF WRITE CYCLE(1, 2, 3, 4, 5)



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NOTES:
1. R/W must be HIGH during all address transitions.
2. tWR is measured from R/W going HIGH to the end of write cycle.
3. During this period, the I/O pins are in the output state, and input signals must not be applied.
4. Transition is measured ±200mV from the Low or High-impedance voltage with the Output Test Load (Figure 2).
5. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If OE is HIGH during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

FUNCTIONAL DESCRIPTION

The IDT7014 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. It lacks the chip enable feature of most Dual-Ports, thus it operates in active mode as soon as power is applied. Each port has its own Output Enable control (OE). In the read mode, the port's OE turns on the output drivers when set LOW. The user application should avoid simultaneous write operations to the same memory location. There is no on-chip arbitration circuitry to resolve write priority and partial data from both ports may be written. READ/WRITE conditions are illustrated in Table 1.

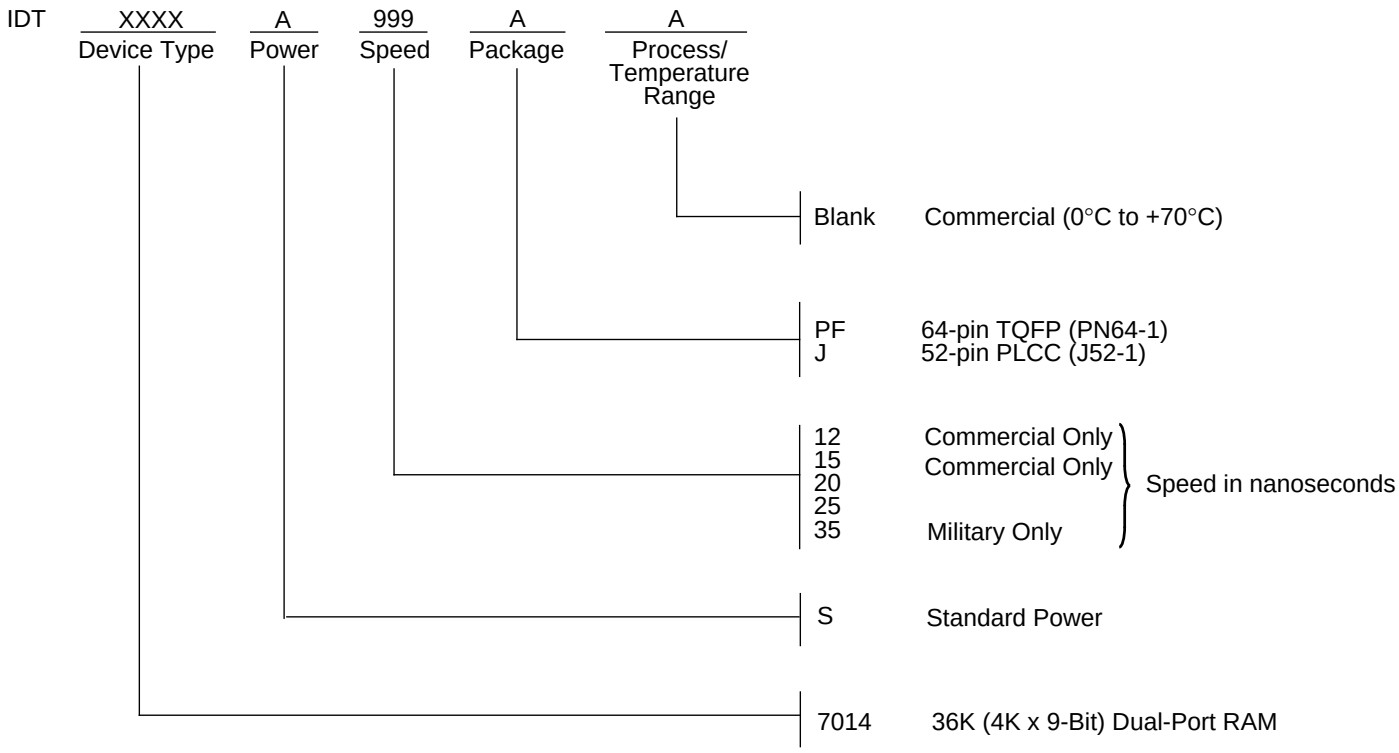
TABLE I – READ/WRITE CONTROL

Left or Right Port(1)			
R/W	OE	D0-8	Function
L	X	DATAIN	Data written into memory
H	L	DATAOUT	Data in memory output on port
X	H	Z	High-impedance outputs

2528 tbl 10

NOTE:
1. AOL - A11L is not equal to AOR - A11R.
'H' = HIGH,'L' = LOW, 'X' = Don't Care, and 'Z' = High-impedance.

ORDERING INFORMATION



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