SIEMENS

Microcomputer Components

8-Bit CMOS Microcontroller

C540U / C541U

Data Sheet 10.97

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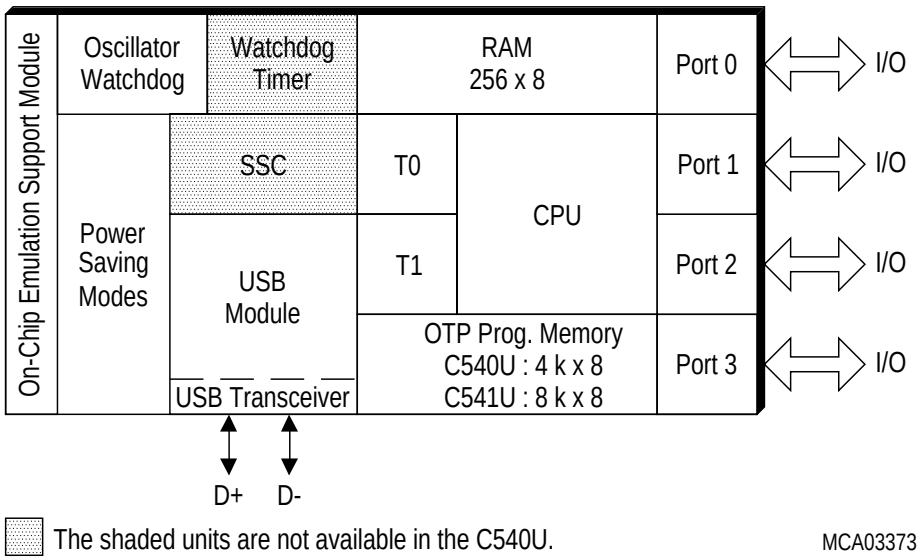
SIEMENS

8-Bit CMOS Microcontroller

C540U
C541U

Advance Information

- Enhanced 8-bit C500 CPU
  - Full software/toolset compatible to standard 80C51/80C52 microcontrollers
- 12 MHz external operating frequency
  - 500 ns instruction cycle
- Built-in PLL for USB synchronization
- On-chip OTP program memory
  - C540U : 4K byte
  - C541U : 8K byte
  - Alternatively up to 64K byte external program memory
  - Optional memory protection
- On-chip USB module
  - Compliant to USB specification
  - Full speed or low speed operation
  - Five endpoints : one bidirectional control endpoint
    four versatile programmable endpoints
  - Registers are located in special function register area
  - On-chip USB transceiver



Features (cont'd) :

- Up to 64K byte external data memory
- 256 byte on-chip RAM
- Four parallel I/O ports
  - P-LCC-44 package : three 8-bit ports and one 6-bit port
  - P-SDIP-52 package : four 8-bit ports
  - LED current drive capability for 3 pins (10 mA)
- Two 16-bit timer/counters (C501 compatible)
- SSC synchronous serial interface (SPI compatible) (only C541U)
  - Master and slave capable
  - Programmable clock polarity / clock-edge to data phase relation
  - LSB/MSB first selectable
  - 1.5 MBaud transfer rate at 12 MHz operating frequency
- 7 interrupt sources (2 external, 5 internal with 2 USB interrupts) selectable at 2 priority levels
- Enhanced fail safe mechanisms
  - Programmable watchdog timer (only C541U)
  - Oscillator watchdog
- Power saving modes
  - idle mode
  - software power down mode with wake-up capability through $\overline{\text{INT0}}$ pin or USB
- On-chip emulation support logic (Enhanced Hooks Technology ™)
- P-LCC-44 and P-SDIP-52 packages
- Power supply voltage range : 4.0V to 5.5V
- Temperature Range : SAB-C540U T_A = 0 to 70 °C
  SAB-C541U T_A = 0 to 70 °C

Table 1
Ordering Information

Type	Ordering Code	Package	Description (8-Bit CMOS microcontroller)
SAB-C540U-EN	Q67126-C2042	P-LCC-44-2	8-Bit CMOS microcontroller (12 MHz)
SAB-C540U-EP	Q67120-C2043	P-SDIP-52-1	8-Bit CMOS microcontroller (12 MHz)
SAB-C541U-1EN	Q67126-C2001	P-LCC-44-2	8-Bit CMOS microcontroller (12 MHz)
SAB-C541U-1EP	Q67120-C2021	P-SDIP-52-1	8-Bit CMOS microcontroller (12 MHz)

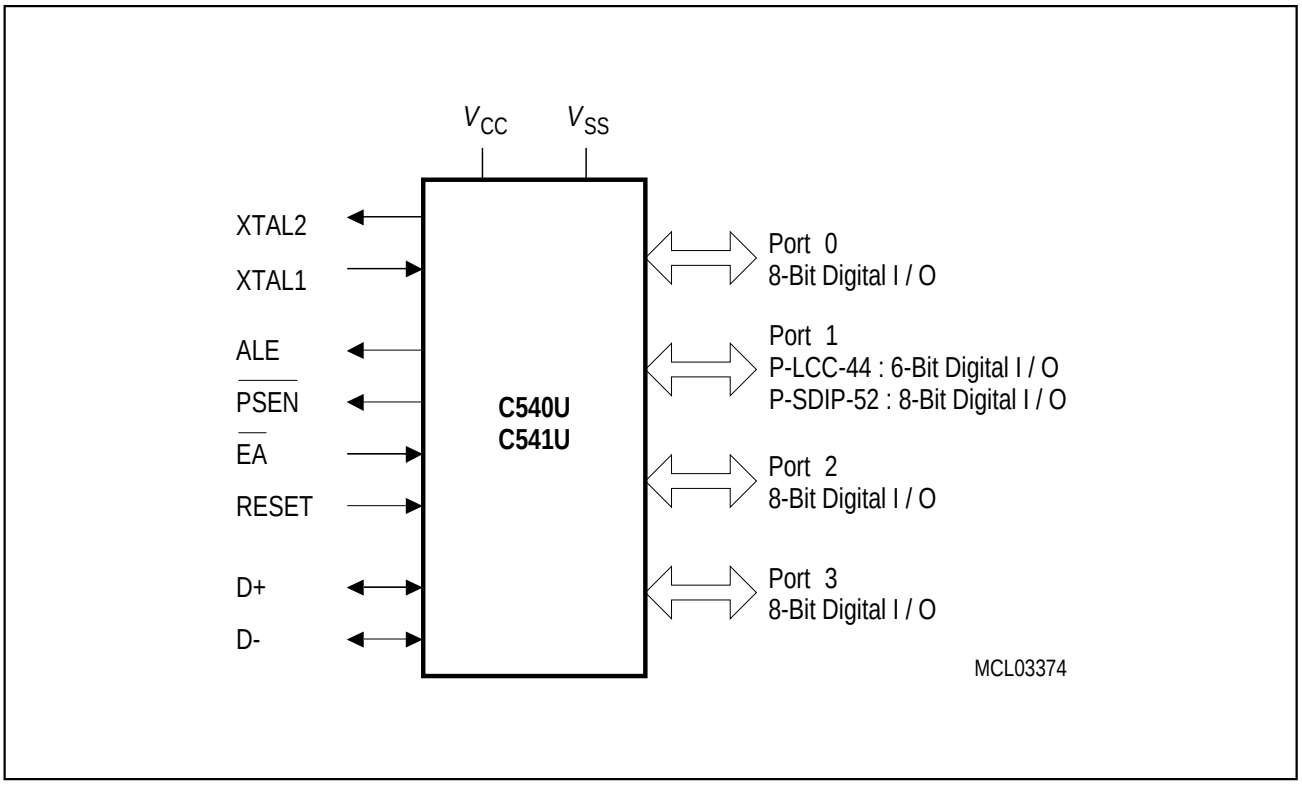


Figure 2
Logic Symbol

Additional Literature

For further information about the C540U/C541U the following literature is available :

Title	Ordering Number
C540U/C541U 8-Bit CMOS Microcontroller User's Manual	B158-H????-X-X-7600
C500 Microcontroller Family Architecture and Instruction Set User's Manual	B158-H6987-X-X-7600
C500 Microcontroller Family - Pocket Guide	B158-H6986-X-X-7600

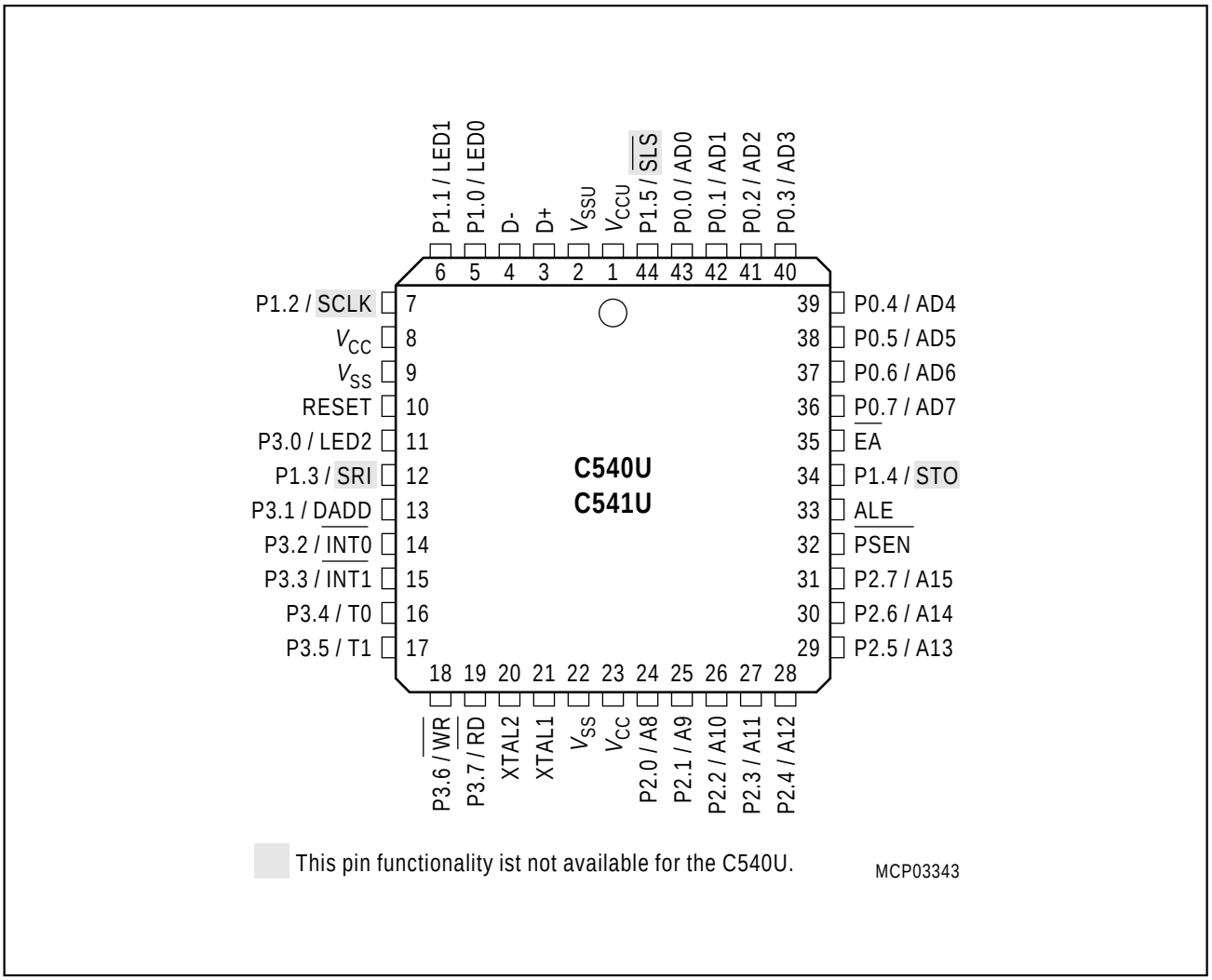


Figure 3
Pin Configuration P-LCC-44 Package (top view)

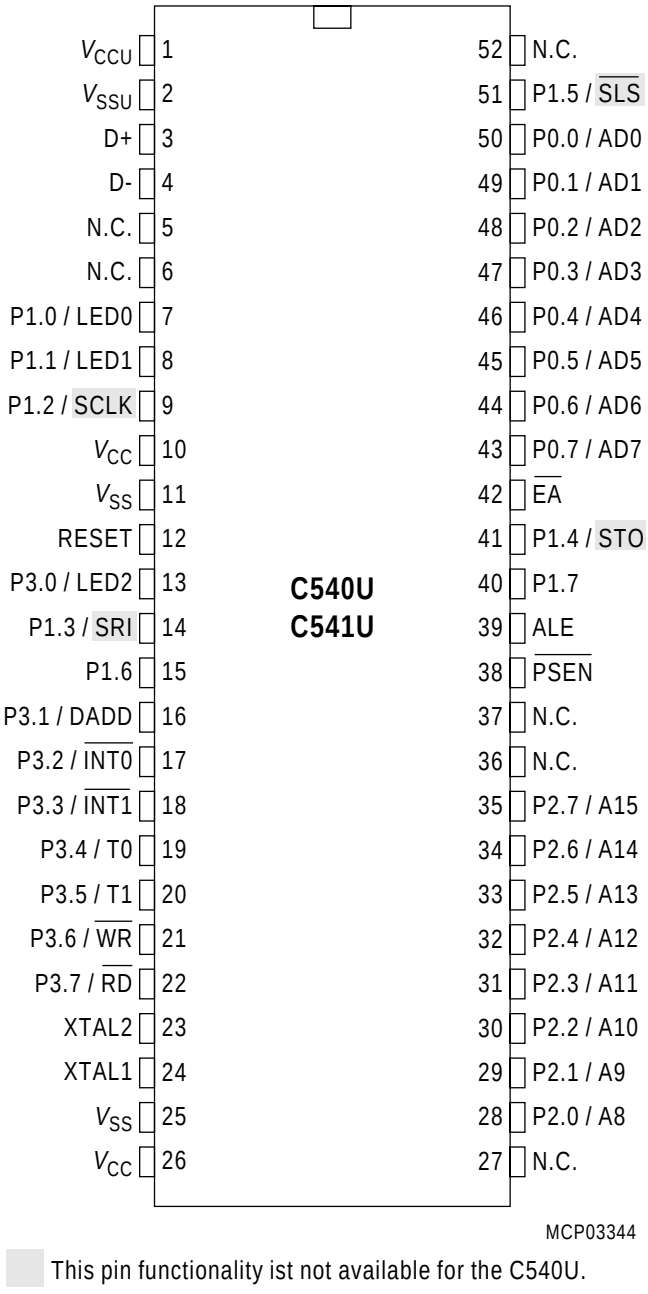


Figure 4
Pin Configuration P-SDIP-52 Package (top view)

Table 2
Pin Definitions and Functions

Symbol	Pin Numbers		I/O*)	Function
	P-LCC-44	P-SDIP-52		
D+	3	3	I/O	**USB D+ Data Line** The pin D+ can be directly connected to USB cable (transceiver is integrated on-chip).
D-	4	4	I/O	**USB D- Data Line** The pin D- can be directly connected to USB cable (transceiver is integrated on-chip).
P1.0 - P1.4	5 - 7, 12, 34, 44	7 - 9, 14, 41, 51, 15, 40	I/O	**Port 1** is an 6-bit (P-LCC-44) or 8-bit (P-SDIP-52) quasi-bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 1 also contains two outputs with LED drive capability as well as the four pins of the SSC (C541U only). The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows : P1.0 / LED0 LED0 output P1.1 / LED1 LED1 output P1.2 / SCLK SSC Master Clock Output / SSC Slave Clock Input (C541U only) P1.3 / SRI SSC Receive Input (C541U only) P1.4 / STO SSC Transmit Output (C541U only) P1.5 / $\overline{SLS}$ SSC Slave Select Inp. (C541U only) P1.6 (P-SDIP-52 only) P1.7 (P-SDIP-52 only)
	5 6 7 12 34 44 – –	7 8 9 13 41 51 15 40		
RESET	10	12	I	**RESET** A high level on this pin for the duration of two machine cycles while the oscillator is running resets the C540U/C541U. A small internal pulldown resistor permits power-on reset using only a capacitor connected to V_{CC}.

*) I = Input
O = Output

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Numbers		I/O*)	Function
	P-LCC-44	P-SDIP-52		
P3.0 - P3.7	11, 13 - 19	13, 16 - 22	I/O	**Port 3** is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows: P3.0 / LED2 LED2 output P3.1 / DADD Device attached input P3.2 / $\overline{INT0}$ External interrupt 0 input / timer 0 gate control input P3.3 / $\overline{INT1}$ External interrupt 1 input / timer 1 gate control input P3.4 / T0 Timer 0 counter input P3.5 / T1 Timer 1 counter input P3.6 / $\overline{WR}$ $\overline{WR}$ control output; latches the data byte from port 0 into the external data memory P3.7 / $\overline{RD}$ $\overline{RD}$ control output; enables the external data memory
XTAL2	20	23	–	**XTAL2** is the output of the inverting oscillator amplifier. This pin is used for the oscillator operation with crystal or ceramic resonator.
XTAL1	21	24	–	**XTAL1** is the input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.

*) I = Input
O = Output

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Numbers		I/O*)	Function
	P-LCC-44	P-SDIP-52		
P2.0 - P2.7	24 - 31	28 - 35	I/O	**Port 2** is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup resistors when issuing 1's. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	32	38	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. The signal remains high during internal program execution.
ALE	33	39	O	The **Address Latch enable** output is used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{\text{EA}}$	35	42	I	**External Access Enable** When held high, the C540U/C541U executes instructions from the internal ROM as long as the PC is less than 1000_H for the C540U or less than 2000_H for the C541U. When held low, the C540U/C541U fetches all instructions from external program memory. For the C540U-L/C541U-L this pin must be tied low.

*) I = Input
O = Output

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Numbers		I/O*)	Function
	P-LCC-44	P-SDIP-52		
P0.0 - P0.7	44 - 36	50 - 43	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1's.
V_{CCU}	1	1	–	**Supply voltage** for the on-chip USB transceiver circuitry.
V_{SSU}	2	2	–	**Ground** (0V) for the on-chip USB transceiver circuitry.
V_{CC}	8, 23	10, 26	–	**Supply voltage** for ports and internal logic circuitry during normal, idle, and power down mode.
V_{SS}	9, 22	11, 25	–	**Ground** (0V) for ports and internal logic circuitry during normal, idle, and power down mode.

*) I = Input
O = Output

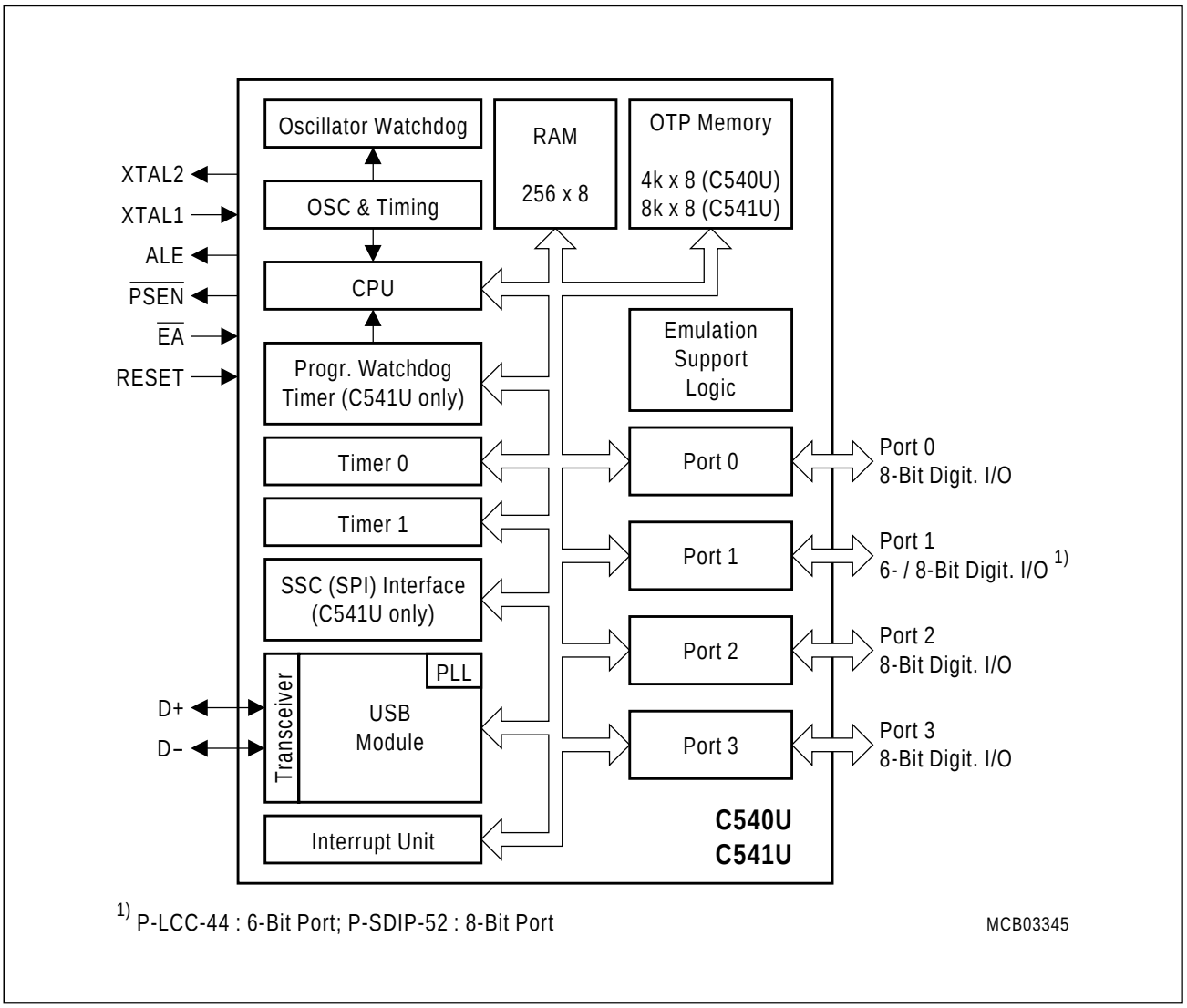


Figure 5
Block Diagram of the C540U/C541U

CPU

The C540U/C541U is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15% three- byte instructions. With a 12 MHz crystal, 58% of the instructions are executed in 500ns.

Special Function Register PSW (Address $D0_H$) **Reset Value : 00_H**

Bit No.	MSB							LSB	
	$D7_H$	$D6_H$	$D5_H$	$D4_H$	$D3_H$	$D2_H$	$D1_H$	$D0_H$	
$D0_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit	Function
CY	**Carry Flag** Used by arithmetic instruction.
AC	**Auxiliary Carry Flag** Used by instructions which execute BCD operations.
F0	**General Purpose Flag**
RS1 RS0	**Register Bank Select Control Bits** These bits are used to select one of the four register banks.

RS1	RS0	Function
0	0	Bank 0 selected, data address 00_H-07_H
0	1	Bank 1 selected, data address 08_H-$0F_H$
1	0	Bank 2 selected, data address 10_H-17_H
1	1	Bank 3 selected, data address 18_H-$1F_H$

OV	**Overflow Flag** Used by arithmetic instruction.
F1	**General Purpose Flag**
P	**Parity Flag** Set/cleared by hardware after each instruction to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.

Memory Organization

The C540U/C541U CPU manipulates operands in the following four address spaces:

- 8 or 4 KByte on-chip OTP program memory
- Totally up to 64 Kbyte internal/external program memory
- up to 64 Kbyte of external data memory
- 256 bytes of internal data memory
- a 128 byte special function register area

Figure 6 illustrates the memory address spaces of the C540U/C541U.

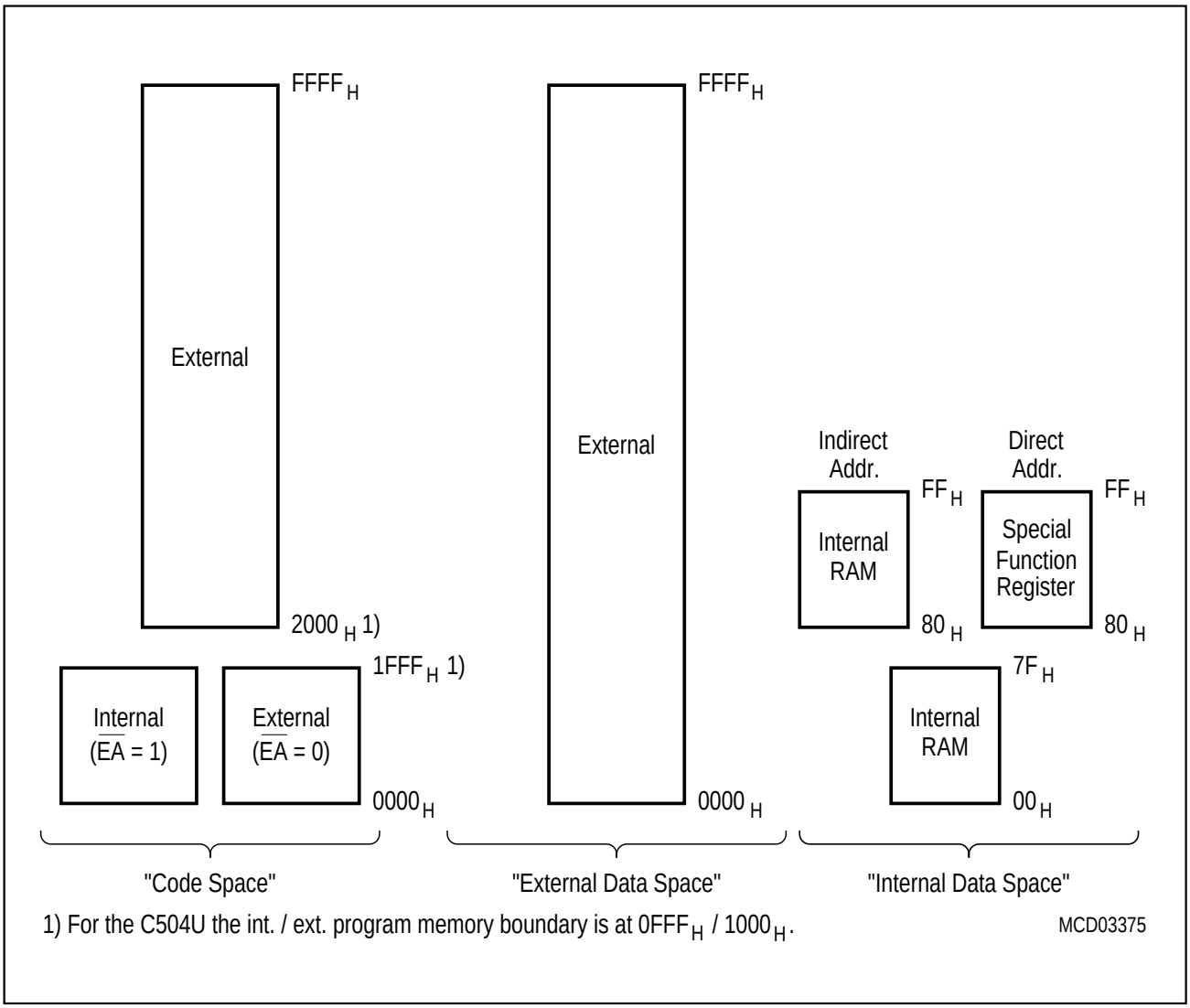


Figure 6
C540U/C541U Memory Map Memory Map

Reset and System Clock

The reset input is an active high input at pin RESET. Since the reset is synchronized internally, the RESET pin must be held high for at least two machine cycles (12 oscillator periods) while the oscillator is running. A pulldown resistor is internally connected to V_{SS} to allow a power-up reset with an external capacitor only. An automatic reset can be obtained when V_{CC} is applied by connecting the RESET pin to V_{CC} via a capacitor. **Figure 7** shows the possible reset circuitries.

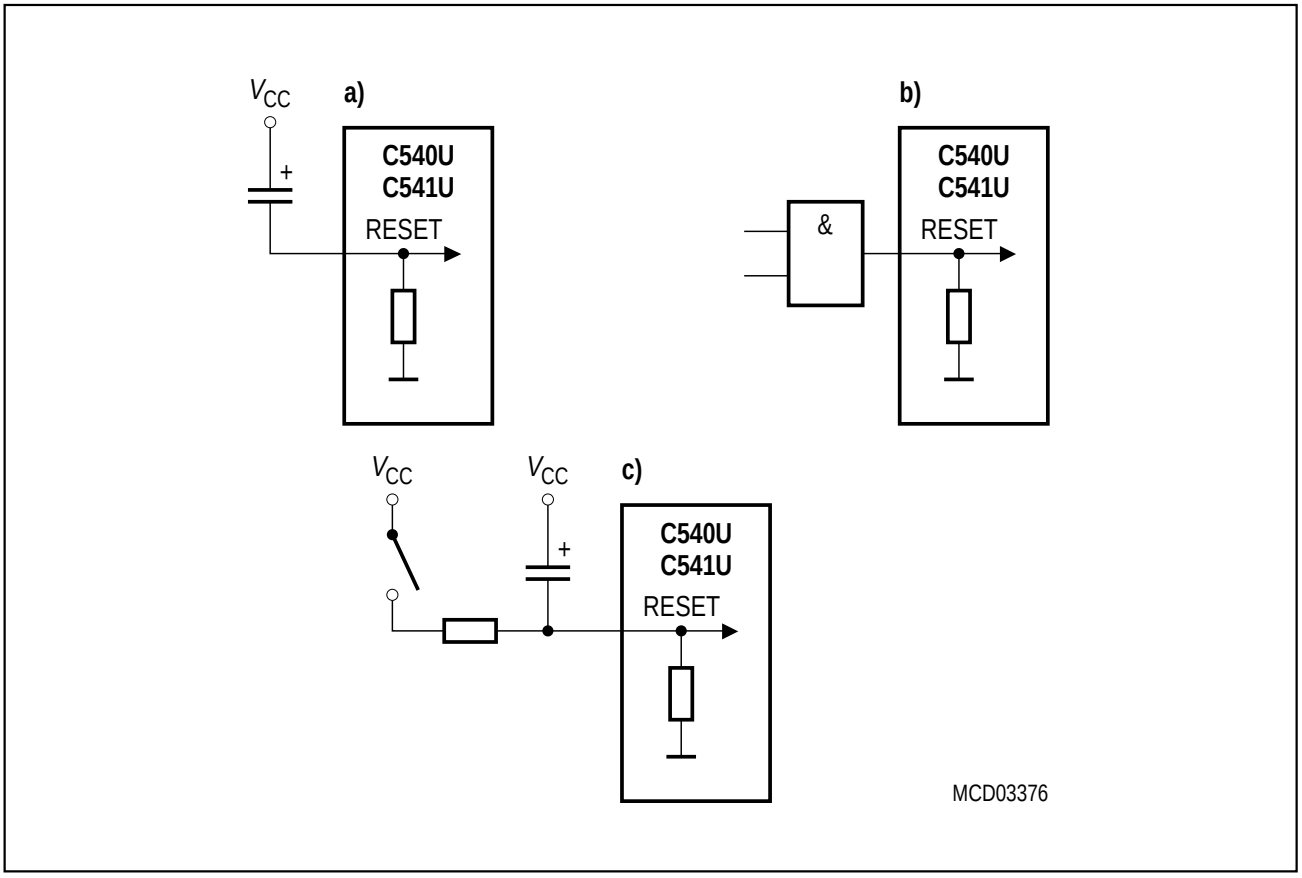


Figure 7
Reset Circuitries

The oscillator and clock generation circuitry of the C540U/C541U is shown in **figure 5-8**. The crystal oscillator generates the system clock for the microcontroller. The USB module can be provided with the following clocks :

– Full speed operation : 48 MHz with a data rate of 12 Mbit/s
– Low speed operation : 6 MHz with a data rate of 1.5 Mbit/s

The low speed clock is generated by a dividing the system clock by 2. The full speed clock is generated by a PLL, which multiplies the system clock by a fix factor of 4. This PLL can be enabled or disabled by bit PCLK of SFR DCR. Depending on full or low speed operation of the USB bit SPEED of SFR has to be set or cleared for the selection of the USB clock. Bit UCLK is a general enable bit for the USB clock.

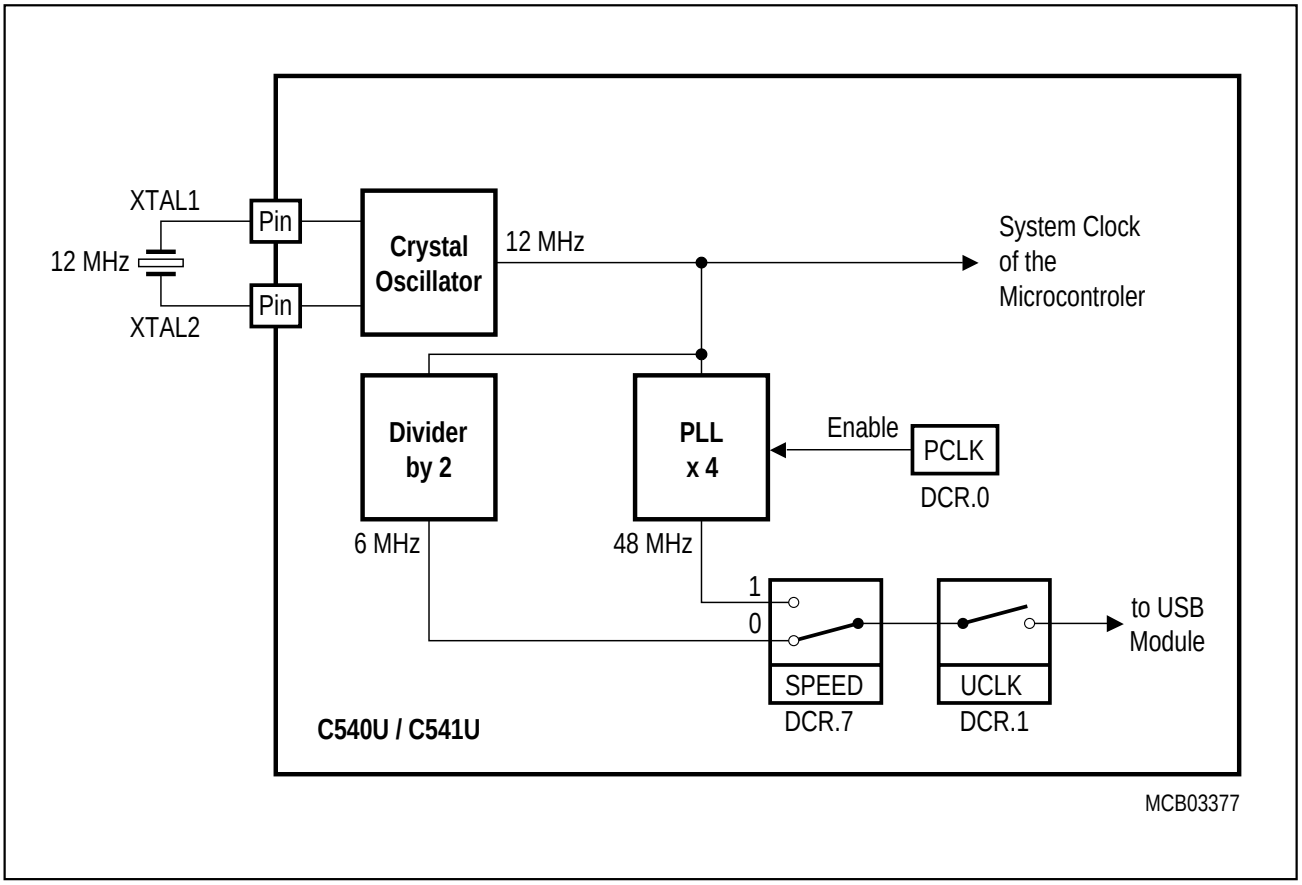


Figure 8
Block Diagram of the Clock Generation Circuitry

The clock generator provides the internal clock signals to the chip. These signals define the internal phases, states and machine cycles. **Figure 9** shows the recommended oscillator circuits for crystal and external clock operation.

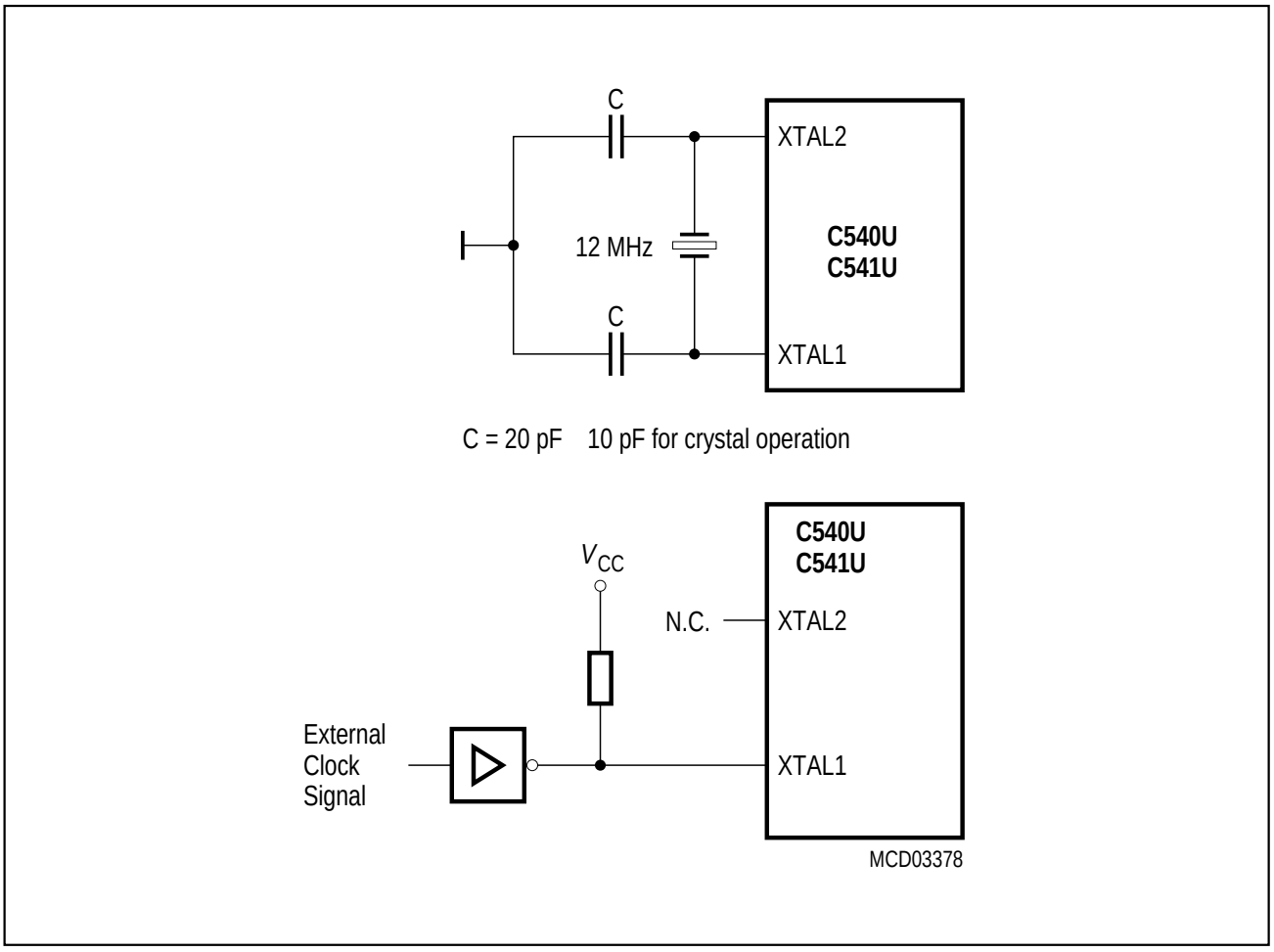


Figure 9
Recommended Oscillator Circuitries

Enhanced Hooks Emulation Concept

The Enhanced Hooks Emulation Concept of the C500 microcontroller family is a new, innovative way to control the execution of C500 MCUs and to gain extensive information on the internal operation of the controllers. Emulation of on-chip ROM based programs is possible, too.

Each production chip has built-in logic for the supprt of the Enhanced Hooks Emulation Concept. Therefore, no costly bond-out chips are necessary for emulation. This also ensure that emulation and production chips are identical.

The Enhanced Hooks Technology™ [1], which requires embedded logic in the C500 allows the C500 together with an EH-IC to function similar to a bond-out chip. This simplifies the design and reduces costs of an ICE-system. ICE-systems using an EH-IC and a compatible C500 are able to emulate all operating modes of the different versions of the C500 microcontrollers. This includes emulation of ROM, ROM with code rollover and ROMless modes of operation. It is also able to operate in single step mode and to read the SFRs after a break.

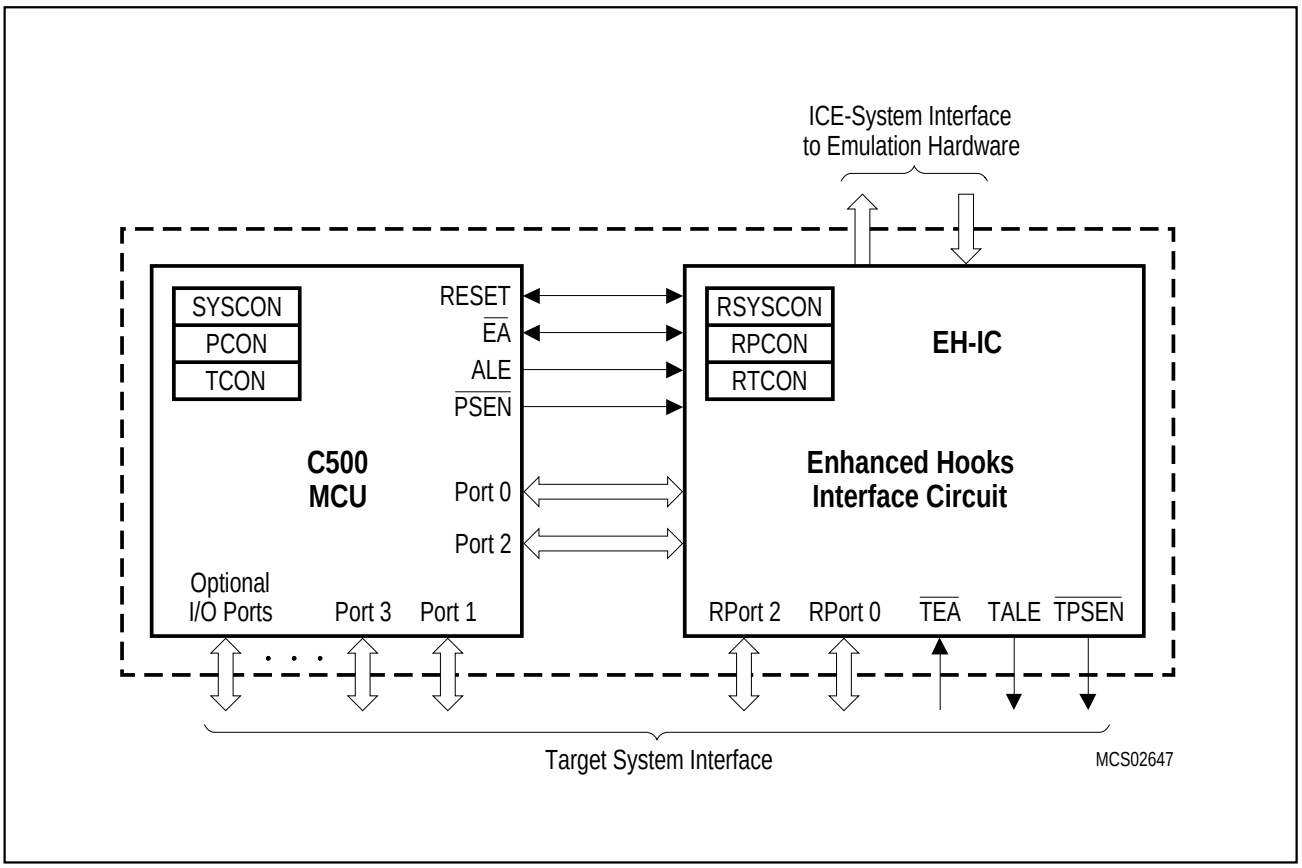


Figure 10
Basic C500 MCU Enhanced Hooks Concept Configuration

Port 0, port 2 and some of the control lines of the C500 based MCU are used by Enhanced Hooks Emulation Concept to control the operation of the device during emulation and to transfer informations about the programm execution and data transfer between the external emulation hardware (ICE-system) and the C500 MCU.

1 “Enhanced Hooks Technology“ is a trademark and patent of Metalink Corporation licensed to Siemens.

Special Function Registers

The registers, except the program counter and the four general purpose register banks, reside in the special function register area. The special function register area consists of two portions: the standard special function register area and the mapped special function register area. One special function register of the C540U/C541U (PCON1) is located in the mapped special function register area. All other SFRs are located in the standard special function register area.

For accessing PCON1 in the mapped special function register area, bit RMAP in special function register SYSCON must be set.

Special Function Register SYSCON (Address $B1_H$) **Reset Value : $XX10XXXX_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$B1_H$	–	–	EALE	RMAP	–	–	–	–	SYSCON

The functions of the shaded bits are not described in this section.

Bit	Function
RMAP	**Special function register map bit** RMAP = 0 : The access to the non-mapped (standard) special function register area is enabled. RMAP = 1 : The access to the mapped special function register area (PCON1) is enabled.

As long as bit RMAP is set, a mapped special function register can be accessed. This bit is not cleared by hardware automatically. Thus, when non-mapped/mapped registers are to be accessed, the bit RMAP must be cleared/set by software, respectively each.

The registers, except the program counter and the four general purpose register banks, reside in the special function register area. All SFRs with addresses where address bits 0-2 are 0 (e.g. 80_H, 88_H, 90_H, 98_H, ..., $F8_H$, FF_H) are bitaddressable.

The 75 special function registers (SFRs) in the SFR area include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. The SFRs of the C540U/C541U are listed in **table 3** to **table 4**. In **table 3** they are organized in groups which refer to the functional blocks of the C540U/C541U. **Table 4 and table 4** illustrate the contents of the SFRs in numeric order of their addresses.

Table 3
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$** 1)	00_H
	B	B Register	**$F0_H$** 1)	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	PSW	Program Status Word Register	**$D0_H$** 1)	00_H
	SP	Stack Pointer	81_H	07_H
	VR0	Version Register 0	FC_H	$C5_H$
	VR1	Version Register 1	FD_H	$C1_H$
	VR2	Version Register 2	FE_H	YY_H 3)
	SYSCON	System Control Register	$B1_H$	$XX10XXXX_B$ 2)
Interrupt System	IEN0	Interrupt Enable Register 0	**$A8_H$** 1)	$0XXX0000_B$ 2)
	IEN1	Interrupt Enable Register 1	$A9_H$	$XXXXX000_B$ 2)
	IP0	Interrupt Priority Register 0	**$B8_H$** 1)	$XXXX0000_B$ 2)
	IP1	Interrupt Priority Register 1	$B9_H$)	$XXXXX000_B$ 2)
	ITCON	External Interrupt Trigger Condition Register	$9A_H$	$XXXX1010_B$ 2)
Ports	P0	Port 0	**80_H** 1)	FF_H
	P1	Port 1	**90_H** 1)	FF_H
	P2	Port 2	**$A0_H$** 1)	FF_H
	P3	Port 3	**$B0_H$** 1)	FF_H
Timer 0 / Timer 1	TCON	Timer 0/1 Control Register	**88_H** 1)	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
SSC Interface (C541U only)	SSCCON	SSC Control Register	93_H 1)	07_H
	STB	SSC Transmit Buffer	94_H	XX_H 2)
	SRB	SSC Receive Register	95_H	XX_H 2)
	SCF	SSC Flag Register	AB_H 1)	$XXXXXX00_B$ 2)
	SCIEN	SSC Interrupt Enable Register	AC_H	$XXXXXX00_B$ 2)
	SSCMOD	SSC Mode Test Register	96_H	00_H
Watchdog (C541U only)	WDCON	Watchdog Timer Control Register	**$C0_H$** 1)	$XXXX0000_B$ 2)
	WDTREL	Watchdog Timer Reload Register	86_H	00_H

1) Bit-addressable special function registers
2) “X“ means that the value is undefined and the location is reserved
3) The content of this SFR varies with the actual of the step C540U/C541U (eg. 01_H for the first step)
4) This SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Pow. Sav. Modes	PCON	Power Control Register	87_H	$X00X0000_B$ 2)
	PCON1	Power Control Register 1	88_H 4)	$0XX0XXXX_B$ 2)
USB Module	EPSEL	USB Endpoint Select Register	$D2_H$	80_H
	USBVAL	USB Data Register	$D3_H$	00_H
	ADROFF	USB Address Offset Register	$D4_H$	00_H 2)
	GEPIR	USB Global Endpoint Interrupt Request Reg.	$D6_H$	00_H
	DCR	USB Device Control Register	$C1_H$	$000X0000_B$
	DPWDR	USB Device Power Down Register	$C2_H$	00_H
	DIER	USB Device Interrupt Control Register	$C3_H$	00_H
	DIRR	USB Device Interrupt Request Register	$C4_H$	00_H
	FNRL	USB Frame Number Register, Low Byte	$C6_H$	XX_H
	FNRH	USB Frame Number Register, High Byte	$C7_H$	$00000XXX_B$
	EPBCn 1)	USB Endpoint n Buffer Control Register	$C1_H$	00_H
	EPBSn 1)	USB Endpoint n Buffer Status Register	$C2_H$	20_H
	EPIEn 1)	USB Endpoint n Interrupt Enable Register	$C3_H$	00_H
	EPIRn 1)	USB Endpoint n Interrupt Request Register	$C4_H$	10_H 3)
	EPBAn 1)	USB Endpoint n Base Address Register	$C5_H$	00_H
	EPLENn 1)	USB Endpoint n Buffer Length Register	$C6_H$	$0XXXXXXX_B$

1) These register are multiple registers (n=0-4) with the same SFR address; selection of register "n" is done by SFR EPSEL.
2) The reset value of ADROFF is valid only if USBVAL has not been read or written since the last hardware reset.
3) The reset value of EPIR0 is 11_H.

Table 4
Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Reset Value[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80_H [2]	P0	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
81_H	SP	07_H	.7	.6	.5	.4	.3	.2	.1	.0
82_H	DPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
83_H	DPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
86_H [4]	WDTREL	00_H	WDT PSEL	.6	.5	.4	.3	.2	.1	.0
87_H	PCON	$X00X\text{-}0000_B$	–	PDS	IDLS	–	GF1	GF0	PDE	IDLE
88_H [2]	TCON	00_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
88_H [2] [3]	PCON1	$0XX0\text{-}XXXX_B$	EWPD	–	–	WS	–	–	–	–
89_H	TMOD	00_H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
$8A_H$	TL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8B_H$	TL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8C_H$	TH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8D_H$	TH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
90_H [2]	P1	FF_H	.7	.6	$\overline{SLS}$	STO	SRI	SCLK	LED1	LED0
93_H [4]	SSCCON	07_H	SCEN	TEN	MSTR	CPOL	CPHA	BRS2	BRS1	BRS0
94_H [4]	STB	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
95_H [4]	SRB	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
96_H [4]	SSCMOD	00_H	LOOPB	TRIO	0	0	0	0	0	LSBSM
$9A_H$	ITCON	$XXXX\text{-}1010_B$	–	–	–	–	I1ETF	I1ETR	I0ETF	I0ETR
$A0_H$ [2]	P2	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$A8_H$ [2]	IEN0	$0XXX\text{-}0000_B$	EA	–	–	–	ET1	EX1	ET0	EX0
$A9_H$	IEN1	$XXXX\text{-}X000_B$	–	–	–	–	–	EUDI	EUEI	ESSC
AB_H [4]	SCF	$XXXX\text{-}XX00_B$	–	–	–	–	–	–	WCOL	TC

1) X means that the value is undefined and the location is reserved
2) Bit-addressable special function registers
3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.
4) This SFR is only available in the C541U.

Table 4
Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Reset Value[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AC_H [4)]	SCIEN	$XXXX\text{-}XX00_B$	–	–	–	–	–	–	WCEN	TCEN
$B0_H$[2)]	P3	FF_H	RD	WR	T1	T0	INT1	INT0	DADD	LED2
$B1_H$	SYSCON	$XX10\text{-}XXXX_B$	–	–	EALE	RMAP	–	–	–	–
$B8_H$[2)]	IP0	$XXXX\text{-}0000_B$	–	–	–	–	PT1	PX1	PT0	PX0
$B9_H$	IP1	$XXXX\text{-}0000_B$	–	–	–	–	–	PUDI	PUEI	PSSC [4)]
$C0_H$ [2)]	WDCON	$XXXX\text{-}0000_B$	–	–	–	–	OWDS	WDTS	WDT	SWDT
$C1_H$ to $C7_H$		USB Device and Endpoint Register definition see **table 3-4**								
$D0_H$ [2)]	PSW	00_H	CY	AC	F0	RS1	RS0	OV	F1	P
$D2_H$	EPSEL	80_H	EPS7	0	0	0	0	EPS2	EPS1	EPS0
$D3_H$	USBVAL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D4_H$	ADROFF	00_H [7)]	0	0	AO5	AO4	AO3	AO2	AO1	AO0
$D6_H$	GEPIR	00_H	0	0	0	EPI4	EPI3	EPI2	EPI1	EPI0
$E0_H$[2)]	ACC	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F0_H$[2)]	B	00_H	.7	.6	.5	.4	.3	.2	.1	.0
FC_H [3) 5)]	VR0	$C5_H$	1	1	0	0	0	1	0	1
FD_H [3) 5)]	VR1	$C1_H$	1	1	0	0	0	0	0	1
FE_H [3) 5)]	VR2	[6)]	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved
2) Bit-addressable special function registers
3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.
4) This SFR respectively bit is only available in the C541U.
5) These are read-only registers
6) The content of this SFR varies with the actual of the step C517A (e.g. 01_H for the first step)
7) The reset value of ADROFF is valid only if USBVAL has not been read or written since the last hardware reset.

Table 5
Contents of the USB Device and Endpoint Registers (Addr. $C1_H$ to $C7_H$)

Addr	Register	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EPSEL = $1XXX.XXXX_B$	**Device Registers**									
$C1_H$	DCR	$000X.0000_B$	SPEED	DA	SWR	SUSP	DINIT	RSM	UCLK	PCLK
$C2_H$	DPWDR	00_H	0	0	0	0	0	0	TPWD	RPWD
$C3_H$	DIER	00_H	SE0IE	DAIE	DDIE	SBIE	SEIE	STIE	SUIE	SOFIE
$C4_H$	DIRR	00_H	SE0I	DAI	DDI	SBI	SEI	STI	SUI	SOFI
$C5_H$	reserved									
$C6_H$	FNRL	XX_H	FNR7	FNR6	FNR5	FNR4	FNR3	FNR2	FNR1	FNR0
$C7_H$	FNRH	$0000.0XXX_B$	0	0	0	0	0	FNR10	FNR9	FNR8
EPSEL = $0XXX.X000_B$	**Endpoint 0 Registers**									
$C1_H$	EPBC0	00_H	STALL0	0	0	GEPIE0	SOFDE0	INCE0	0	DBM0
$C2_H$	EPBS0	20_H	UBF0	CBF0	DIR0	ESP0	SETRD0	SETWR0	CLREP0	DONE0
$C3_H$	EPIE0	00_H	AIE0	NAIE0	RLEIE0	–	DNRIE0	NODIE0	EODIE0	SODIE0
$C4_H$	EPIR0	11_H	ACK0	NACK0	RLE0	–	DNR0	NOD0	EOD0	SOD0
$C5_H$	EPBA0	00_H	PAGE0	0	0	0	A06	A05	A04	A03
$C6_H$	EPLEN0	$0XXX.XXXX_B$	0	L06	L05	L04	L03	L02	L01	L00
$C7_H$	reserved									
EPSEL = $0XXX.X001_B$	**Endpoint 1 Registers**									
$C1_H$	EPBC1	00_H	STALL1	0	0	GEPIE1	SOFDE1	INCE1	0	DBM1
$C2_H$	EPBS1	20_H	UBF1	CBF1	DIR1	ESP1	SETRD1	SETWR1	CLREP1	DONE1
$C3_H$	EPIE1	00_H	AIE1	NAIE1	RLEIE1	–	DNRIE1	NODIE1	EODIE1	SODIE1
$C4_H$	EPIR1	10_H	ACK1	NACK1	RLE1	–	DNR1	NOD1	EOD1	SOD1
$C5_H$	EPBA1	00_H	PAGE1	0	0	0	A16	A15	A14	A13
$C6_H$	EPLEN1	$0XXX.XXXX_B$	0	L16	L15	L14	L13	L12	L11	L10
$C7_H$	reserved									

Table 5
Contents of the USB Device and Endpoint Registers (Addr. $C1_H$ to $C7_H$) (cont'd)

Addr	Register	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EPSEL = $0XXX.X010_B$	**Endpoint 2 Registers**									
$C1_H$	EPBC2	00_H	STALL2	0	0	GEPIE2	SOFDE2	INCE2	0	DBM2
$C2_H$	EPBS2	20_H	UBF2	CBF2	DIR2	ESP2	SETRD2	SETWR2	CLREP2	DONE2
$C3_H$	EPIE2	00_H	AIE2	NAIE2	RLEIE2	–	DNRIE2	NODIE2	EODIE2	SODIE2
$C4_H$	EPIR2	10_H	ACK2	NACK2	RLE2	–	DNR2	NOD2	EOD2	SOD2
$C5_H$	EPBA2	00_H	PAGE2	0	0	0	A62	A52	A42	A32
$C6_H$	EPLEN2	$0XXX.XXXX_B$	0	L62	L52	L42	L32	L22	L12	L02
$C7_H$	reserved									
EPSEL = $0XXX.X011_B$	**Endpoint 3 Registers**									
$C1_H$	EPBC3	00_H	STALL3	0	0	GEPIE3	SOFDE3	INCE3	0	DBM3
$C2_H$	EPBS3	20_H	UBF3	CBF3	DIR3	ESP3	SETRD3	SETWR3	CLREP3	DONE3
$C3_H$	EPIE3	00_H	AIE3	NAIE3	RLEIE3	–	DNRIE3	NODIE3	EODIE3	SODIE3
$C4_H$	EPIR3	10_H	ACK3	NACK3	RLE3	–	DNR3	NOD3	EOD3	SOD3
$C5_H$	EPBA3	00_H	PAGE3	0	0	0	A63	A52	A43	A33
$C6_H$	EPLEN3	$0XXX.XXXX_B$	0	L63	L53	L43	L33	L23	L13	L03
$C7_H$	reserved									
EPSEL = $0XXX.X100_B$	**Endpoint 4 Registers**									
$C1_H$	EPBC4	00_H	STALL4	0	0	GEPIE4	SOFDE4	INCE4	0	DBM4
$C2_H$	EPBS4	20_H	UBF4	CBF4	DIR4	ESP4	SETRD4	SETWR4	CLREP4	DONE4
$C3_H$	EPIE4	00_H	AIE4	NAIE4	RLEIE4	–	DNRIE4	NODIE4	EODIE4	SODIE4
$C4_H$	EPIR4	10_H	ACK4	NACK4	RLE4	–4	DNR4	NOD4	EOD4	SOD4
$C5_H$	EPBA4	00_H	PAGE4	0	0	0	A64	A54	A44	A34
$C6_H$	EPLEN4	$0XXX.XXXX_B$	0	L64	L54	L44	L34	L24	L14	L04
$C7_H$	reserved									

Digital I/O Ports

The C540U/C541U in the P-SDIP-52 package has four 8-bit I/O ports. In the P-LCC-44 package port 1 is a 6-bit I/O port only. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 3 are quasi-bidirectional I/O ports with internal pullup resistors. That means, when configured as inputs, ports 1 to 3 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

The output drivers of port 0 and 2 and the input buffers of port 0 are also used for accessing external memory. In this application, port 0 outputs the low byte of the external memory address, time multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise, the port 2 pins continue emitting the P2 SFR contents. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET.

Two port lines of port 1 (P1.0/LED0, P1.1/LED1) and one port line of port 3 (P3.0/LED2) have the capability of driving external LEDs in the output low state.

Timer / Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **table 6** :

Table 6
Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD		Input Clock	
		M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	0	0	f_{OSC}/6x32	f_{OSC}/12x32
1	16-bit timer/counter	1	1	f_{OSC}/6	f_{OSC}/12
2	8-bit timer/counter with 8-bit autoreload	1	0		
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	1	1		

In the “timer” function (C/$\overline{T}$ = ‘0’) the register is incremented every machine cycle. Therefore the count rate is f_{OSC}/6.

In the “counter” function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is f_{OSC}/12. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 11** illustrates the input clock logic.

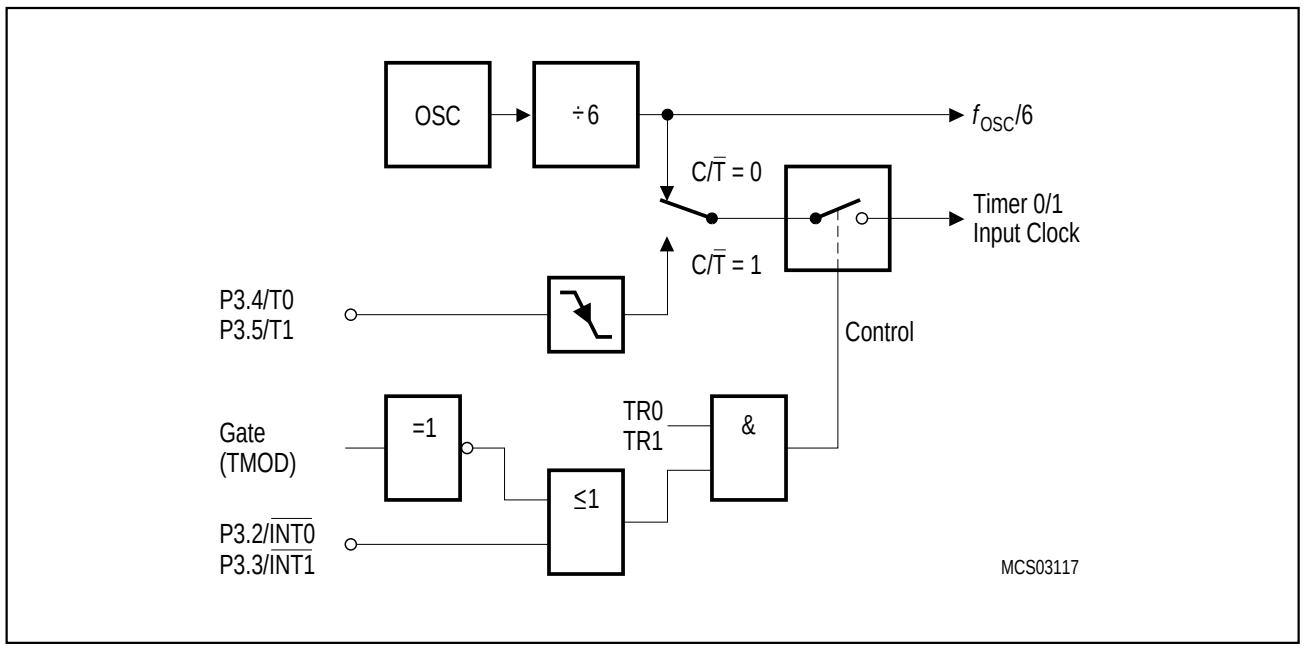


Figure 11
Timer/Counter 0 and 1 Input Clock Logic

SSC Interface (C541U only)

The C541U microcontroller provides a Synchronous Serial Channel unit, the SSC. This interface is compatible to the popular SPI serial bus interface. **Figure 12** shows the block diagram of the SSC. The central element of the SSC is an 8-bit shift register. The input and the output of this shift register are each connected via a control logic to the pin P1.3 / SRI (SSC Receiver In) and P1.4 / STO (SSC Transmitter Out). This shift register can be written to (SFR STB) and can be read through the Receive Buffer Register SRB.

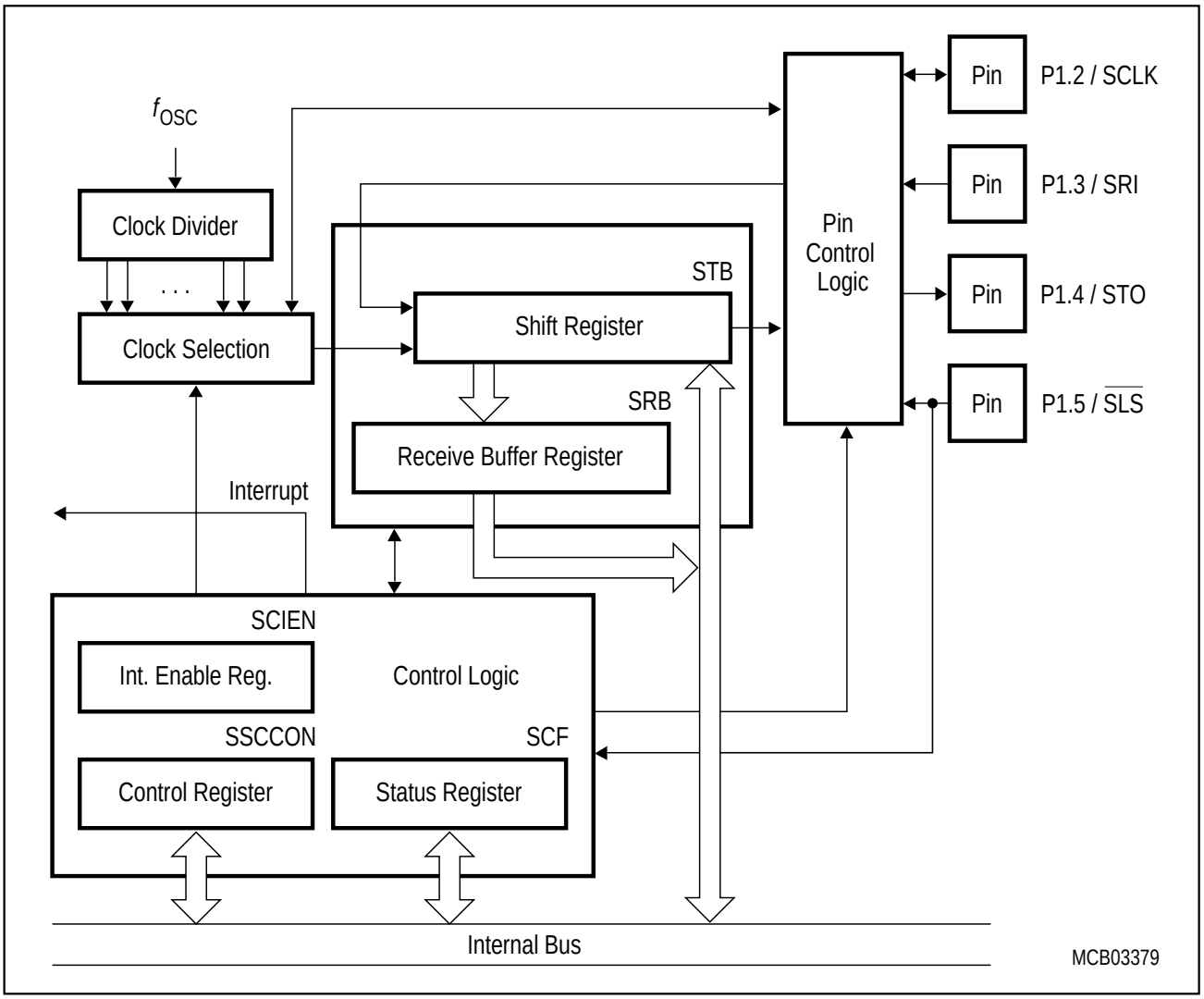


Figure 12
SSC Block Diagram

The SSC has implemented a clock control circuit, which can generate the clock via a baud rate generator in the master mode, or receive the transfer clock in the slave mode. The clock signal is fully programmable for clock polarity and phase. The pin used for the clock signal is P1.2/ SCLK. When operating in slave mode, a slave select input ¯is provided which enables the SSC interface and also will control the transmitter output. The pin used for this is P1.5 / $\overline{\text{SLS}}$.

The SSC control block is responsible for controlling the different modes and operation of the SSC, checking the status, and generating the respective status and interrupt signals.

USB Module

The USB module in the C540U/C541U handles all transactions between the serial USB bus and the internal (parallel) bus of the microcontroller. The USB module includes several units which are required to support data handling with the USB bus : the on-chip USB bus transceiver, the USB memory with two pages of 128 bytes each, the memory management unit (MMU) for USB and CPU memory access control, the UDC device core for USB protocol handling, the microcontroller interface with the USB specific special function registers and the interrupt control logic. A clock generation unit provides the clock signal for the USB module for full speed and low speed USB operation. **Figure 13** shows the block diagram of the functional units of the USB module with their interfaces.

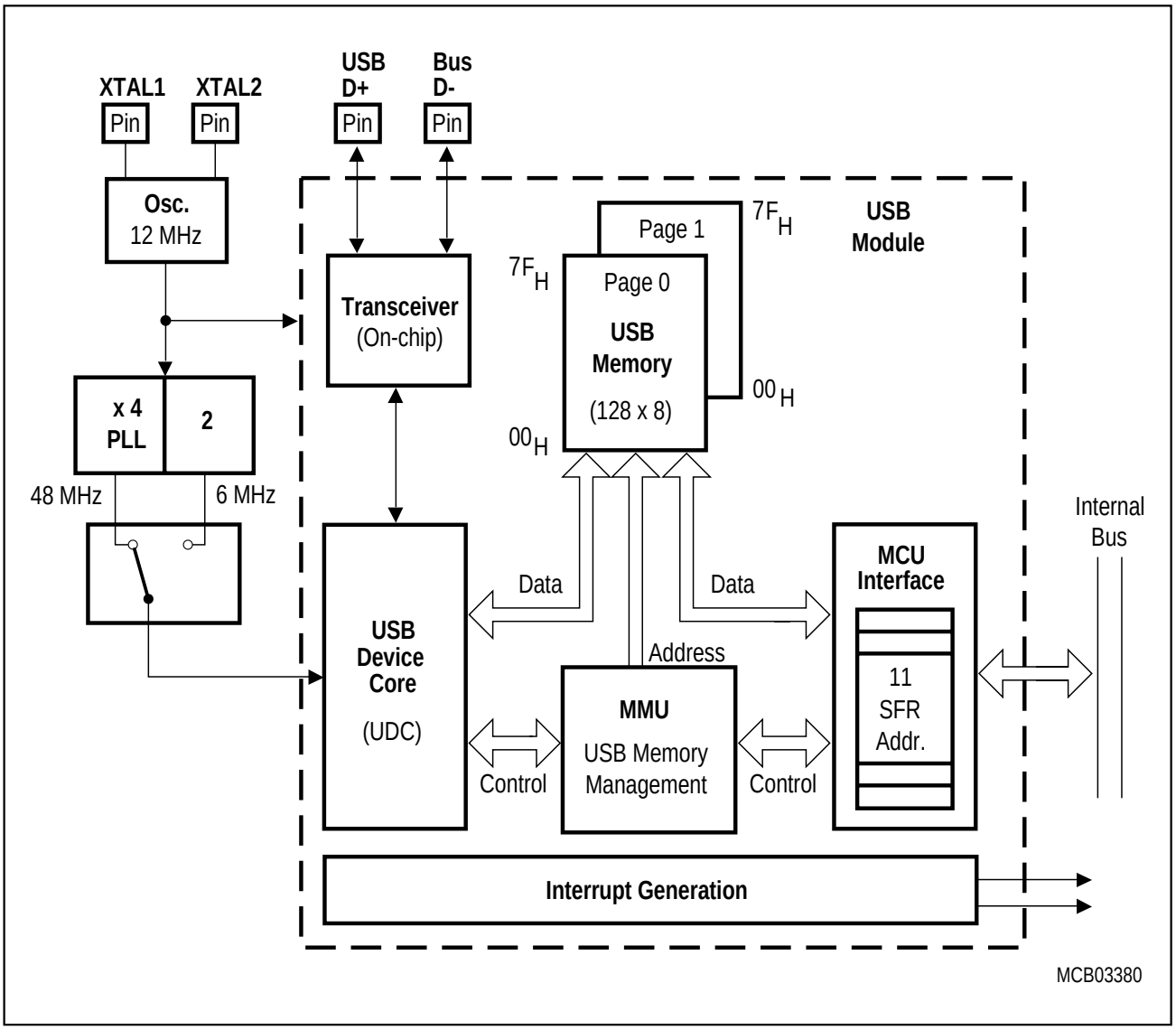


Figure 13
USB Module Block Diagram

USB Registers

Two different kinds of registers are implemented in the USB module. The global registers (GEPIR, EPSEL, ADROFF, USBVAL) describe the basic functionality of the complete USB module and can be accessed via unique SFR addresses. For reduction of the number of SFR addresses which are needed to control the USB module inside the C540U/C541U, device registers and endpoint registers are mapped into an SFR address block of seven SFR addresses ($C1_H$ to $C7_H$). The endpoint specific functionality of the USB module is controlled via the device registers DCR, DPWDR, DIER, DIRR and the frame number registers. An endpoint register set is available for each endpoint (n=0..4) and describes the functionality of the selected endpoint. **Figure 14** explains the structure of the USB module registers.

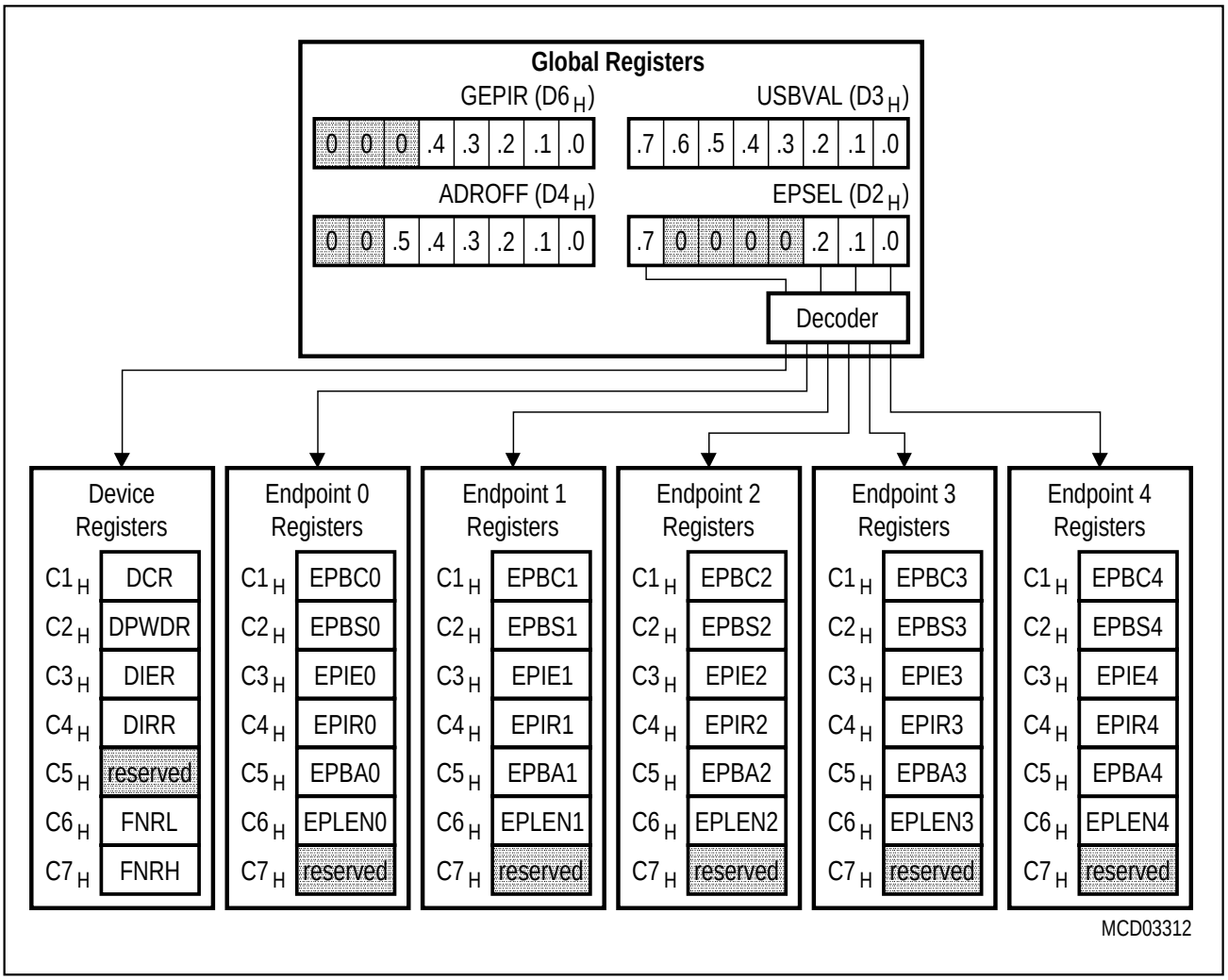


Figure 14
Register Structure of the USB Module

Interrupt System

The C541U provides seven (C540U : six) interrupt sources with two priority levels. Five interrupts can be generated by the on-chip peripherals (timer 0, timer 1, SSC interface, and USB module), and two interrupts may be triggered externally (P3.2/$\overline{INT0}$ and P3.3/$\overline{INT1}$).

Figure 15 to **17** give a general overview of the interrupt sources and illustrate the request and control flags which are described in the next sections.

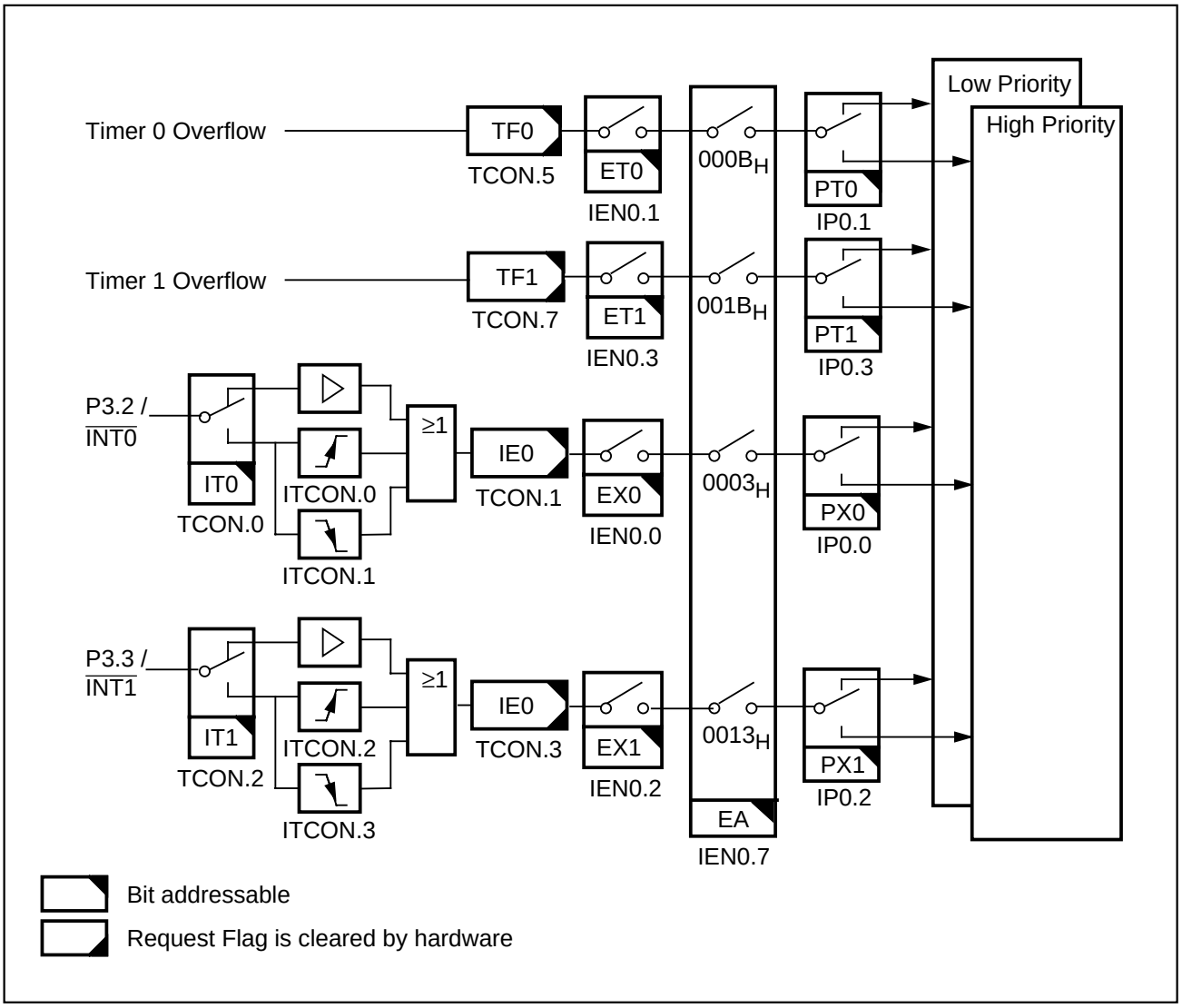


Figure 15
Interrupt Request Sources (Part 1)

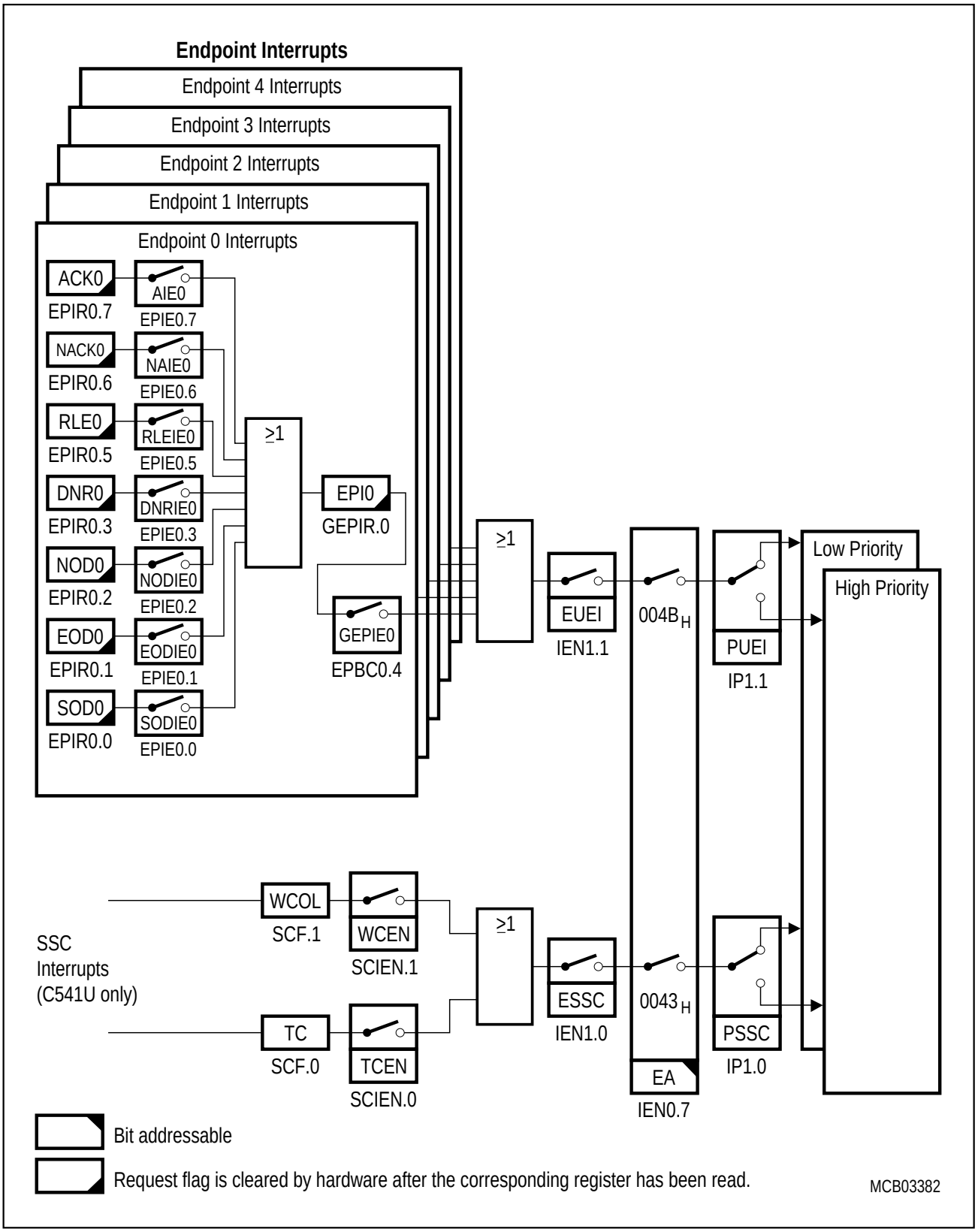


Figure 16
Interrupt Request Sources (Part 2)

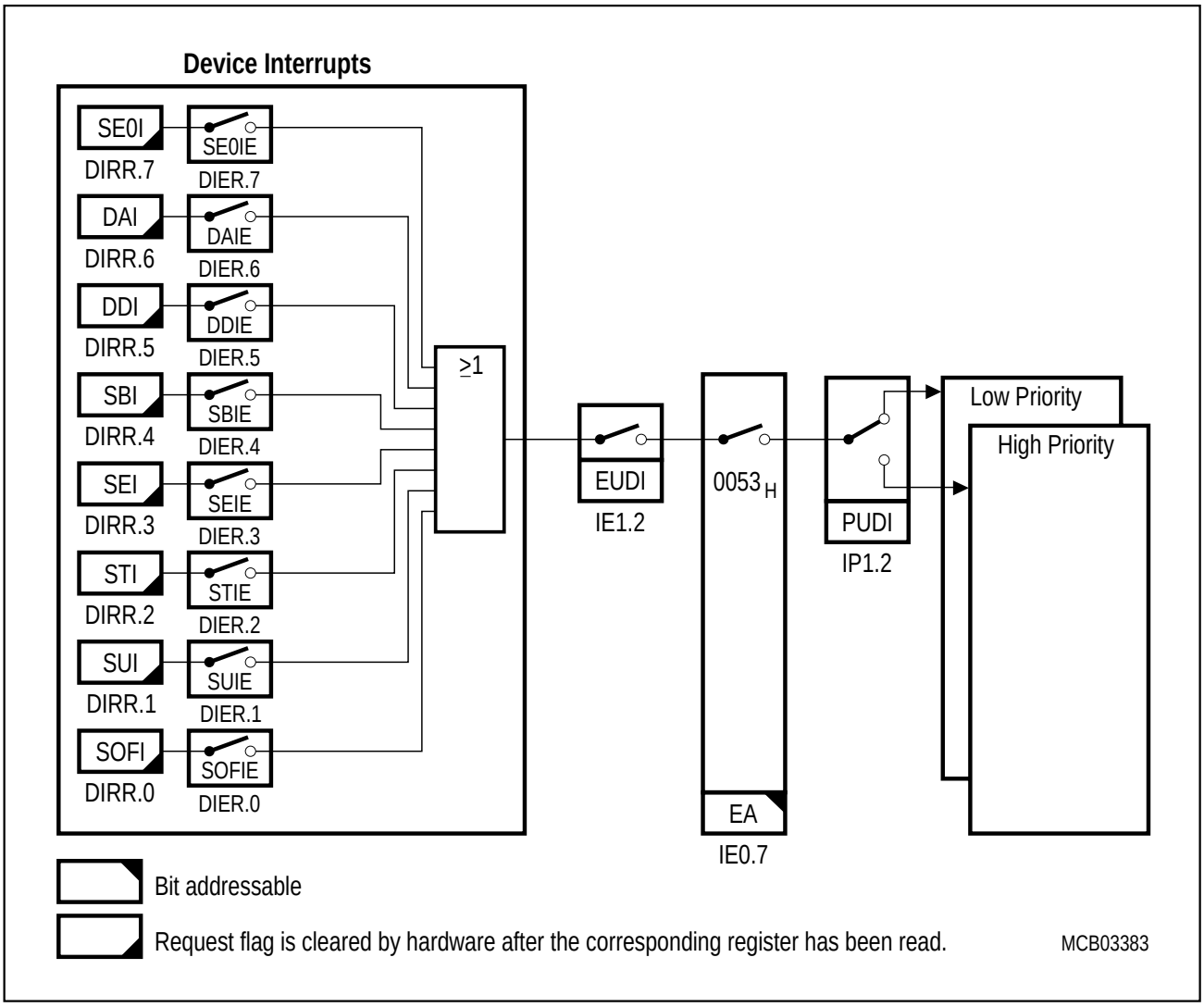


Figure 17
Interrupt Request Sources (Part 3)

Table 7
Interrupt Source and Vectors

Interrupt Source	Interrupt Vector Address	Interrupt Request Flags (SFRs)
External Interrupt 0	0003_H	IE0
Timer 0 Overflow	$000B_H$	TF0
External Interrupt 1	0013_H	IE1
Timer 1 Overflow	$001B_H$	TF1
SSC Interrupt (C541U only)	0043_H	TC, WCOL
USB Endpoint Interrupt	$004B_H$	in SFRs EPIR0-4 and GEIPR
USB Device Interrupt	0053_H	in SFRs DIRR
Wake-up from power down	$007B_H$	–

Fail Save Mechanisms

The C540U/C541U offers enhanced fail safe mechanisms, which allow an automatic recovery from software upset or hardware failure :

- a programmable watchdog timer (WDT), with variable time-out period from 256 µs up to approx. 0.55 µs at 12 MHz. The WDT is not available in the C540U.
- an oscillator watchdog (OWD) which monitors the on-chip oscillator and forces the microcontroller into reset state in case the on-chip oscillator fails; it also provides the clock for a fast internal reset after power-on.

The watchdog timer in the C517A is a 15-bit timer, which is incremented by a count rate of $f_{OSC}/12$ or $f_{OSC}/192$. The system clock of the C517A is divided by two prescalers, a divide-by-two and a divide-by-16 prescaler which are selected by bit WDTPSEL (WDTREL.7). For programming of the watchdog timer overflow rate, the upper 7 bit of the watchdog timer can be written. **Figure 8-18** shows the block diagram of the watchdog timer unit.

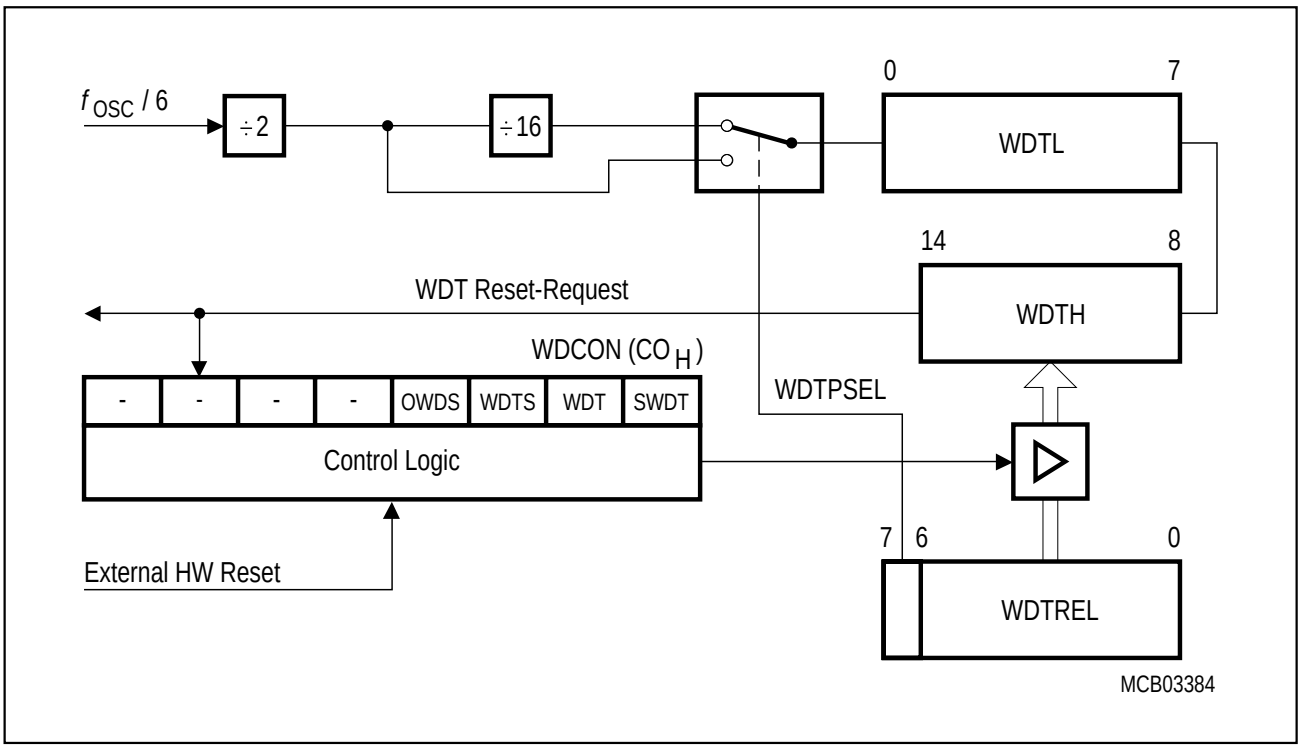


Figure 18
Block Diagram of the Watchdog Timer

The watchdog timer can be started by software (bit SWDT) but it cannot be stopped during active mode of the C541U. If the software fails to refresh the running watchdog timer an internal reset will be initiated on watchdog timer overflow. For refreshing of the watchdog timer the content of the SFR WDTREL is transfered to the upper 7-bit of the watchdog timer. The refresh sequence consists of two consequtive instructions which set the bits WDT and SWDT each. The reset cause (external reset or reset caused by the watchdog) can be examined by software (flag WDTS). It must be noted, however, that the watchdog timer is halted during the idle mode and power down mode of the processor.

Oscillator Watchdog

The oscillator watchdog unit serves for three functions:

- **Monitoring of the on-chip oscillator's function**
  The watchdog supervises the on-chip oscillator's frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is brought into reset; if the failure condition disappears (i.e. the on-chip oscillator has a higher frequency than the RC oscillator), the part executes a final reset phase of typ. 1 ms in order to allow the oscillator to stabilize; then the oscillator watchdog reset is released and the part starts program execution again.
- **Fast internal reset after power-on**
  The oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. The oscillator watchdog unit also works identically to the monitoring function.
- **Control of external wake-up from software power-down mode** (description see chapter 9)
  When the power-down mode is left by a low level at the $\overline{\text{INT0}}$ pin or by the USB, the oscillator watchdog unit assures that the microcontroller resumes operation (execution of the power-down wake-up interrupt) with the nominal clock rate. In the power-down mode the RC oscillator and the on-chip oscillator are stopped. Both oscillators are started again when power-down mode is released. When the on-chip oscillator has a higher frequency than the RC oscillator, the microcontroller starts operation after a final delay of typ. 1 ms in order to allow the on-chip oscillator to stabilize.

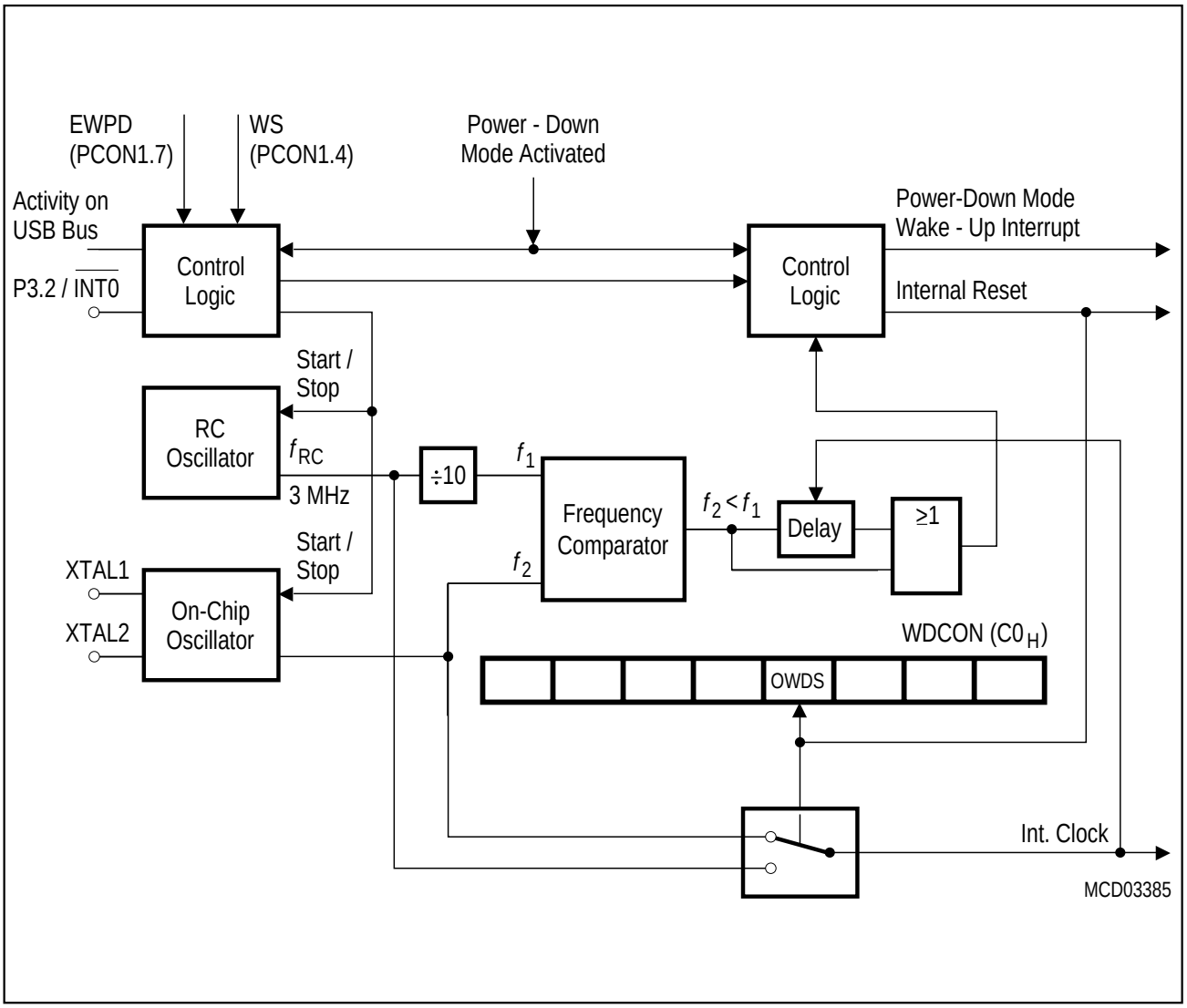


Figure 19
Functional Block Diagram of the Oscillator Watchdog

Power Saving Modes

The C540U/C541U provides two basic power saving modes, the idle mode and the power down mode.

- **Idle mode**
  In the idle mode the main oscillator of the C540U/C541U continues to run, but the CPU is gated off from the clock signal. However, the interrupt system, the SSC (C541U only), the USB module, and the timers with the exception of the watchdog timer (C541U only) are further provided with the clock. The CPU status is preserved in its entirety : the stack pointer, program counter, program status word, accumulator, and all other registers maintain their data during idle mode. The idle mode can be terminated by activating any enabled interrupt. or by a hardware reset.
- **Power down mode**
  In the power down mode, the RC osciillator and the on-chip oscillator which operates with the XTAL pins is stopped. Therefore, all functions of the microcontroller are stopped and only the contents of the on-chip RAM, XRAM and the SFR's are maintained. The power down mode can be left either by an active reset signal or by a low signal at the P3.2/$\overline{\text{INT0}}$ pin or any activity on the USB bus. Using reset to leave power down mode puts the microcontroller with its SFRs into the reset state. Using the $\overline{\text{INT0}}$ pin or USB bus for power down mode exit maintains the state of the SFRs, which has been frozen when power down mode is entered.

In the power down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the power down mode is invoked, and that V_{CC} is restored to its normal operating level, before the power down mode is terminated. **Table 8** gives a general overview of the entry and exit procedures of the power saving modes.

Table 8
Power Saving Modes Overview

Mode	Entering 2-Instruction Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H ORL PCON, #20H	Ocurrence of an interrupt from a peripheral unit	CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with clock
		Hardware Reset	
Power Down Mode	ORL PCON, #02H ORL PCON, #40H	Hardware Reset	Oscillator is stopped; contents of on-chip RAM and SFR’s are maintained;
		Short low pulse at pin P3.2/$\overline{\text{INT0}}$ or activity on the USB bus	

OTP Memory Operation

The C540U/C541U contains a 8k byte one-time programmable (OTP) program memory (C540U : 4k byte). With the C540U/C541U fast programming cycles are achieved (1 byte in 100 µsec). Also several levels of OTP memory protection can be selected.

For programming of the device, the C540U/C541U must be put into the programming mode. This typically is done not in-system but in a special programming hardware. In the programming mode the C540U/C541U operates as a slave device similar as an EPROM standalone memory device and must be controlled with address/data information, control lines, and an external 11.5V programming voltage. **Figure 20** shows the pins of the C504-2E which are required for controlling of the OTP programming mode.

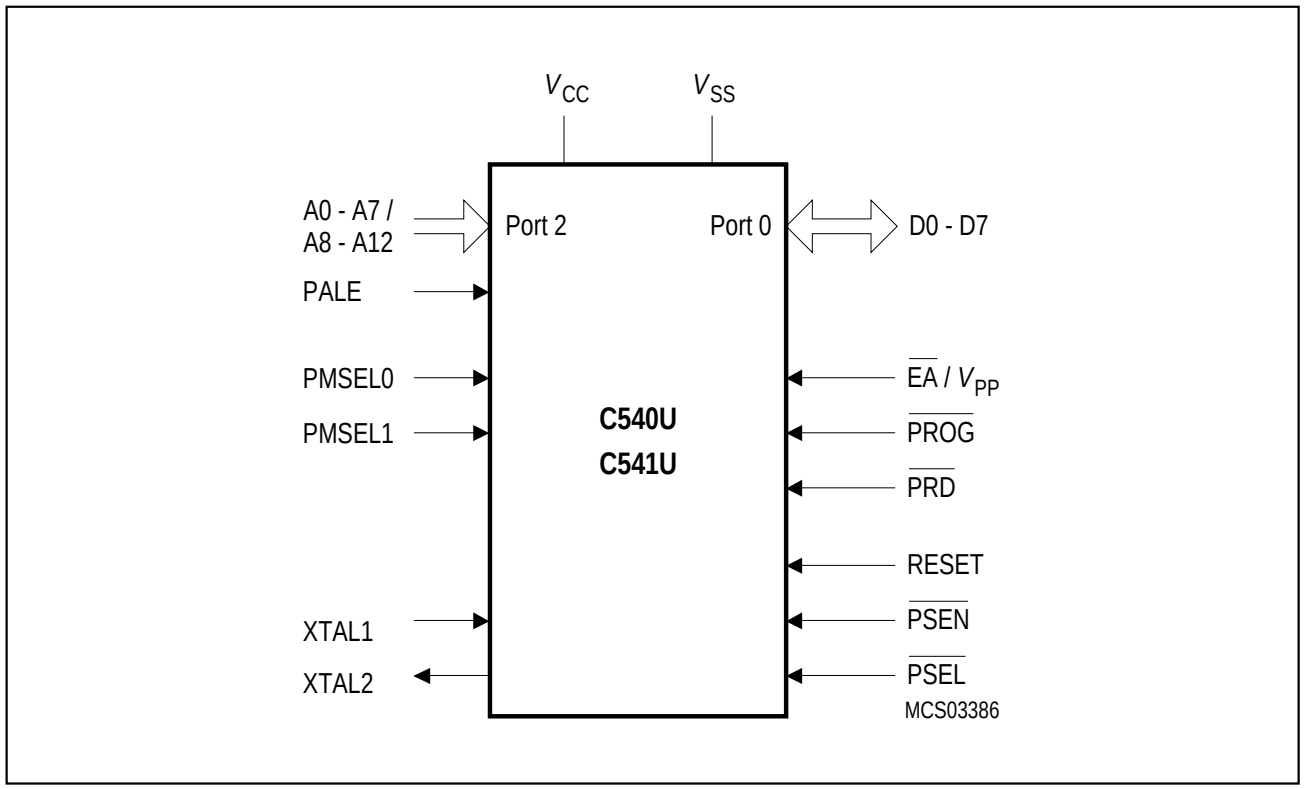


Figure 20
Programming Mode Configuration

Pin Configuration in Programming Mode

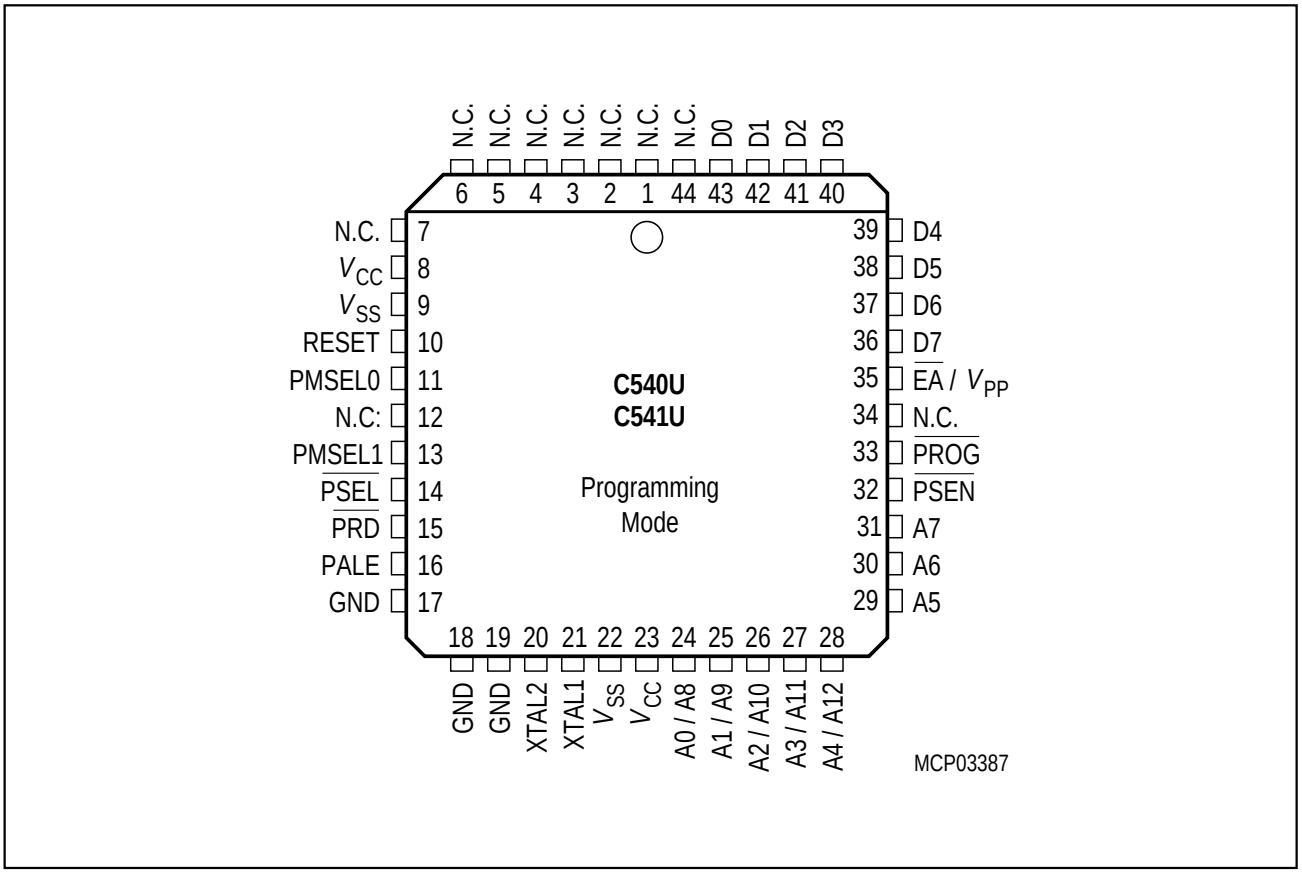


Figure 21
P-LCC-44 Pin Configuration of the C540U/C541U in Programming Mode (Top View)

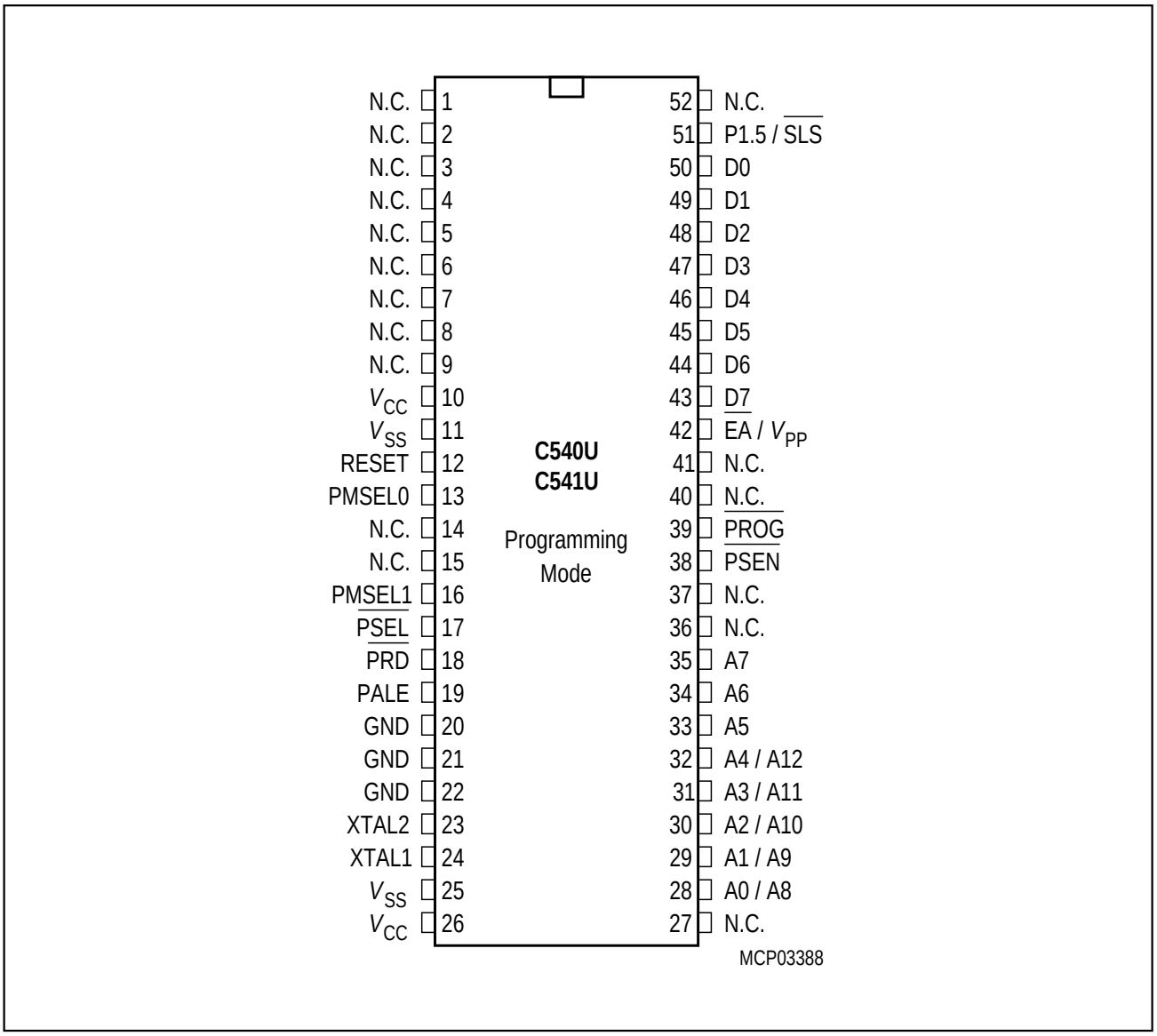


Figure 22
P-SDIP-52 Pin Configuration of the C540U/C541U in Programming Mode (Top View)

The following **table 9** contains the functional description of all C517A-2E pins which are required for OTP memory programming.

Table 9
Pin Definitions and Functions in Programming Mode

Symbol	Pin Numbers		I/O*)	Function
	P-LCC-44	P-SDIP-52		
RESET	10	12	I	**Reset** This input must be at static “1“ (active) level during the whole programming mode.
PMSEL0 PMSEL1	11 13	13 16	I I	**Programming mode selection pins** These pins are used to select the different access modes in programming mode. PMSEL1,0 must satisfy a setup time to the rising edge of PALE. When the logic level of PMSEL1,0 is changed, PALE must be at low level.
$\overline{\text{PSEL}}$	14	17	I	**Basic programming mode select** This input is used for the basic programming mode selection and must be switched according **figure 10-23**.
$\overline{\text{PRD}}$	15	18	I	**Programming mode read strobe** This input is used for read access control for OTP memory read, version byte read, and lock bit read operations.
PALE	16	19	I	**Programming mode address latch enable** PALE is used to latch the high address lines. The high address lines must satisfy a setup and hold time to/ from the falling edge of PALE. PALE must be at low level whenever the logic level of PMSEL1,0 is changed.
XTAL2	20	23	O	**XTAL2** Output of the inverting oscillator amplifier.

PMSEL1	PMSEL0	Access Mode
0	0	Reserved
0	1	Read version bytes
1	0	Program/read lock bits
1	1	Program/read OTP memory byte

*) I = Input
O = Output

Table 9
Pin Definitions and Functions in Programming Mode (cont'd)

Symbol	Pin Numbers		I/O*)	Function
	P-LCC-44	P-SDIP-52		
XTAL1	21	24	I	**XTAL1** Input to the oscillator amplifier.
A0/A8 - A7	24 - 31	28 - 35	I	**Address lines** P2.0-7 are used as multiplexed address input lines A0-A7 and A8-A12. A8-A12 must be latched with PALE. Address A12 is requred only for the C541U.
$\overline{\text{PSEN}}$	32	38	I	**$\overline{\text{Program store enable}}$** This input must be at static "0" level during the whole programming mode.
$\overline{\text{PROG}}$	33	39	I	**$\overline{\text{Programming mode write strobe}}$** This input is used in programming mode as a write strobe for OTP memory program and lock bit write operations During basic programming mode selection a low level must be applied to $\overline{\text{PROG}}$.
$\overline{\text{EA}}/V_{PP}$	35	42	I	**$\overline{\text{External Access}}$ / Programming voltage** This pin must be at 11.5 V (V_{PP}) voltage level during programming of an OTP memory byte or lock bit. During an OTP memory read operation this pin must be at high level (V_{IH}). This pin is also used for basic programming mode selection. At basic programming mode selection a low level must be applied to $\overline{\text{EA}}/V_{PP}$.
D0 - 7	43 - 38	50 - 43	I/O	**Data lines 0-7** During programming mode, data bytes are read or written from or to the C540U/C541U via the bidirectional D0-7 lines which are located at port 0.
V_{SS}	9, 22	11, 25	–	**Circuit ground potential** must be applied to these pins in programming mode.
V_{CC}	8, 23	10, 26	–	**Power supply terminal** must be applied to these pins in programming mode.
N.C.	1, 12,, 34, 44	1 - 9, 14, 15, 27, 36, 37, 40, 41, 52	–	**Not Connected** These pins should not be connected in programming mode.
GND	17 - 19	20 - 22	I	**Ground pins** In programming mode these pins must be connected to V_{IL} level.

*) I = Input
O = Output

Basic Programming Mode Selection

The basic programming mode selection scheme is shown in **figure 23**.

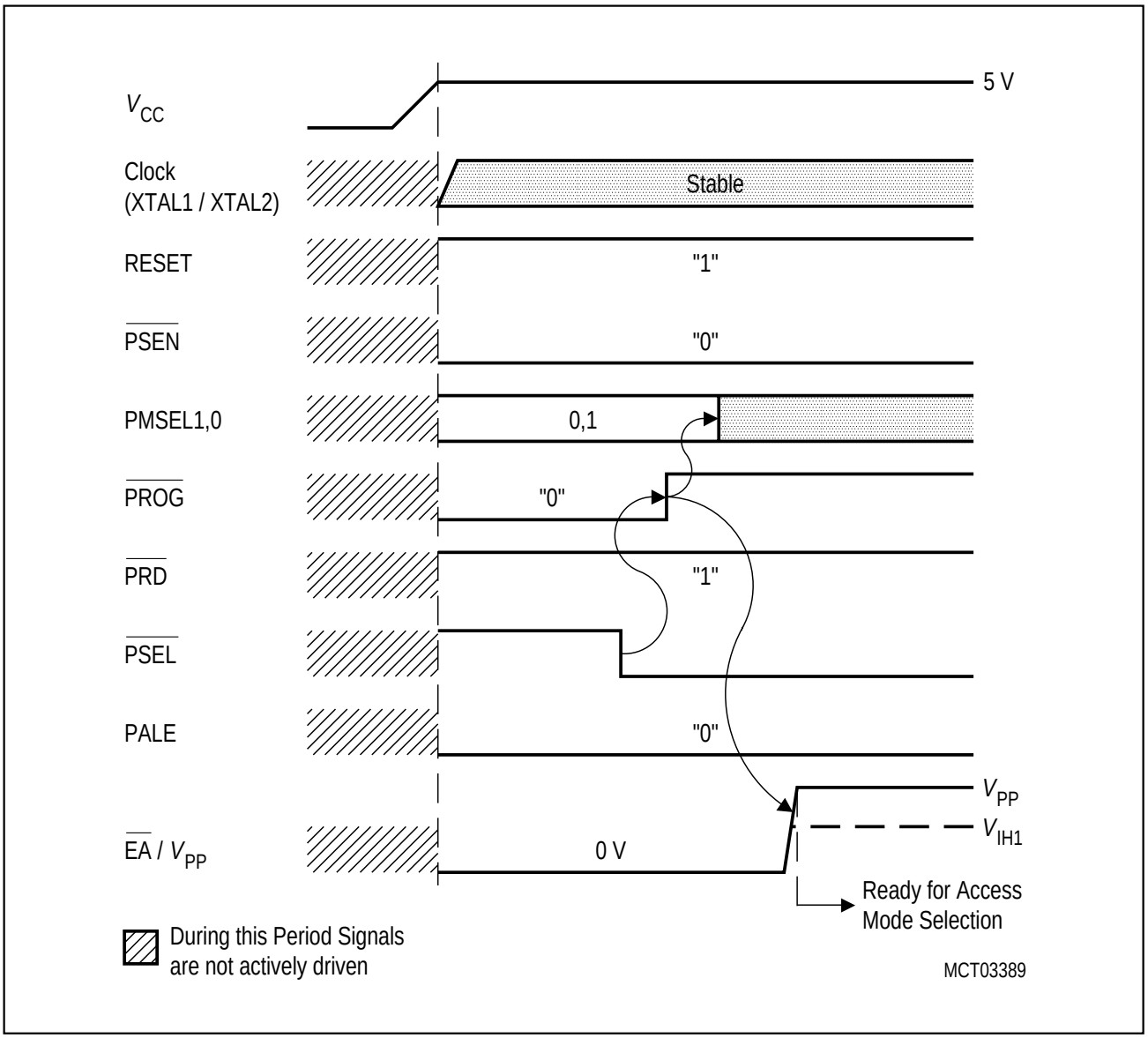


Figure 23
Basic Programming Mode Selection

Table 10
Access Modes Selection

Access Mode	$\overline{EA}$/ V_{PP}	$\overline{PROG}$	$\overline{PRD}$	PMSEL		Address (Port 2)	Data (Port 0)
				1	0		
Program OTP memory byte	V_{PP}	⊓	H	H	H	A0-7 A8-15	D0-7
Read OTP memory byte	V_{IH}	H	⊓				
Program OTP lock bits	V_{PP}	⊓	H	H	L	–	D1,D0 see **table 11**
Read OTP lock bits	V_{IH}	H	⊓				
Read OTP version byte	V_{IH}	H	⊓	L	H	Byte addr. of sign. byte	D0-7

Lock Bits Programming / Read

The C540U/C541U has two programmable lock bits which, when programmed according **tabie 11**, provide four levels of protection for the on-chip OTP code memory. The state of the lock bits can also be read.

Table 11
Lock Bit Protection Types

Lock Bits at D1,D0		Protection Level	Protection Type
D1	D0		
1	1	Level 0	The OTP lock feature is disabled. During normal operation of the C540U/C541U, the state of the $\overline{EA}$ pin is not latched on reset.
1	0	Level 1	During normal operation of the C540U/C541U, MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset. An OTP memory read operation is only possible using the OTP verification mode for protection level 1. Further programming of the OTP memory is disabled (reprogramming security).
0	1	Level 2	Same as level 1, but also OTP memory read operation using OTP verification mode is disabled.
0	0	Level 3	Same as level 2; but additionally external code execution by setting $\overline{EA}$=low during normal operation of the C540U/C541U is no more possible. External code execution, which is initiated by an internal program (e.g. by an internal jump instruction above the ROM boundary), is still possible.

Absolute Maximum Ratings

Ambient temperature under bias (T_A)	0 to 70 °C
Storage temperature (T_{stg})	– 65 °C to 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS})	– 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS})	– 0.5 V to V_{CC} +0.5 V
Input current on any pin during overload condition	– 10 mA to 10 mA
Absolute sum of all input currents during overload condition	I 100 mA I
Power dissipation	TBD

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.*

DC Characteristics

V_{CC} = 4.0V to 5.5V (5V +10%, -20%); V_{SS} = 0 V T_A = 0 to 70 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{EA}$, RESET)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input low voltage (RESET)	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltage (except XTAL1, RESET)	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL1	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	–
Input high voltage to RESET	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage Ports 1, 2, 3 P1.0, P1.1, P3.0	V_{OL}	 – –	 0.45 0.45	 V V	 I_{OL} = 1.6 mA [1] I_{OL} = 10 mA [1]
Output low voltage (port 0, ALE, $\overline{PSEN}$)	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 80 µA, I_{OH} = – 10 µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)	V_{OH2}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 800 µA I_{OH} = – 80 µA [2]
Logic 0 input current (ports 1, 2, 3)	I_{IL}	– 10	– 50	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$)	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	–	10	pF	f_c = 1 MHz, T_A = 25 °C [7]
Overload current	I_{OV}	–	± 5	mA	[6] [7]
Programming voltage	V_{PP}	10.9	12.1	V	11.5 V ± 5%

Notes see next page

Power Supply Current

Parameter		Symbol	Limit Values		Unit	Test Condition
			typ. [8]	max. [9]		
Active mode	12 MHz	I_{CC}	15	TBD	mA	[4]
Idle mode	12 MHz	I_{CC}	TBD	TBD	mA	[5]
Power-down mode		I_{PD}	TBD	50	µA	V_{CC} = 2…5.5 V [3]

Notes :

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (power-down mode) is measured under following conditions:
$\overline{EA}$ = Port 0 = V_{CC} ; XTAL2 = N.C.; XTAL1 = V_{SS} ; RESET = V_{SS}; all other pins are disconnected.
the USB transceiver is switched off;

4) I_{CC} (active mode) is measured with:
XTAL1 driven with t_{CLCH} , t_{CHCL} = 5 ns , V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
$\overline{EA}$ = RESET = Port 0 = Port 1 = V_{CC} ; all other pins are disconnected.
I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

5) I_{CC} (idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_{CLCH} , t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
$\overline{EA}$ = RESET = V_{ss} ; Port 0 = V_{CC} ; all other pins are disconnected;

6) Overload conditions occur if the standard operating conditions are exceeded, ie. the voltage on any pin exceeds the specified range (i.e. V_{OV} > V_{CC} + 0.5 V or V_{OV} < V_{SS} - 0.5 V). The supply voltage V_{CC} and V_{SS} must remain within the specified limits. The absolute sum of input currents on all port pins may not exceed 50 mA.

7) Not 100% tested, guaranteed by design characterization.

8) The typical I_{CC} values are periodically measured at T_A = +25 °C but not 100% tested.

9) The maximum I_{CC} values are measured under worst case conditions (T_A = 0 °C and V_{CC} = 5.5 V)

AC Characteristics

V_{CC} = 4.0V to 5.5V (5V +10%, -20%); V_{SS} = 0 V T_A = 0 to 70 °C

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		10-MHz clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP = 2 MHz to 12 MHz **)		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	43	–	CLP - 40	–	ns
Address setup to ALE	t_{AVLL}	13	–	TCL_{Hmin} -20	–	ns
Address hold after ALE	t_{LLAX}	13	–	TCL_{Hmin} -20	–	ns
ALE to valid instruction in	t_{LLIV}	–	80	–	2 CLP - 87	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	13	–	TCL_{Lmin} -20	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	86	–	CLP+ TCL_{Hmin} -30	–	ns
$\overline{\text{PSEN}}$ to valid instruction in	t_{PLIV}	–	51	–	CLP+ TCL_{Hmin}- 65	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	23	–	TCL_{Lmin} -10	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	28	–	TCL_{Lmin} - 5	–	ns
Address to valid instruction in	t_{AVIV}	–	140	–	2 CLP + TCL_{Hmin} -60	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0		0	–	ns

*) Interfacing the C540U/C541U to devices with float times up to 28 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

**) For correct function of the USB module the C540U/C541U must operate with 12 MHz external clock. The microcontroller (except the USB module) operates down to 2 MHz.

AC Characteristics (cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		10-MHz clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP= 2 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	180	–	3 CLP - 70	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	180	–	3 CLP - 70	–	ns
Address hold after ALE	t_{LLAX2}	56	–	CLP - 27	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	110	–	2 CLP+ TCL_{Hmin} - 90	ns
Data hold after $\overline{RD}$	t_{RHDX}	0		0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	63	–	CLP - 20	ns
ALE to valid data in	t_{LLDV}	–	200	–	4 CLP - 133	ns
Address to valid data in	t_{AVDV}	–	211	–	4 CLP + TCL_{Hmin} -155	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	66	166	CLP + TCL_{Lmin} - 50	CLP+ TCL_{Lmin}+ 50	ns
Address valid to $\overline{WR}$	t_{AVWL}	70	–	2 CLP - 97	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	8	58	TCL_{Hmin} - 25	TCL_{Hmin} + 25	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	8	–	TCL_{Lmin} - 25	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	163	–	3 CLP + TCL_{Lmin} - 120	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	8	–	TCL_{Hmin} - 25	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

AC Characteristics (cont'd)

External Clock Drive Characteristics

Parameter	Symbol	CPU Clock = 12 MHz Duty cycle 0.4 to 0.6		Variable CPU Clock 1/CLP = 2 to 12 MHz		Unit
		min.	max.	min.	max.	
Oscillator period	CLP	83.3	83.3	83.3	500	ns
High time	TCL_H	33	–	33	$CLP-TCL_L$	ns
Low time	TCL_L	33	–	33	$CLP-TCL_H$	ns
Rise time	t_R	–	12	–	12	ns
Fall time	t_F	–	12	–	12	ns
Oscillator duty cycle	DC	0.4	0.6	33 / CLP	1 - 33 / CLP	–
Clock cycle	TCL	33	50	$CLP * DC_{min}$	$CLP * DC_{max}$	ns

SSC Interface Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock Cycle Time : Master Mode Slave Mode	t_{SCLK} t_{SCLK}	667 667	– –	ns ns
Clock high time	t_{SCH}	300	–	ns
Clock low time	t_{SCL}	300	–	ns
Data output delay	t_D	–	100	ns
Data output hold	t_{HO}	0	–	ns
Data input setup	t_S	100	–	ns
Data input hold	t_{HI}	50	–	ns
TC bit set delay	t_{DTC}	–	8 CLP	ns
$\overline{SLS}$ low to first SCLK clock edge	t_{SC}	2 t_{CLCL}	–	ns
Last SCLK clock edge to $\overline{SLS}$ high	t_{CS}	t_{CLCL}	–	ns
$\overline{SLS}$ low to STO active	t_{TS}	0	100	ns
$\overline{SLS}$ high to STO tristate	t_{ST}	–	100	ns
Data output delay (already defined)	t_D	–	100	ns

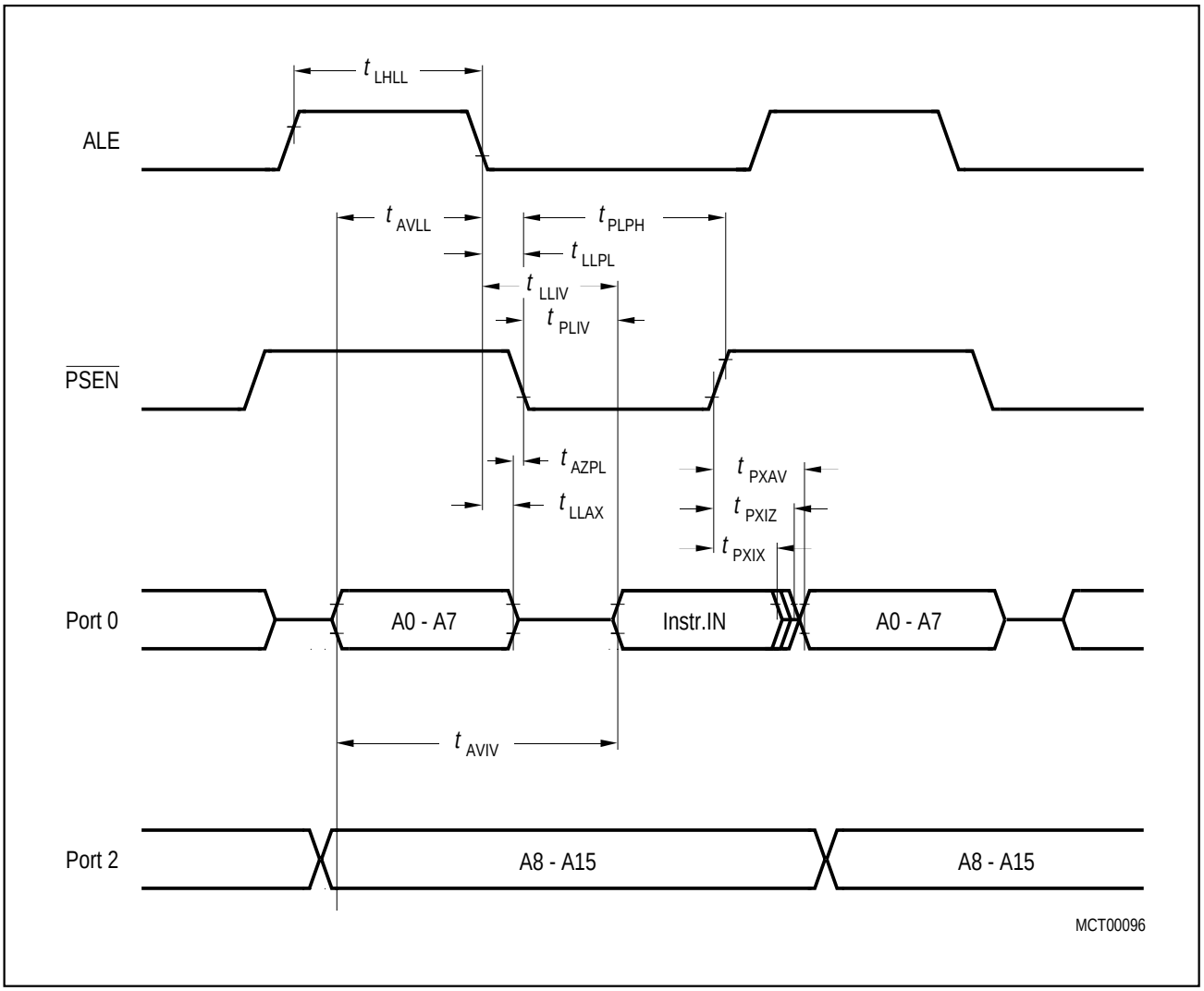


Figure 24
Program Memory Read Cycle

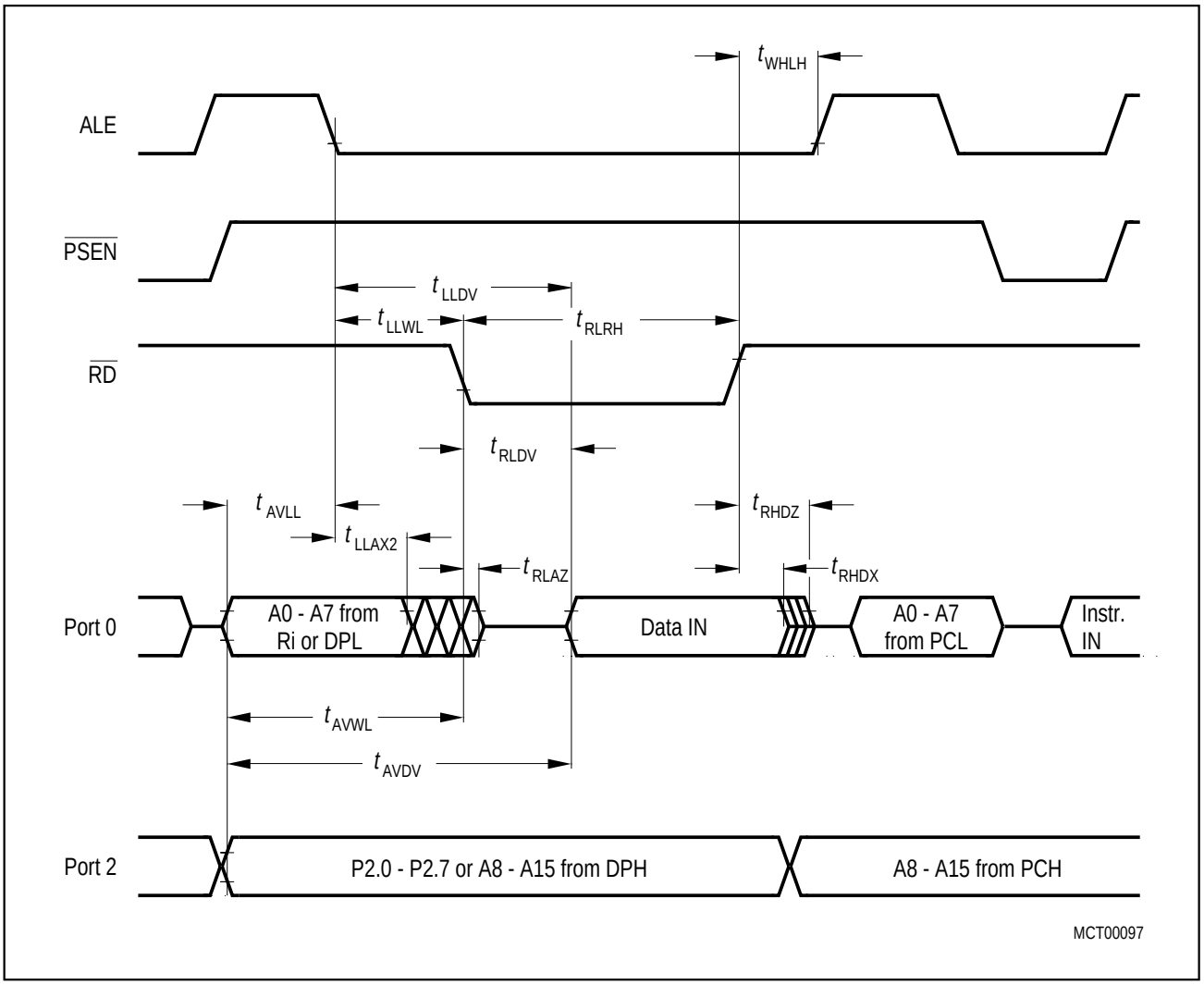


Figure 25
Data Memory Read Cycle

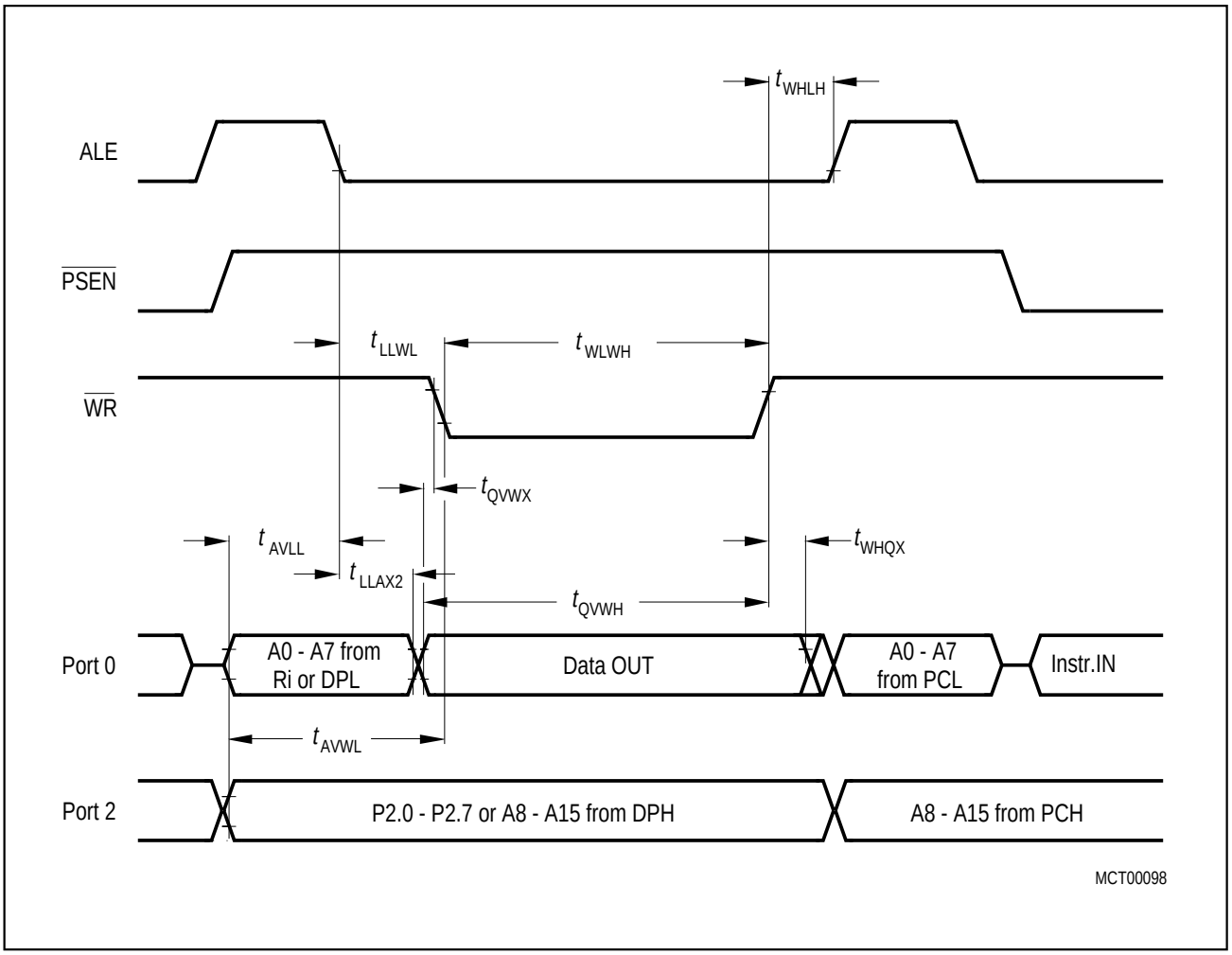


Figure 26
Data Memory Write Cycle

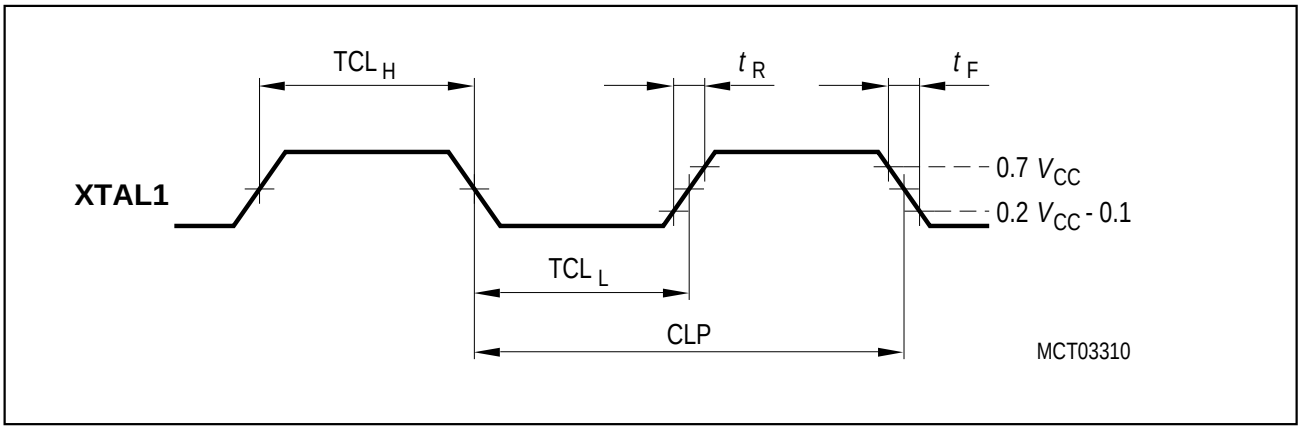
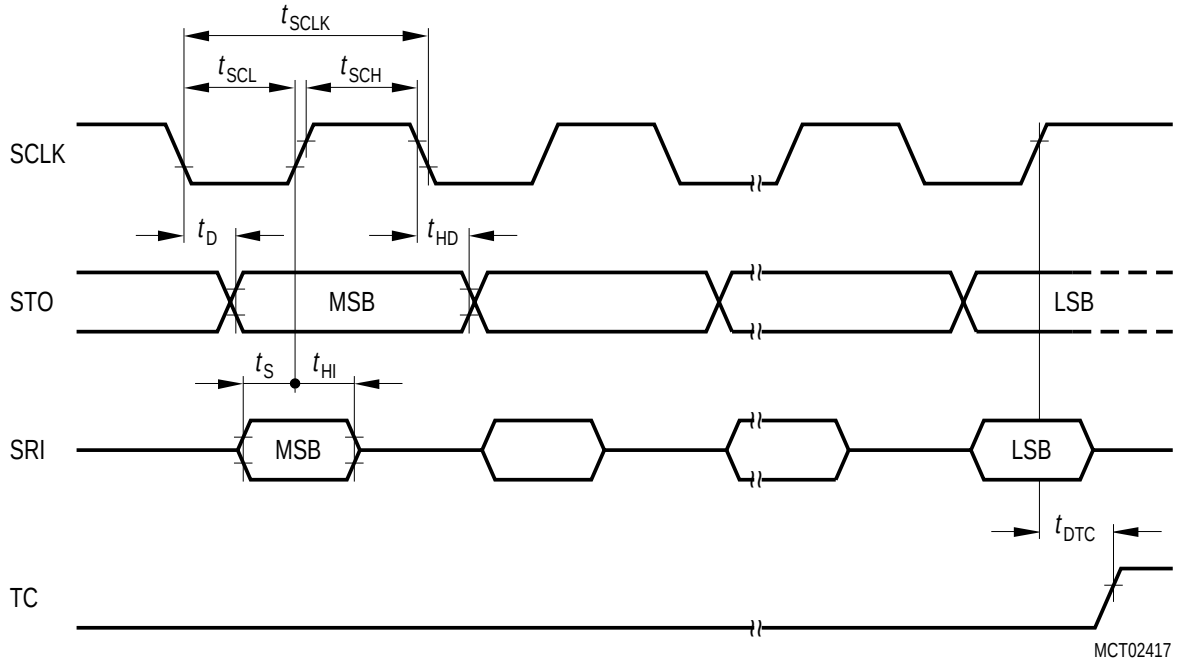


Figure 27
External Clock Drive on XTAL1



Notes : Shown is the data/clock relationship for CPOL=CPHA=1. The timing diagram is valid for the other cases accordingly.

In the case of slave mode and CPHA=0, the output delay for the MSB applies to the falling edge of $\overline{SLS}$ (if transmitter is enabled).

In the case of master mode and CPHA=0, the MSB becomes valid after the data has been written into the shift register, i.e. at least one half SCLK clock cycle before the first clock transition.

Figure 28
SSC Master Mode Timing

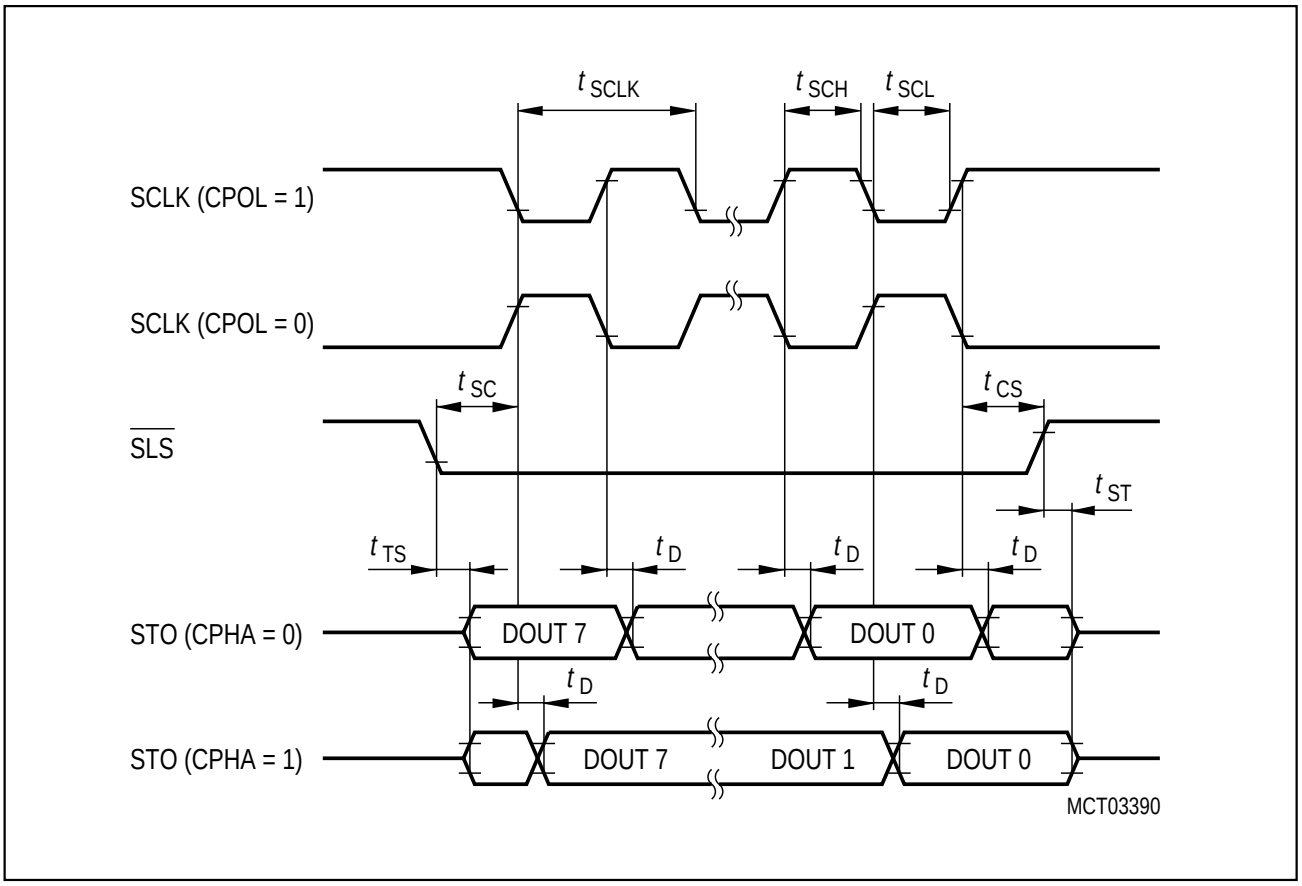


Figure 29
SSC Slave Mode Timing

AC Characteristics of Programming Mode

V_{CC} = 5 V ± 10 %; V_{PP} = 11.5 V ± 5 %; T_A = 25 °C ± 10 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{PAW}	35	–	ns
PMSEL setup to ALE rising edge	t_{PMS}	10	–	
Address setup to ALE, $\overline{PROG}$, or $\overline{PRD}$ falling edge	t_{PAS}	10	–	ns
Address hold after ALE, $\overline{PROG}$, or $\overline{PRD}$ falling edge	t_{PAH}	10	–	ns
Address, data setup to $\overline{PROG}$ or $\overline{PRD}$	t_{PCS}	100	–	ns
Address, data hold after $\overline{PROG}$ or $\overline{PRD}$	t_{PCH}	0	–	ns
PMSEL setup to $\overline{PROG}$ or $\overline{PRD}$	t_{PMS}	10	–	ns
PMSEL hold after $\overline{PROG}$ or $\overline{PRD}$	t_{PMH}	10	–	ns
$\overline{PROG}$ pulse width	t_{PWW}	100	–	µs
$\overline{PRD}$ pulse width	t_{PRW}	100	–	ns
Address to valid data out	t_{PAD}	–	75	ns
$\overline{PRD}$ to valid data out	t_{PRD}	–	20	ns
Data hold after $\overline{PRD}$	t_{PDH}	0	–	ns
Data float after $\overline{PRD}$	t_{PDF}	–	20	ns
$\overline{PROG}$ high between two consecutive $\overline{PROG}$ low pulses	t_{PWH1}	1	–	µs
$\overline{PRD}$ high between two consecutive $\overline{PRD}$ low pulses	t_{PWH2}	100		ns
XTAL clock period	t_{CLKP}	83.3	500	ns

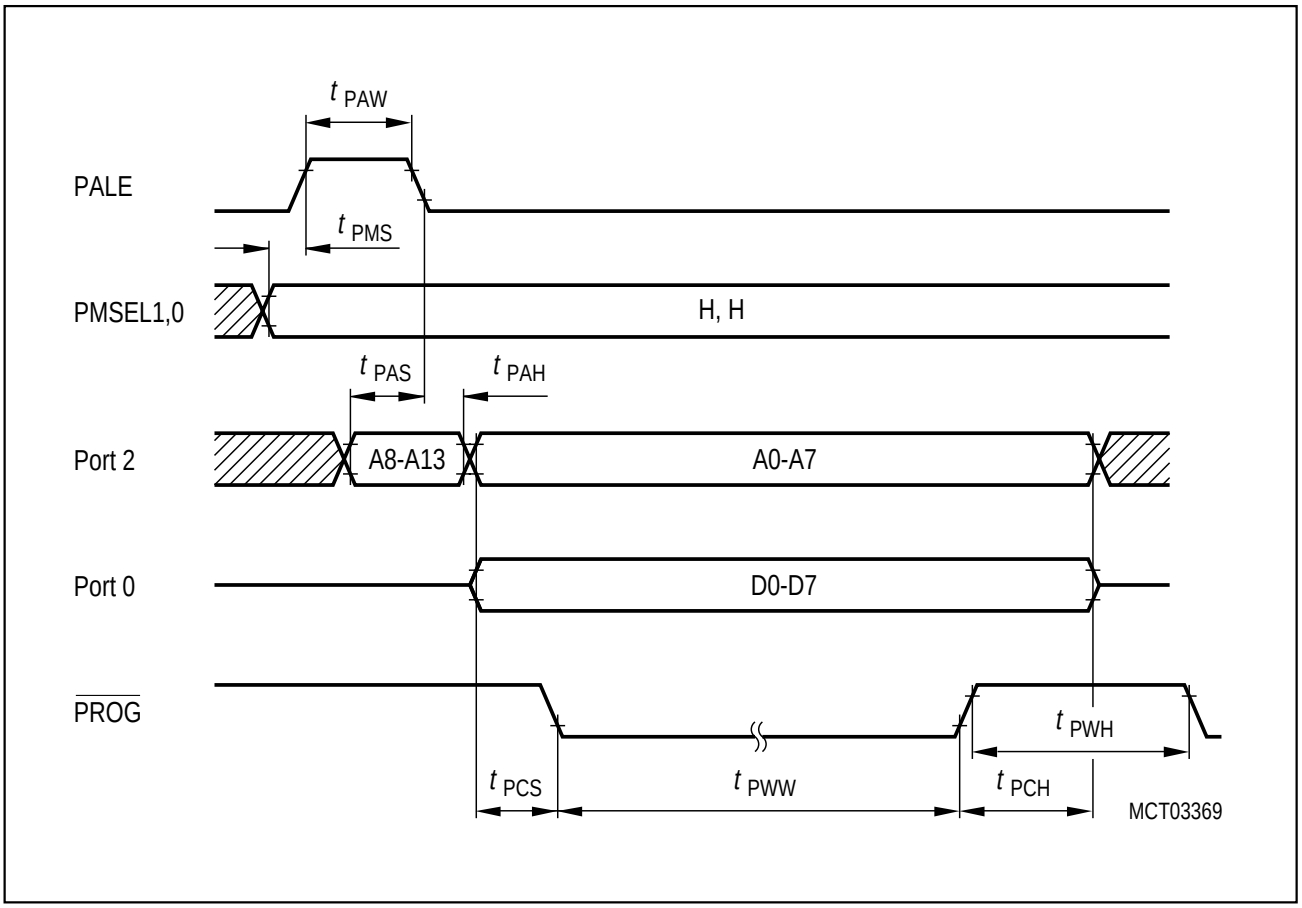


Figure 30
Programming Code Byte - Write Cycle Timing

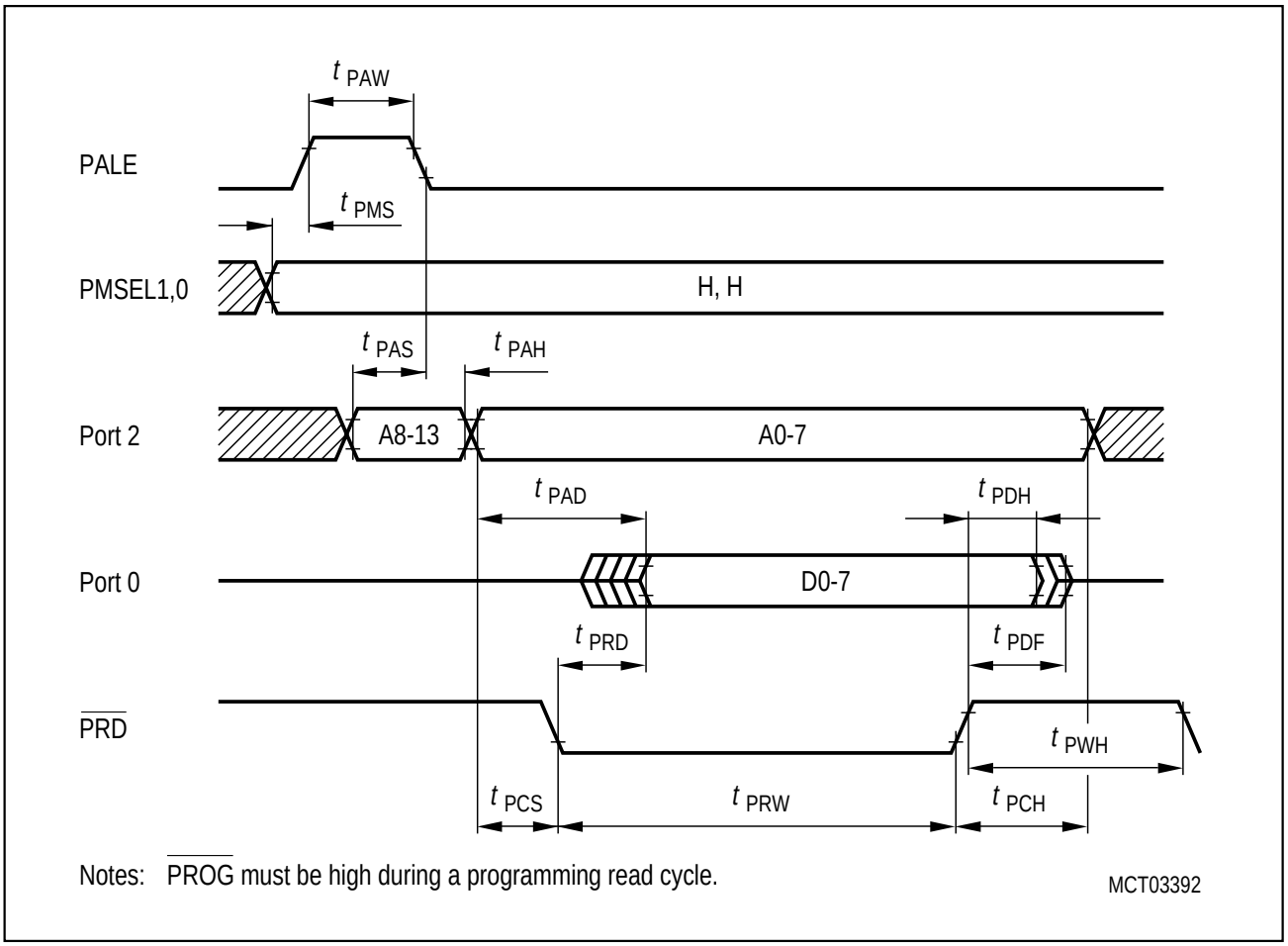


Figure 31
Verify Code Byte - Read Cycle Timing

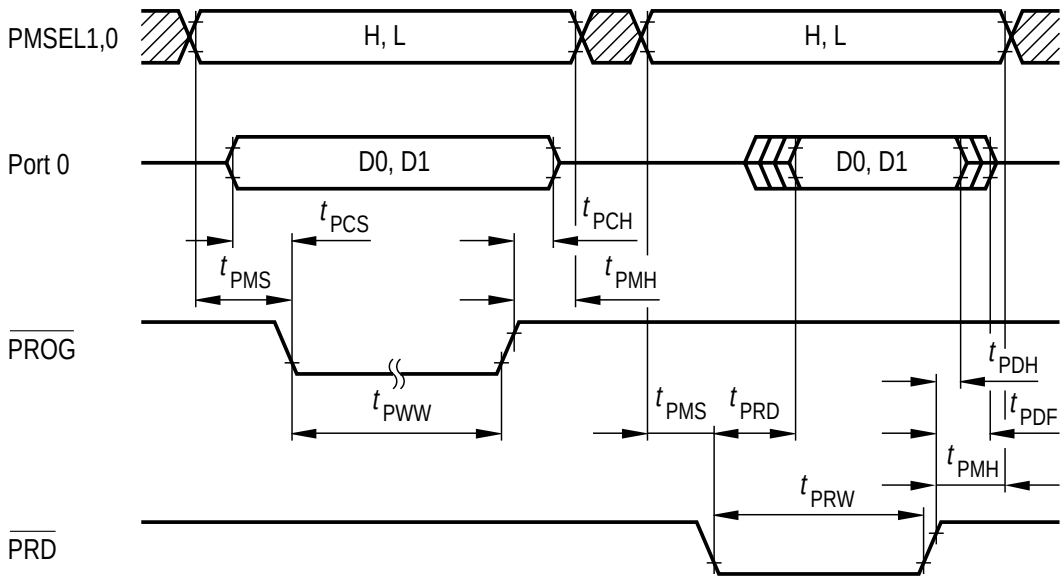


Figure 32
Lock Bit Access Timing

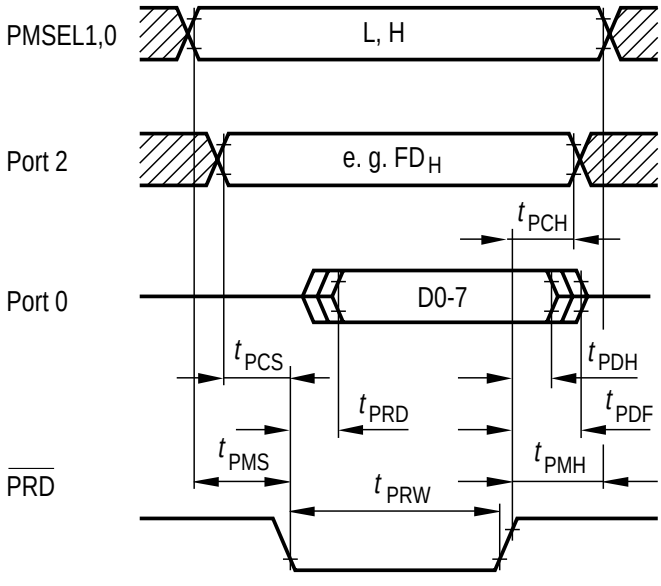


Figure 33
Version Byte Read Timing

OTP Verification Characteristics

OTP Verification Mode for Protection Level 1

Parameter	Symbol	Limit Values			Unit
		min.	typ	max.	
ALE pulse width	t_{AWD}	–	2 t_{CLCL}	–	ns
ALE period	t_{ACY}	–	12 t_{CLCL}	–	ns
Data valid after ALE	t_{DVA}	–	–	4 t_{CLCL}	ns
Data stable after ALE	t_{DSA}	8 t_{CLCL}	–	–	ns
P3.5 setup to ALE low	t_{AS}	–	t_{CLCL}	–	ns
Oscillator frequency	$1/t_{CLCL}$	4	–	6	MHz

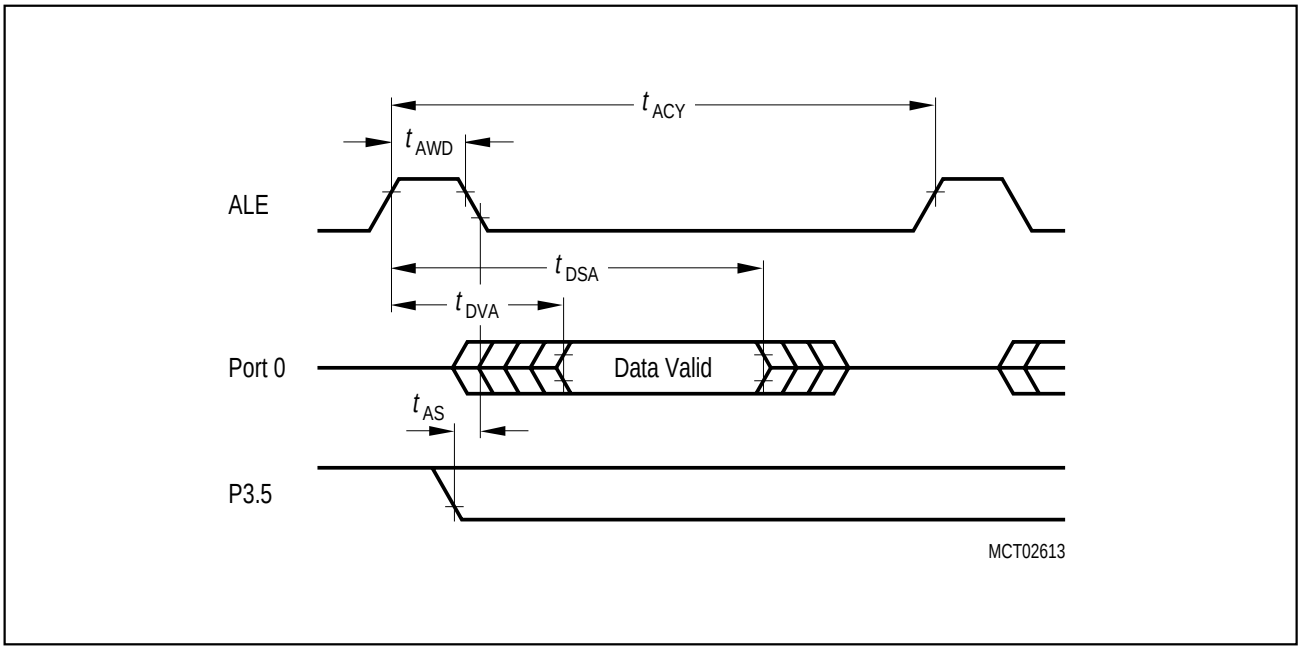


Figure 34
OTP Verification Mode for Protection Level 1

USB Transceiver Characteristics

V_{CC} = 4.0V to 5.5V (5V +10%, -20%); V_{SS} = 0 V T_A = 0 to 70 °C

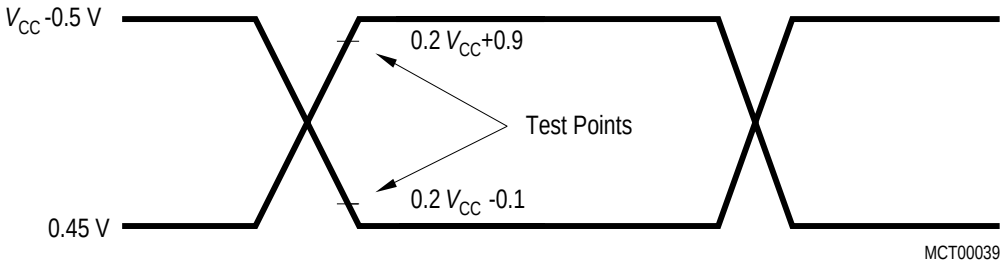
Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Output impedance (high state)	R_{DH}	28	43	Ω	1)
Output impedance (low state)	R_{DL}	28	51	Ω	
Input leakage current	I_I	–	± 5	µA	V_{IN} = V_{SS} or V_{CC}
Tristate output off-state current	I_{OZ}	–	± 10	µA	V_{OUT} = V_{SS} or V_{CC} 1)
Crossover point	V_{CR}	1.3	2.0	V	2)

Notes :

1) This value includes an external resistor of 30Ω ± 1% (see “Load for D+/D-“ diagram for testing details)

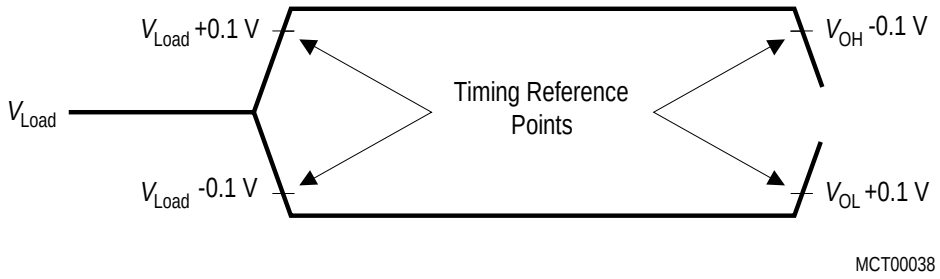
2) The crossover point is in the range of 1.3V to 2.0V for the high speed mode with a 50pF capacitance. In the low-speed mode with a 100pF or greater capacitance, the crossover point is in the range of 1.3V to 2.0V.

Parameter	Symbol	Limit Values		Unit
		min.	max.	
High speed mode rise time	t_{FR}	4	20	ns
High speed mode fall time	t_{FF}	4	20	ns
Low speed mode rise time	t_{LR}	75	300	ns
Low speed mode fall time	t_{LF}	75	300	ns



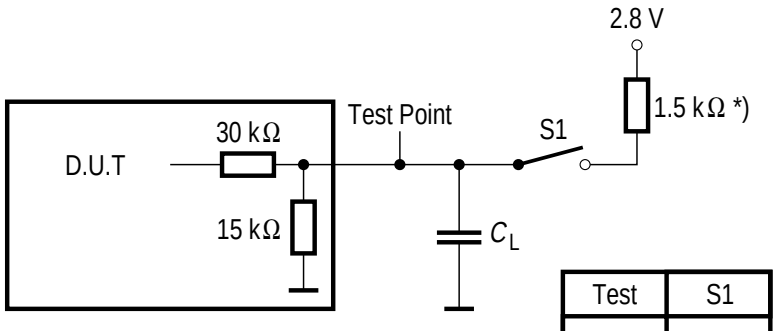
AC Inputs during testing are driven at V_{CC} - 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Figure 35
AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm$ 20 mA

Figure 36
AC Testing : Float Waveforms



Test	S1
D- / LS	Close
D+ / LS	Open
D- / FS	Open
D+ / FS	Close

Figure 37
Load for D+/D-

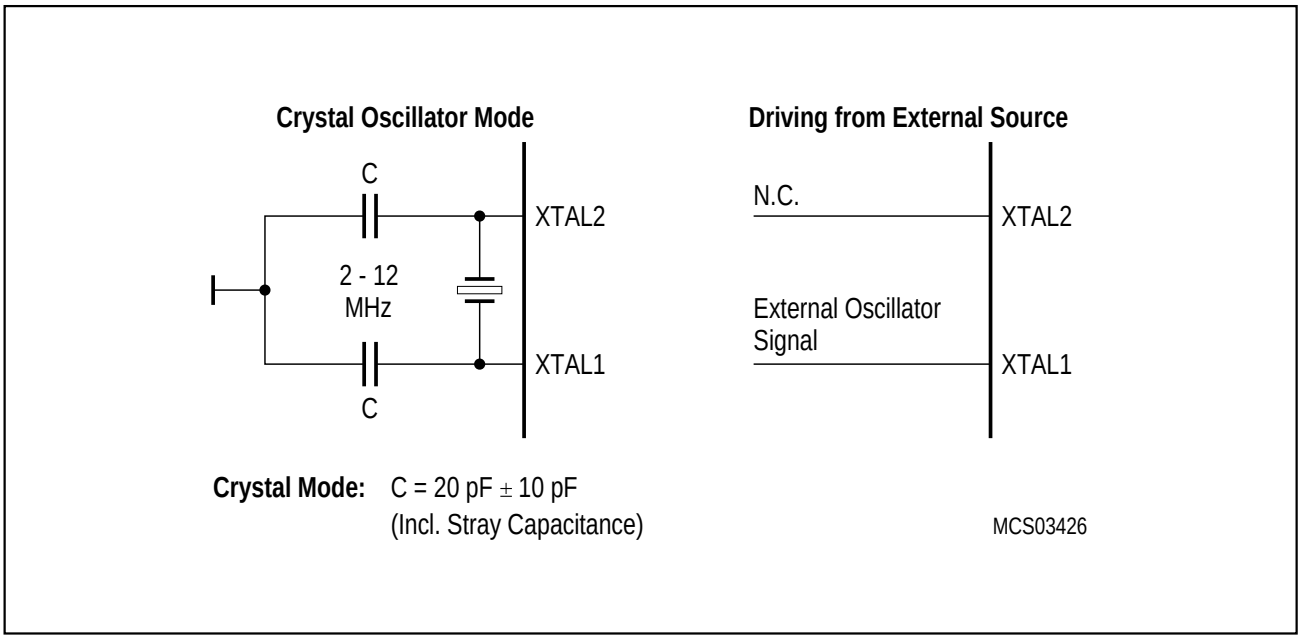


Figure 38
Recommended Oscillator Circuits for Crystal Oscillator

Plastic Package, P-LCC-44-1 (SMD)
(Plastic Leaded Chip Carrier Package)

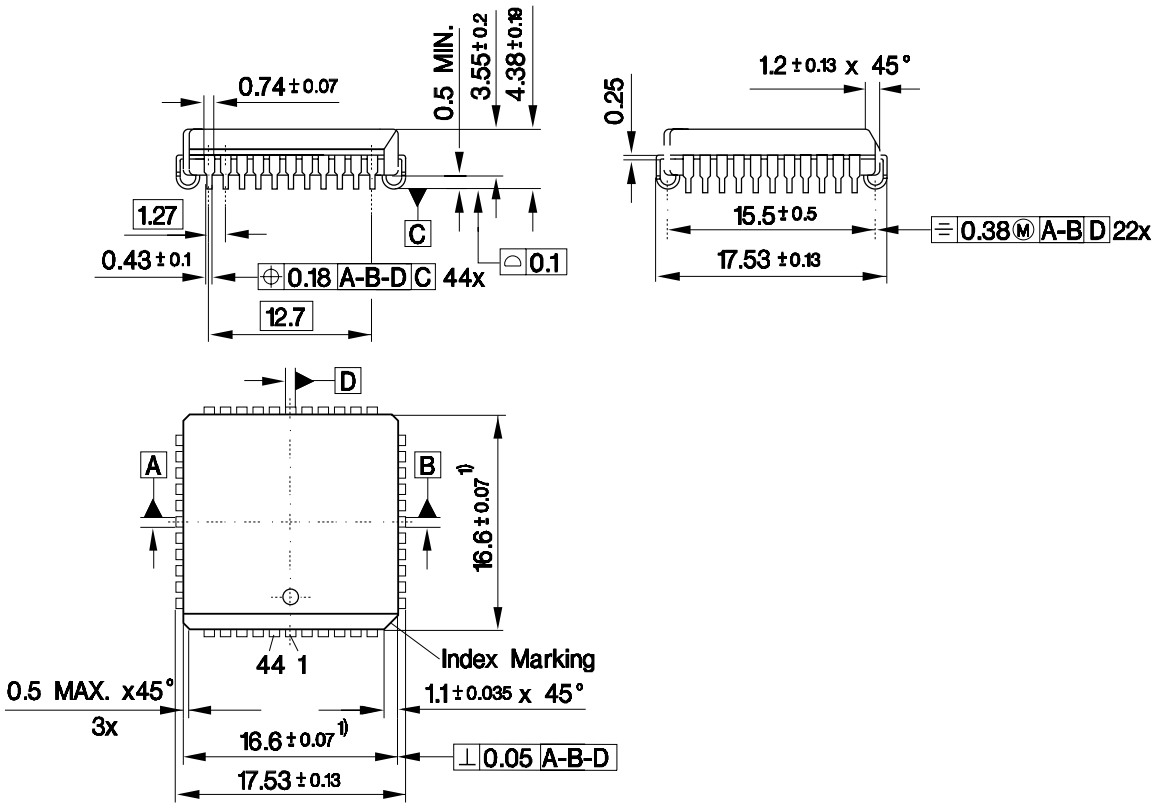


Figure 39
P-LCC-44-1 Package Outline

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”
SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, P-SDIP-52-1
(Plastic Shrink Dual In-Line Package)

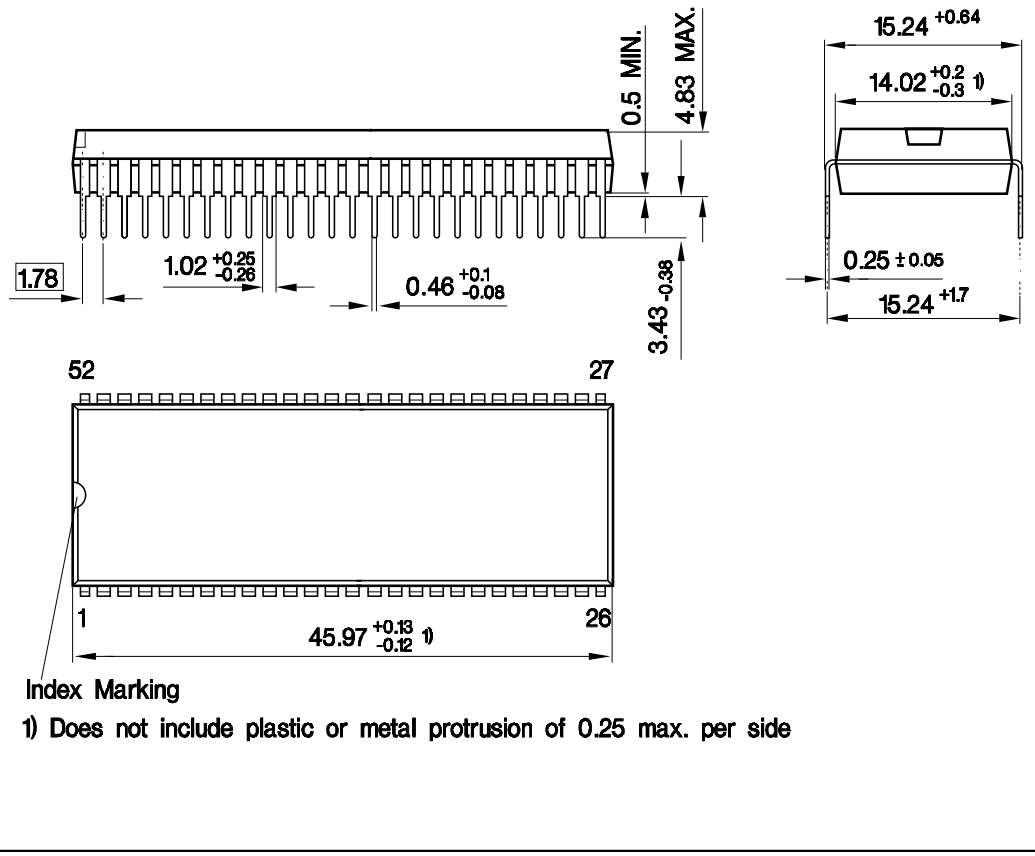


Figure 40
P-SDIP-52-1 Package Outline

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

Dimensions in mm