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February 1996

## NDS9956A

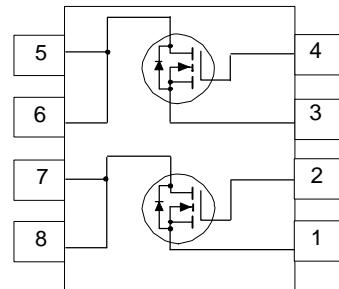
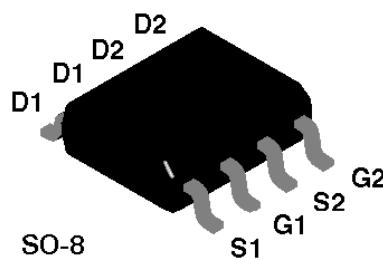
### Dual N-Channel Enhancement Mode Field Effect Transistor

#### General Description

These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as DC/DC conversion and DC motor control where fast switching, low in-line power loss, and resistance to transients are needed.

#### Features

- 3.7A, 30V.  $R_{DS(ON)} = 0.08\Omega$  @  $V_{GS} = 10V$
- High density cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.



#### Absolute Maximum Ratings

$T_A = 25^\circ C$  unless otherwise noted

Symbol	Parameter	NDS9956A	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous - Pulsed	$\pm 3.7$	A
		$\pm 15$	
$P_D$	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a) (Note 1b)	1.6	
		1	
	(Note 1c)	0.9	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

NDS9956A.SAM

Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise noted)						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}} = 0 \text{ V}, I_{\text{D}} = 250 \mu\text{A}$	30			V
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{\text{DS}} = 24 \text{ V}, V_{\text{GS}} = 0 \text{ V}$		2		$\mu\text{A}$
		$T_J = 55^\circ\text{C}$		25		$\mu\text{A}$
$I_{\text{GSSF}}$	Gate - Body Leakage, Forward	$V_{\text{GS}} = 20 \text{ V}, V_{\text{DS}} = 0 \text{ V}$			100	nA
$I_{\text{GSSR}}$	Gate - Body Leakage, Reverse	$V_{\text{GS}} = -20 \text{ V}, V_{\text{DS}} = 0 \text{ V}$			-100	nA
<b>ON CHARACTERISTICS</b> (Note 2)						
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}, I_{\text{D}} = 250 \mu\text{A}$	1	1.7	2.8	V
		$T_J = 125^\circ\text{C}$	0.7	1.2	2.2	
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance	$V_{\text{GS}} = 10 \text{ V}, I_{\text{D}} = 2.2 \text{ A}$		0.06	0.08	$\Omega$
		$T_J = 125^\circ\text{C}$		0.08	0.13	
		$V_{\text{GS}} = 4.5 \text{ V}, I_{\text{D}} = 1.0 \text{ A}$		0.08	0.11	
		$T_J = 125^\circ\text{C}$		0.11	0.18	
$I_{\text{D(on)}}$	On-State Drain Current	$V_{\text{GS}} = 10 \text{ V}, V_{\text{DS}} = 10 \text{ V}$	15			A
		$V_{\text{GS}} = 4.5 \text{ V}, V_{\text{DS}} = 10 \text{ V}$	3.5			
$g_{\text{FS}}$	Forward Transconductance	$V_{\text{DS}} = 15 \text{ V}, I_{\text{D}} = 3.7 \text{ A}$		6		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{\text{iss}}$	Input Capacitance	$V_{\text{DS}} = 10 \text{ V}, V_{\text{GS}} = 0 \text{ V}, f = 1.0 \text{ MHz}$		320		pF
$C_{\text{oss}}$	Output Capacitance			225		pF
$C_{\text{rss}}$	Reverse Transfer Capacitance			85		pF
<b>SWITCHING CHARACTERISTICS</b> (Note 2)						
$t_{\text{D(on)}}$	Turn - On Delay Time	$V_{\text{DD}} = 10 \text{ V}, I_{\text{D}} = 1 \text{ A}, V_{\text{GEN}} = 10 \text{ V}, R_{\text{GEN}} = 6 \Omega$		10	20	ns
$t_r$	Turn - On Rise Time			13	20	ns
$t_{\text{D(off)}}$	Turn - Off Delay Time			21	50	ns
$t_f$	Turn - Off Fall Time			5	50	ns
$Q_g$	Total Gate Charge	$V_{\text{DS}} = 10 \text{ V}, I_{\text{D}} = 3.7 \text{ A}, V_{\text{GS}} = 10 \text{ V}$		9.5	27	nC
$Q_{\text{gs}}$	Gate-Source Charge			1.5		nC
$Q_{\text{gd}}$	Gate-Drain Charge			3.3		nC

**Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				1.2	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}$ , $I_S = 1.25 \text{ A}$ (Note 2)		0.8	1.3	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0 \text{ V}$ , $I_F = 1.25 \text{ A}$ , $dI_F/dt = 100 \text{ A}/\mu\text{s}$			100	ns

Notes:

1.  $R_{\text{JJC}}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\text{JJC}}$  is guaranteed by design while  $R_{\text{BCA}}$  is determined by the user's board design.

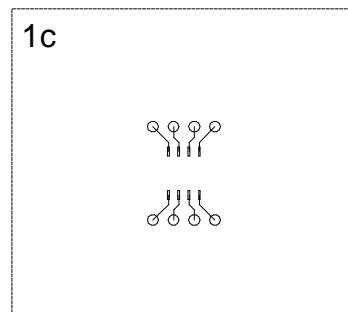
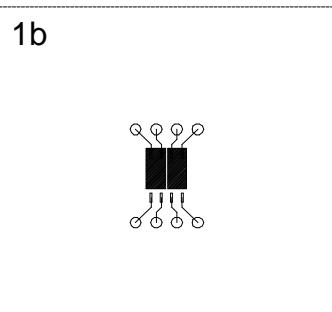
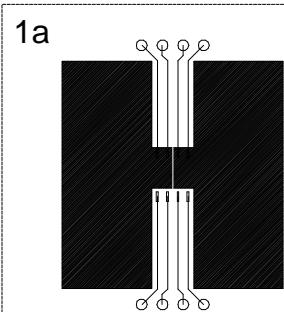
$$P_D(t) = \frac{T_J - T_A}{R_{\text{JJC}}(t)} = \frac{T_J - T_A}{R_{\text{JJC}} + R_{\text{BCA}}(t)} = I_D^2(t) \times R_{\text{DS(on)}} @ T_J$$

Typical  $R_{\text{JJC}}$  for single device operation using the board layouts shown below on 4.5" x 5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in<sup>2</sup> pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in<sup>2</sup> pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in<sup>2</sup> pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## Typical Electrical Characteristics

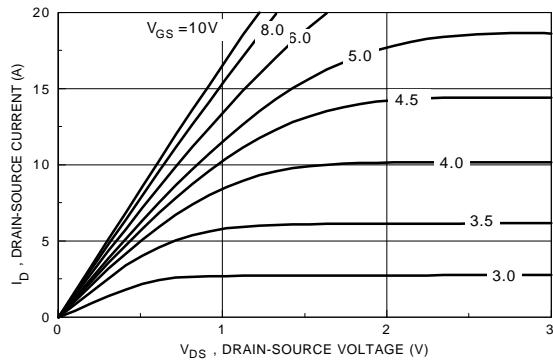


Figure 1. On-Region Characteristics.

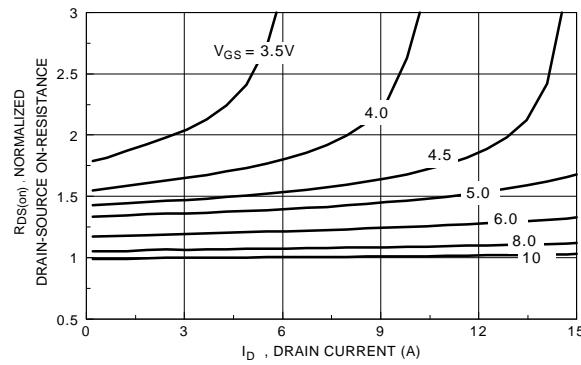


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

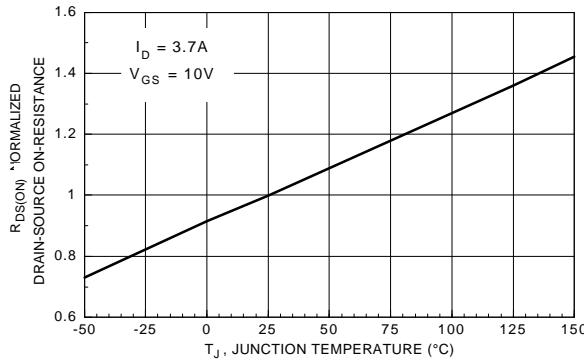


Figure 3. On-Resistance Variation with Temperature.

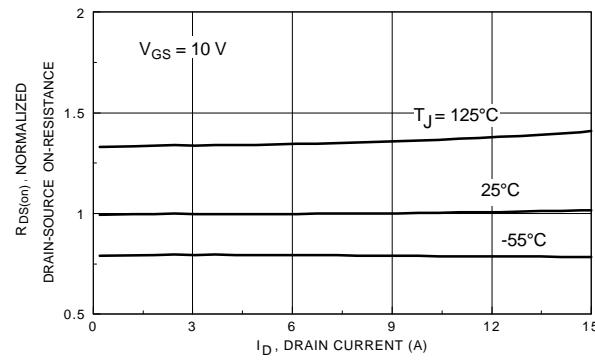


Figure 4. On-Resistance Variation with Drain Current and Temperature.

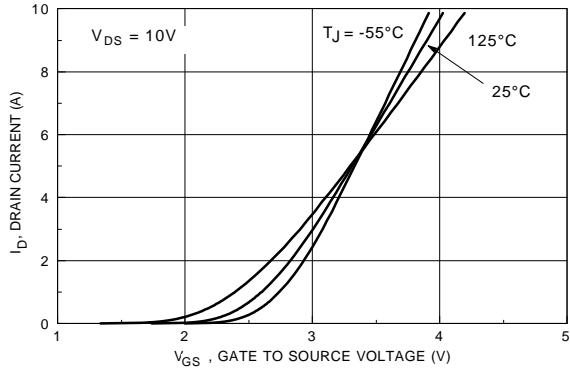


Figure 5. Transfer Characteristics.

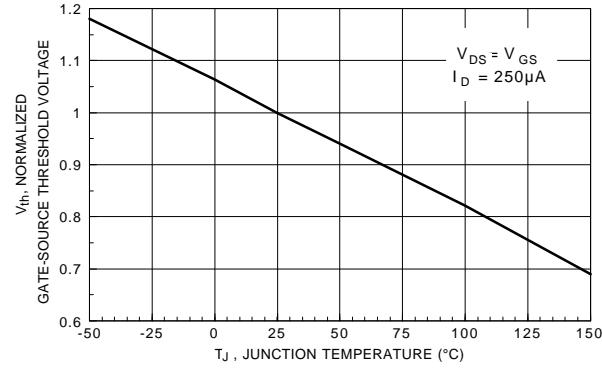
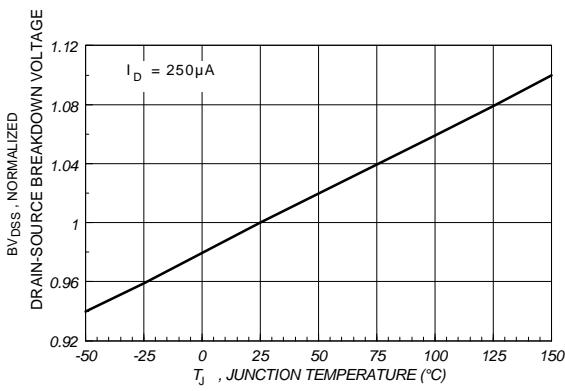
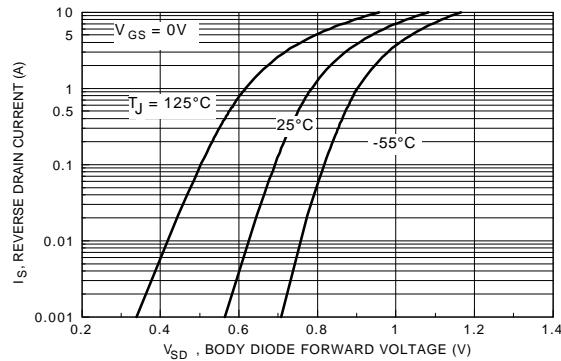


Figure 6. Gate Threshold Variation with Temperature.

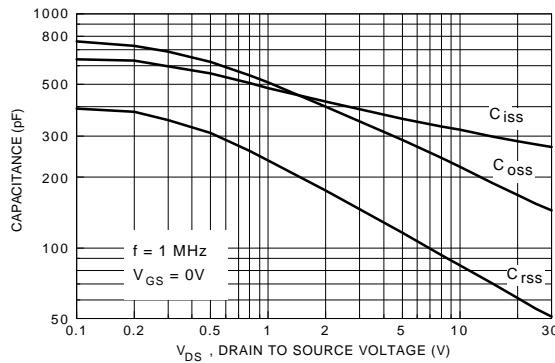
## Typical Electrical Characteristics



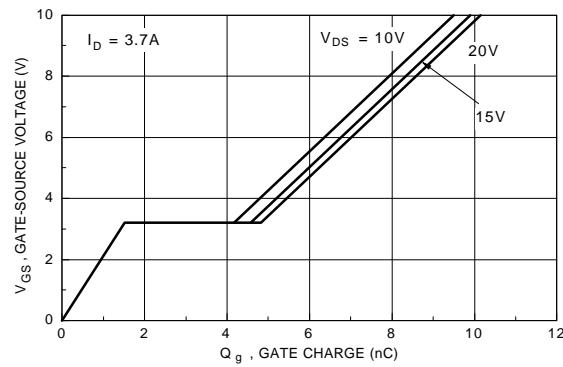
**Figure 7. Breakdown Voltage Variation with Temperature.**



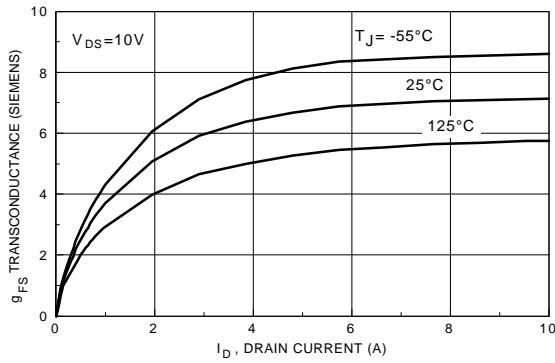
**Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.**



**Figure 9. Capacitance Characteristics.**

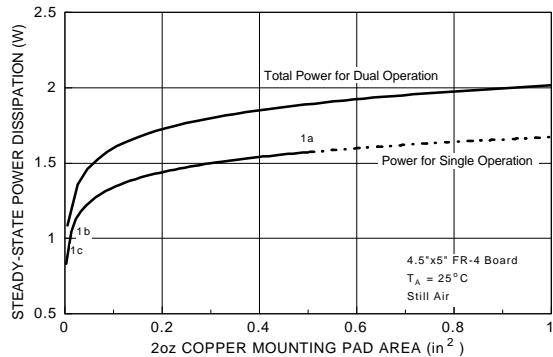


**Figure 10. Gate Charge Characteristics.**

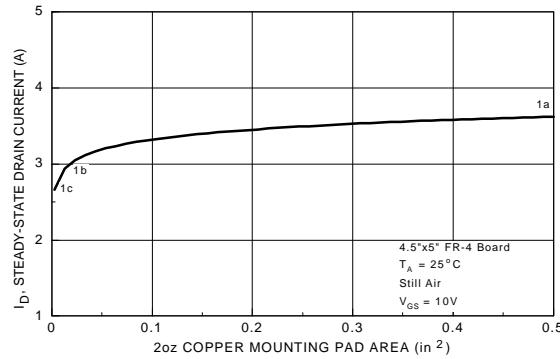


**Figure 11. Transconductance Variation with Drain Current and Temperature.**

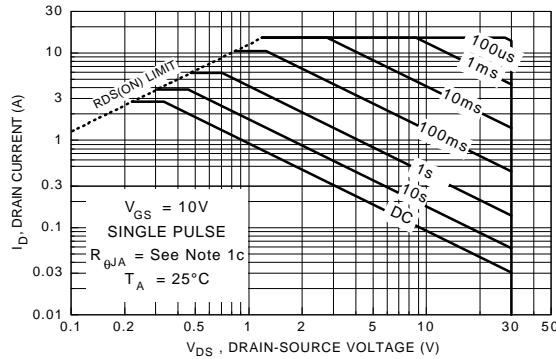
## Typical Thermal Characteristics



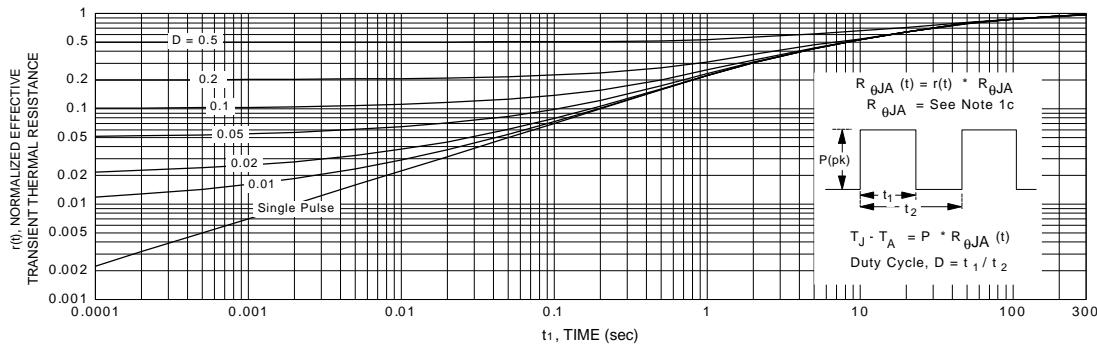
**Figure 12. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.**



**Figure 13. Maximum Steady- State Drain Current versus Copper Mounting Pad Area.**



**Figure 14. Maximum Safe Operating Area.**



**Figure 15. Transient Thermal Response Curve.**

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.