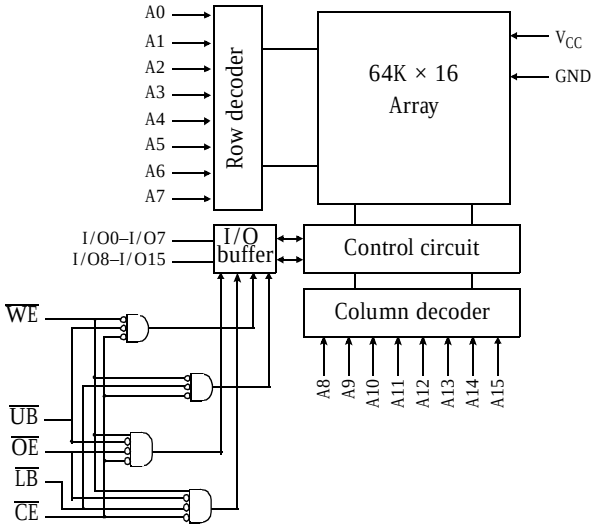
5V/3.3V 64K×16 CMOS SRAM

Features

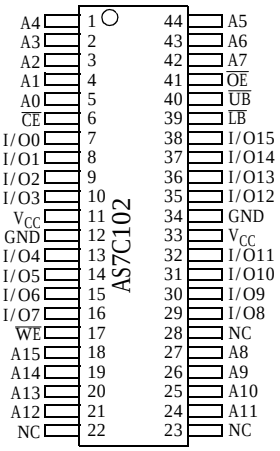
- AS7C1026 (5V version)
- AS7C31026 (3.3V version)
- Industrial and commercial versions
- Organization: 65,536 words x 16 bits
- Center power and ground pins for low noise
- High speed
  - 10/12/15/20 ns address access time
  - 5/6/8/10 ns output enable access time
- Low power consumption: ACTIVE
  - 880 mW (AS7C1026) / max @ 12 ns
  - 396 mW (AS7C31026) / max @ 12 ns
- Low power consumption: STANDBY
  - 28 mW (AS7C1026) / max CMOS I/O
  - 18 mW (AS7C31026) / max CMOS I/O
- 2.0V data retention
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
- JEDEC standard packaging
  - 44-pin 400 mil SOJ
  - 44-pin 400 mil TSOP II
  - 48-ball 6 mm × 8 mm CSP mBGA
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram



Pin arrangement

44-Pin SOJ, TSOP II (400 mil)



48-CSP mini Ball-Grid-Array Package

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	NC
B	I/O8	$\overline{UB}$	A3	A4	$\overline{CE}$	I/O0
C	I/O9	I/O10	A5	A6	I/O1	I/O2
D	V_{SS}	I/O11	NC	A7	I/O3	V_{DD}
E	V_{DD}	I/O12	NC	NC	I/O4	V_{SS}
F	I/O14	I/O13	A14	A15	I/O5	I/O6
G	I/O15	NC	A12	A13	$\overline{WE}$	I/O7
H	NC	A8	A9	A10	A11	NC

Selection guide

		AS7C31026-10	AS7C1026-12 AS7C31026-12	AS7C1026-15 AS7C31026-15	AS7C1026-20 AS7C31026-20	Unit
Maximum address access time		10	12	15	20	ns
Maximum output enable access time		5	6	8	10	ns
Maximum operating current	AS7C1026	–	160	150	140	mA
	AS7C31026	125	110	100	90	mA
Maximum CMOS standby current	AS7C1026	–	3	3	3	mA
	AS7C31026	3	3	3	3	mA

Shaded areas indicate preliminary information.

Functional description

The AS7C1026 and AS7C31026 are high-performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) devices organized as 65,536 words x 16 bits. They are designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 5/6/8/10 ns are ideal for high-performance applications.

When $\overline{CE}$ is high the devices enter stanby mode. The AS7C1026 is guaranteed not to exceed 28 mW power consumption in CMOS standby mode. The devices also offer 2.0V data retention.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O0–I/O15 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and chip enable ($\overline{CE}$), with write enable ($\overline{WE}$) high. the chips drive I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

The devices provide multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. $\overline{LB}$ controls the lower bits, I/O0–I/O7, and $\overline{UB}$ controls the higher bits, I/O8–I/O15.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5V supply (AS7C1026) or 3.3V supply (AS7C31026). the device is packaged in common industry standard packages. Chip scale BGA packaging, easy to use in manufacturing, provides the smallest possible footprint. This 48-ball JEDEC-registered package has a ball pitch of 0.75 mm and external dimensions of 8 mm × 6 mm.

Absolute maximum ratings

Parameter		Symbol	Min	Max	Unit
Voltage on V_{CC} relative to GND	AS7C1026	V_{t1}	–0.50	+7.0	V
	AS7C31026	V_{t1}	–0.50	+5.0	V
Voltage on any pin relative to GND		V_{t2}	–0.50	V_{CC} +0.50	V
Power dissipation		P_D	–	1.0	W
Storage temperature (plastic)		T_{stg}	–65	+150	°C
Ambient temperature with VCC applied		T_{bias}	–55	+125	°C
DC current into outputs (low)		I_{OUT}	–	20	mA

Note: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O0–I/O7	I/O8–I/O15	Mode
H	X	X	X	X	High Z	High Z	Standby (I_{SB}), I_{SBI})
L	H	L	L	H	D_{OUT}	High Z	Read I/O0–I/O7 (I_{CC})
L	H	L	H	L	High Z	D_{OUT}	Read I/O8–I/O15 (I_{CC})
L	H	L	L	L	D_{OUT}	D_{OUT}	Read I/O0–I/O15 (I_{CC})
L	L	X	L	L	D_{IN}	D_{IN}	Write I/O0–I/O15 (I_{CC})
L	L	X	L	H	D_{IN}	High Z	Write I/O0–I/O7 (I_{CC})

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O0–I/O7	I/O8–I/O15	Mode
L	L	X	H	L	High Z	D_{IN}	Write I/O8–I/O15 (I_{CC})
L L	H X	H X	X H	X H	High Z	High Z	Output disable (I_{CC})

Key: H = High, L = Low, X = don't care.

Recommended operating conditions

Parameter		Device	Symbol	Min	Typ	Max	Unit
Supply voltage		AS7C1026	V_{CC}	4.5	5.0	5.5	V
		AS7C31026 (–10)	V_{CC}	3.15	3.3	3.6	V
		AS7C31026 (12/15/20)	V_{CC}	3.0	3.3	3.6	V
Input voltage		AS7C1026	V_{IH}	2.2	–	V_{CC} + 0.5	V
		AS7C31026	V_{IH}	2.0	–	V_{CC} + 0.5	V
			V_{IL}	–0.5†	–	0.8	V
Ambient operating temperature	commercial		T_A	0	–	70	°C
	industrial		T_A	–40	–	85	°C

† V_{IL} min = –3.0V for pulse width less than $t_{RC}/2$.

DC operating characteristics (over the operating range)

Parameter	Sym	Test conditions	Device	-10		-12		-15		-20		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current	$\lvert I_{LI} \rvert$	V_{CC} = Max V_{IN} = GND to V_{CC}		–	1	–	1	–	1	–	1	µA
Output leakage current	$\lvert I_{LO} \rvert$	V_{CC} = Max $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		–	1	–	1	–	1	–	1	µA
Operating power supply current	I_{CC}	V_{CC} = Max, $\overline{CE} \le V_{IL}$ outputs open, f = f_{Max} = $1/t_{RC}$	AS7C1026	–	–	–	160	–	150	–	140	mA
			AS7C31026	–	125	–	110	–	100	–	90	mA
Standby power supply current	I_{SB}	V_{CC} = Max, $\overline{CE} \le V_{IL}$, outputs open, f = f_{Max} = $1/t_{RC}$	AS7C1026	–	–	–	40	–	40	–	40	mA
			AS7C31026	–	25	–	25	–	25	–	25	
	I_{SB1}	V_{CC} = Max, $\overline{CE} \ge V_{CC}$–0.2V, $V_{IN} \le$ GND + 0.2V or $V_{IN} \ge V_{CC}$–0.2V, f = 0	AS7C1026	–	–	–	10	–	10	–	10	mA
			AS7C31026	–	10	–	10	–	10	–	10	
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min		–	0.4	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min		2.4	–	2.4	–	2.4	–	2.4	–	V

Shaded areas indicate preliminary information.

Capacitance (f = 1MHz, T_a = 25 °C, V_{CC} = NOMINAL)

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$, $\overline{LB}$, $\overline{UB}$	V_{IN} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{IN} = V_{OUT} = 0V	7	pF

Read cycle (over the operating range)

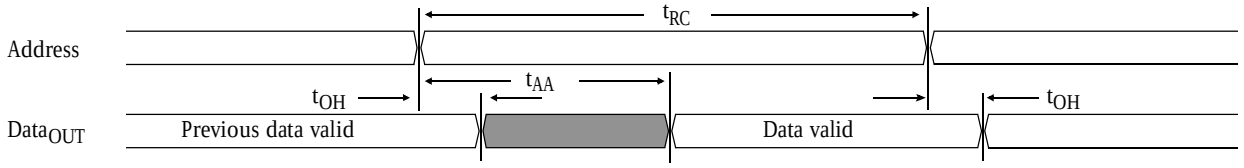
Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	10	–	12	–	15	–	20	–	ns	
Address access time	t_{AA}	–	10	–	12	–	15	–	20	ns	3
Chip enable ($\overline{CE}$) access time	t_{ACE}	–	10	–	12	–	15	–	20	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}	–	5	–	5	–	8	–	10	ns	
Output hold from address change	t_{OH}	4	–	4	–	4	–	4	–	ns	5
$\overline{CE}$ Low to output in low Z	t_{CLZ}	0	–	0	–	0	–	0	–	ns	4, 5
$\overline{CE}$ High to output in high Z	t_{CHZ}	–	6	–	6	–	6	–	8	ns	4, 5
$\overline{OE}$ Low to output in low Z	t_{OLZ}	0	–	0	–	0	–	0	–	ns	4, 5
Byte select access time	t_{BA}	–	5	–	6	–	8	–	10	ns	
Byte select Low to low Z	t_{BLZ}	0	–	0	–	0	–	0	–	ns	4,5
Byte select High to high Z	t_{BHZ}	–	5	–	6	–	6	–	8	ns	4,5
$\overline{OE}$ High to output in high Z	t_{OHZ}	–	5	–	6	–	6	–	8	ns	4, 5
Power up time	t_{PU}	0	–	0	–	0	–	0	–	ns	4, 5
Power down time	t_{PD}	–	10	–	12	–	15	–	20	ns	4, 5

Shaded areas indicate preliminary information.

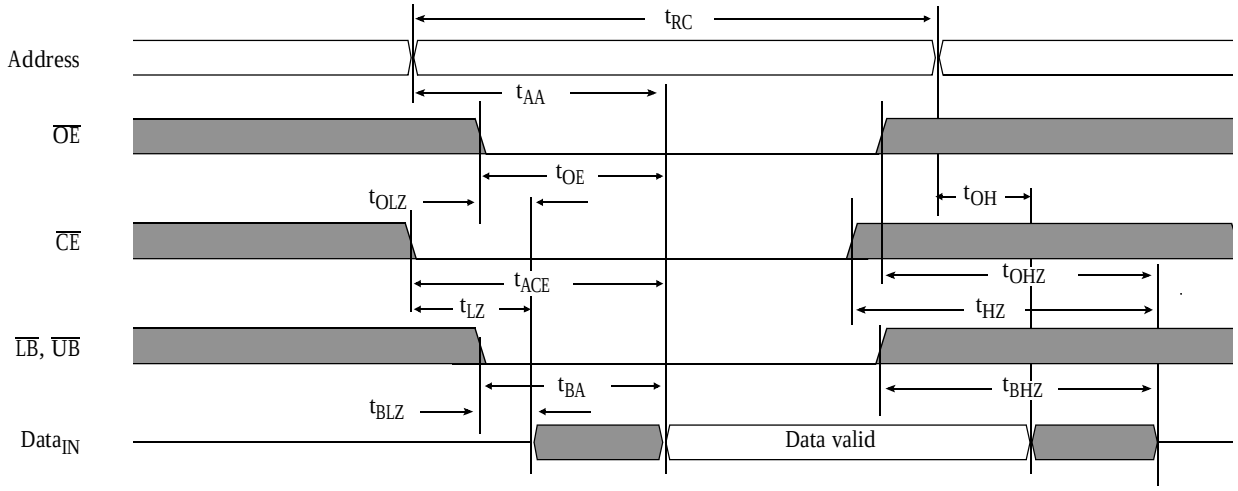
Key to switching waveforms

Rising input Falling input Undefined output/don't care

Read waveform 1 (address controlled)



Read waveform 2 ($\overline{OE}$, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ controlled)

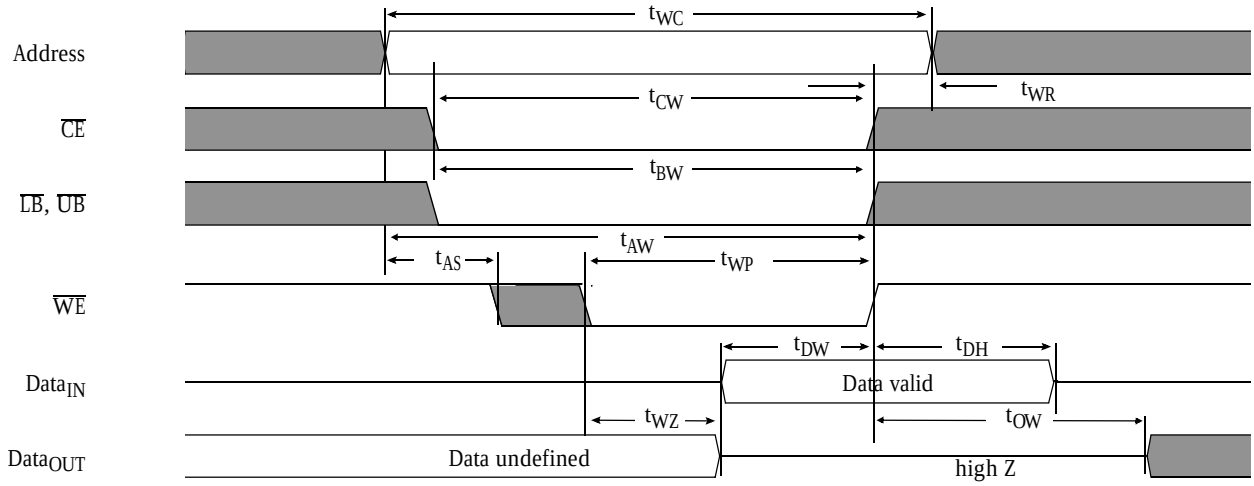


Write cycle (over the operating range)

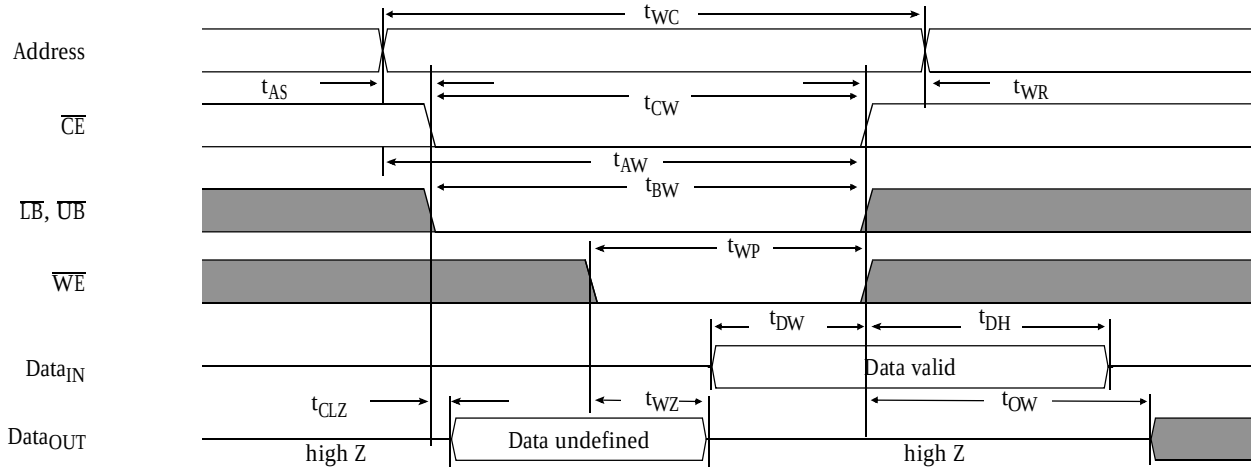
Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	10	–	12	–	15	–	20	–	ns	
Chip enable ($\overline{CE}$) to write end	t_{CW}	8	–	8	–	12	–	13	–	ns	
Address setup to write end	t_{AW}	8	–	9	–	10	–	12	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	ns	
Write pulse width	t_{WP}	8	–	8	–	10	–	12	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	5	–	6	–	8	–	10	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	0	–	ns	5
Write enable to output in high Z	t_{WZ}	–	6	–	6	–	6	–	8	ns	4, 5
Output active from write end	t_{OW}	1	–	1	–	1	–	2	–	ns	4, 5
Byte select low to end of write	t_{BW}	8	–	8	–	9	–	12	–	ns	

Shaded areas indicate preliminary information.

Write waveform 1 ($\overline{WE}$ controlled)



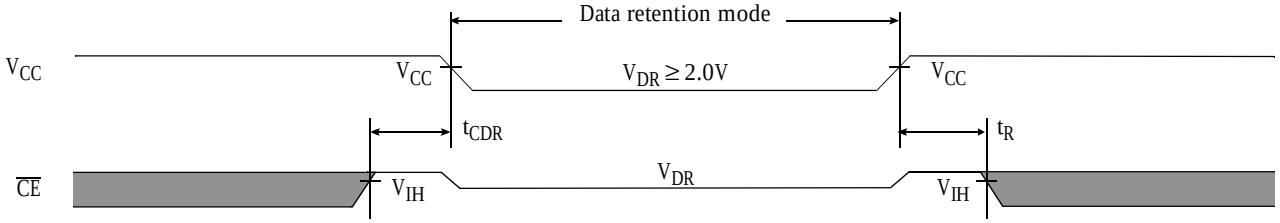
Write waveform 2 ($\overline{CE}$ controlled)



Data retention characteristics (over the operating range)

Parameter	Symbol	Test conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	V_{CC} = 2.0V $\overline{CE} \geq V_{CC}-0.2V$ $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	2.0	–	V
Data retention current	I_{CCDR}		–	500	µA
Chip deselect to data retention time	t_{CDR}		0	–	ns
Operation recovery time	t_R		t_{RC}	–	ns
Input leakage current	$\lvert I_{LI} \rvert$		–	1	µA

Data retention waveform



AC test conditions

- Output load: see Figure B or Figure C, except as noted.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

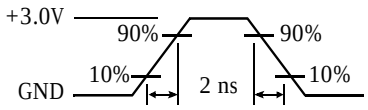


Figure A: Input pulse

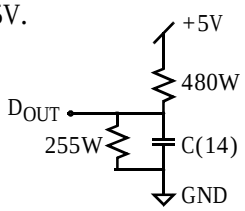


Figure B: 5V Output load

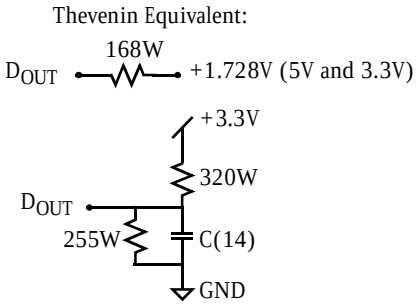


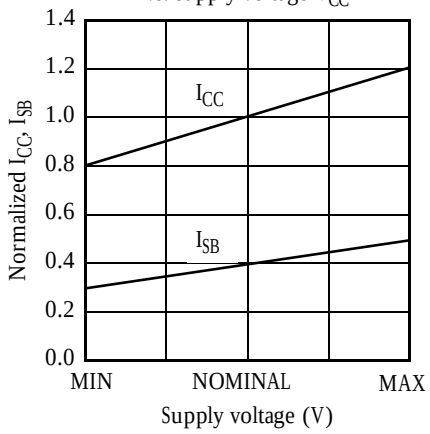
Figure C: 3.3V Output load

Notes

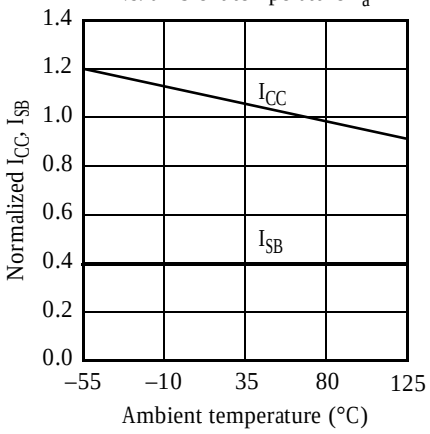
1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
2 This parameter is sampled, but not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A, B, and C.
4 These parameters are specified with C_L = 5pF, as in Figures B or C. Transition is measured ± 500 mV from steady-state voltage.
5 This parameter is guaranteed, but not tested.
6 $\overline{WE}$ is High for read cycle.
7 $\overline{CE}$ and $\overline{OE}$ are Low for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition Low.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CE}$ or $\overline{WE}$ must be High during address transitions. Either $\overline{CE}$ or $\overline{WE}$ asserting high terminates a write cycle.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 Not applicable.
13 2V data retention applies to commercial temperature range operation only.
14 C=30pF, except all high Z and low Z parameters where C=5pF.

Typical DC and AC characteristics

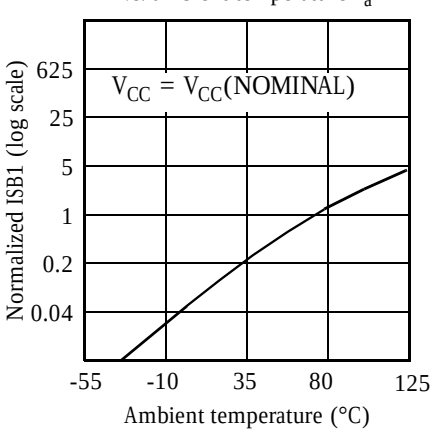
Normalized supply current I_{CC}, I_{SB} vs. supply voltage V_{CC}



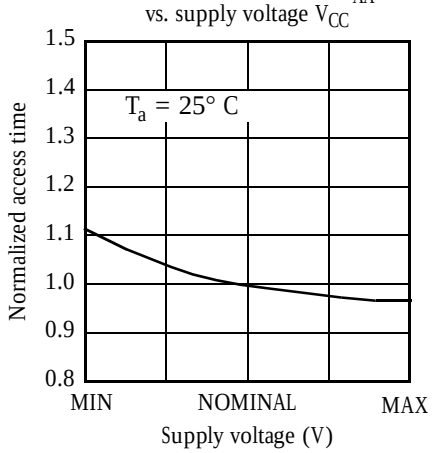
Normalized supply current I_{CC}, I_{SB} vs. ambient temperature T_a



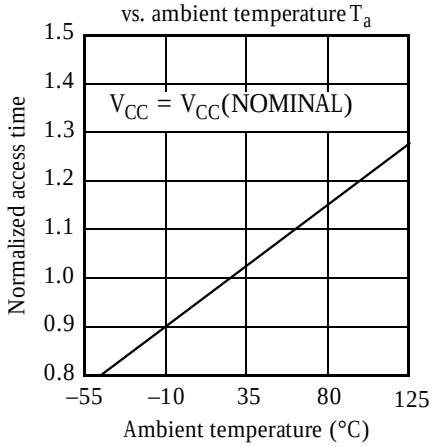
Normalized supply current I_{SB1} vs. ambient temperature T_a



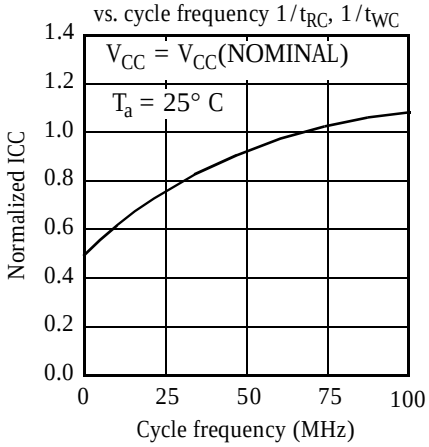
Normalized access time t_{AA} vs. supply voltage V_{CC}



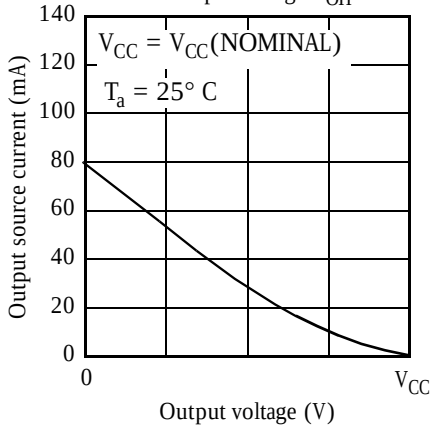
Normalized access time t_{AA} vs. ambient temperature T_a



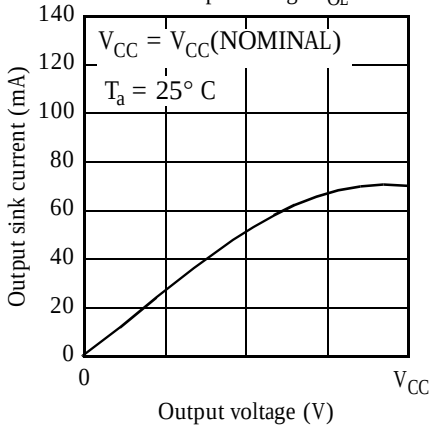
Normalized supply current I_{CC} vs. cycle frequency $1/t_{RC}$, $1/t_{WC}$



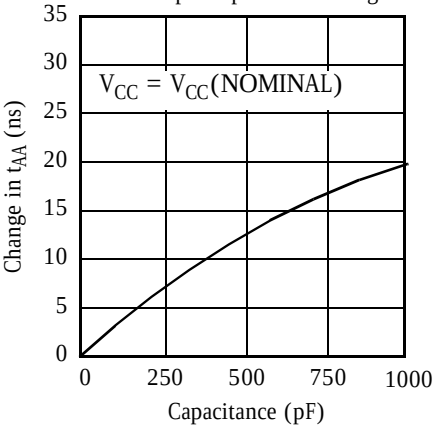
Output source current I_{OH} vs. output voltage V_{OH}



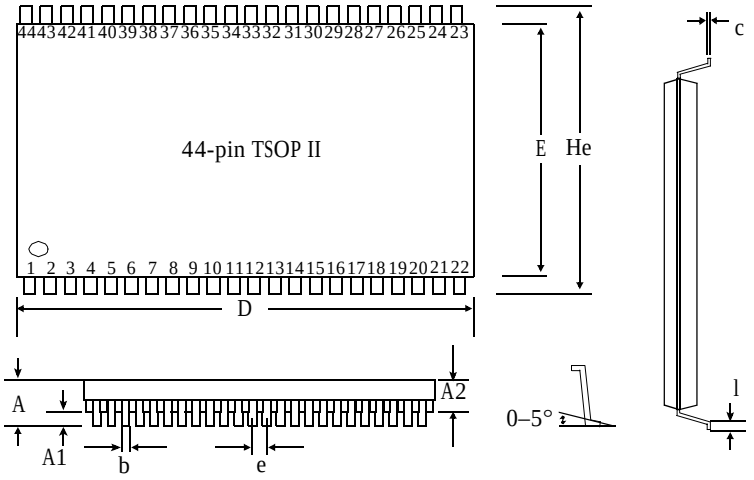
Output sink current I_{OL} vs. output voltage V_{OL}



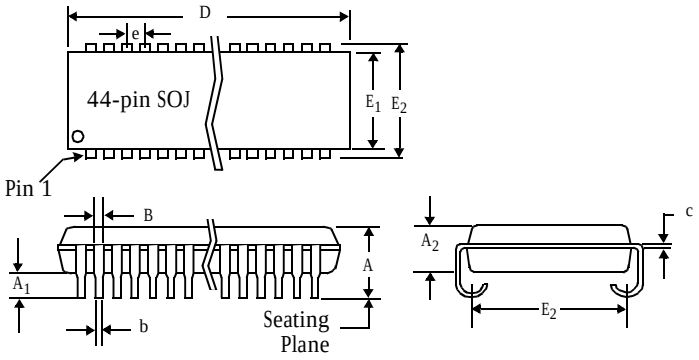
Typical access time change Δt_{AA} vs. output capacitive loading



Package dimensions

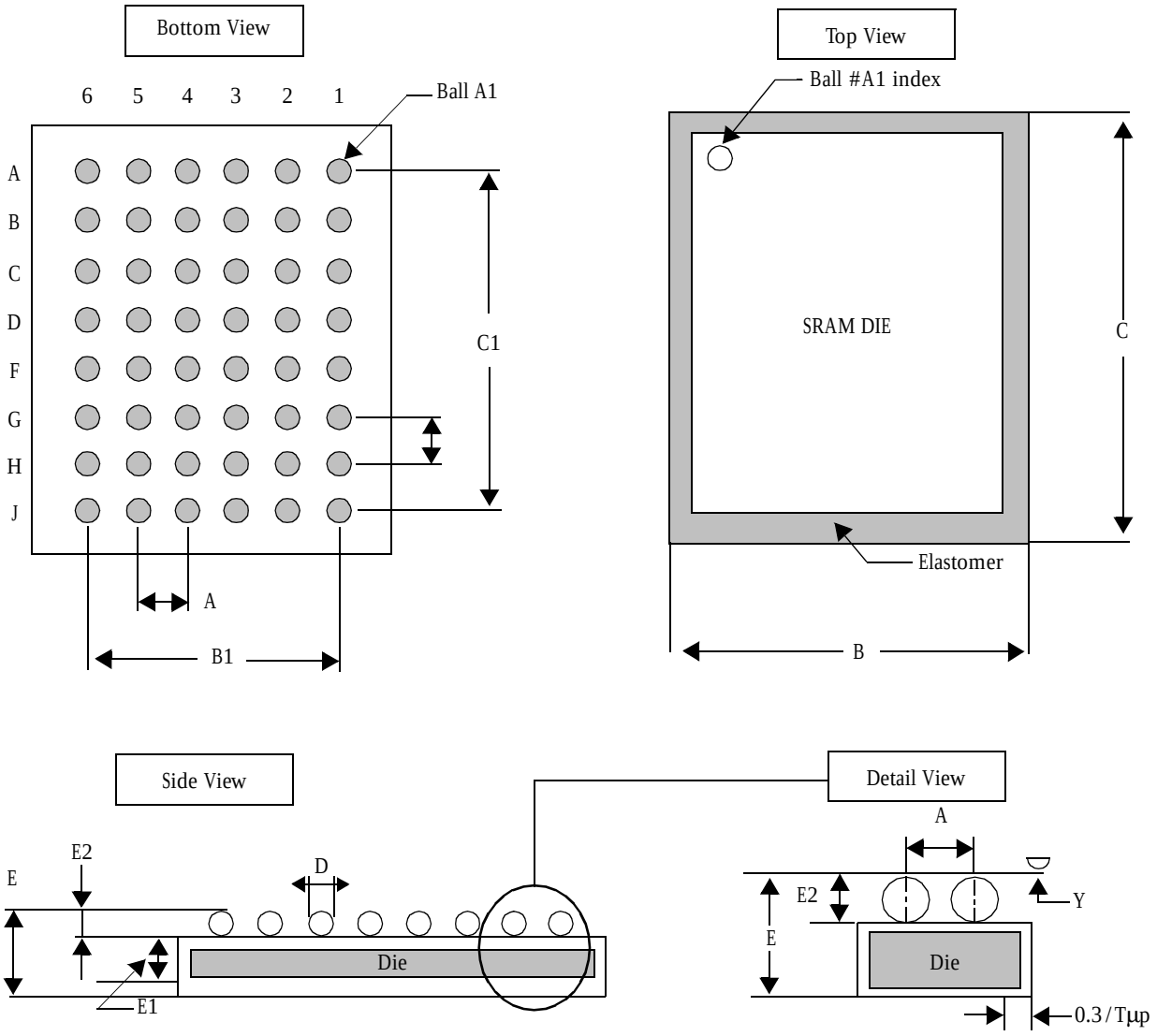


	44-pin TSOP II	
	Min (mm)	Max (mm)
A		1.2
A1	0.05	
A2	0.95	1.05
b	0.30	0.45
c	0.127 (typical)	
D	18.28	18.54
E	10.03	10.29
He	11.56	11.96
e	0.80 (typical)	
l	0.40	0.60



	44-pin SOJ 400 mL	
	Min	Max
A	0.128	0.148
A_1	0.025	–
A_2	1.105	1.115
B	0.026	0.032
b	0.015	0.020
c	0.007	0.013
D	1.120	1.130
E	0.370 NOM	
E_1	0.395	0.405
E_2	0.435	0.445
e	0.050 NOM	

48-ball FBGA



	Minimum	Typical	Maximum
A	–	0.75	–
B	5.90	8.00	8.10
B1	–	3.75	–
C	7.90	8.00	8.10
C1	–	5.25	–
D	–	0.35	–
E	–	–	1.20
E1	–	0.68	–
E2	0.22	0.25	0.27
Y	–	–	0.08

Notes
1 Bump counts: 48 (8 row x 6 column).
2 Pitch: (x,y) = 0.75 mm x 0.75 mm (typ).
3 Units: millimeters.
4 All tolerance are + / - 0.050 unless otherwise specified.
5 Typ: typical.
6 Y is coplanarity: 0.08 (max).

SRAM

Ordering codes

Package \ Access time	Volt/Temp	10 ns	12 ns	15 ns	20 ns
Plastic SOJ, 400 mil	5V commercial	NA	AS7C1026-12JC	AS7C1026-15JC	AS7C1026-20JC
	5V industrial	NA	AS7C1026-12JI	AS7C1026-15JI	AS7C1026-20JI
	3.3V commercial	AS7C31026-10JC	AS7C31026-12JC	AS7C31026-15JC	AS7C31026-20JC
TSOP II, 18.4×10.2 mm	5V commercial	NA	AS7C1026-12TC	AS7C1026-15TC	AS7C1026-20TC
	3.3V commercial	AS7C31026-10TC	AS7C31026-12TC	AS7C31026-15TC	AS7C31026-20TC
	3.3V industrial	NA	AS7C31026-12TI	AS7C31026-15TI	AS7C31026-20TI
CSP BGA, 8×6 mm	5V commercial	NA	AS7C1026-12BC	AS7C1026-15BC	AS7C1026-20BC
	3.3V commercial	AS7C31026-10BC	AS7C31026-12BC	AS7C31026-15BC	AS7C31026-20BC
	3.3V industrial	NA	AS7C31026-12BI	AS7C31026-15BI	AS7C31026-20BI

NA: not available.

Part numbering system

AS7C	X	1026	–XX	X	C
SRAM prefix	Blank=5V CMOS 3=3.3V CMOS	Device number	Access time	Package: J=SOJ 400 mil T=TSOP type 2, 18.4 × 10.2 mm B=CSP BGA, 8 × 6 mm	Temperature range, C=Commercial: 0° C to 70° C I=Industrial: -40° C to 85° C