SWITCHING POWER SUPPLY CONTROL LOOP DESIGN

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1. Introduction

In a switched mode power converter, the conduction time of the power switch is regulated according to the input and output voltages. Thus, a power converter is a self-contained control system in which the conduction time is modulated in reaction to changes in the input and output voltages. From a theoretical approach, control loop design often involves complicated equations, making control a challenging but often misunderstood area in switched mode power supply design. A simplified approach to feedback control loop analysis is presented in the following pages, beginning with a general overview of various parameters affecting performance in a switching power system. A demonstration of an actual power supply is given to show the components involved in designing the characteristics of the control loop. Test results and measurement techniques are also included.

2. Basic Control Loop Concepts

2.1 Transfer Functions and the Bode Plots

The transfer function of a system is defined as the output divided by the input. It consists of a gain and a phase element that can be plotted separately in a Bode plot. The gain around a closed loop system is the product of the gains of all the elements around the loop. In a Bode plot, the gain is plotted logarithmically. Since the product of two numbers is their logarithmic sum, their gains can be summed graphically. The phase of the system is the sum of all phase shifts around the loop.

2.2 Poles

Mathematically, in a transfer equation, a pole occurs when its denominator becomes zero. Graphically, a pole in the bode plot occurs when the slope of the gain decreases by 20 dB per decade. Figure 1 illustrates a low pass filter commonly used for creating a pole in the system. Its transfer function and Bode plots are also shown.

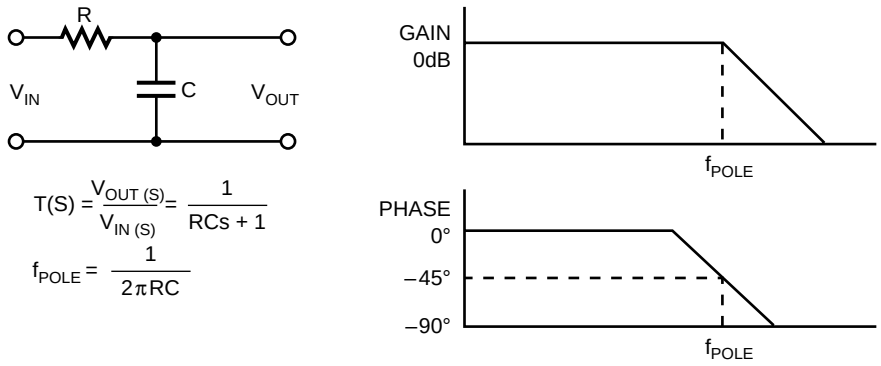
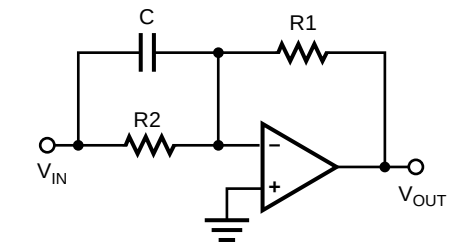


Figure 1.



$$T(S) = \frac{V_{OUT}(S)}{V_{IN}(S)} = \frac{-1}{\frac{1}{R1Cs} + \frac{R2}{R1}}$$

$$f_{ZERO} = \frac{1}{2\pi R2C}$$

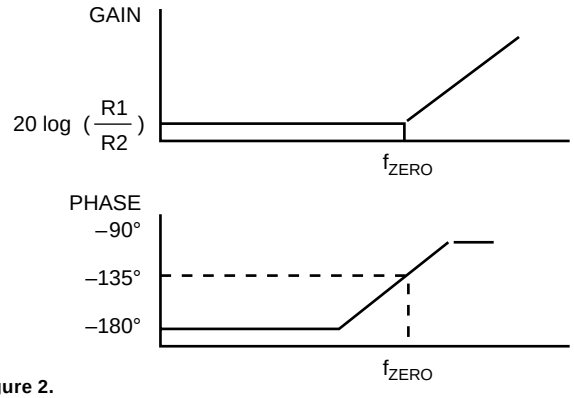


Figure 2.

2.3 Zeros

A zero in a frequency domain transfer function occurs when the numerator of the equation goes to zero. In a Bode plot, a zero occurs at a point where the slope of the gain increases by 20 dB per decade accompanied by 90° phase lead. A high pass filter circuit causing a zero is depicted in Figure 2.

There is a second type of zero, known as a right half plane zero, that causes phase lag instead of phase lead. A right half plane zero causes a 90° phase lag, accompanied by an increase in gain. Right half plane zeros are usually found in boost and buck-boost converters and so extra precaution should be taken during feedback compensation design so the crossover frequency of the system is well below the frequency of the right half plane zero. The Bode plot of a right half plane zero is shown below in Figure 3.

3.0 Ideal Gain-phase Plots for a Switching Mode Power Supply

A goal must be clearly defined prior to designing any control system. Generally, the goal is simply a Bode plot constructed to achieve the best system dynamic response, tightest line and load regulation, and greatest stability. An ideal closed loop Bode plot should possess three characteristics: sufficient phase margin, wide bandwidth, and high gain. A high phase margin damps oscillations and shortens the transient settling time. Wide bandwidth allows the power system to quickly respond to sudden line and load changes. A high gain ensures good line and load regulation.

3.1 Phase Margin

Referring to Figure 4, the phase margin is the amount of phase above 0° at the crossover frequency (f_{cs}). This is different from most control system textbooks that present a measuring phase margin from -180°. They include the

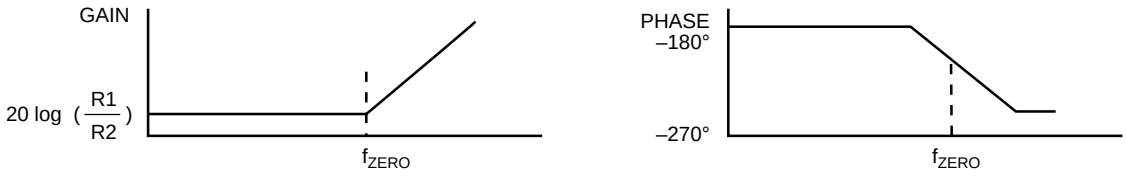


Figure 3.

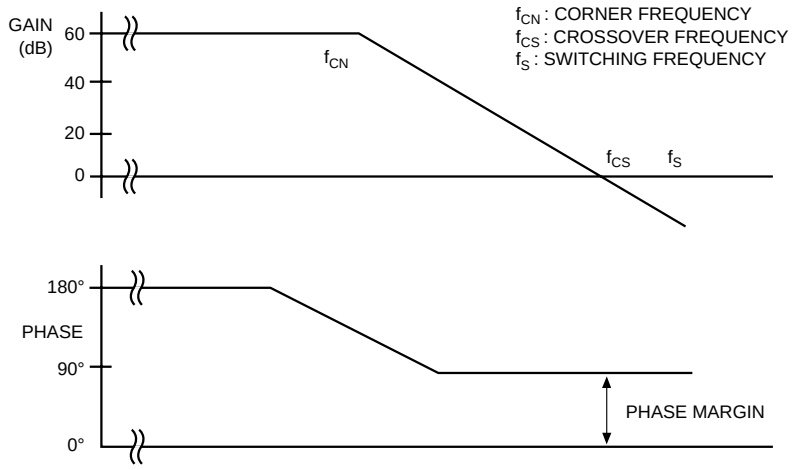


Figure 4.

negative feedback at DC that gives them 180° phase shift at the beginning. In the actual measurement, the 180° phase shift is compensated at DC and enables the phase margin to be measured from 0°.

According to Nyquist's stability criterion, a system is stable when its phase margin exceeds 0°. However, a region of marginal stability exists where the system transient response oscillates and eventually damps out after a long settling time. A system is marginally stable if its phase margin is less than 45°. A phase margin above 45° provides the best dynamic response, short settling time and minimal amount of overshoot.

3.2 Gain-Bandwidth

The gain-bandwidth is the frequency at which the gain is unity. In Figure 4, the gain-bandwidth is the crossover frequency, f_{cs}. A major limiting factor of the maximum crossover frequency is the power supply switching frequency. According to sampling theory, if the sampling frequency is less than 2 times the frequency of the information, the information will not be properly read.

In a switched mode power supply, the switching frequency is seen in the output ripple, which is false information and must not be transmitted by the control loop.

Therefore, the crossover frequency of the system must not exceed half the switching frequency. Otherwise, the switching noise, the ripple, distorts the desired information, the output voltage, causing the system to be unstable.

3.3 Gain

High system gain contributes significantly to ensuring good line and load regulation. It enables the PWM comparator to accurately change the power switch duty cycle in response to variants in the input and output voltage. Often, a tradeoff needs to be determined between higher gain and lower phase margin.

4. A Practical Design Analysis Example

Applying classical control loop analysis techniques, the control loop of a switching regulator is divided into four main stages, output filter, PWM circuit, error amplifier compensation, and feedback . Figure 5 illustrates a block diagram of the four stages and Figure 6 illustrates a power supply circuit diagram.

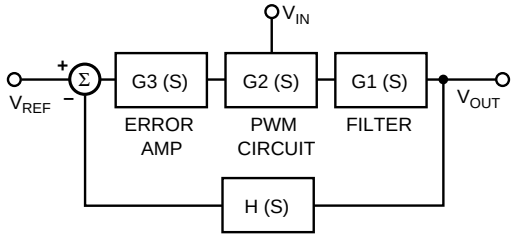


Figure 5.

The output voltage is first divided down by the feedback network. The feedback voltage is then fed into an error amplifier, which compares it with a reference level and generates an error voltage. The pulse width modulation stage takes the error voltage and compares with the power transformer current and converts it to the proper duty cycle to control the amount of power pulsing to the output stage. The output filter stage smoothes out the chopped voltage or current from the power transformer, completing the feedback control loop. The following determines gain and phase of each stage and combines them to form the system transfer function and the system gain and phase plots.

4.1 Feedback Network, H(s):

The feedback network divides the output voltage down to the reference level of the error amplifier. Its transfer equation is simply a resistor divider equation:

$$H(S) = \frac{R2}{R1 + R2} \qquad (1)$$

4.2 Output Filter Stage, G1(s)

In a current mode control system, the output current is regulated to achieve the desired output voltage. The output filter stage converts the pulsating output current into the desired output voltage. Small signal analysis reveals that the

$$R_{FB} = R1 + R2 \qquad (2)$$

$$V_{OUT(S)} = I_{OUT(S)} \left[R_{FB} \parallel \left(\frac{1}{CS} + ESR \right) \right] \qquad (3)$$

$$G1(S) = \frac{V_{OUT(S)}}{I_{OUT(S)}} = \frac{R_{FB}\,(1 + ESRCS)}{(R_{FB} + ESR)\,CS + 1} \qquad (4)$$

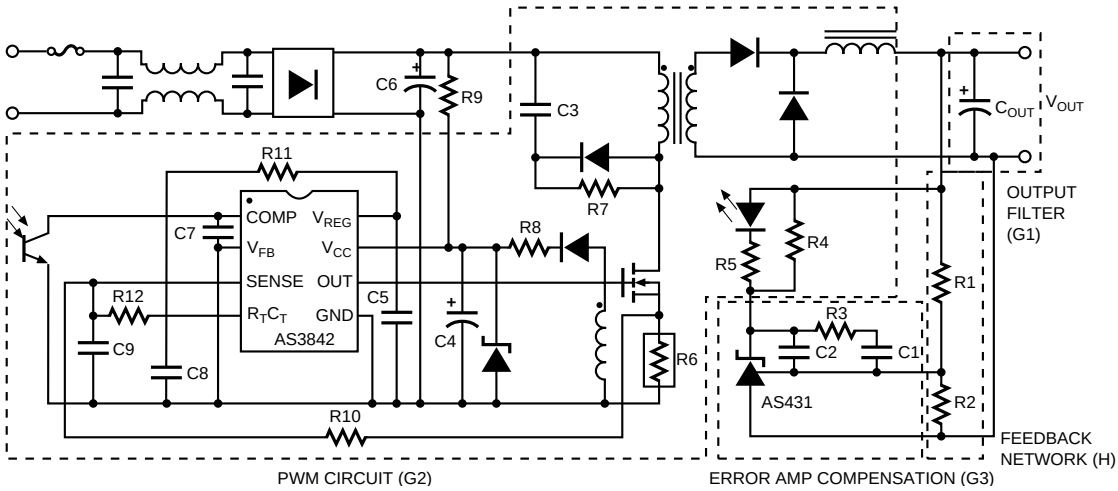


Figure 6.

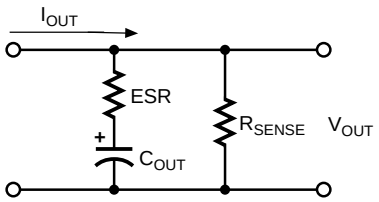


Figure 7.

ESR of the output capacitor and the feedback network resistors (R_1 + R_2 = R_{FB}) dictate the characteristics of the output filter transfer function. The circuit analysis of Figure 7 demonstrates the effects of ESR and R_{SENSE}.

Transfer equation G1(s) shows an initial low frequency gain of R_{FB}. The gain starts to roll off at fpole = 1/2π (R_{FB}+ESR)C and levels off at f_{ZERO} = 1/2πESRC. The Bode plots of G1(s) are shown in Figure 8.

4.3 PWM Circuit Stage, G2(s)

The optocoupler circuit transfers the error signal created by the error amplifier network to the primary side. The AS3842 PWM circuit compares the error voltage with current through primary side of the power transformer. The duty cycle of the power FET is then modulated to supply sufficient current to the secondary to maintain a desired output level.

The small signal transfer function of the optocoupler has a constant gain proportional to the current transfer ratio of the optocoupler, R6,a current limit resistor in series with the optocoupler diode, and the output impedance of the AS3842 error amplifier. This is discussed extensively in the application note "Secondary Error Amplifier with the AS431." The transfer function from the output of the error amplifier to the comp pin of the AS3842 is:

$$\frac{\Delta V_{COMP}}{\Delta V_{CATHODE}} = \frac{CTR}{R6} R_{COMP} \qquad (5)$$

$V_{CATHODE}$ is the cathode voltage of the AS431 and the output of the compensation error amplifier. CTR is the current transfer ratio of the optocoupler. R6 is the current limit resistor in series with the optocoupler diode. R_{COMP} is the output impedance of the AS3842 Comp pin when it tries to source above its maximum output current.

After the error signal is transferred to the compensation pin, it is compared with a current sense signal. Figure 9 shows a simplified block diagram of the current sense comparator and switching stages.

In a closed loop system V_{COMP} is maintained in the same level as I_{SENSE}; therefore, $I_{PRIMARY}$ is effectively regulated by V_{COMP}.

$$I_{PRIMARY} = \frac{V_{COMP}}{R_{SENSE}} \qquad (6)$$

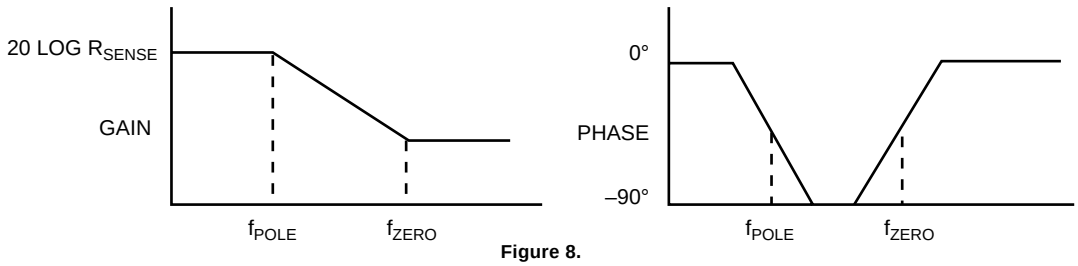


Figure 8.

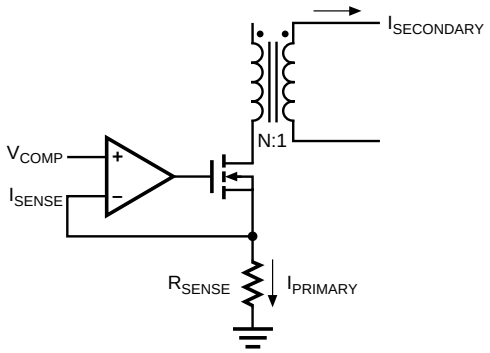


Figure 9.

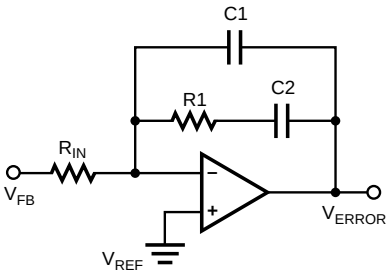
$$I_{PRIMARY} = \frac{I_{SECONDARY}}{N} = \frac{V_{COMP}}{R_{SENSE}} = \frac{I_{OUT}}{N} \quad (7)$$

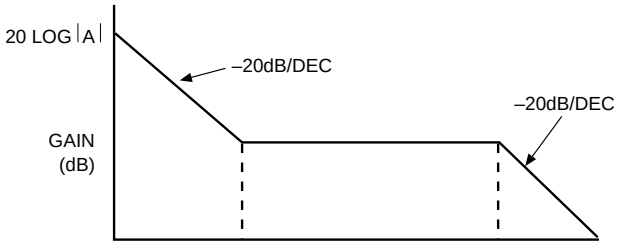
Since $I_{SECONDARY}$, the secondary current or output current, is proportional to the primary current, equation (4) can be rearranged to show a relationship between secondary current and V_{COMP}.

$$\frac{\Delta V_{COMP}}{\Delta I_{OUT}} = \frac{R_{SENSE}}{N} \quad (8)$$

The transfer function of PWM stage can be created by combining equation (3) and (6):

$$G2(S) = \frac{\Delta I_{OUT}}{\Delta V_{CATHODE}} = \frac{N}{R_{SENSE}} \frac{CTR}{R6} R_{COMP} \quad (9)$$





$$G3(s) = \frac{V_{ERROR}}{V_{FB}} = \frac{1 + R1C2}{R_{IN}(C2 + C1) + SR1(C2 \bullet C1)}$$

$f_{p1} = 0$

$$f_Z = \frac{1}{2\pi R1C2}$$

$$f_{p}2 = \frac{1}{2\pi R1C2\left(\frac{C1}{C1 + C2}\right)}$$

A = OPEN LOOP GAIN OF THE AMPLIFIER

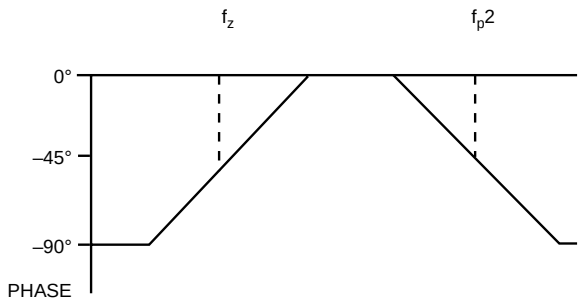


Figure 10.

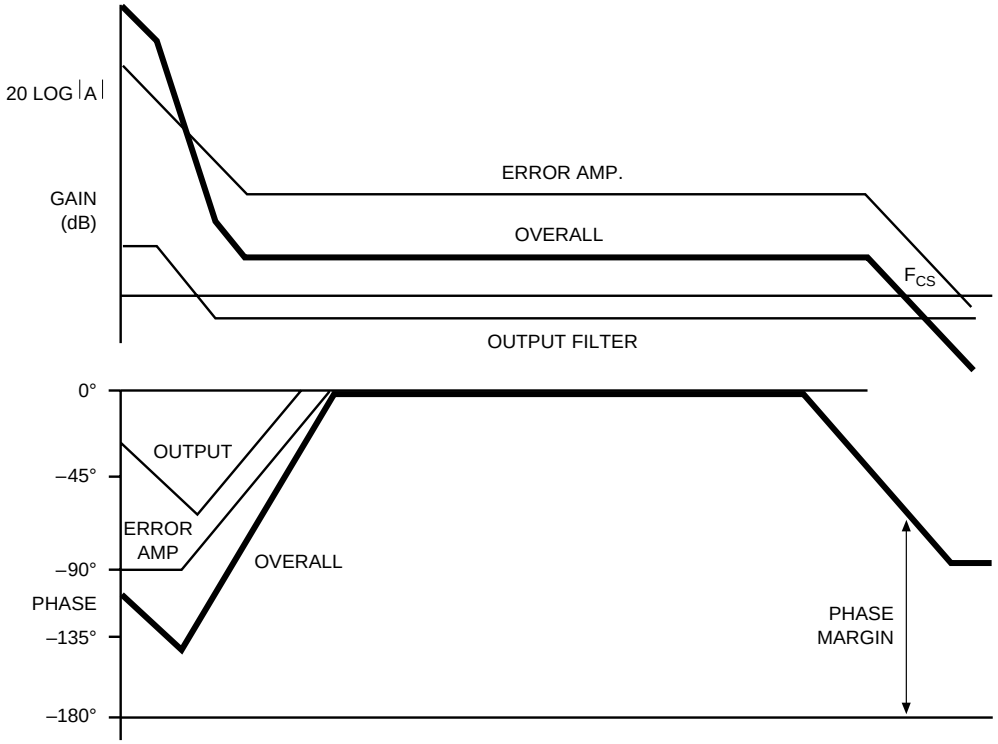


Figure 11.

Transfer function G2 consists of only gain and no phase shift.

4.4 Error Amplifier Compensation Network,G3(s)

Once the transfer functions of the output filter and PWM circuit stage are determined, the error amplifier compensation network can then be configured to achieve the optimum system performance. Figure 10 illustrates a compensation scheme that gives high frequency roll-off and high gain at low frequency.

This compensation scheme has some favorable characteristics for error amplifier compensation. It has very high DC gain and well-controlled roll off.

4.5 Overall System

Since this is a linear system, superposition technique can be applied to derive the overall system transfer function. By superimposing the gains and phases of the stages around the loop, a Bode plot of the overall system is generated. The poles and zeros of the compensation network can then be placed to optimize the system performance. Figure 11 combines the Bode plots of the stages and 180° phase shift is also added to account for the negative feedback of the system.

5. Measurement Results

A 150-watt current mode forward converter was constructed and its small signal loop characteristics modified to demonstrate its effects on system transient response. Figure 12 shows its gain-phase plot. As predicted by Figure 11, the same Bode plot curvature was acquired. The gain-phase shows the system has a phase margin

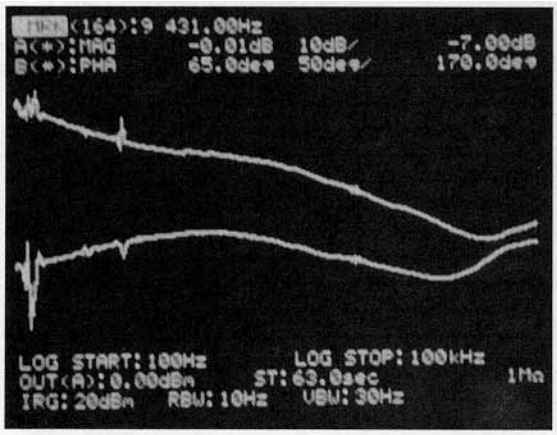


Figure 12.

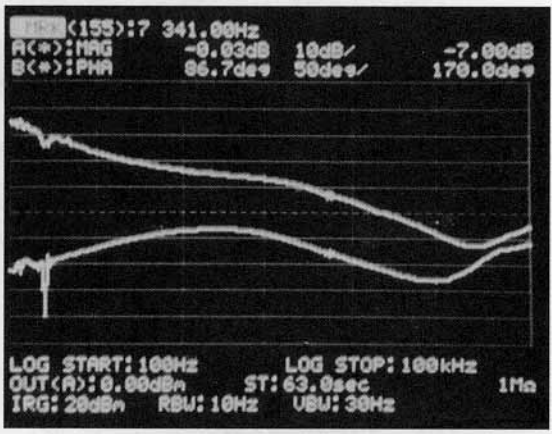


Figure 13.

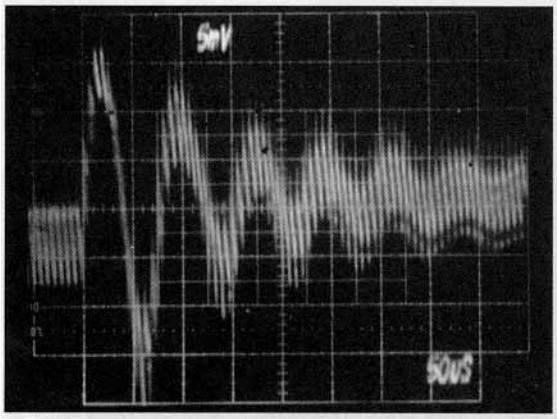


Figure 14.

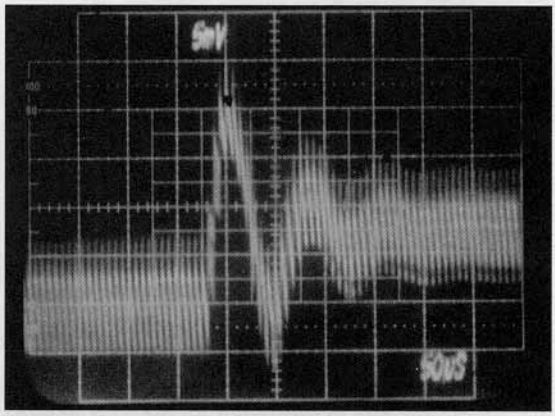


Figure 15.

of 86.7°, implying a stable system with a fast transient response. Figure 13 shows the transient response of the system. To demonstrate the effects of phase margin, the phase margin of the system was decreased by increasing the overall gain of the system, increasing the crossover frequency. The phase margin decreases with increasing crossover frequency. Figure 14 shows a Bode plot of the system with higher cross over frequency and smaller phase margin of 65°. Its transient response is shown on figure 15. Note that smaller phase margin results in greater oscillation and longer settling time. Table 1 compares the changes in line and load regulations between two systems with different gain magnitudes. As discussed previously, high loop gain results in tighter line and load regulation. It should also be noted that a tradeoff has been made between the high phase margin and lower loop gain.

Load Regulation	**High Loop Gain**	**Low Loop Gain**
V_{IN} = 85 V_{AC}	127 mV	132 mV
$_{IN}$ = 135 V_{AC}	101 mV	116 mV
Line Regulation		
Low Load	21 mV	25 mV
High Load	5 mV	9 mV

(Table 1.)

6.0 Measurement Techniques

To guarantee accurate results, the input impedance of the test signal injection node must be larger than its output impedance. In the test circuit (Figure 6) where the error amplifier is on the secondary side and the PWM circuit is on the primary side, the test signal is injected at the output of the optocoupler and before the V_{COMP} input of the AS3842. The input impedance is the impedance looking into the V_{COMP} pin and the output impedance is the output impedance of the optocoupler. In other applications where the error amplifier can not be separated from the PWM circuitry, the test signal can be injected following the output filter capacitor, in series with the input to the error amplifier.

References

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Chetty, P.R.K., “Modeling and Design of Switching Regulators,” IEEE Transactions on Aerospace and Electric Systems, May 1992, page 333–343.

Jamerson, C., and Hosseini, “A Simplified Procedure for Compensation Current-Mode Control Loops,” HFPC Proceedings, June 1991, page 299–318.

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Notes