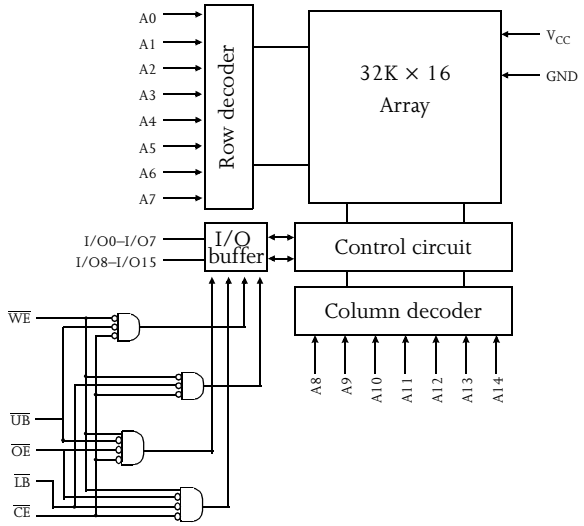
5V/3.3V 32K×16 CMOS SRAM

Features

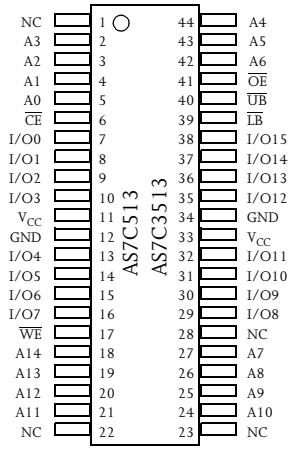
- AS7C513 (5V version)
- AS7C3513 (3.3V version)
- Industrial and commercial temperature
- Organization: 32,768 words × 16 bits
- Center power and ground pins
- High speed
  - 12/15/20 ns address access time
  - 6,7,8 ns output enable access time
- Low power consumption: ACTIVE
  - 800 mW (AS7C513) / max @ 12 ns
  - 432 mW (AS7C3513) / max @ 12 ns
- Low power consumption: STANDBY
  - 28 mW (AS7C513) / max CMOS
  - 18 mW (AS7C3513) / max CMOS
- 2.0V data retention
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
- 44-pin JEDEC standard package
  - 400 mil SOJ
  - 400 mil TSOP II
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram



Pin arrangement

44-Pin SOJ, TSOP II (400 mil)



Selection guide

		AS7C513-12 AS7C3513-12	AS7C513-15 AS7C3513-15	AS7C513-20 AS7C3513-20	Unit
Maximum address access time		12	15	20	ns
Maximum output enable access time		5	7	9	ns
Maximum operating current	AS7C513	160	150	140	mA
	AS7C3513	120	110	100	mA
Maximum CMOS standby current	AS7C513	5	5	5	mA
	AS7C3513	5	5	5	mA

Shaded areas indicate advance information.

Functional description

The AS7C513 and the AS7C3513 are high performance CMOS 524,288-bit Static Random Access Memory (SRAM) devices organized as 32,768 words × 16 bits. They are designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 12/15/20 ns with output enable access times (t_{OE}) of 6,7,8 ns are ideal for high performance applications. The chip enable input $\overline{CE}$ permits easy memory expansion with multiple-bank memory systems.

When $\overline{CE}$ is high, the devices enter standby mode. The AS7C513 and AS7C3513 are guaranteed not to exceed 28/18 mW power consumption in CMOS standby mode. The devices also offer 2.0V data retention.

A write cycle is accomplished by asserting write enable ($\overline{WE}$), ($\overline{UB}$) and/or ($\overline{LB}$), and chip enable ($\overline{CE}$). Data on the input pins I/O0-I/O7, and/or I/O8–I/O15, is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$), ($\overline{UB}$) and ($\overline{LB}$), and chip enable ($\overline{CE}$), with write enable ($\overline{WE}$) high. The chips drive I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, or ($\overline{UB}$) and ($\overline{LB}$), output drivers stay in high-impedance mode.

The devices provide multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. $\overline{LB}$ controls the lower bits, I/O0–I/O7, and $\overline{UB}$ controls the higher bits, I/O8–I/O15.

All chip inputs and outputs are TTL-compatible. The AS7C513 and AS7C3513 are packaged in common industry standard packages.

Absolute maximum ratings

Parameter	Device	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to GND	AS7C513	V_{t1}	−0.50	+7.0	V
	AS7C3513	V_{t1}	−0.50	+5.0	V
Voltage on any pin relative to GND		V_{t2}	−0.50	V_{CC} +0.50	V
Power dissipation		P_D	–	1.0	W
Storage temperature (plastic)		T_{stg}	−65	+150	°C
Ambient temperature with V_{CC} applied		T_{bias}	−55	+125	°C
DC current into outputs (low)		I_{OUT}	–	50	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O0–I/O7	I/O8–I/O15	Mode
H	X	X	X	X	High Z	High Z	Standby (I_{SB}, I_{SBI})
L	H	L	L	H	D_{OUT}	High Z	Read I/O0–I/O7 (I_{CC})
L	H	L	H	L	High Z	D_{OUT}	Read I/O8–I/O15 (I_{CC})
L	H	L	L	L	D_{OUT}	D_{OUT}	Read I/O0–I/O15 (I_{CC})
L	L	X	L	L	D_{IN}	D_{IN}	Write I/O0–I/O15 (I_{CC})
L	L	X	L	H	D_{IN}	High Z	Write I/O0–I/O7 (I_{CC})
L	L	X	H	L	High Z	D_{IN}	Write I/O8–I/O15 (I_{CC})
L L	H X	H X	X H	X H	High Z	High Z	Output disable (I_{CC})

Key: X = Don't care; L = Low; H = High

Recommended operating conditions

Parameter		Device	Symbol	Min	Typical	Max	Unit
Supply voltage		AS7C513	V_{CC}	4.5	5.0	5.5	V
		AS7C3513	V_{CC}	3.0	3.3	3.6	V
Input voltage		AS7C513	V_{IH}	2.2	–	V_{CC} + 0.5	V
		AS7C3513	V_{IH}	2.0	–	V_{CC} + 0.5	
			V_{IL}	–0.5†	–	0.8	V
Ambient operating temperature	commercial		T_A	0	–	70	° C
	industrial		T_A	–40	–	05	° C

† V_{IL} min = –3.0V for pulse width less than $t_{RC}/2$.

DC operating characteristics (over the operating range)[1]

Parameter	Symbol	Test conditions	Device	-12		-15		-20		Unit
				Min	Max	Min	Max	Min	Max	
Input leakage current	$\lvert I_{LI} \rvert$	V_{CC} = Max V_{IN} = GND to V_{CC}		–	1	–	1	–	1	µA
Output leakage current	$\lvert I_{LO} \rvert$	V_{CC} = Max V_{OUT} = GND to V_{CC}		–	1	–	1	–	1	µA
Operating power supply current	I_{CC}	V_{CC} = Max, CE ≤ V_{IL} f = f_{Max} , I_{OUT} = 0mA	AS7C513	–	160	–	150	–	140	mA
			AS7C3513	–	120	–	110	–	100	
Standby power supply current	I_{SB}	V_{CC} = Max, CE ≤ V_{IL} f = f_{Max} , I_{OUT} = 0mA	AS7C513	–	40	–	40	–	40	mA
			AS7C3513	–	40	–	40	–	40	
	I_{SB1}	V_{CC} = Max, $\overline{CE}$ ≥ V_{CC}–0.2V V_{IN} ≤ GND + 0.2V or V_{IN} ≥ V_{CC} –0.2V, f = 0	AS7C513	–	3	–	3	–	3	mA
			AS7C3513	–	3	–	3	–	3	
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min		–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min		2.4	–	2.4	–	2.4	–	V

Shaded areas indicate advance information.

Capacitance (f = 1MHz, T_a = 25° C, V_{CC} = NOMINAL)[2]

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$, $\overline{LB}$, $\overline{UB}$	V_{in} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{in} = V_{out} = 0V	7	pF

Read cycle (over the operating range) [3,9]

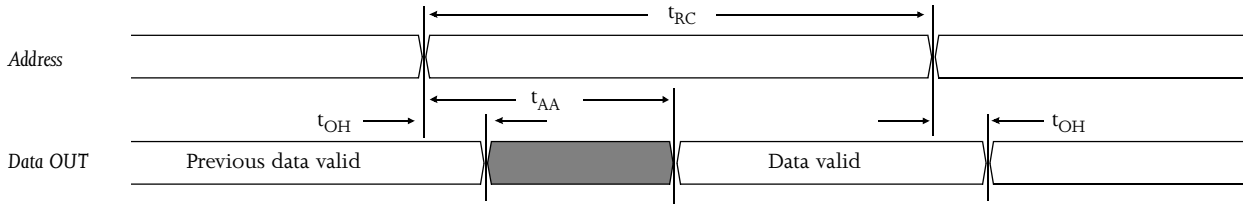
Parameter	Symbol	-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	12	–	15	–	20	–	ns	
Address access time	t_{AA}	–	12	–	15	–	20	ns	3
Chip enable ($\overline{CE}$) access time	t_{ACE}	–	12	–	15	–	20	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}	–	6	–	7	–	8	ns	
Output hold from address change	t_{OH}	3	–	4	–	4	–	ns	5
$\overline{CE}$ Low to output in low Z	t_{CLZ}	0	–	0	–	0	–	ns	4, 5
$\overline{CE}$ High to output in high Z	t_{CHZ}	–	6	–	7	–	8	ns	4, 5
$\overline{OE}$ Low to output in low Z	t_{OLZ}	0	–	0	–	0	–	ns	4, 5
Byte select access time	t_{BA}	–	6	–	7	–	8	ns	
Byte select Low to low Z	t_{BLZ}	0	–	0	–	0	–	ns	4,5
Byte select High to high Z	t_{BHZ}	–	6	–	7	–	9	ns	4,5
$\overline{OE}$ High to output in high Z	t_{OHZ}	–	6	–	7	–	9	ns	4, 5
Power up time	t_{PU}	0	–	0	–	0	–	ns	4, 5
Power down time	t_{PD}	–	12	–	15	–	20	ns	4, 5

Shaded areas indicate advance information.

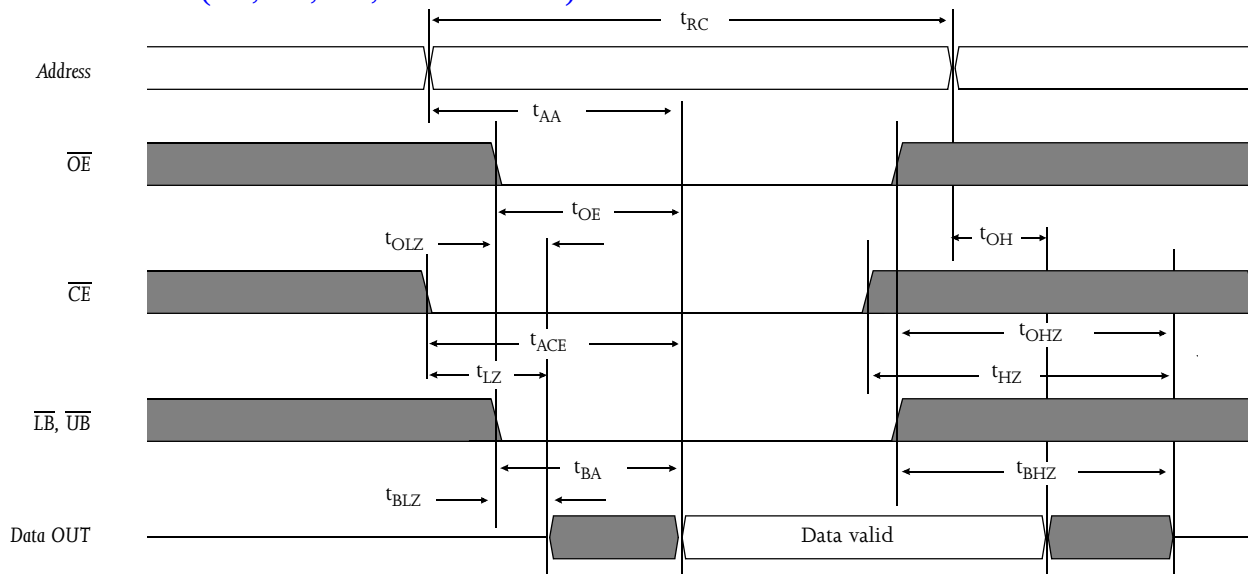
Key to switching waveforms

Rising input Falling input Undefined output/don't care

Read waveform 1 (address controlled)[3,6,7,9]



Read waveform 2 ($\overline{CE}$, $\overline{OE}$, UB, LB controlled)[3,6,8,9]

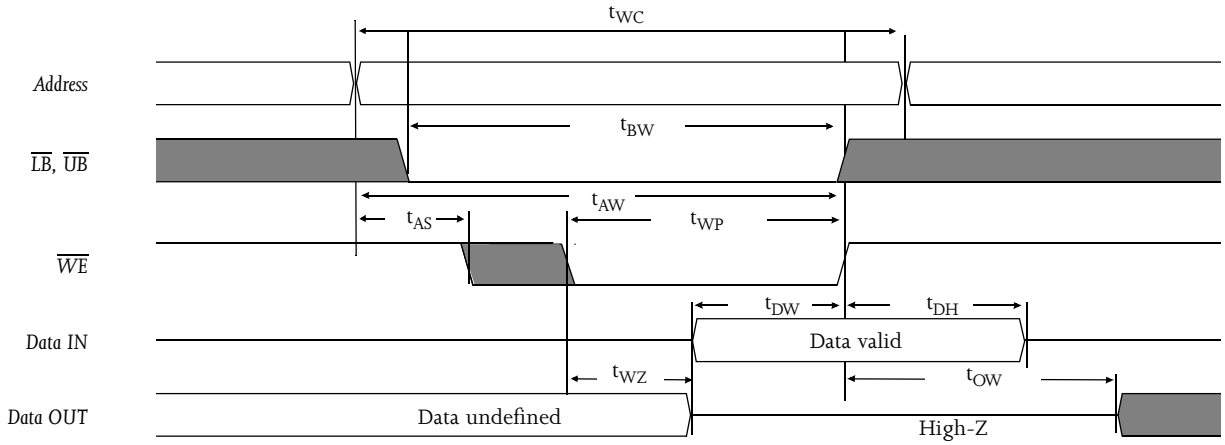


Write cycle (over the operating range)[11]

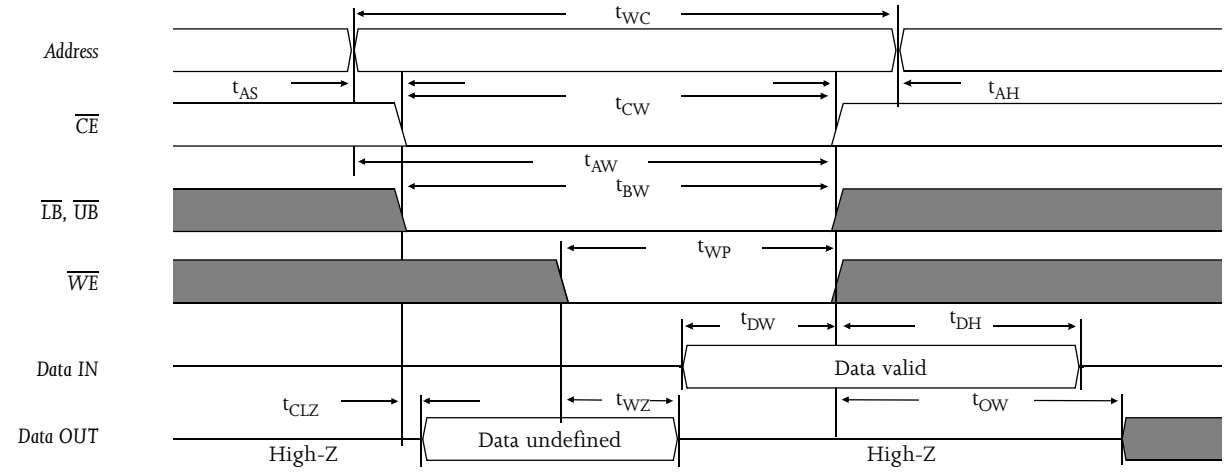
Parameter	Symbol	-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	12	–	15	–	20	–	ns	
Chip enable ($\overline{CE}$) to write end	t_{CW}	9	–	10	–	12	–	ns	
Address setup to write end	t_{AW}	8	–	10	–	12	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	ns	
Write pulse width	t_{WP}	8	–	10	–	12	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	6	–	8	–	10	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	ns	5
Write enable to output in high Z	t_{WZ}	–	6	–	7	–	9	ns	4, 5
Output active from write end	t_{OW}	3	–	3	–	3	–	ns	4, 5
Byte select Low to end of write	t_{BW}	8	–	9	–	12	–	ns	

Shaded areas indicate advance information.

Write waveform 1($\overline{WE}$ controlled)[10,11]



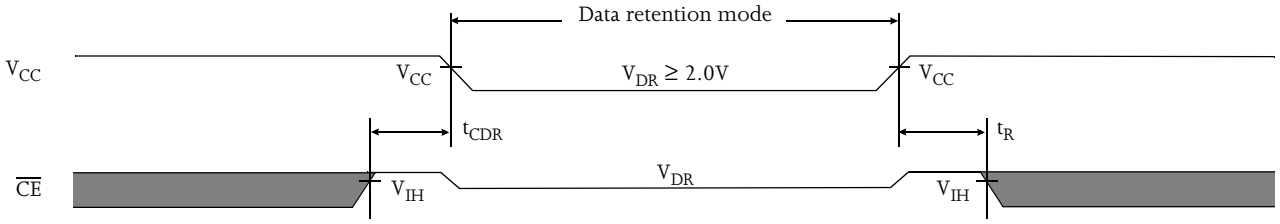
Write waveform 2 ($\overline{CE}$ controlled)[10,11]



Data retention characteristics (over the operating range)[13]

Parameter	Symbol	Test conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	V_{CC} = 2.0V $\overline{CE} \geq V_{CC}-0.2V$ $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	2.0	–	V
Data retention current	I_{CCDR}		–	500	µA
Chip deselect to data retention time	t_{CDR}		0	–	ns
Operation recovery time	t_R		t_{RC}	–	ns
Input leakage current	$\lvert I_{LI} \rvert$		–	1	µA

Data retention waveform



AC test conditions

- Output load: see Figure B or Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

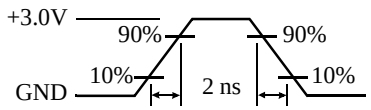


Figure A: Input pulse

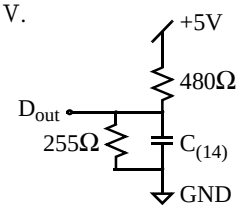


Figure B: 5V Output load

Thevenin equivalent:

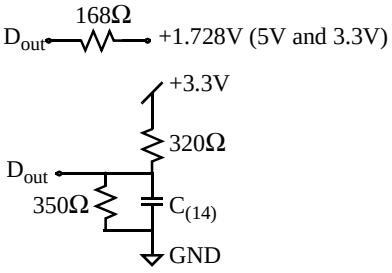


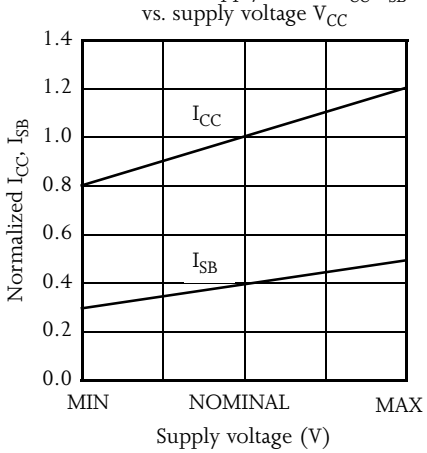
Figure C: 3.3V Output load

Notes

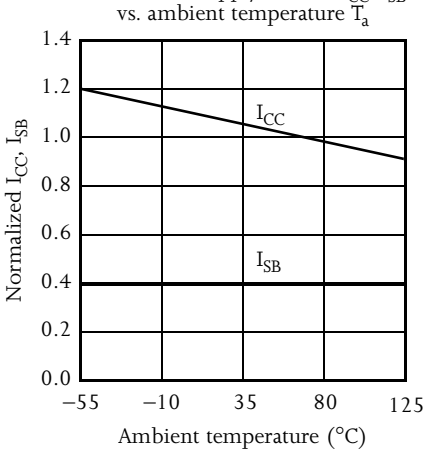
1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
2 This parameter is sampled, but not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A, B, and C.
4 These parameters are specified with C_L = 5pF, as in Figures B or C. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed, but not 100% tested.
6 $\overline{WE}$ is High for read cycle.
7 $\overline{CE}$ and $\overline{OE}$ are Low for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition Low.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CE}$ or $\overline{WE}$ must be High during address transitions. Either $\overline{CE}$ or $\overline{WE}$ asserting high terminates a write cycle.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 Not applicable.
13 2V data retention applies to the commercial operating range only.
14 C=30pF, except on High Z and Low Z parameters, where C=5pF.

Typical DC and AC characteristics

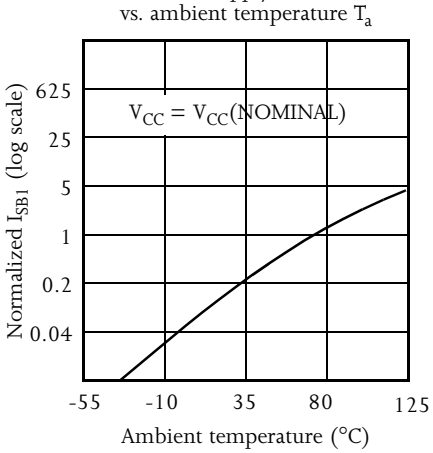
Normalized supply current I_{CC}, I_{SB} vs. supply voltage V_{CC}



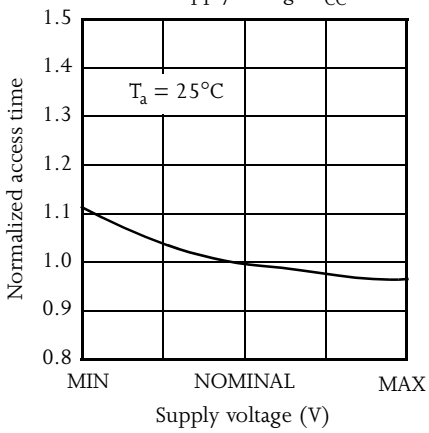
Normalized supply current I_{CC}, I_{SB} vs. ambient temperature T_a



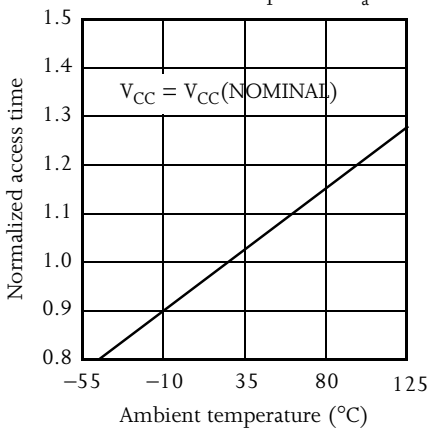
Normalized supply current ISB1 vs. ambient temperature T_a



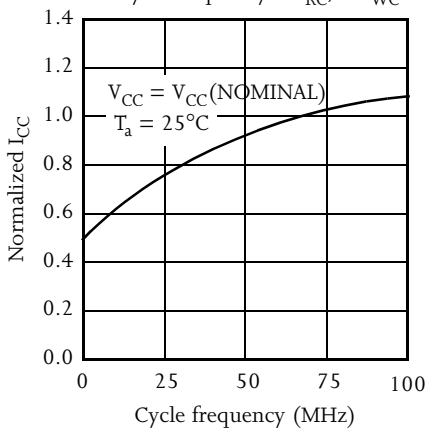
Normalized access time t_{AA} vs. supply voltage V_{CC}



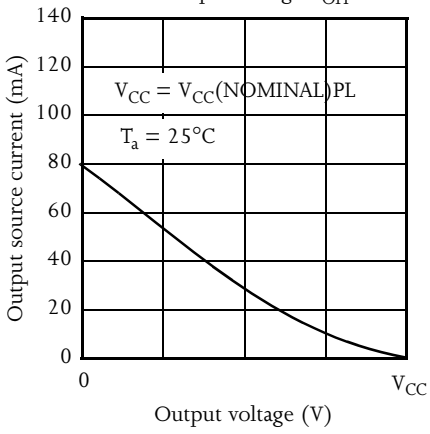
Normalized access time t_{AA} vs. ambient temperature T_a



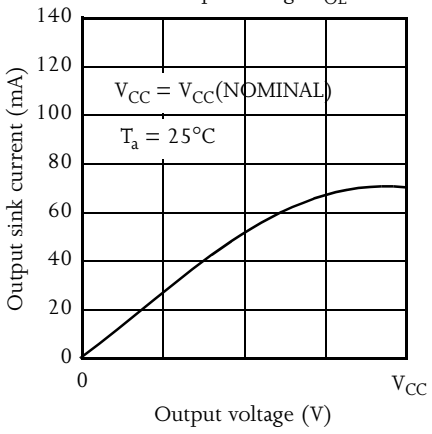
Normalized supply current I_{CC} vs. cycle frequency $1/t_{RC}$, $1/t_{WC}$



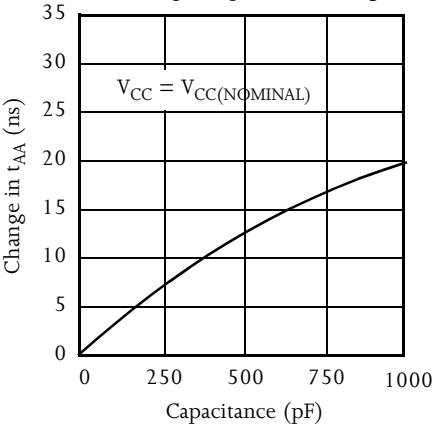
Output source current I_{OH} vs. output voltage V_{OH}



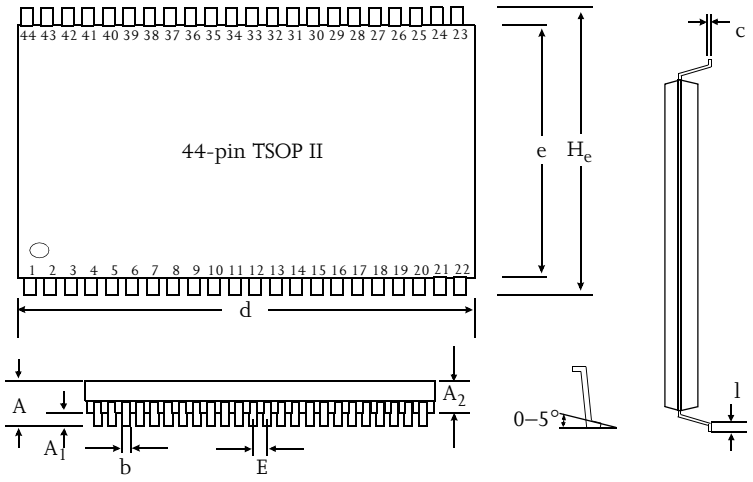
Output sink current I_{OL} vs. output voltage V_{OL}



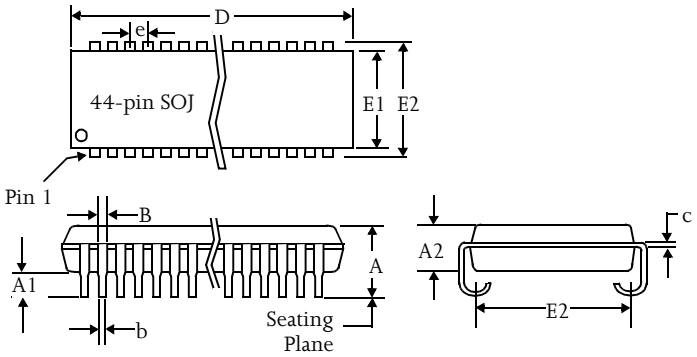
Typical access time change Δt_{AA} vs. output capacitive loading



Package dimensions



	44-pin TSOP II	
	Min (mm)	Max (mm)
A		1.2
A_1	0.05	
A_2	0.95	1.05
b	0.25	0.45
c	0.15 (typical)	
d	18.28	18.54
e	10.06	10.26
H_e	11.56	11.96
E	0.80 (typical)	
l	0.40	0.60



	44-pin SOJ 400 mil	
	Min	Max
A	0.128	0.148
A1	0.025	-
A2	1.105	1.115
B	0.026	0.032
b	0.015	0.020
c	0.007	0.013
D	1.120	1.130
E	0.370 NOM	
E1	0.395	0.405
E2	0.435	0.445
e	0.050 NOM	

Ordering codes

Package\Access time	Volt/Temp	12 ns	15 ns	20 ns
Plastic SOJ, 400 mil	5V commercial	AS7C513-12JC	AS7C513-15JC	AS7C513-20JC
	3.3V commercial	AS7C3513-12JC	AS7C3513-15JC	AS7C3513-20JC
TSOP II, 18.4×10.2 mm	5V commercial	AS7C513-12TC	AS7C513-15TC	AS7C513-20TC
	3.3V commercial	AS7C3513-12TC	AS7C3513-15TC	AS7C3513-20TC

NA: not available.

Part numbering system

AS7C	X	513	–XX	X	C
SRAM prefix	Voltage:Blank = 5V CMOS 3 = 3.3V CMOS	Device number	Access time	Package: J = SOJ 400 mil T = TSOP II, 18.4×10.2 mm	Commercial temperature range: 0 °C to 70 °C Industrial temperature range: -40C to 85C