Closed-Loop High Speed Buffer

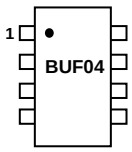
BUF04*

FEATURES
Bandwidth – 110 MHz
Slew Rate – 3000 V/μs
Low Offset Voltage – <1 mV
Very Low Noise – < 4 nV/√Hz
Low Supply Current – 8.5 mA Mux
Wide Supply Range – ±5 V to ±15 V
Drives Capacitive Loads
Pin Compatible with BUF03

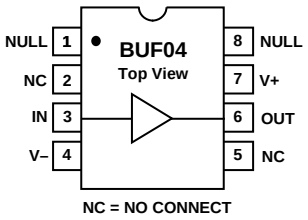
APPLICATIONS
Instrumentation Buffer
RF Buffer
Line Driver
High Speed Current Source
Op Amp Output Current Booster
High Performance Audio
High Speed AD/DA

FUNCTIONAL BLOCK DIAGRAMS

8-Lead Narrow-Body SO
(S Suffix)



Plastic DIP
8-Lead and Cerdip
(P, Z Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The BUF04 is a wideband, closed-loop buffer that combines state of the art dynamic performance with excellent dc performance. This combination enables designers to maximize system performance without any speed versus dc accuracy compromises.

Built on a high speed Complementary Bipolar (CB) process for better power performance ratio, the BUF04 consumes less than 8.5 mA operating from ±5 V or ±15 V supplies. With a 2000 V/μs min slew rate, and 100 MHz gain bandwidth product, the BUF04 is ideally suited for use in high speed applications where low power dissipation is critical.

Full ±10 V output swing over the extended temperature range along with outstanding ac performance and high loop gain accuracy makes the device useful in high speed data acquisition systems.

High slew rate and very low noise and THD, coupled with wide input and output dynamic range, make the BUF04 an excellent choice for video and high performance audio circuits.

The BUF04's inherent ability to drive capacitive loads over a wide voltage and temperature range makes it extremely useful for a wide variety of applications in military, industrial, and commercial equipment.

The BUF04 is specified over the extended industrial (–40°C to +85°C) and military (–55°C to +125°C) temperature range. BUF04s are available in plastic and ceramic DIP plus SO-8 surface mount packages.

Contact your local sales office for MIL-STD-883 data sheet and availability.

***Patent pending.**

REV. 0

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Tel: 617/329-4700 **Fax: 617/326-8703**

BUF04–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.3	1	mV
		–40°C ≤ T_A ≤ +85°C		1.3	4	mV
Input Bias Current	I_B	V_{CM} = 0		0.7	5	µA
		–40°C ≤ T_A ≤ +85°C		2.2	10	µA
Input Voltage Range	V_{CM}			±13		V
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			30		µV/°C
Offset Null Range				±25		mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 150 Ω,	±10.5	±11.1		V
		–40°C ≤ T_A ≤ +85°C	±10	±11		V
		R_L = 2 kΩ,	±13	±13.5		V
		–40°C ≤ T_A ≤ +85°C	±13	±13.15		V
Output Current – Continuous	I_{OUT}		±50	±65		mA
Peak Output Current	I_{OUTP}	Note 2		±80		mA
TRANSFER CHARACTERISTICS						
Gain	A_{VCL}	R_L = 2 kΩ	0.995	0.9985	1.005	V/V
		–40°C ≤ T_A ≤ +85°C	0.995	0.9980	1.005	V/V
Gain Linearity	NL	R_L = 1 kΩ, V_O = ±10 V		0.005		%
		R_L = 150 kΩ		0.008		%
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V	76	93		dB
		–40°C ≤ T_A ≤ +85°C	76	93		dB
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞		6.9	8.5	mA
		–40°C ≤ T_A ≤ +85°C		6.9	8.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, C_L = 70 pF	2000	3000		V/µs
Bandwidth	BW	–3 dB, C_L = 20 pF, R_L = ∞		110		MHz
Bandwidth	BW	–3 dB, C_L = 20 pF, R_L = 1 kΩ		110		MHz
Bandwidth	BW	–3 dB, C_L = 20 pF, R_L = 150 Ω		110		MHz
Settling Time		V_{IN} = ±10 V Step to 0.1%		60		ns
Differential Phase		f = 3.58 MHz, R_L = 150 Ω		0.02		Degrees
		f = 4.43 MHz, R_L = 150 Ω		0.03		Degrees
Differential Gain		f = 3.58 MHz, R_L = 150 Ω		0.014		%
		f = 4.43 MHz, R_L = 150 Ω		0.008		%
Input Capacitance				3		pF
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		4		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		2		pA/√Hz

NOTE

[1]Long term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at +125°C with an LTPD of 1.3.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = ±5.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.8	2.0	mV
		–40°C ≤ T_A ≤ +85°C		1.0	4	mV
Input Bias Current	I_B	V_{CM} = 0 V		0.15	5	µA
		–40°C ≤ T_A ≤ +85°C		1.6	10	µA
Input Voltage Range	V_{CM}			±3.0		V
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			30		µV/°C
Offset Null Range				±25		mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 150 Ω,	±3.0			V
		–40°C ≤ T_A ≤ +85°C	±2.75	±3.00		V
		R_L = 2 kΩ,	±3.0	±3.6		V
		–40°C ≤ T_A ≤ +85°C	±3.0	±3.35		V
Output Current - Continuous	I_{OUT}		±40			mA
Peak Output Current	I_{OUTP}	Note 2		±75		mA
TRANSFER CHARACTERISTICS						
Gain	A_{VCL}	R_L = 2 kΩ,	0.995	0.9977	1.005	V/V
		–40°C ≤ T_A ≤ +85°C	0.995		1.005	V/V
Gain Linearity	NL	R_L = 1 kΩ		0.005		%
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V	76	93		dB
		–40°C ≤ T_A ≤ +85°C	76	93		dB
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞		6.60	8	mA
		–40°C ≤ T_A ≤ +85°C		6.70	8	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, C_L = 70 pF		2000		V/µs
Bandwidth	BW	–3 dB, C_L = 20 pF, R_L = ∞		100		MHz
Bandwidth	BW	–3 dB, C_L = 20 pF, R_L = 1 kΩ		100		MHz
Bandwidth	BW	–3 dB, C_L = 20 pF, R_L = 150 Ω		100		MHz
Differential Phase		f = 3.58 MHz, R_L = 150 Ω		0.13		Degrees
		f = 4.43 MHz, R_L = 150 Ω		0.15		Degrees
Differential Gain		f = 3.58 MHz, R_L = 150 Ω		0.04		%
		f = 4.43 MHz, R_L = 150 Ω		0.06		%
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		4		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		2		pA/√Hz

NOTE

[1]Long term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at +125 °C, with an LTPD of 1.3.

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}	V_S = ±15 V	1	mV max
	V_{OS}	V_S = ±5 V	2	mV max
Input Bias Current	I_B	V_{CM} = 0 V	5	µA max
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±18 V	76	dB
Output Voltage Range	V_O	R_L = 150 Ω	±10.5	V min
Supply Current	I_{SY}	V_O = 0 V, R_L = 2 kΩ	8.5	mA max
Gain	A_{VCL}	V_O = ±10 V, R_L = 2 kΩ	1 ± 0.005	V/V

NOTE
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Input Voltage . . . . . ±18 V
Maximum Power Dissipation . . . . . See Figure 16
Storage Temperature Range
  Z Package . . . . . –65°C to +175°C
  P, S Package . . . . . –65°C to +150°C
Operating Temperature Range
  BUF04Z . . . . . –55°C to +125°C
  BUF04S, P . . . . . –40°C to +85°C
Junction Temperature Range
  Z Package . . . . . –65°C to +150°C
  P, S Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

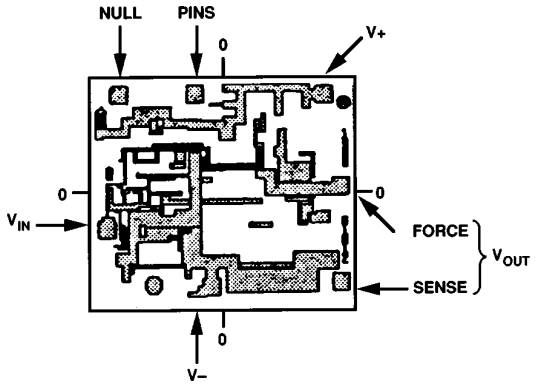
Package Type	θ_{JA}[2]	θ_{JC}	Units
8-Pin Cerdip (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
BUF04AZ/883	–55°C to +125°C	Cerdip	Q-8
BUF04GP	–40°C to +85°C	Plastic DIP	N-8
BUF04GS	–40°C to +85°C	SO	SO-8
BUF04GBC	+25°C	DICE	DICE

DICE CHARACTERISTICS



BUF04 Die Size 0.075 x 0.064 inch, 5,280 Sq. Mils Substrate (Die Backside) Is Connected to V+ Transistor Count 45.

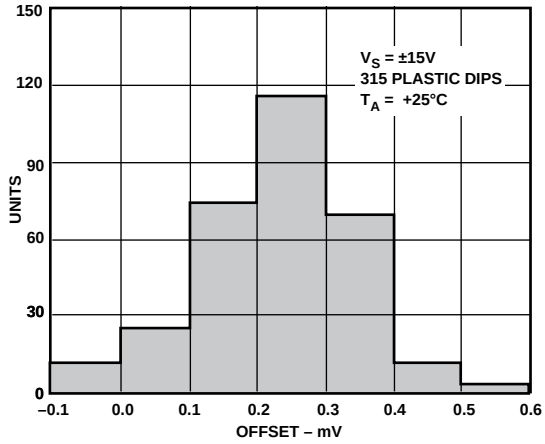


Figure 1. Input Offset Voltage (V_{OS}) Distribution @ ±15 V, P-DIP

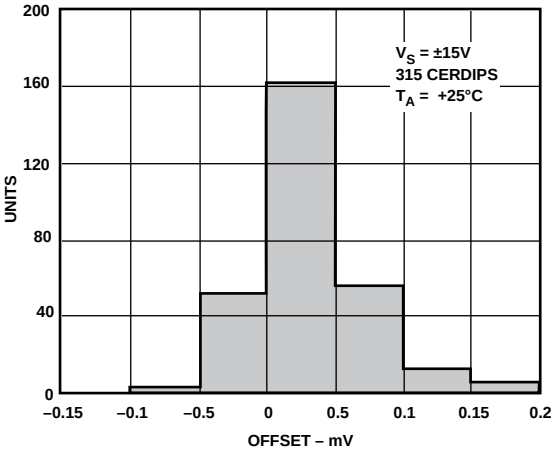


Figure 4. Input Offset Voltage (V_{OS}) Distribution @ ±15 V, Cerdip

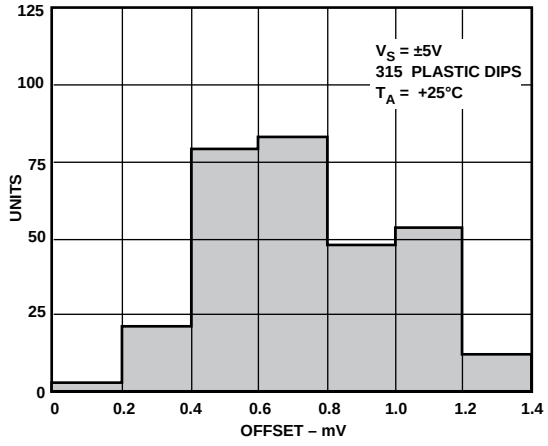


Figure 2. Input Offset Voltage (V_{OS}) Distribution @ ±5 V, P-DIP

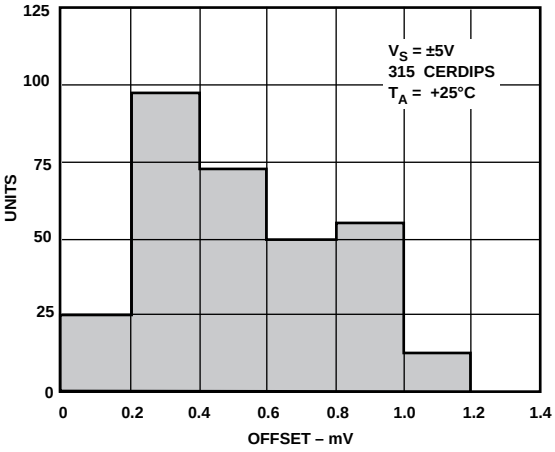


Figure 5. Input Offset Voltage (V_{OS}) Distribution @ ±5 V, Cerdip

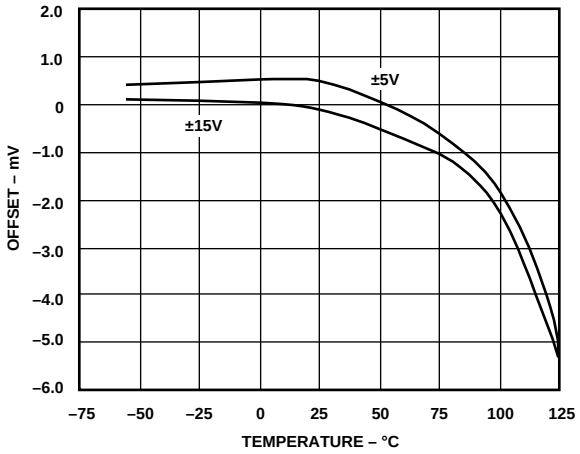


Figure 3. Input Offset Voltage (V_{OS}) vs. Temperature

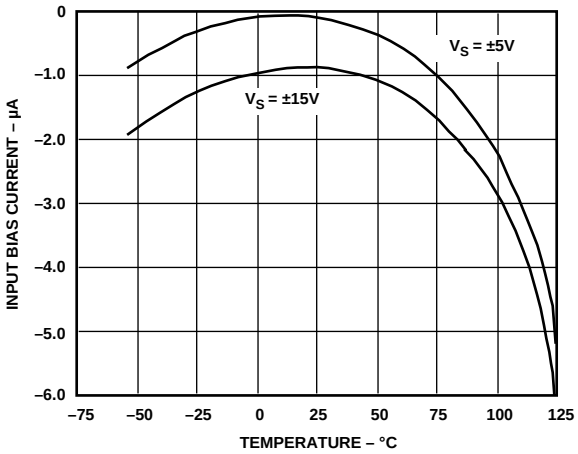


Figure 6. Input Bias Current vs. Temperature

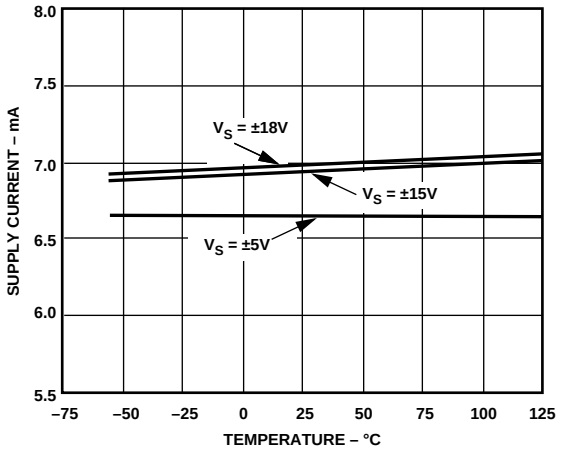


Figure 7. Supply Current vs. Temperature

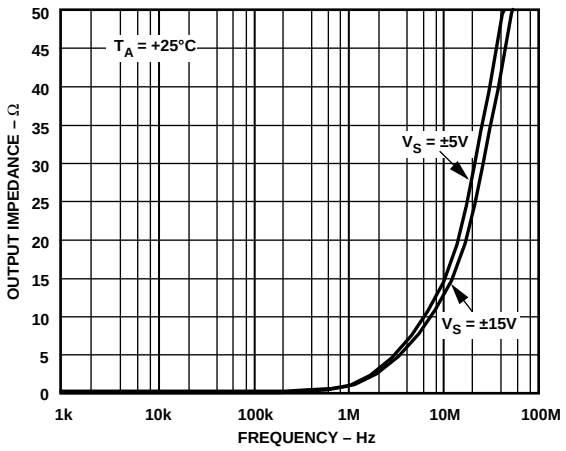


Figure 10. Output Impedance vs. Frequency

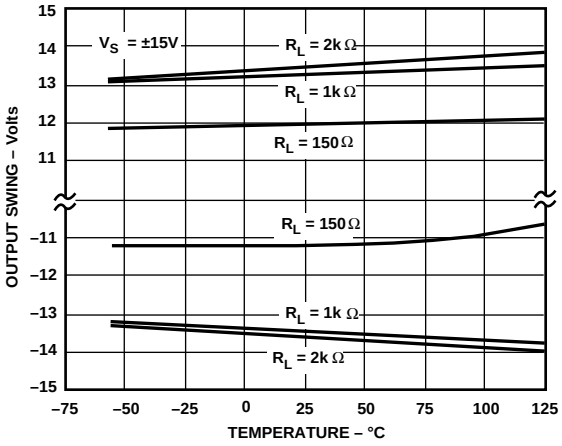


Figure 8. Output Voltage Swing vs. Temperature @ ±15 V

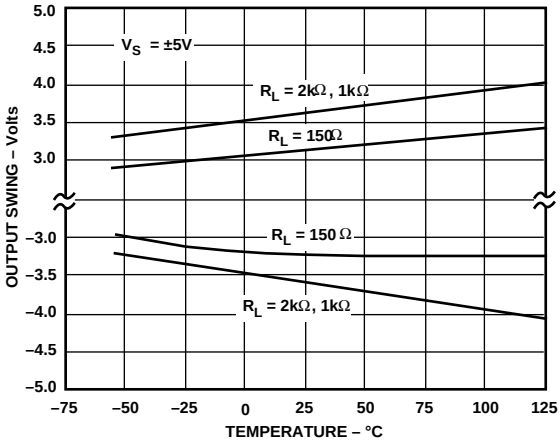


Figure 11. Output Voltage Swing vs. Temperature @ ±5 V

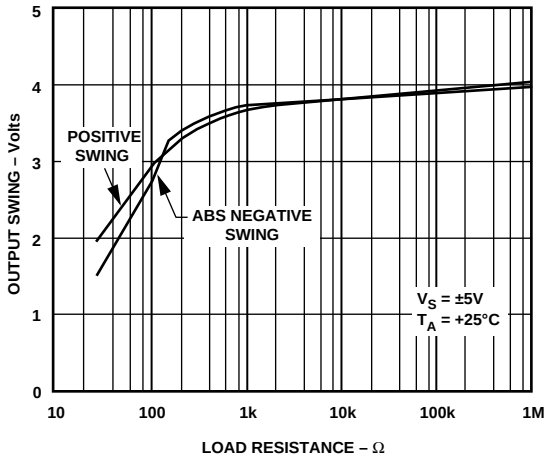


Figure 9. Maximum V_{OUT} Swing vs. Load @ ±5 V

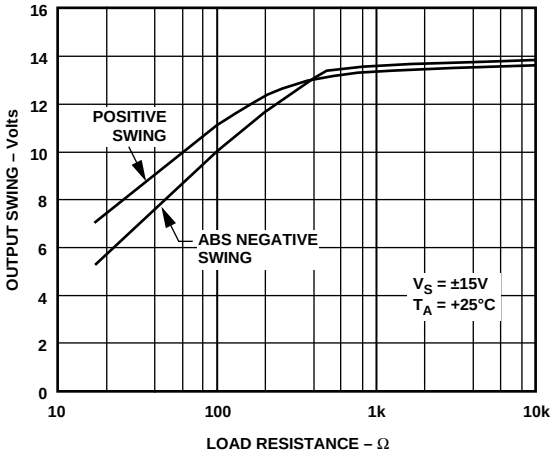


Figure 12. Maximum V_{OUT} Swing vs. Load @ ±15 V

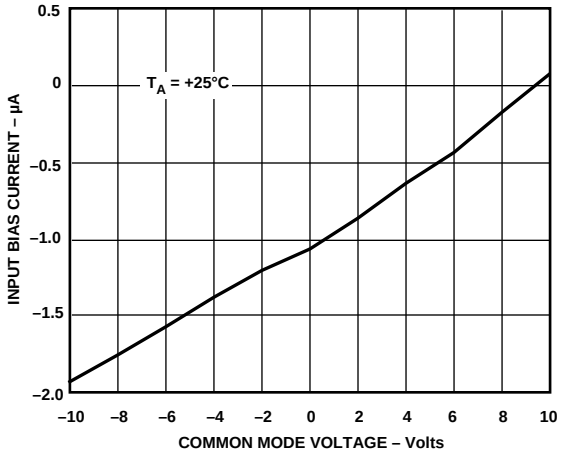


Figure 13. Bias Current vs. Input Voltage

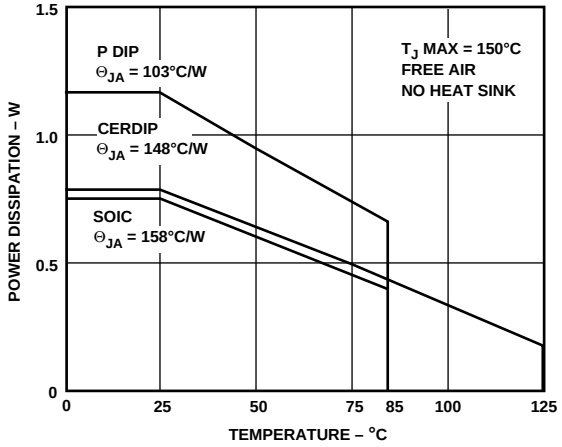


Figure 16. Maximum Power Dissipation vs. Ambient Temperature

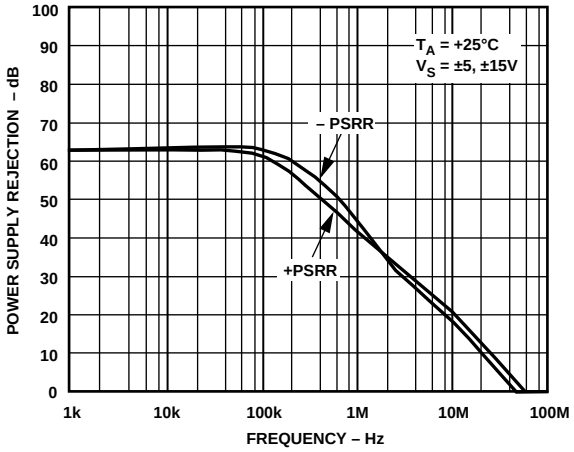


Figure 14. Power Supply Rejection vs. Frequency

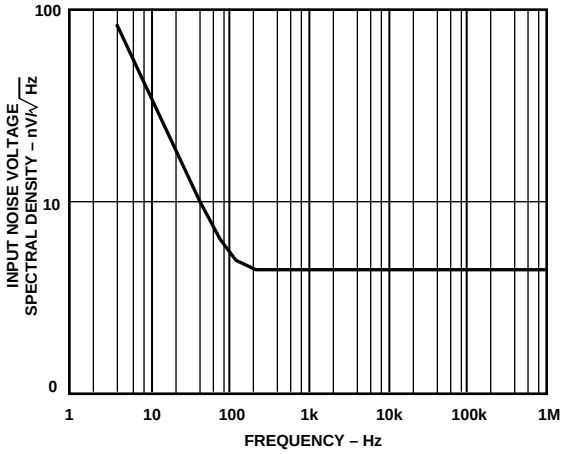


Figure 17. Input Noise Voltage vs. Frequency

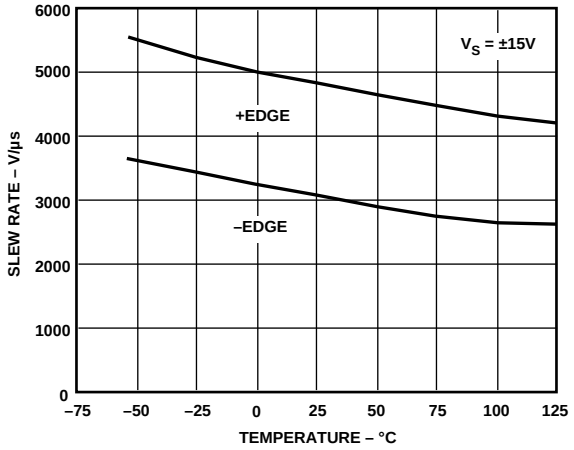


Figure 15. Slew Rate vs. Temperature

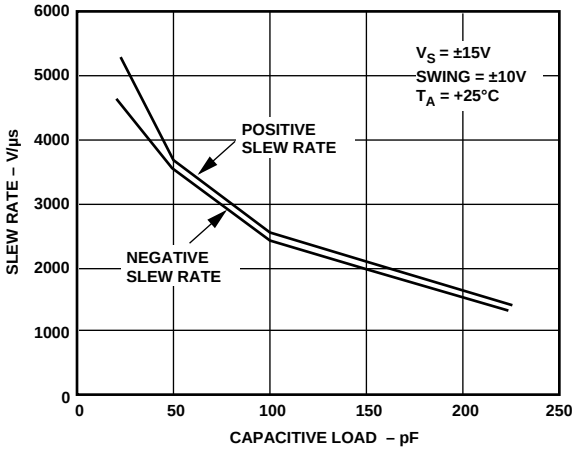


Figure 18. Slew Rate vs. Capacitive Loads

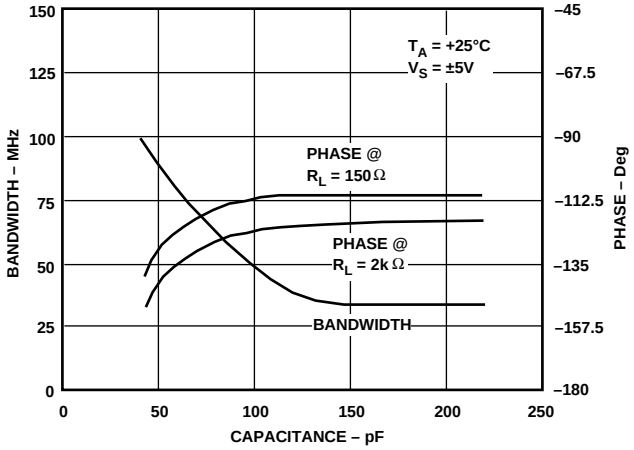


Figure 19. Bandwidth and Phase vs. Capacitive Loads @ ±5 V

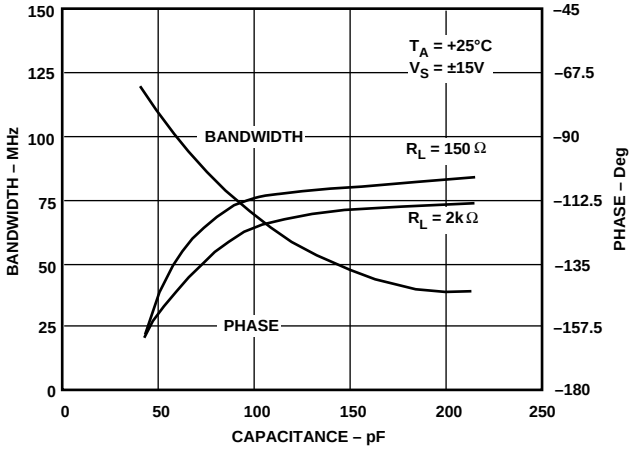


Figure 22. Bandwidth & Phase vs. Capacitive Loads @ ±15 V

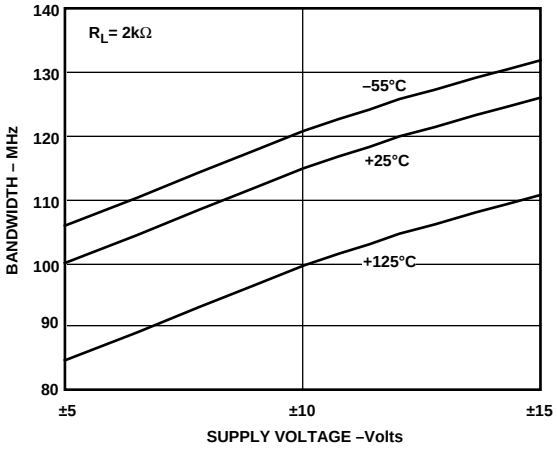


Figure 20. Bandwidth vs. Supply Voltage and Temperature

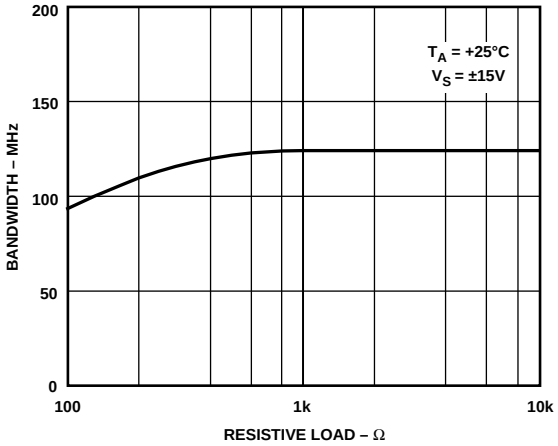


Figure 23. Bandwidth vs. Loads

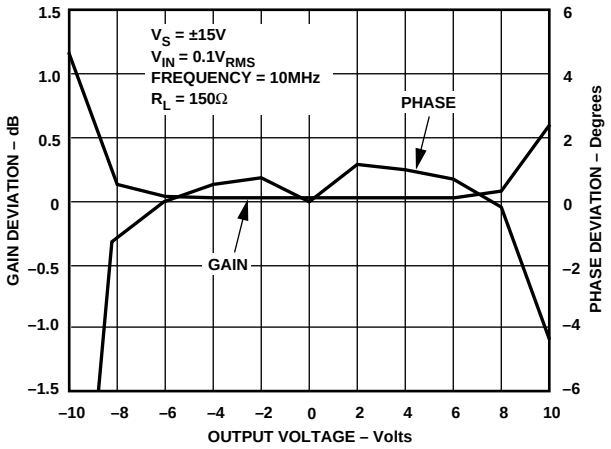


Figure 21. Gain and Phase Deviation, R_L = 150 Ω

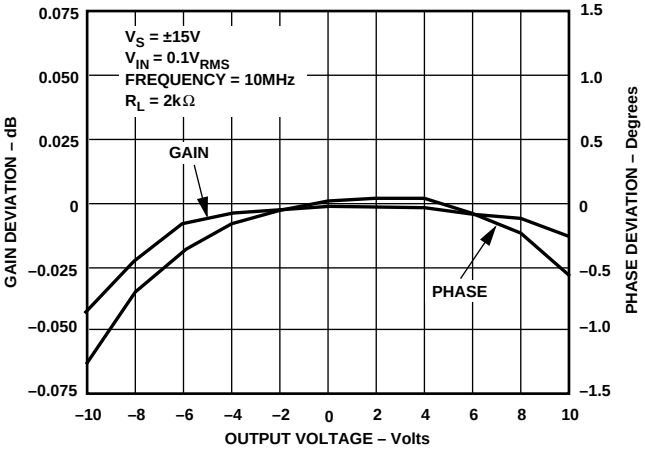
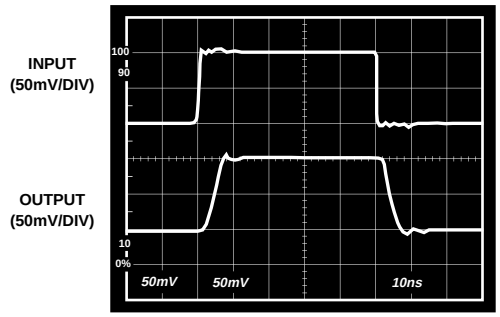
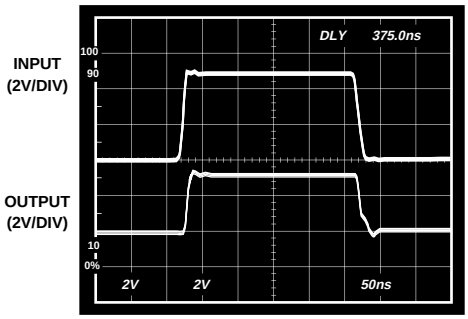


Figure 24. Gain and Phase Deviation, R_L = 2 kΩ



V_S = ±15V, R_L = 2kΩ, C_L = 15pF

Figure 25. Small-Signal Transient Response



V_S = ±15V, R_L = 2kΩ, C_L = 15pF

Figure 26. Large-Signal Transient Response

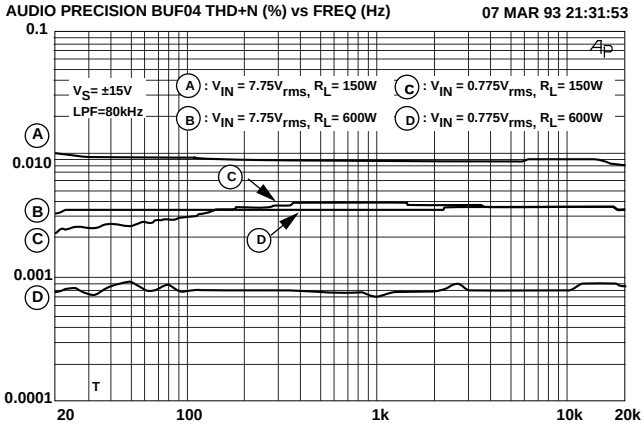


Figure 27. THD + Noise vs. Amplitude

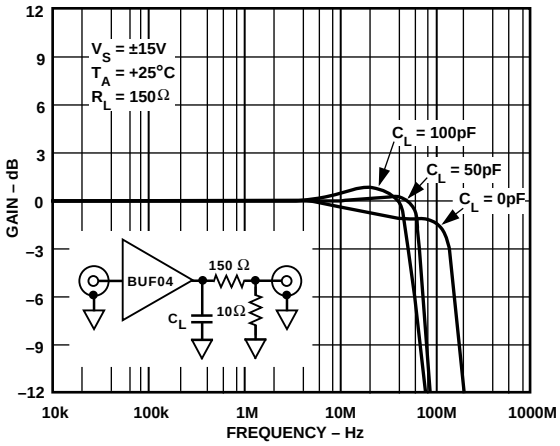


Figure 28. Bandwidth vs. Frequency

FUNCTIONAL DESCRIPTION

The BUF04 is a closed-loop voltage buffer based on a current feedback architecture. Its high open-loop transimpedance, high output current drive capability, and its low input offset voltage makes it useful in a variety of applications, such as buffering the inputs of sampling and flash A/D converters, audio and video line drivers, active filters, and precision op amp hoosters.

A transistor-level equivalent circuit for the BUF04 is illustrated in Figure 29. The input stage consists of a pair of emitter follower transistors, Q1 and Q2, whose outputs drive a second set of transistors, Q3 and Q4. The emitters of Q3 and Q4 are connected together through diodes, D1 and D2, to form a low impedance input for the feedback signal (in current mode) from the output stage. The outputs of Q3 and Q4 are then "mirrored" to Q5 and Q6 which form the gain stage of the BUF04. The signal is taken from the collectors of Q5 and Q6 which drive a "Darlington-connected" output stage made up of transistors Q7-Q10. Three R-C networks (R1–C1, R2–C2, and R3–C3) form feed-forward paths which bypass certain sections of the BUF04 for improved high frequency performance and capacitive load drive capability. Since the signal conveyed internally in the BUF04 is a current, the frequency response and slew rate of the BUF04 are insensitive to supply voltage variations.

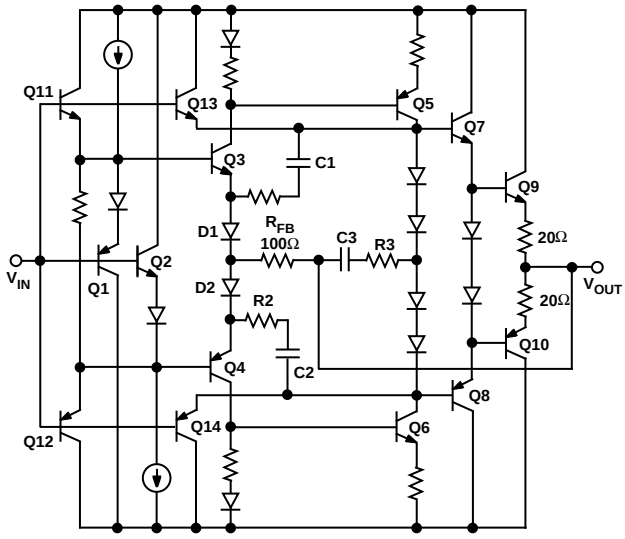


Figure 29. Transistor-Level Equivalent Circuit

An interesting feature of the BUF04 architecture is the use of "slew-enhancement" transistors, Q11–Q14. Under normal small signal (V_{IN} < 2 V_{be}s) conditions, these transistors are normally "OFF." In large signals, high speed transient applications where the input signal is > 2 V_{be}s, these transistors turn on and literally "brute-force" the output to follow the input. When the input signal drops below 2 V_{be}s, the transistors return to their normally "OFF" state.

A two-terminal equivalent circuit of the BUF04 is shown in Figure 30 where the transistor-level equivalent circuit is reduced to its essential elements. The input stage develops a signal current, I_{IN}, that is replicated by an internal current conveyor so as to flow through R_t, the transimpedance of the BUF04. The voltage developed across R_t is buffered by a unity-gain output voltage follower. With an open-loop R_t of 400 kΩ and an R_{IN} of 30 Ω, the voltage gain of the BUF04, given by the ratio R_t/R_{IN} is approximately 13,000—accurate to approximately 13.5 bits. The BUF04's open-loop ac transimpedance response is determined by the open-loop pole formed by R_t and C_t. Since C_t is typically 8 pF, the open-loop pole occurs at approximately 50 kHz.

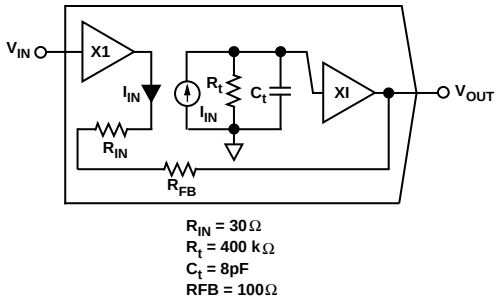


Figure 30. Current-Feedback Functional Equivalent Circuit of the BUF04

Grounding and Bypassing Considerations

To take full advantage of the BUF04's very wide bandwidth, high slew rates, and dynamic range capabilities requires due diligence with regard to supply bypassing. In high speed circuits, the supply bypassing network must provide a very low impedance return path for currents flowing to and from the load network. As with any high speed application, multiple bypassing is always recommended. A 10 µF tantalum electrolytic in parallel with a 0.1 µF ceramic capacitor is sufficient for most applications. For those high speed applications where output load currents approach 50 mA, small valued resistors (1.1 Ω to 4.7 Ω) in series with the tantalum capacitors may improve circuit transient response by damping out the capacitor's self-inductance. Figure 31 illustrates bypassing recommendations.

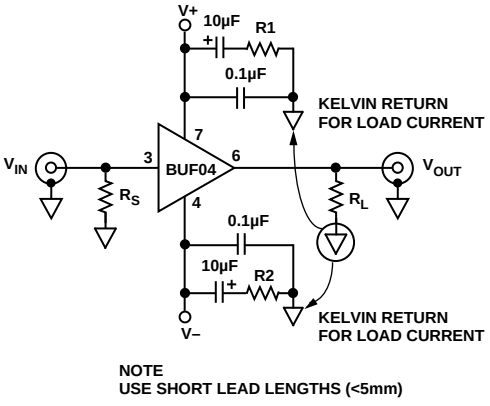


Figure 31. Recommended Power-Supply Bypassing

To minimize the effects of high-frequency coupling, circuits must be built with short interconnect leads, and large ground planes should he used whenever possible to provide a low resistance, low-inductance circuit path. Sockets should be avoided because the increased interlead capacitance can degrade bandwidth and stability. If sockets are necessary, individual pin sockets (oftentimes called "cage jacks," AMP Part No. 5-330808-3 or 5-330808-6) should be used. They contribute far less stray reactance than molded socket assemblies.

Offset Voltage Nulling

Although the offset voltage of the BUF04 is very low (1 mV, maximum) for such a high speed buffer, the circuit shown in Figure 32 can be used if additional offset voltage nulling is required. A potentiometer ranging from 1 k to 10 k can be used for V_{OS} nulling; with a 10 kΩ potentiometer, the trim range is ±30 mV.

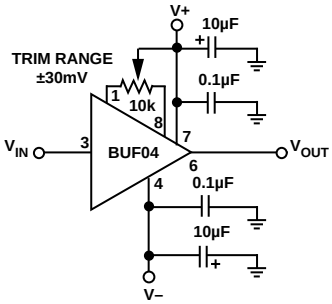


Figure 32. Optional Offset Voltage Nulling Scheme

APPLICATIONS

Output Short-Circuit Protection

To optimize the transient response and output voltage swing of the BUF04, internal output short-circuit current limiting was omitted. Although the BUF04 can provide continuous output currents of 50 mA without protection, direct connection of the BUF04's output to ground or to the supplies will destroy the device. An active current limit technique, illustrated in Figure 33, provides the necessary short-circuit protection while retaining full dc output voltage swing to the load.

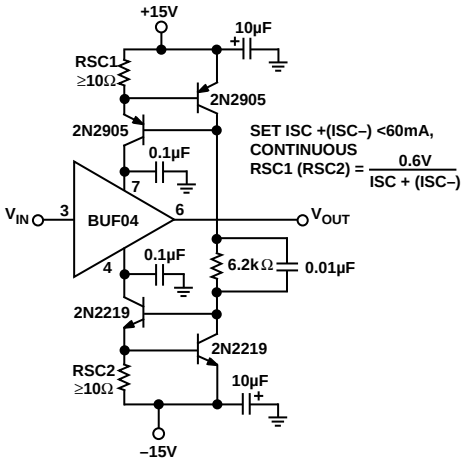


Figure 33. Short-Circuit Current Limiting Using Current Sources

Output Current Transient Recovery

Settling characteristics of high speed buffers also include the buffer's ability to recover, i.e., settle, from a transient output current load condition. When driving the input of an A/D converter, especially the successive-approximation converter types, the buffer must maintain a constant output voltage under dynamically changing load current conditions. In these types of converters, the comparison point is usually diode-clamped, but it may deviate several hundred millivolts resulting in high frequency modulation of the A/D input current. Open-loop and closed-loop buffers (also, op amps configured as followers) that exhibit high closed-loop output impedances and/or low unity gain crossover frequencies recover very slowly from output load current transients. This slow recovery leads to linearity errors or missing codes because of errors in the instantaneous input voltage. Therefore, the buffer (or op amp) chosen for this type of application should exhibit low output impedance and high unity gain bandwidth so that its output has had a chance to settle to its nominal value before the converter makes its comparison.

The circuit in Figure 34 illustrates a settling measurement circuit for evaluating the recovery time of high speed buffers from an output load current transient. The input to the buffer is grounded for ease of measuring the recovery time, and two resistors are used to sum steady-state and transient load currents at the output. As a worst-case condition, R1, was chosen such that the BUF04 would source (or sink) a steady-state current of 25 mA. R2 was then chosen to add a 10 mA transient current upon the steady-state value. To set accurately the nodal voltages internal to the BUF04, the supply voltages were offset by the voltage applied to R1. Because of its high transimpedance, wide bandwidth, and low output impedance, the BUF04 exhibits an extremely fast recovery time of 60 ns to 0.01%, as shown in Figure 34. Results were identical regardless whether the BUF04 was sourcing or sinking current.

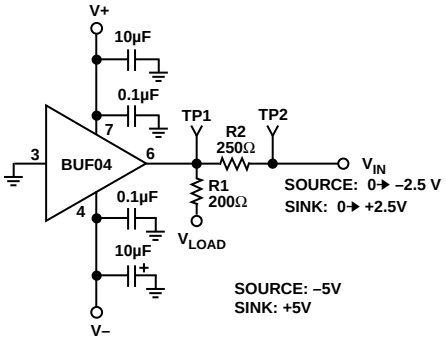


Figure 34. Transient Output Load Current Test Circuit

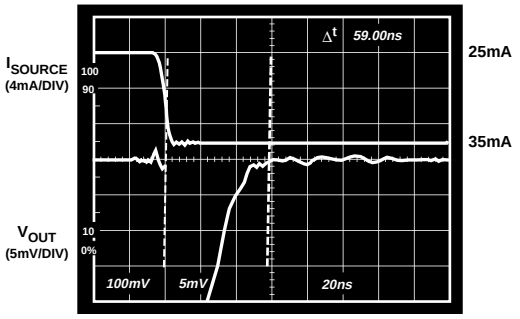
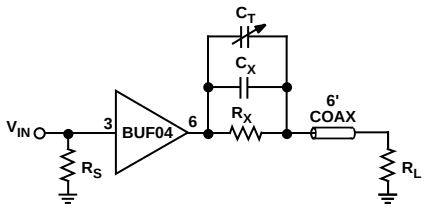


Figure 35. BUF04's Output Load Current Recovery Time

Terminated Line Drivers

The BUF04's high output current, large slew rate, and wide bandwidth all combine to make it an ideal device for high speed line driver applications. As shown in Figure 36, the BUF04 can be configured for driving doubly terminated 50 Ω and 75 Ω cables. To optimize the circuit's pulse response, a capacitor, C_T (C_X + C_{TRIM}), is connected across the series back termination. The BUF04 can drive a 50 Ω line to ±2.5 V and a 75 Ω line to ±3.75 V when operating on ±15 V supplies.



Z_O	COAX	R_S, R_L	R_X	C_X	C_T
50Ω	RG-58	50Ω	50	91pF	3–15pF
75Ω	RG-59	75Ω	75	62pF	3–15pF

Figure 36. Line Driver Configuration

Low-Pass Active Filter

In many signal-conditioning applications, filters are required to band-limit noise or altogether eliminate other unwanted signals prior to conversion. Often, high frequency filters are needed for these applications; however, there are few op amps that exhibit the high open-loop gain and wide unity-gain crossover frequency required for these applications. As illustrated in Figure 37, the BUF04 and a handful of passive components can be configured as a high frequency, low-pass active filter. Since the filter configuration is a unity-gain Sallen-Key topology, the BUF04 is particularly well suited for this application. In this circuit, an additional resistor, R3, was added to prevent interaction between C2 and the BUF04's input capacitance.

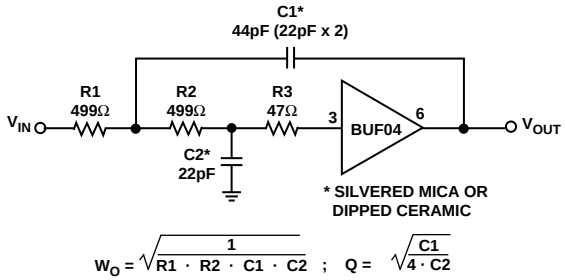


Figure 37. A 10 MHz Low-Pass Active Filter

Operation Within an Op Amp Feedback Loop

The BUF04 is well suited as a current booster or isolation buffer within the closed loop of precision op amps such as the OP177, the OP97, the OP27, or the OP77. Since the BUF04 is a closed loop voltage buffer, no interstage coupling resistor between the op amp and the buffer's input is required for circuit stability. The wide bandwidth and high slew rate of the BUF04 assure that the loop has the characteristics of the op amp; hence, no additional rolloff is required.

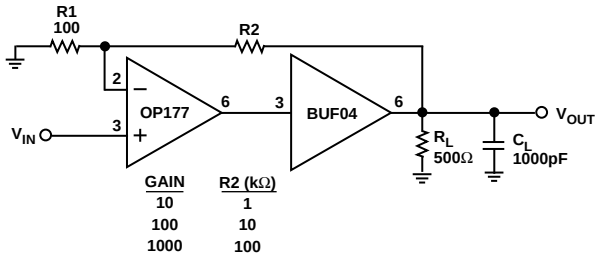


Figure 38. BUF04 as Booster Stage for a Precision Op Amp

Paralleling BUF04s for Increased Load Drive Capability

In applications where continuous output currents greater than 50 mA are required or where heat management is an issue, a number of BUF04s can be connected in parallel to reduce the drive requirement of any one buffer. An example of one such application is illustrated in Figure 39. In this circuit, the BUF04s are required to drive a doubly terminated 50 Ω line to ±5 V. This type of a load for a single BUF04 would certainly cause a power dissipation problem. Parallel operation results in lower input and output impedances and increased bias currents; on the other hand, input equivalent noise voltage is reduced and input offset voltage remains unchanged.

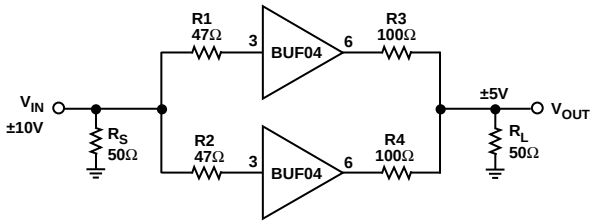


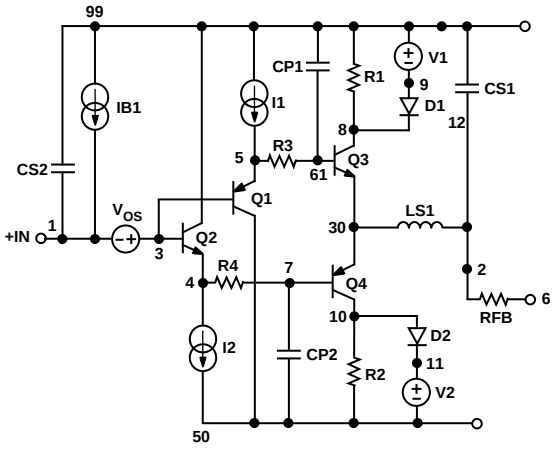
Figure 39. Paralleling BUF04s for High Output Currents

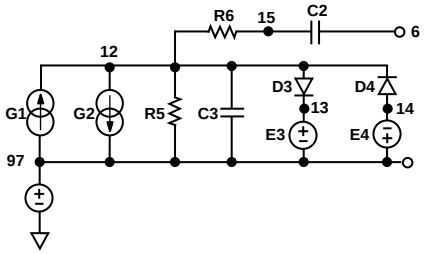
Overdrive Recovery and Phase Reversal

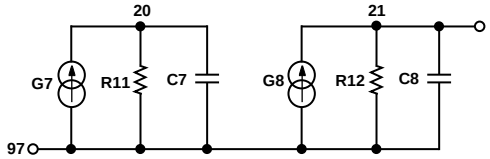
In applications where the inputs could be driven to the supply rails, the BUF04 recovers in 10 ns from positive or negative overdrive. The BUF04 does not exhibit any output voltage phase reversal when the input signal exceeds its input voltage range.

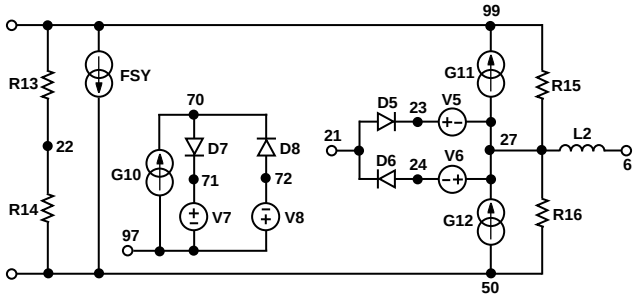
```
* BUF04 SPICE Macro-model                    7/93, Rev. A
*                                           JCB / PMI
*
* Copyright 1993 by Analog Devices, Inc.
*
*
* Node assignments
*                       noninverting input
*                       |       positive supply
*                       |       |       negative supply
*                       |       |       |       output
*                       |       |       |       |
*                       |       |       |       |
.SUBCKT BUF04   1       99      50      6
*
* INPUT STAGE
*
R1      99      8       200
R2      10      50      200
V1      99      9       4.4
D1      9       8       DX
V2      11      50      4.4
D2      10      11      DX
I1      99      5       1.8E-3
I2      4       50      1.8E-3
Q1      50      3       5       QP
Q2      99      3       4       QN
Q3      8       61      30      QN
Q4      10      7       30      QP
R3      5       61      50E3
R4      4       7       50E3
CP1     61      99      14E-15
CP2     7       50      14E-15
RFB     6       2       100
*
* INPUT ERROR SOURCES
*
IB1     99      1       0.7E-6
VOS     3       1       0.7E-6
LS1     30      2       1E-9
CS1     99      2       2.0E-12
CS2     99      1       3.0E-12
*
EREF    97      0       22 0 1
*
* TRANSCONDUCTANCE STAGE
*
R5      12      97      365E3
C3      12      97      8E-12
G1      97      12      99 8 SE-3
G2      12      97      10 50 SE-3
E3      13      97      POLY(1)  99   97 –2.5   1.1
E4      97      14      POLY(1)  97   50 –2.5   1.1
D3      12      13      DX
D4      14      12      DX
R6      12      15      200
C2      15      6       20E-12
*
* POLE AT 200 MHz
*
R11     20      97      1E6
C7      20      97      0.759E-15
G7      97      20      12  22  1E-6
*
* POLE AT 200 MHz
*
R12     21      97      1E6
C8      21      97      0.759E-15
G8      97      21      20  22  1E-6
*
* OUTPU T STAGE
*
FSY     99      50      POLY(2) V7 V8 1.85E-3 1 1
R13     22      99      16.67E3
R14     22      50      16.67E3
R15     27      99      80
R16     27      50      80
L2      27      6       10E-9
G11     27      99      99 21 12.5E-3
G12     50      27      21 50 12.5E-3
V5      23      27      3.3
V6      27      24      3.3
D5      21      23      DX
D6      24      21      DX
G10     97      70      27 21 12.5E-3
D7      70      71      DX
D8      72      70      DX
V7      71      97      DC 0
V8      97      72      DC 0
*
* MODELS USED
*
.MODEL QN NPN(BF= 1000 IS= 1E-15)
.MODEL QP PNP(BF= 1000 IS= 1E-15)
.MODEL DX D(IS= 1E-15)
.ENDS BUF04
```

BUF04 SPICE





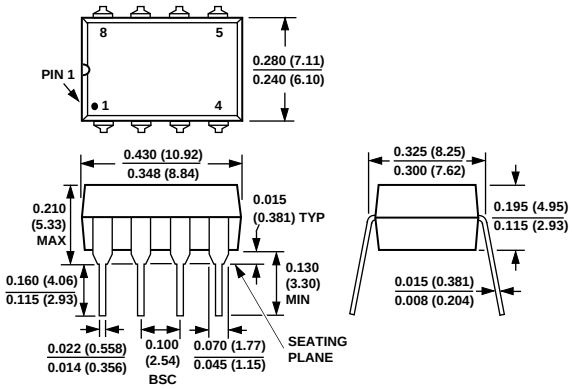




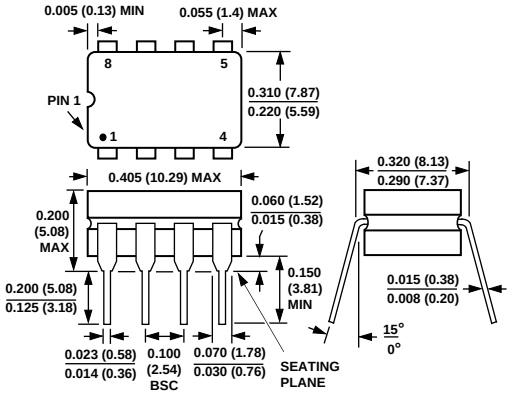
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

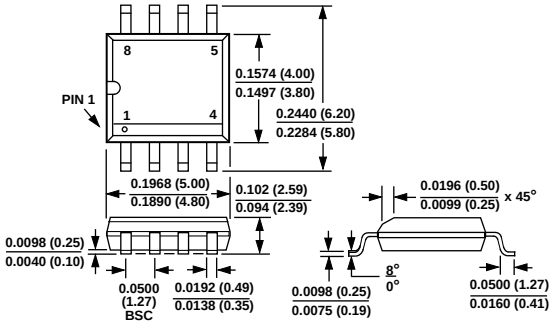
8-Lead Plastic DIP (N-8)



8-Lead Cerdip (Q-8)



8-Lead Narrow-Body SO (R-8)



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