

BIPOLAR ANALOG INTEGRATED CIRCUIT μ PC666

7:28

3 CHANNEL D/A CONVERTER FOR VIDEO PROCESSING

DESCRIPTION

μPC666 is a video 6-bit 3-channel digital analog converter having the following features: High speed and high precision bipolar processing technology for excellent performance of 35 MHz, ±0.5 LSB (MAX.); three channels of identical digital analog converters; power consumption minimized to 175 mW (TYP.); because the three channels are laid out on the same chip, little deviation among the converters, ideal for processing RGB, R-Y, B-Y, and Y signals, where strict deviation control is essential; and reference voltage generating circuit for simplified circuit configuration.

FEATURES

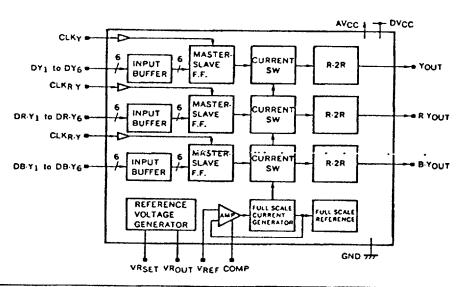
- 6-bit digital analog converter
- Clock rate: 35 Msps
- Conversion precision: ±0.5 LSB (MAX.)
- 5 V single power supply
- 3 channels incorporated
- Reference voltage generating circuit incorporated
- Power consumption: 175 mW (TYP.)

ORDERING INFORMATION

PART NUMBER	PACKAGE	QUALITY GRADE
μPC666GS	36 Pin Plastic SOP (300 mil)	Stendard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

BLOCK DIAGRAM



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FROM 半導体応用技術本部 ΤO dept 665

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ページ 03 TOTAL :10

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Power Voltage	AVCC, DVCC	-0.3 to +6.0	V
Pin Input Voltage	VIN	-0.3 to V _{CC} +0.3	V
Operation Temperature Range	Topt	-20 to +75	°c
Storage Temperature Range	Tstg	-40 to +125	°c
Package Allowable Loss	PD	560	mW

RECOMMENDED OPERATING CONDITIONS (Ta = -20 to +75 °C)

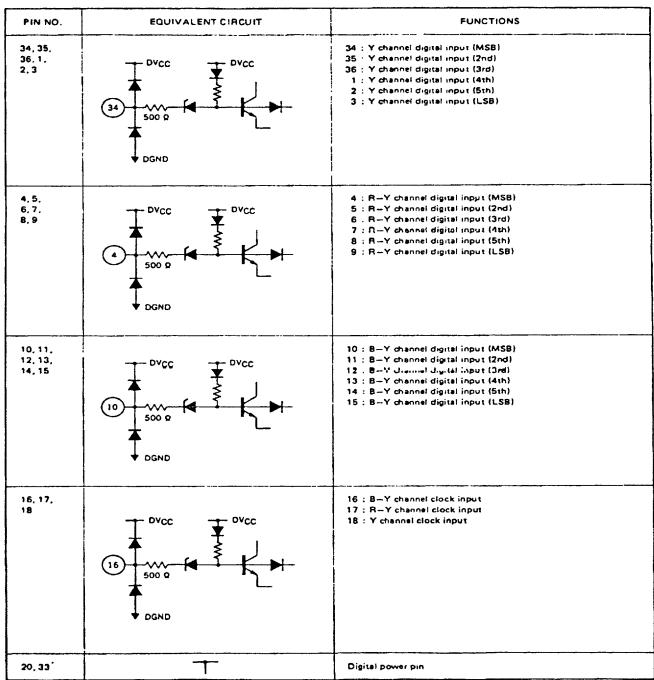
ITEM	SYMBOL	MIN,	TYP.	MAX.	UNIT	TEST CONDITION
Power Voltage	AVCC, DVCC	4.75	5.0	5.25	V	AGNO - DGND - 0
Analog Reference Voltage	VREF	3.70	4.00	4.30	V	
Digital Input High Level Voltage	VINDH	2.0	 	1 -	V	
Digital Input Low Level Voltage	VINDL	-	† -	0.8	V	
Sampling Frequency	†samp	-		35	MHz	
Data Input Set Up Time	l _s	15.0		 - -	ns	
Data Input Hold Time	th	4.0	1 -	 	ns	
Sampling Clock High Pulse Width	₹PWH	10	† · · · · · · · · · · · · · · · · · · ·	1000	ns	
Sampling Clock Low Pulse Width	1PWL	10	<u> </u>	1000	ns	
Compensation Capacity	C _{comp}	1.0	_	1 -	μF	

ELECTRIC CHARACTERISTICS (Ta = -20 to +75 °C, AVCC = DVCC = 5±0.25 V)

ITEM	SYMBOL	MIN.	TYP.	MAX	UNIT	TEST CONDITIONS
Power Cansumption	¹cc		35	49	mA	T. = 25 °C
Integral Linearity Error	1LE			±0.5	LSB	T _a = 0 to +75 °C
Differential Linearity Error	DLE			±0.5	LSB	T _a = 0 to +75 °C
Output Voltage Full-Scale Precision	Vofs	0.836	0.984	1.132	v	AVCC = DVCC = 5.0 V, VREF = 4.0 V This precision is the difference between the full-scale output voltage and zero- scale output voltage.
RG8 Output Voltage Ratio	FSR	-0.8	0	+8.0	%	
Reference Power Supply Output Voltage	VROUT	3.8	4.0	4.2	V	AVCC = DVCC = 5.0 V
Output Delay Time	۵,		15	25	n)	
Setting Time	¹ SET	<u> </u>	25	40	ns	CL # 5 pF

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DESCRIPTION OF PINS



FROM

TO

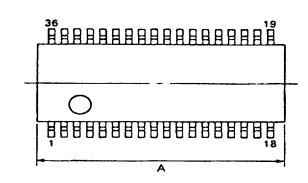
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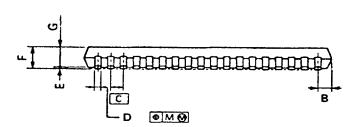
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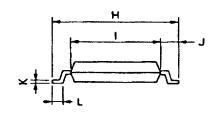
PIN NO.	EQUIVALENT CIRCUIT	FUNCTIONS
28	AVCC	R-Y signal output pin. The output resistance is approx 333 Ω (TYP.)
30	30 \$ 1 kg 500 g 1 kg 500 g	Y signal output pin. The output resistance is approximately 333 Ω (TYP.).
19, 27, 29, 31	,,,	Grounding pin

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36 PIN PLASTIC SHRINK SOP(300mil)







NOTE

Each lead centerline is located within 0-10 mm (0-004 inch) of its true position (T.P.) at maximum material condition.

P36GM-80-3008-1	
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ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0 612 MAX.
8	0.97 MAX.	0 039 MAX.
С	0.8 (T.P.)	0 031 (T.P.)
D	0.35:8%	0 014:8 883
E	0.1707	0 004 = 0 004
F	1.8 MAX	0 071MAX.
G	1.55	0.061
н	7.7 +0 3	0 303 = 0 013
1	5 6	0 220
J	1.1	0.043
К	0.20:838	0.008:888
L	06102	0 024 '8 88\$
м	0 10	0.004