



32K × 8 CMOS STATIC RAM

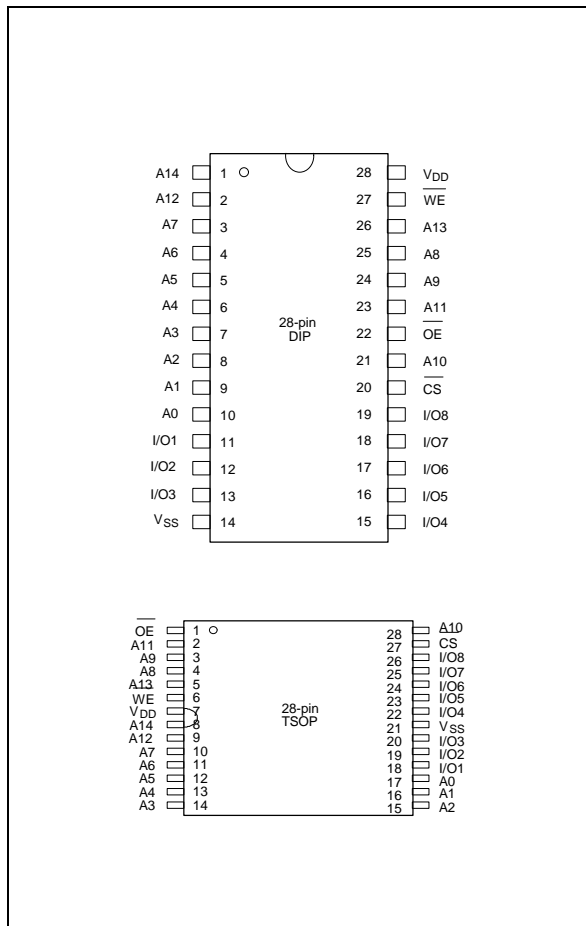
GENERAL DESCRIPTION

The W24258/LL is a normal speed, very low power CMOS static RAM organized as 32768 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

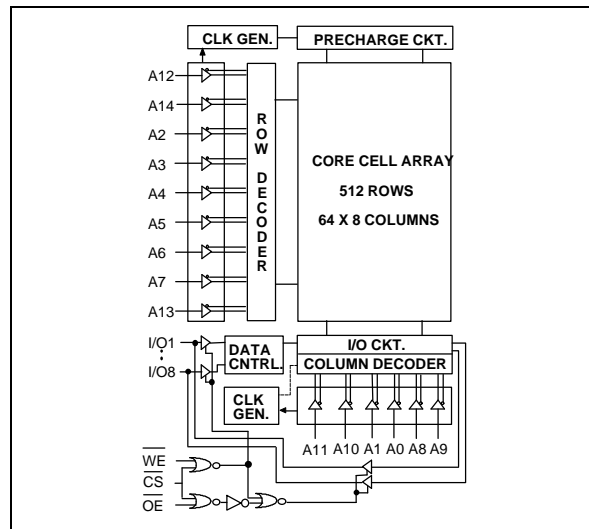
FEATURES

- Low power consumption:
 - Active: 350 mW (max.)
 - Standby: 25 μW (max.)
- Access time: 55/70 nS (max.)
- Single 5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 2V (min.)
- Packaged in 28-pin 600 mil DIP, 330 mil SOP and standard type one TSOP (8 mm × 13.4 mm)

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A14	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
\overline{CS}	Chip Select Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
VDD	Power Supply
VSS	Ground

TRUTH TABLE

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	MODE	I/O1 - I/O8	V _{DD} CURRENT
H	X	X	Not Selected	High Z	I _{SB} , I _{SB1}
L	H	H	Output Disable	High Z	I _{DD}
L	L	H	Read	Data Out	I _{DD}
L	X	L	Write	Data In	I _{DD}

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to V _{SS} Potential	-0.5 to +7.0	V
Input/Output to V _{SS} Potential	-0.5 to V _{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to 70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 5V ±10%; V_{SS} = 0V; T_A = 0° C to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.*	MAX.	UNIT	
Input Low Voltage	V _{IL}	-	-0.5	-	+0.8	V	
Input High Voltage	V _{IH}	-	+2.2	-	V _{DD} +0.5	V	
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{DD}	-1	-	+1	μA	
Output Leakage Current	I _{LO}	V _{I/O} = V _{SS} to V _{DD} , $\overline{\text{CS}}$ = V _{IH} (min.) or $\overline{\text{OE}}$ = V _{IH} (min.) or $\overline{\text{WE}}$ = V _{IL} (max.)	-1	-	+1	μA	
Output Low Voltage	V _{OL}	I _{OL} = +2.1 mA	-	-	0.4	V	
Output High Voltage	V _{OH}	I _{OH} = -1.0 mA	2.4	-	-	V	
Operating Power Supply Current	I _{DD}	$\overline{\text{CS}}$ = V _{IL} (max.), I/O = 0 I/O = 0 mA, Cycle = min. Duty = 100%	55	-	-	70	mA
			70	-	-	60	mA
Standby Power Supply Current	I _{SB}	$\overline{\text{CS}}$ = V _{IH} (min.), Cycle = min. Duty = 100%	-	-	3	mA	
	I _{SB1}	$\overline{\text{CS}}$ ≥ V _{DD} -0.2V	-	0.7	5	μA	

Note : Typical parameter is measured under ambient temperature T_A = 25° C and V_{DD} = 5V.



CAPACITANCE

(VDD = 5V, TA = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	CIN	VIN = 0V	6	pF
Input/Output Capacitance	C _{I/O}	VOUT = 0V	8	pF

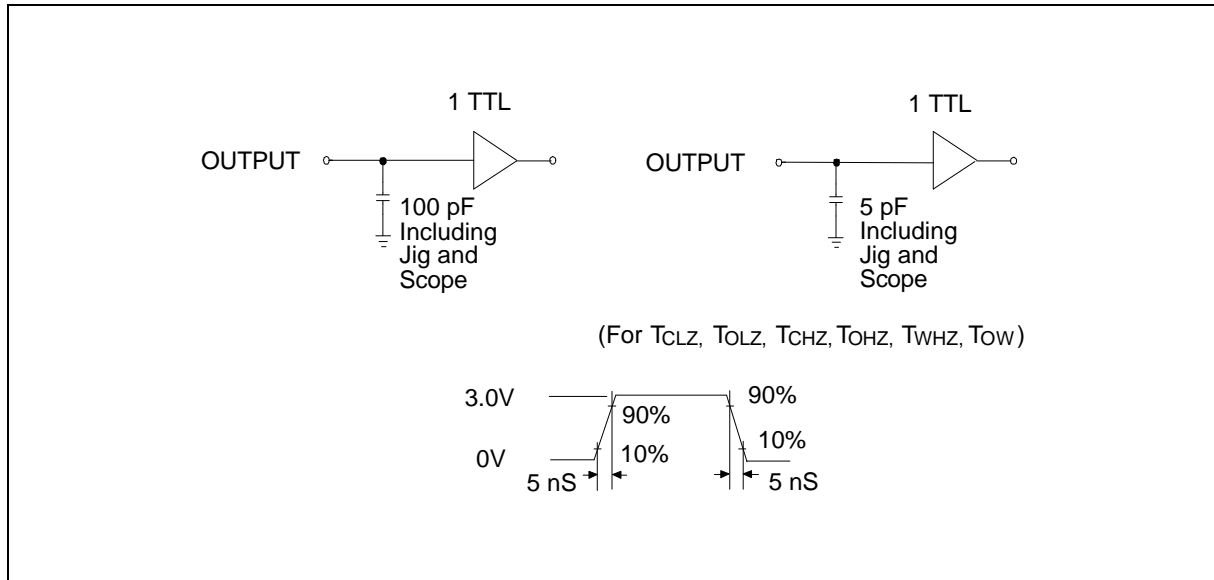
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	See the drawing below

AC TEST LOADS AND WAVEFORM





AC Characteristics, continued

(V_{DD} = 5V ±10%; V_{SS} = 0V; T_A = 0° C to 70° C)

Read Cycle

PARAMETER	SYM.	W24258-55LL		W24258-70LL		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	TRC	55	-	70	-	nS
Address Access Time	TAA	-	55	-	70	nS
Chip Select Access Time	TACS	-	55	-	70	nS
Output Enable to Output Valid	TAOE	-	27	-	35	nS
Chip Selection to Output in Low Z	TCLZ*	10	-	10	-	nS
Output Enable to Output in Low Z	TOLZ*	5	-	5	-	nS
Chip Deselection to Output in High Z	TCHZ*	-	25	-	30	nS
Output Disable to Output in High Z	TOHZ*	-	25	-	30	nS
Output Hold from Address Change	TOH	10	-	10	-	nS

* These parameters are sampled but not 100% tested

Write Cycle

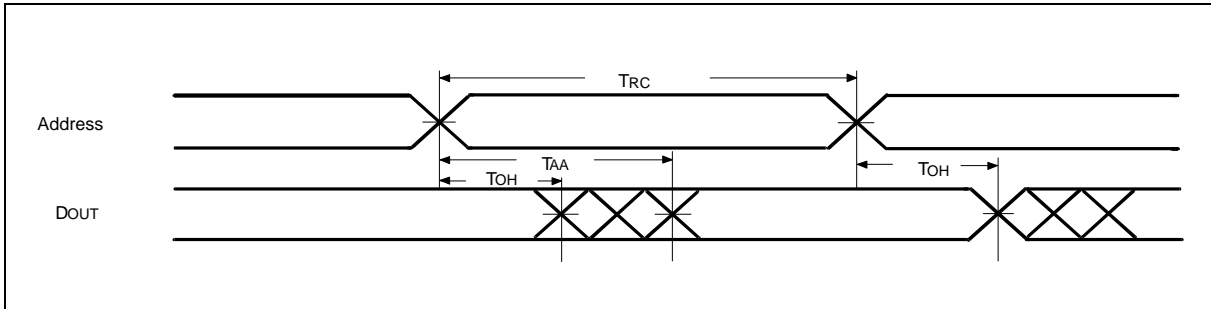
PARAMETER	SYM.	W24258-55LL		W24258-70LL		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	TWC	55	-	70	-	nS
Chip Selection to End of Write	TCW	40	-	50	-	nS
Address Valid to End of Write	TAW	40	-	50	-	nS
Address Setup Time	TAS	0	-	0	-	nS
Write Pulse Width	TWP	40	-	50	-	nS
Write Recovery Time	$\overline{\text{CS}}, \overline{\text{WE}}$ TWR	0	-	0	-	nS
Data Valid to End of Write	TDW	25	-	30	-	nS
Data Hold from End of Write	TDH	0	-	0	-	nS
Write to Output in High Z	TWHZ*	-	20	-	25	nS
Output Disable to Output in High Z	TOHZ*	-	20	-	25	nS
Output Active from End of Write	TOW	5	-	5	-	nS

* These parameters are sampled but not 100% tested

TIMING WAVEFORMS

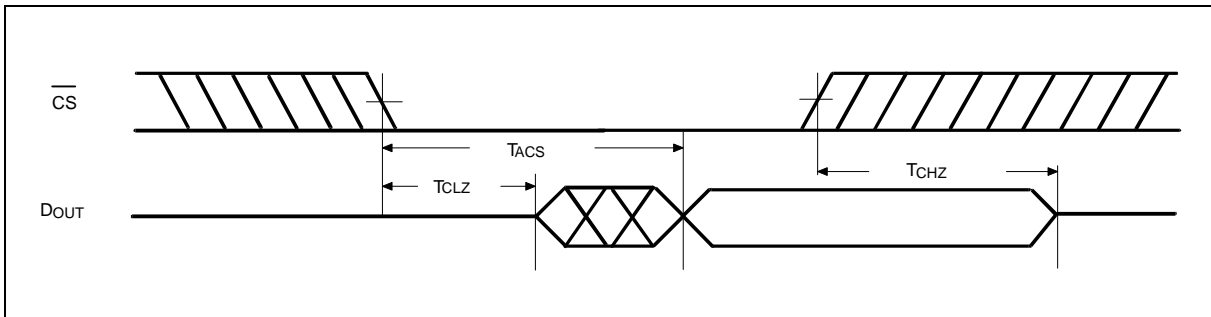
Read Cycle 1

(Address Controlled)



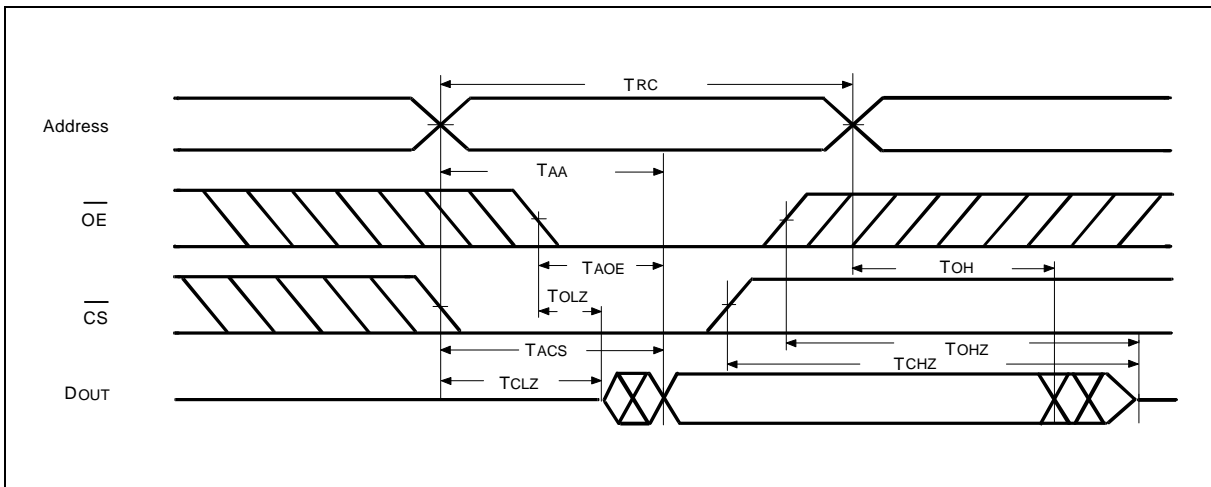
Read Cycle 2

(Chip Select Controlled)



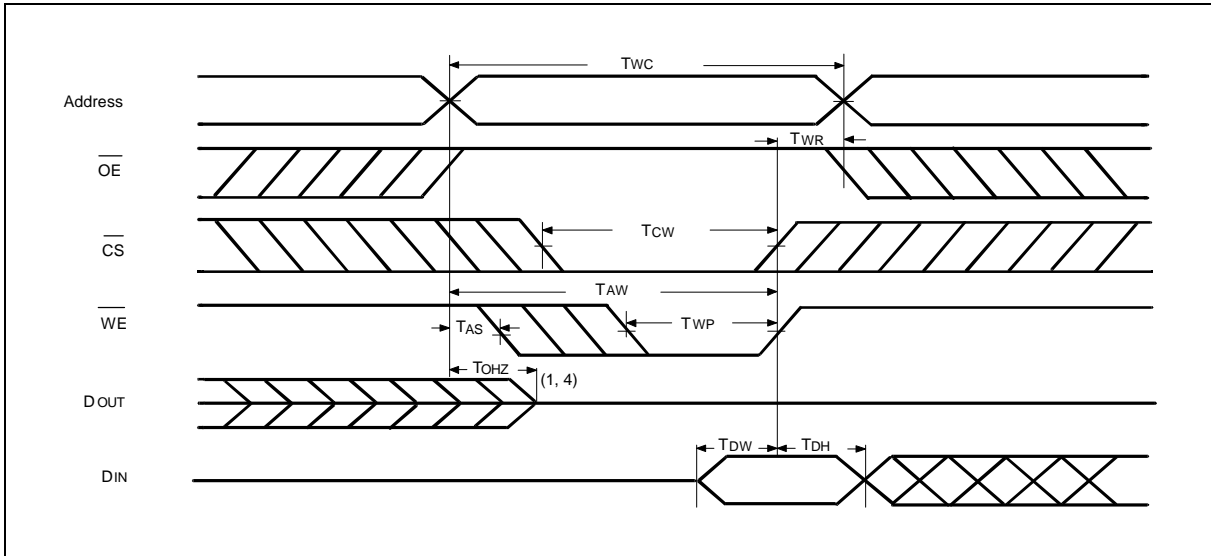
Read Cycle 3

(Output Enable Controlled)



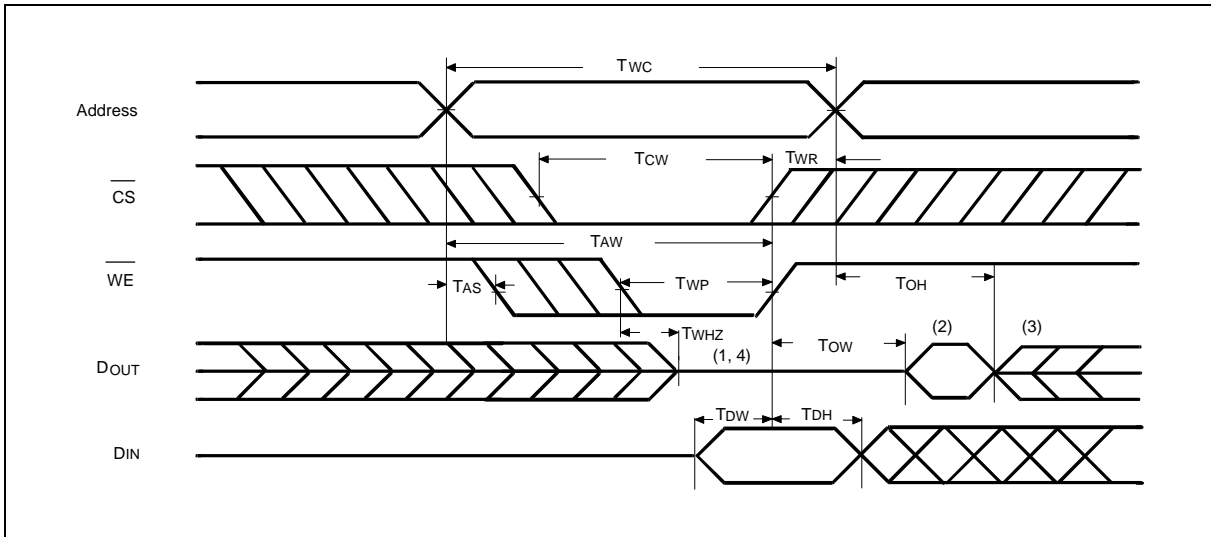
Timing Waveforms, continued

Write Cycle 1



Write Cycle 2

($\overline{OE} = V_{IL}$ Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.

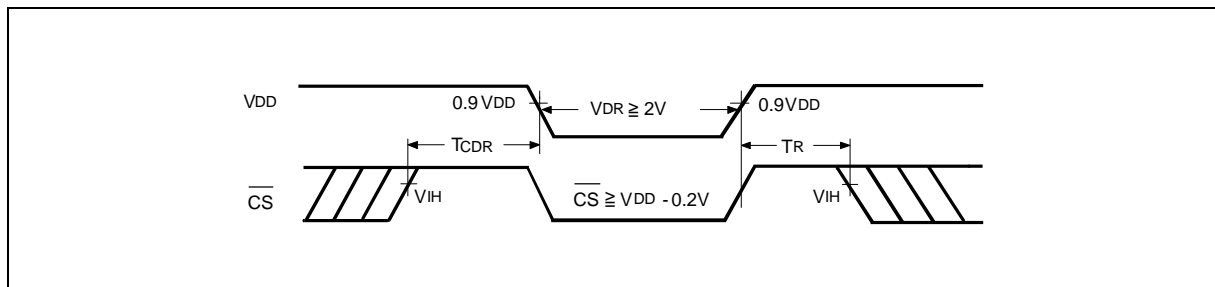
DATA RETENTION CHARACTERISTICS

(TA = 0° C to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VDD for Data Retention	VDR	$\overline{CS} \geq V_{DD} - 0.2V$	2.0	-	-	V
Data Retention Current	I _{DDDR}	$\overline{CS} \geq V_{DD} - 0.2V, V_{DD} = 3V$	-	-	2	μA
Chip Deselect to Data Retention Time	T _{CDR}	See data retention waveform	0	-	-	nS
Operation Recovery Time	T _R		T _{RC} *	-	-	nS

* Read Cycle Time

DATA RETENTION WAVEFORM



ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W24258-55LL	55	70	5	600 mil DIP
W24258-70LL	70	60	5	600 mil DIP
W24258S-55LL	55	70	5	330 mil SOP
W24258S-70LL	70	60	5	330 mil SOP
W24258Q-55LL	55	70	5	Standard type one TSOP
W24258Q-70LL	70	60	5	Standard type one TSOP

Notes:

- Winbond reserves the right to make changes to its products without prior notice.
- Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

28-pin P-DIP

Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A ₁	0.010	—	—	0.25	—	—
A ₂	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B ₁	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.460	1.470	—	37.08	37.34
E	0.590	0.600	0.610	14.99	15.24	15.49
E ₁	0.540	0.545	0.550	13.72	13.84	13.97
e ₁	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e _A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.090	—	—	2.29

Notes:

- Dimensions D Max. & S include mold flash or tie bar burrs.
- Dimension E₁ does not include interlead flash.
- Dimensions D & E₁ include mold mismatch and are determined at the mold parting line.
- Dimension B₁ does not include dambar protrusion/intrusion.
- Controlling dimension: Inches.
- General appearance spec. should be based on final visual inspection spec.

28-pin SOP Wide Body

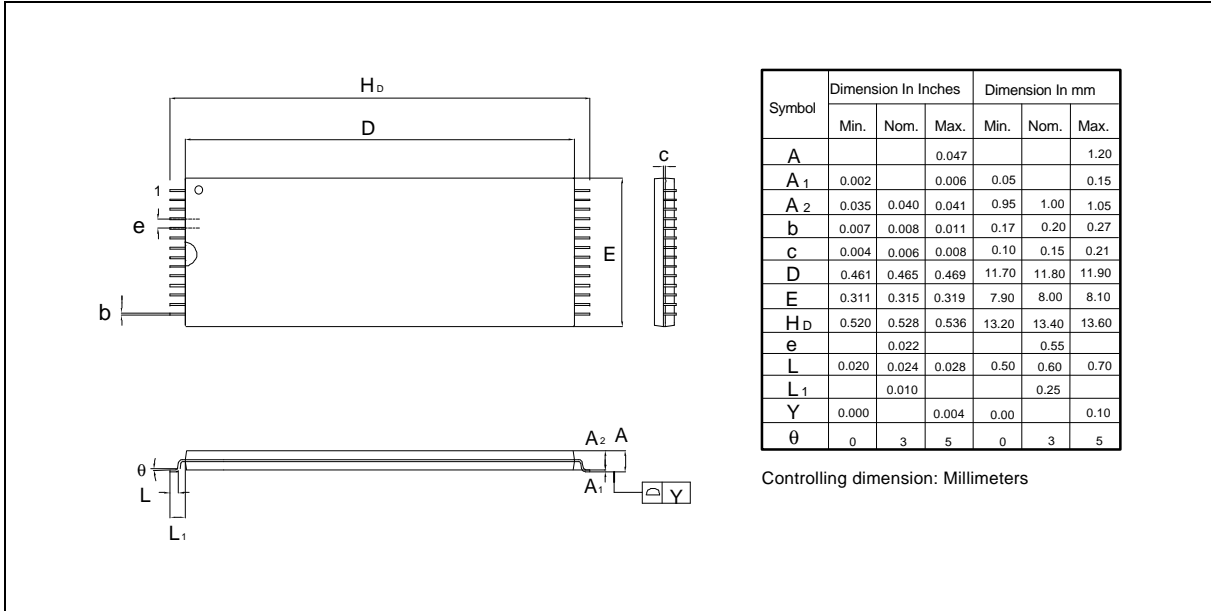
Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.112	—	—	2.85
A ₁	0.004	—	—	0.10	—	—
A ₂	0.093	0.098	0.103	2.36	2.49	2.62
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	0.713	0.733	—	18.11	18.62
E	0.326	0.331	0.336	8.28	8.41	8.53
⊖	0.044	0.050	0.056	1.12	1.27	1.42
H _E	0.453	0.465	0.477	11.51	11.81	12.12
L	0.028	0.036	0.044	0.71	0.91	1.12
L _E	0.059	0.067	0.075	1.50	1.70	1.91
S	—	—	0.047	—	—	1.19
y	—	—	0.004	—	—	0.10
θ	α°	—	10°	α°	—	10°

Notes:

- Dimensions D Max. & S include mold flash or tie bar burrs.
- Dimension b does not include dambar protrusion/intrusion.
- Dimensions D & E include mold mismatch and determined at the mold parting line.
- Controlling dimension: Inches.
- General appearance spec should be based on final visual inspection spec.

Package Dimensions, continued

28-pin Standard Type One TSOP





VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A4	Apr. 1998	2	Add standby power supply current (I _{SB1}) typical parameter when operation temperature T _A = 25° C
A5	Nov. 1998	1, 2, 7, 9	Deduct reverse type one TSOP package



Headquarters

No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5796096
<http://www.winbond.com.tw/>
Voice & Fax-on-demand: 886-2-27197006

Taipei Office

11F, No. 115, Sec. 3, Min-Sheng East Rd.,
Taipei, Taiwan
TEL: 886-2-27190505
FAX: 886-2-27197502

Winbond Electronics (H.K.) Ltd.

Rm. 803, World Trade Square, Tower II,
123 Hoi Bun Rd., Kwun Tong,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

Winbond Electronics North America Corp.

Winbond Memory Lab.
Winbond Microelectronics Corp.
Winbond Systems Lab.
2727 N. First Street, San Jose,
CA 95134, U.S.A.
TEL: 408-9436666
FAX: 408-5441798

Note: All data and specifications are subject to change without notice.