

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M5M5408BFP/TP/RT

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5408B is a family of 4-Mbit static RAMs organized as 524,288-words by 8-bit, fabricated by Mitsubishi's high-performance 0.25µm CMOS technology.

The M5M5408B is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

M5M5408B is packaged in 32-pin plastic SOP, 32-pin plastic TSOP. Two types of TSOPs are available, M5M5408BTP (normal-lead-bend TSOP), M5M5408BRT (reverse-lead-bend TSOP). These two types TSOPs are suitable for a surface mounting on double-sided printed circuit boards.

From the point of operating temperature, the family is divided into two versions; "Standard" and "I- version". Those are

FEATURES

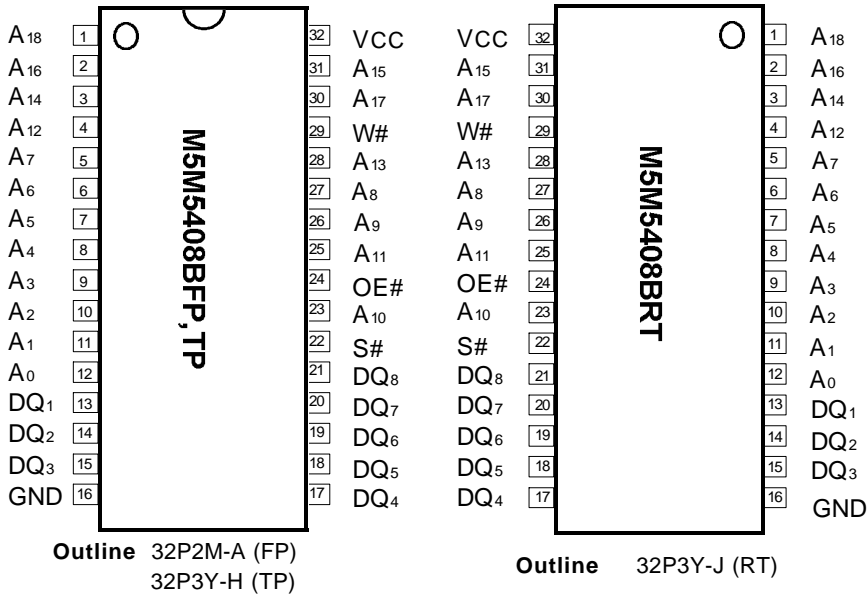
- Single +5V power supply
- Small stand-by current: 0.4µA(3V,typ.)
- No clocks, No refresh
- Data retention supply voltage=2.0V to 5.5V
- All inputs and outputs are TTL compatible.
- Easy memory expansion by S#
- Common Data I/O
- Three-state outputs: OR-tie capability
- OE# prevents data contention in the I/O bus
- Process technology: 0.25µm CMOS
- Package:
 - M5M5408BFP: 32 pin 525 mil SOP
 - M5M5408BTP/RT: 32 pin 400 mil TSOP(II)

PART NAME TABLE

| Version, Operating temperature | Part name (## stands for "FP","TP",and "RT") | Power Supply | Access time max. | Stand-by current I _{cc} (PD), V _{cc} =3.0V | | | | Active current I _{cc1} (5.0V, typ.*) |
|--------------------------------------|--|-----------------|------------------------|--|---------------|------|------|--|
| | | | | typical * | Limits (max.) | | | |
| | | | | | 25°C | 25°C | 70°C | |
| Standard 0 ~ +70°C | M5M5408B## -55H | 5.0V | 55ns | 0.4µA | 1µA | 15µA | --- | 50mA (10MHz) |
| | M5M5408B## -70H | | 70ns | | | | | |
| I- version -40 ~ +85°C | M5M5408B## -55H | 5.0V | 55ns | 0.4µA | 1µA | 15µA | 30µA | 25mA (1MHz) |
| | M5M5408B## -70H | | 70ns | | | | | |

*Typical values are sampled, and are not 100% tested.

PIN CONFIGURATION (TOP VIEW)



| Pin | Function |
|--------------------|---------------------|
| A0 ~ A18 | Address input |
| DQ1 ~ DQ8 | Data input / output |
| S# (\bar{S}) | Chip select input |
| W# (\bar{W}) | Write control input |
| OE# (\bar{OE}) | Output inable input |
| Vcc | Power supply |
| GND | Ground supply |

M5M5408BFP/TP/RT

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

FUNCTION

The M5M5408BFP,TP,RT is organized as 524,288-words by 8-bit. These devices operate on a single +5.0V power supply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

A write operation is executed during the S# low and W# low overlap time. The address(A0~A18) must be set up before the write cycle

A read operation is executed by setting W# at a high level and OE# at a low level while S# are in an active state (S#=L).

When setting S# at a high level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips. Setting the OE# at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

The power supply current is reduced as low as 0.4μA (25°C, typical), and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

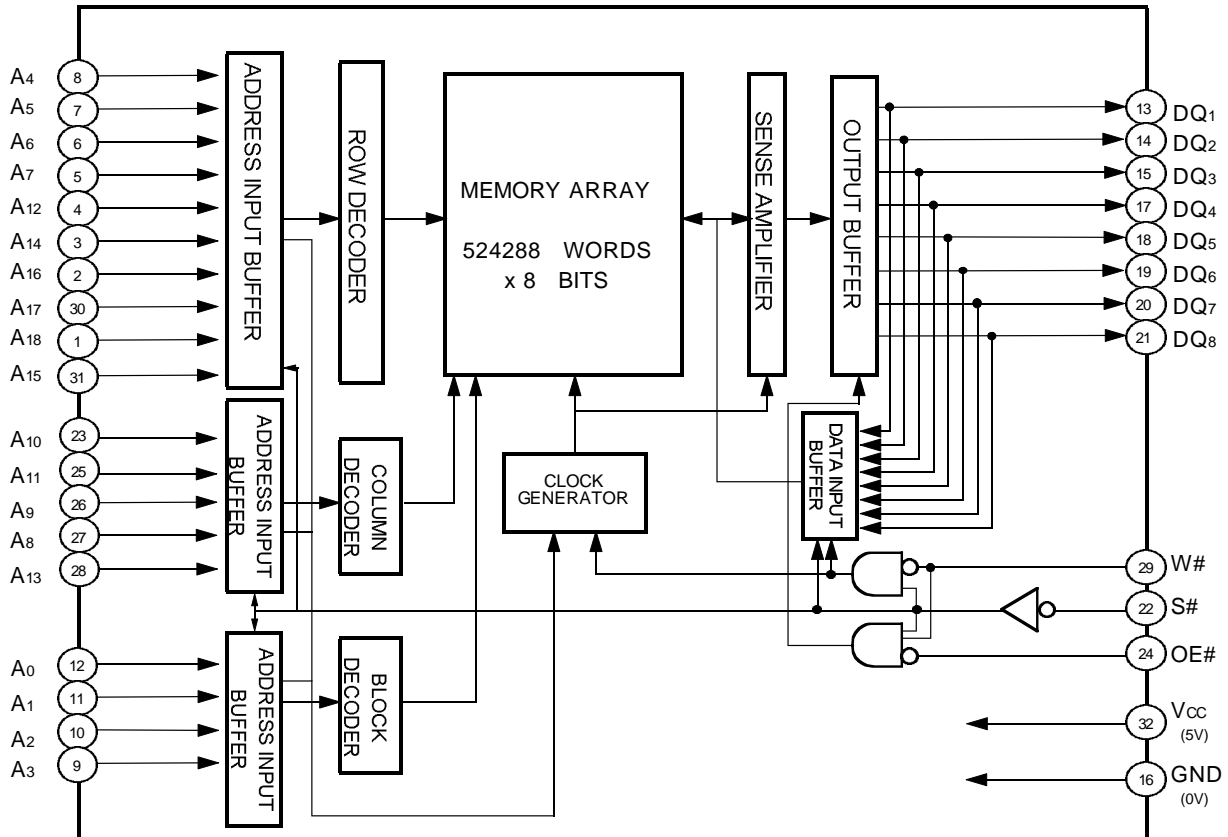
FUNCTION TABLE

| S# | W# | OE# | Mode | DQ | I _{cc} |
|----|----|-----|---------------|-----------------|-----------------|
| H | X | X | Non selection | High-impedance | Standby |
| L | L | X | Write | Data input (D) | Active |
| L | H | L | Read | Data output (Q) | Active |
| L | H | H | Read | High-impedance | Active |

note: "H" and "L" in this table mean VIH and VIL, respectively.
 "X" in this table should be "H" or "L".

| Pin | Function |
|-------------------------|---------------------|
| A0 ~ A18 | Address input |
| DQ1 ~ DQ8 | Data input / output |
| S# (\overline{S}) | Chip select input |
| W# (\overline{W}) | Write control input |
| OE# (\overline{OE}) | Output inable input |
| V _{cc} | Power supply |
| GND | Ground supply |

BLOCK DIAGRAM



M5M5408BFP/TP/RT

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Units |
|------------------|-----------------------|----------------------|-------------------------------|-------|
| V _{CC} | Supply voltage | With respect to GND | -0.3* ~ +7 | V |
| V _I | Input voltage | With respect to GND | -0.3* ~ V _{CC} + 0.3 | |
| V _O | Output voltage | With respect to GND | 0 ~ V _{CC} | |
| P _d | Power dissipation | T _a =25°C | 700 | mW |
| T _a | Operating temperature | Standard | 0 ~ +70 | °C |
| | | I-version | -40 ~ +85 | |
| T _{stg} | Storage temperature | | -65 ~ +150 | °C |

* -3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS

(V_{CC}= 5V ±10%, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | | | Units | |
|------------------|--|--|-----------------------|------|-----------------------|-------|----|
| | | | Min | Typ. | Max | | |
| V _{IH} | High-level input voltage | | 2.2 | | V _{CC} +0.3V | V | |
| V _{IL} | Low-level input voltage | | -0.3* | | 0.8 | | |
| V _{OH1} | High-level output voltage 1 | I _{OH} = -1mA | 2.4 | | | | |
| V _{OH2} | High-level output voltage 2 | I _{OH} = -0.1mA | V _{CC} -0.5V | | | | |
| V _{OL} | Low-level output voltage | I _{OL} =2mA | | | 0.4 | | |
| I _I | Input leakage current | V _I =0 ~ V _{CC} | | | ±1 | µA | |
| I _O | Output leakage current | S# = V _{IH} or OE# = V _{IH} , V _{I/O} = 0 ~ V _{CC} | | | ±1 | | |
| I _{CC1} | Active supply current (CMOS-level input) | S# ≤ 0.2V, output-open Other inputs ≤ 0.2V or ≥ V _{CC} -0.2V | f=10MHz | - | 50 | 80 | mA |
| | | | f=1MHz | - | 25 | 30 | |
| I _{CC2} | Active supply current (TTL-level input) | S# = V _{IL} , output-open Other inputs = V _{IH} or V _{IL} | f=10MHz | - | 60 | 90 | |
| | | | f=1MHz | - | 30 | 40 | |
| I _{CC3} | Stand by supply current (CMOS-level input) | V _{CC} = 5.5V, max. S# ≥ V _{CC} -0.2V, other inputs=0~V _{CC} | Standard | - | 1.0 | 30 | µA |
| | | | I-version | - | 1.0 | 60 | |
| I _{CC4} | Stand by supply current (TTL-level input) | S# = V _{IH} , other inputs = 0 ~ V _{CC} | - | - | 3 | mA | |

Note 1: Direction for current flowing into IC is indicated as positive (no mark).

* -3.0V in case of AC (Pulse width ≤ 30ns)

Note 2: Typical values are sampled at V_{CC}=5.0V and T_a=25°C, and are not 100% tested.

CAPACITANCE

(V_{CC}=5.0V±10%, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | | | Units |
|----------------|--------------------|--|--------|------|-----|-------|
| | | | Min | Typ. | Max | |
| C _I | Input capacitance | V _I =GND, V _I =25mVrms, f=1MHz | | | 8 | pF |
| C _O | Output capacitance | V _O =GND, V _O =25mVrms, f=1MHz | | | 10 | |

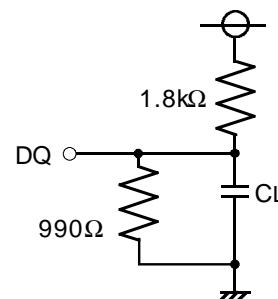
M5M5408BFP/TP/RT

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

AC ELECTRICAL CHARACTERISTICS (V_{CC}=5.0V±10%, unless otherwise noted)

(1) TEST CONDITIONS

| | |
|-------------------------------|--|
| Supply voltage | 5.0V |
| Input pulse | VIH=2.4V, VIL=0.6V (-70H, -70HI) VIH=3.0V, VIL=0V (-55H, -55HI) |
| Input rise time and fall time | 5ns |
| Reference level | VOH=VOL=1.5V Transition is measured ±500mV from steady state voltage for <i>t_{en}</i> and <i>t_{dis}</i> . |
| Output loads | Fig.1, CL=100pF (-70H, -70HI) CL=30pF (-55H, -55HI) CL=5pF (for <i>t_{en}</i> , <i>t_{dis}</i>) |



CL Includes scope and jig capacitance

Fig.1 Output load

(2) READ CYCLE

| Symbol | Parameter | Limits | | | | Units |
|----------------------------|------------------------------------|-------------|-----|-------------|-----|-------|
| | | -55H, -55HI | | -70H, -70HI | | |
| | | Min | Max | Min | Max | |
| <i>t_{CR}</i> | Read cycle time | 55 | | 70 | | ns |
| <i>t_a(A)</i> | Address access time | | 55 | | 70 | ns |
| <i>t_a(S)</i> | Chip select access time | | 55 | | 70 | ns |
| <i>t_a(OE)</i> | Output enable access time | | 25 | | 35 | ns |
| <i>t_{dis}(S)</i> | Output disable time after S# high | | 20 | | 25 | ns |
| <i>t_{dis}(OE)</i> | Output disable time after OE# high | | 20 | | 25 | ns |
| <i>t_{en}(S)</i> | Output enable time after S# low | 10 | | 10 | | ns |
| <i>t_{en}(OE)</i> | Output enable time after OE# low | 5 | | 5 | | ns |
| <i>t_v(A)</i> | Data valid time after address | 10 | | 10 | | ns |

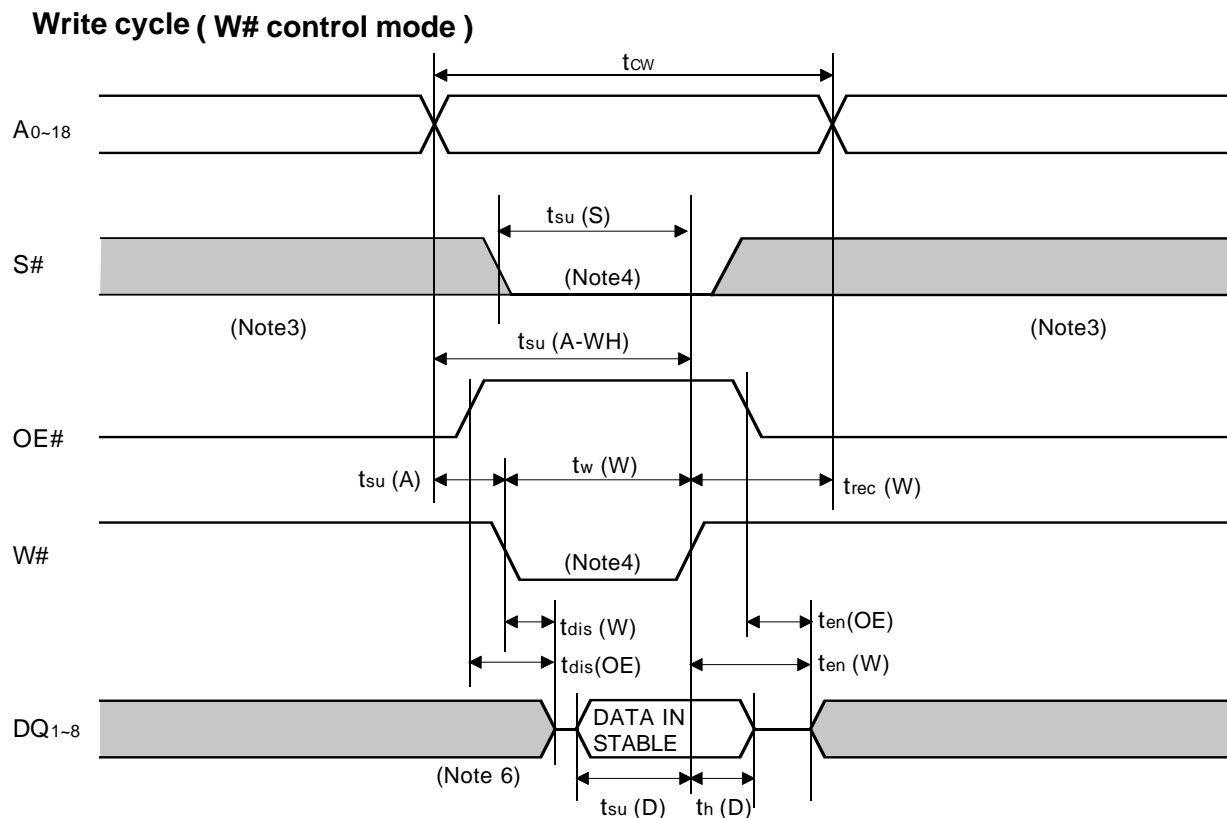
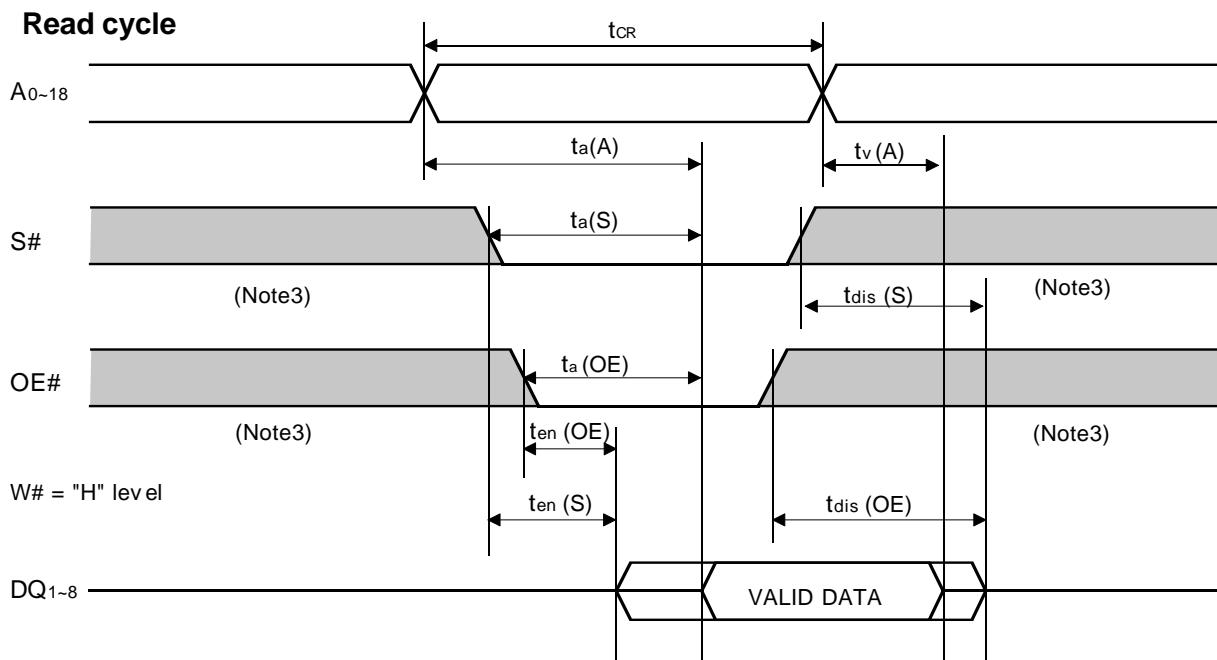
(3) WRITE CYCLE

| Symbol | Parameter | Limits | | | | Units |
|-----------------------------|---|-------------|-----|-------------|-----|-------|
| | | -55H, -55HI | | -70H, -70HI | | |
| | | Min | Max | Min | Max | |
| <i>t_{cw}</i> | Write cycle time | 55 | | 70 | | ns |
| <i>t_w(W)</i> | Write pulse width | 40 | | 50 | | ns |
| <i>t_{su}(A)</i> | Address set up time | 0 | | 0 | | ns |
| <i>t_{su}(A-WH)</i> | Address set up time with respect to W# high | 50 | | 60 | | ns |
| <i>t_{su}(S)</i> | Chip select set up time | 50 | | 60 | | ns |
| <i>t_{su}(D)</i> | Data set up time | 25 | | 30 | | ns |
| <i>t_h(D)</i> | Data hold time | 0 | | 0 | | ns |
| <i>t_{rec}(W)</i> | Write recovery time | 0 | | 0 | | ns |
| <i>t_{dis}(W)</i> | Output disable time after W# low | | 20 | | 25 | ns |
| <i>t_{dis}(OE)</i> | Output disable time after OE# high | | 20 | | 25 | ns |
| <i>t_{en}(W)</i> | Output enable time after W# high | 5 | | 5 | | ns |
| <i>t_{en}(OE)</i> | Output enable time after OE# low | 5 | | 5 | | ns |

M5M5408BFP/TP/RT

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

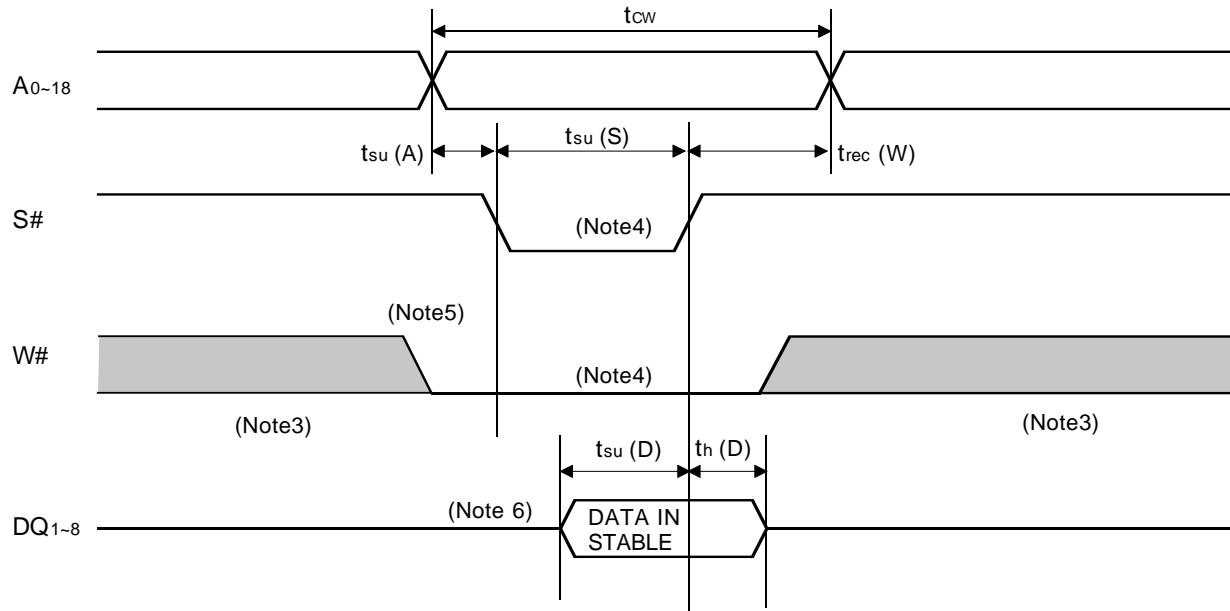
(4)TIMING DIAGRAMS



M5M5408BFP/TP/RT

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

Write cycle (S# control mode)



Note 3: Hatching indicates the state is "don't care".

Note 4: A Write occurs during the overlap of a low S# and a low W#.

Note 5: If W goes low simultaneously with or prior to S#, the output remains in the high impedance state.

Note 6: Don't apply inverted phase signal externally when DQ pin is in output mode.

M5M5408BFP/TP/RT

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test conditions | Limits | | | Units | | |
|----------------------|---------------------------|--|-----------|----------------------|-----|-------|----|----|
| | | | Min | Typical | Max | | | |
| V _{CC} (PD) | Power down supply voltage | | 2 | - | - | V | | |
| V _I (S#) | Chip select input S# | V _{CC} (PD) ≥ 2.2V | 2.2 | - | - | | | |
| | | 2.2V ≥ V _{CC} (PD) ≥ 2.0V | - | V _{CC} (PD) | - | | | |
| I _{CC} (PD) | Power down supply current | V _{CC} =3.0V, S# ≥ V _{CC} -0.2V, Other input =0 ~ V _{CC} | I-version | 85°C | - | - | 30 | μA |
| | | | Standard, | 70°C | - | - | 15 | |
| | | | I-version | 40°C | - | 1* | 3 | |
| | | | Standard | 0~ 25°C | - | 0.4* | 1 | |
| | | | I-version | -40~ 25°C | - | 0.4* | 1 | |

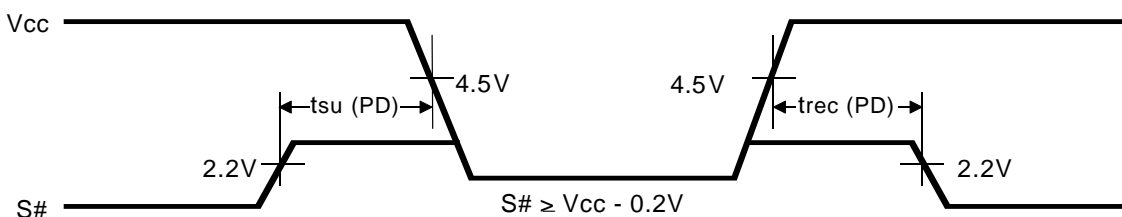
*Typical values are sampled, and are not 100% tested.

(2) TIMING REQUIREMENTS

| Symbol | Parameter | Test conditions | Limits | | | Units |
|-----------------------|--------------------------|-----------------|--------|-----|-----|-------|
| | | | Min | Typ | Max | |
| t _{su} (PD) | Power down set up time | | 0 | | | ns |
| t _{rec} (PD) | Power down recovery time | | 5 | | | ms |

(3) TIMING DIAGRAM

S# control mode



M5M5408BFP/TP/RT

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

Revision History

| <u>Revision No.</u> | <u>History</u> | <u>Date</u> | |
|---------------------|---|-------------|-------------|
| K0.1e | The first edition | Jul.30, '98 | Preliminary |
| K0.2e | 1) lcc3 limit revised 2) lcc(PD) limit revised 3) lcc1,lcc2 conditions revised | Jun. 3, '99 | Preliminary |
| K0.3e | 1) Vcc Level in the Block Diagram revised 2) lcc3 limit (typ) revised | Jun.28, '99 | Preliminary |
| K1.0e | The first product version | Oct.12, '99 | --- |
| K1.1e | Product lineup revised | Oct.21, '99 | --- |
| 2.0e | 1) Product lineup revised 2) Symbol notations revised: \bar{S} -> S#, \bar{W} -> W#, \bar{OE} -> OE# 3) lcc(PD) conditions revised | Feb.12, '02 | --- |

Keep safety first in your circuit designs!

Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

These materials are intended as a reference to assist our customers in the selection of the Mitsubishi semiconductor product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Mitsubishi Electric Corporation or a third party.

Mitsubishi Electric Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.

All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Mitsubishi Electric Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for the latest product information before purchasing a product listed herein.

The information described here may contain technical inaccuracies or typographical errors. Mitsubishi Electric Corporation assumes no responsibility for any damage, liability, or other loss arising from these inaccuracies or errors.

Please also pay attention to information published by Mitsubishi Electric Corporation by various means, including the Mitsubishi Semiconductor home page (<http://www.mitsubishichips.com>).

When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Mitsubishi Electric Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.

Mitsubishi Electric Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.

The prior written approval of Mitsubishi Electric Corporation is necessary to reprint or reproduce in whole or in part these materials.

If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination. Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.

Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for further details on these materials or the products contained therein.