To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

RENESAS
Renesas Technology Corp.

M5M5408BFP/TP/RT

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5408B is a family of 4-Mbit static RAMs organized as 524,288-words by 8-bit, fabricated by Mitsubishi's high-performance 0.25µm CMOS technology.

The M5M5408B is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

M5M5408B is packaged in 32-pin plastic SOP, 32-pin plastic TSOP. Two types of TSOPs are available, M5M5408BTP (normal-lead-bend TSOP), M5M5408BRT (reverse-lead-bend TSOP). These two types TSOPs are suitable for a surface mounting on double-sided printed circuit boards.

From the point of operating temperature, the family is divided into two versions; "Standard" and "I-version". Those are

FEATURES

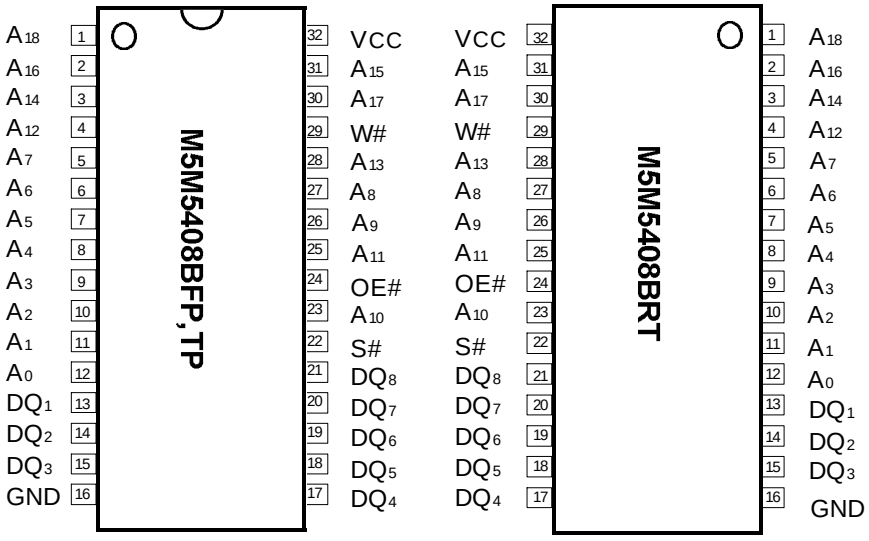
- Single +5V power supply
- Small stand-by current: 0.4µA(3V,typ.)
- No clocks, No refresh
- Data retention supply voltage=2.0V to 5.5V
- All inputs and outputs are TTL compatible.
- Easy memory expansion by S#
- Common Data I/O
- Three-state outputs: OR-tie capability
- OE# prevents data contention in the I/O bus
- Process technology: 0.25µm CMOS
- Package:
  M5M5408BFP: 32 pin 525 mil SOP
  M5M5408BTP/RT: 32 pin 400 mil TSOP(II)

PART NAME TABLE

Version, Operating temperature	Part name (## stands for "FP","TP",and "RT")	Power Supply	Access time max.	Stand-by current Icc(PD), Vcc=3.0V				Active current Icc1 (5.0V, typ.*)
				typical *	Limits (max.)			
				25°C	25°C	70°C	85°C	
Standard 0 ~ +70°C	M5M5408B## -55H	5.0V	55ns	0.4µA	1µA	15µA	---	50mA (10MHz)
	M5M5408B## -70H		70ns					
I-version -40 ~ +85°C	M5M5408B## -55H	5.0V	55ns	0.4µA	1µA	15µA	30µA	25mA (1MHz)
	M5M5408B## -70H		70ns					

*Typical values are sampled, and are not 100% tested.

PIN CONFIGURATION (TOP VIEW)



Outline 32P2M-A (FP)
32P3Y-H (TP)

Outline 32P3Y-J (RT)

Pin	Function
A0 ~ A18	Address input
DQ1 ~ DQ8	Data input / output
S# ($\overline{S}$)	Chip select input
W# ($\overline{W}$)	Write control input
OE# ($\overline{OE}$)	Output inable input
Vcc	Power supply
GND	Ground supply

M5M5408BFP/TP/RT

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

FUNCTION

The M5M5408BFP,TP,RT is organized as 524,288-words by 8-bit. These devices operate on a single +5.0V power supply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

A write operation is executed during the S# low and W# low overlap time. The address(A0~A18) must be set up before the write cycle

A read operation is executed by setting W# at a high level and OE# at a low level while S# are in an active state (S#=L).

When setting S# at a high level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips. Setting the OE# at a high level,the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

The power supply current is reduced as low as 0.4µA (25°C, typical), and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

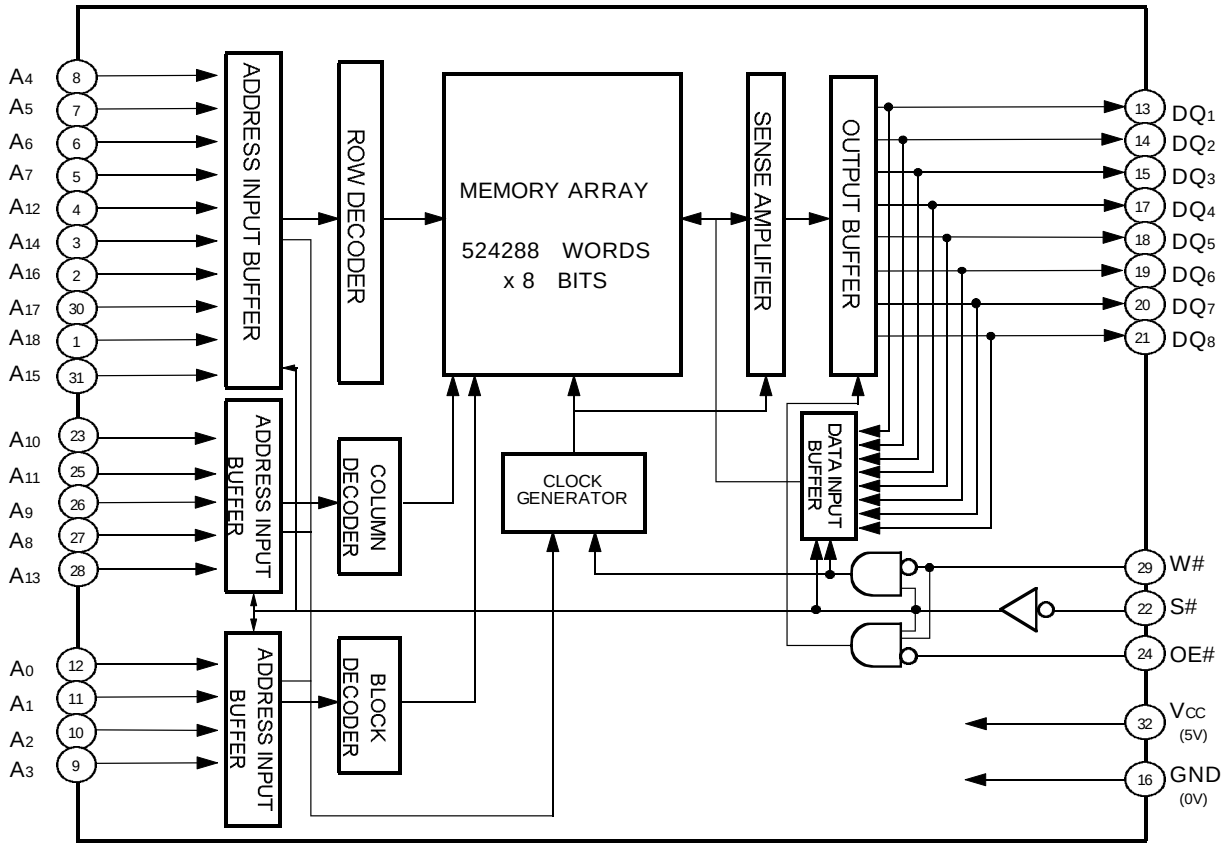
FUNCTION TABLE

S#	W#	OE#	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Standby
L	L	X	Write	Data input (D)	Active
L	H	L	Read	Data output (Q)	Active
L	H	H	Read	High-impedance	Active

note: "H" and "L" in this table mean VIH and VIL, respectively.
"X" in this table should be "H" or "L".

Pin	Function
A0 ~ A18	Address input
DQ1 ~ DQ8	Data input / output
S# ($\overline{S}$)	Chip select input
W# ($\overline{W}$)	Write control input
OE# ($\overline{OE}$)	Output inable input
Vcc	Power supply
GND	Ground supply

BLOCK DIAGRAM



M5M5408BFP/TP/RT

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V_{CC}	Supply voltage	With respect to GND	-0.3* ~ +7	V
V_I	Input voltage	With respect to GND	-0.3* ~ Vcc + 0.3	
V_O	Output voltage	With respect to GND	0 ~ Vcc	
P_d	Power dissipation	Ta=25°C	700	mW
T_a	Operating temperature	Standard	0 ~ +70	°C
		I-version	-40 ~ +85	
T_{stg}	Storage temperature		-65 ~ +150	°C

* -3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS

(Vcc= 5V ±10%, unless otherwise noted)

Symbol	Parameter	Conditions		Limits			Units
				Min	Typ.	Max	
V_{IH}	High-level input voltage			2.2		Vcc+0.3V	V
V_{IL}	Low-level input voltage			-0.3 *		0.8	
V_{OH1}	High-level output voltage 1	I_{OH}= -1mA		2.4			
V_{OH2}	High-level output voltage 2	I_{OH}= -0.1mA		Vcc-0.5V			
V_{OL}	Low-level output voltage	I_{OL}=2mA				0.4	
I_I	Input leakage current	V_I =0 ~ Vcc				±1	µA
I_O	Output leakage current	S# = V_{IH} or OE# =V_{IH}, $V_{I/O}$ = 0 ~ Vcc				±1	
Icc1	Active supply current (CMOS-level input)	S# ≤ 0.2V, output-open Other inputs ≤ 0.2V or ≥ Vcc-0.2V	f=10MHz	-	50	80	mA
			f=1MHz	-	25	30	
Icc2	Active supply current (TTL-level input)	S# =V_{IL}, output-open Other inputs= V_{IH} or V_{IL}	f=10MHz	-	60	90	
			f=1MHz	-	30	40	
Icc3	Stand by supply current (CMOS-level input)	Vcc =5.5V, max. S# ≥ Vcc-0.2V,other inputs=0~Vcc	Standard	-	1.0	30	µA
			I-version	-	1.0	60	
Icc4	Stand by supply current (TTL-level input)	S# =V_{IH}, other inputs= 0 ~ Vcc		-	-	3	mA

Note 1: Direction for current flowing into IC is indicated as positive (no mark). * -3.0V in case of AC (Pulse width ≤30ns)

Note 2: Typical values are sampled at Vcc=5.0V and Ta=25°C, and are not 100% tested.

CAPACITANCE

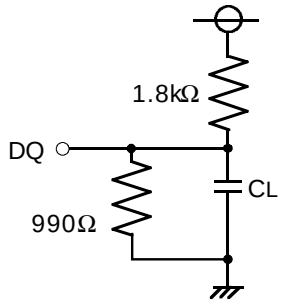
(Vcc=5.0V±10%, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ.	Max	
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			8	pF
C_O	Output capacitance	V_O=GND, V_O=25mVrms, f=1MHz			10	

AC ELECTRICAL CHARACTERISTICS (Vcc=5.0V±10%, unless otherwise noted)

(1) TEST CONDITIONS

Supply voltage	5.0V
Input pulse	VIH=2.4V,VIL=0.6V (-70H, -70HI) VIH=3.0V,VIL=0V (-55H, -55HI)
Input rise time and fall time	5ns
Reference level	VOH=VOL=1.5V Transition is measured ±500mV from steady state voltage for t_{en} and t_{dis}.
Output loads	Fig.1, CL=100pF (-70H, -70HI) CL=30pF (-55H, -55HI) CL=5pF (for t_{en},t_{dis})



CL Includes scope and jig capacitance

Fig.1 Output load

(2) READ CYCLE

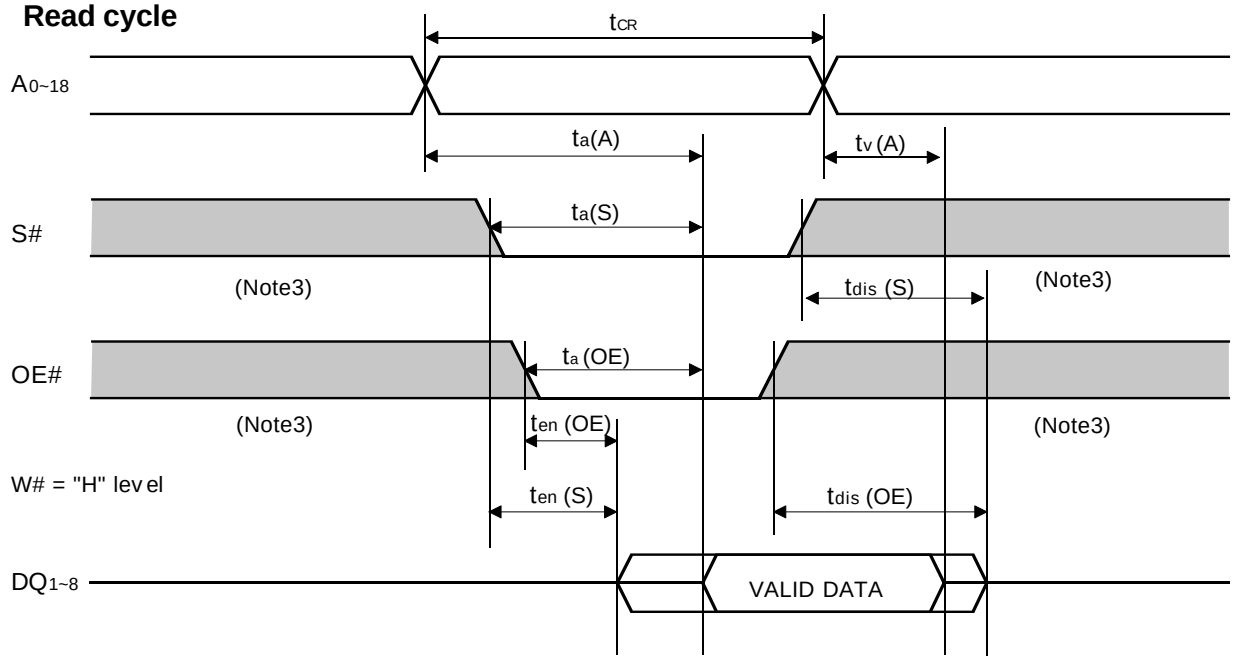
Symbol	Parameter	Limits				Units
		-55H, -55HI		-70H, -70HI		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	55		70		ns
t_a(A)	Address access time		55		70	ns
t_a(S)	Chip select access time		55		70	ns
t_a(OE)	Output enable access time		25		35	ns
t_{dis}(S)	Output disable time after S# high		20		25	ns
t_{dis}(OE)	Output disable time after OE# high		20		25	ns
t_{en}(S)	Output enable time after S# low	10		10		ns
t_{en}(OE)	Output enable time after OE# low	5		5		ns
t_V(A)	Data valid time after address	10		10		ns

(3) WRITE CYCLE

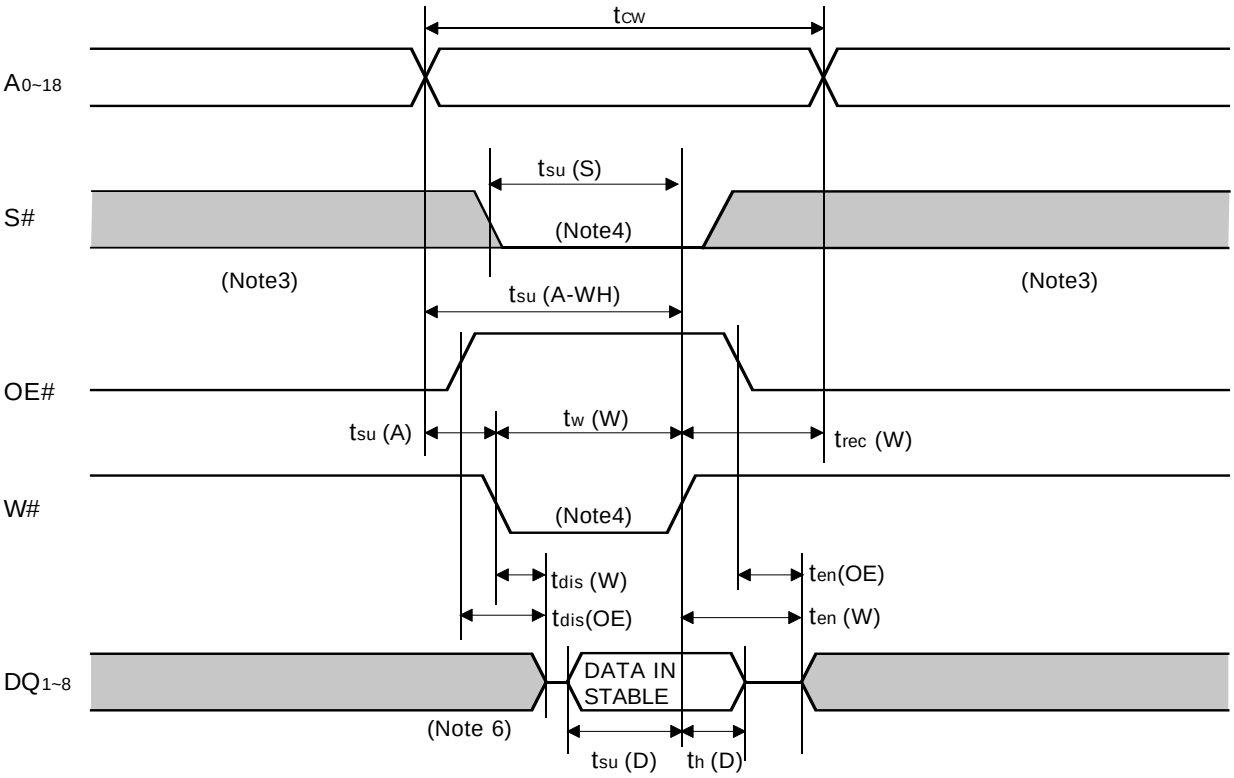
Symbol	Parameter	Limits				Units
		-55H, -55HI		-70H, -70HI		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	55		70		ns
t_w(W)	Write pulse width	40		50		ns
t_{su}(A)	Address set up time	0		0		ns
t_{su}(A-WH)	Address set up time with respect to W# high	50		60		ns
t_{su}(S)	Chip select set up time	50		60		ns
t_{su}(D)	Data set up time	25		30		ns
t_h(D)	Data hold time	0		0		ns
t_{rec}(W)	Write recovery time	0		0		ns
t_{dis}(W)	Output disable time after W# low		20		25	ns
t_{dis}(OE)	Output disable time after OE# high		20		25	ns
t_{en}(W)	Output enable time after W# high	5		5		ns
t_{en}(OE)	Output enable time after OE# low	5		5		ns

(4)TIMING DIAGRAMS

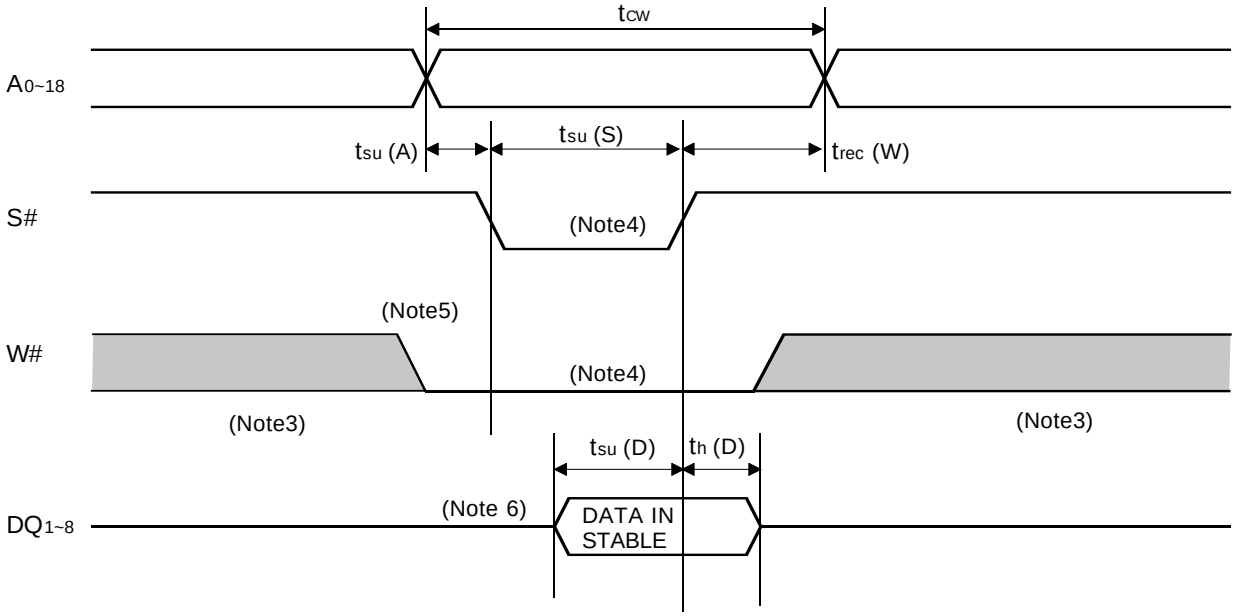
Read cycle



Write cycle (W# control mode)



Write cycle (S# control mode)



Note 3: Hatching indicates the state is "don't care".

Note 4: A Write occurs during the overlap of a low S# and a low W#.

Note 5: If W goes low simultaneously with or prior to S#, the output remains in the high impedance state.

Note 6: Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions			Limits			Units
					Min	Typical	Max	
V_{CC} (PD)	Power down supply voltage				2	-	-	V
V_I (S#)	Chip select input S#	Vcc(PD) ≥ 2.2V			2.2	-	-	
		2.2V ≥ Vcc(PD) ≥ 2.0V			-	Vcc(PD)	-	
I_{CC} (PD)	Power down supply current	Vcc=3.0V, S# ≥ Vcc-0.2V, Other input =0 ~ Vcc	I-version	85°C	-	-	30	µA
			Standard, I-version	70°C	-	-	15	
				40°C	-	1*	3	
			Standard	0~ 25°C	-	0.4*	1	
			I-version	-40~ 25°C	-	0.4*	1	

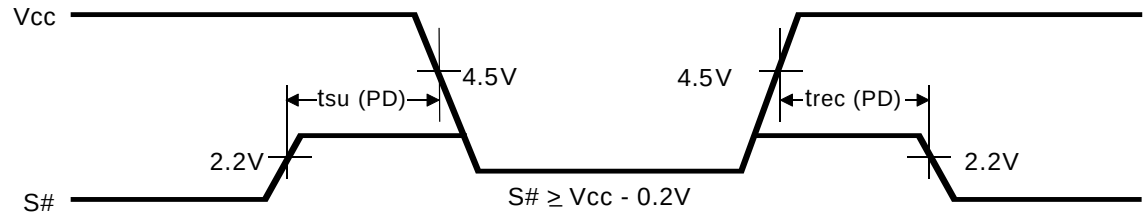
*Typical values are sampled, and are not 100% tested.

(2) TIMING REQUIREMENTS

Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
t_{su} (PD)	Power down set up time		0			ns
t_{rec} (PD)	Power down recovery time		5			ms

(3) TIMING DIAGRAM

S# control mode



Revision History

Revision No.	History	Date	
K0.1e	The first edition	Jul.30, '98	Preliminary
K0.2e	1) Icc3 limit revised 2) Icc(PD) limit revised 3) Icc1,Icc2 conditions revised	Jun. 3, '99	Preliminary
K0.3e	1) Vcc Level in the Block Diagram revised 2) Icc3 limit (typ) revised	Jun.28, '99	Preliminary
K1.0e	The first product version	Oct.12, '99	---
K1.1e	Product lineup revised	Oct.21, '99	---
2.0e	1) Product lineup revised 2) Symbol notations revised: $\overline{S}$ -> S#, $\overline{W}$-> W#, $\overline{OE}$ -> OE# 3) Icc(PD) conditions revised	Feb.12, '02	---

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