M5M44256BP,J,L,VP,RV-7,-8,-10

FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 262144-word by 4-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of triple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

In addition to the $\overline{RAS}$-only refresh mode, the hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ refresh mode are available.

FEATURES

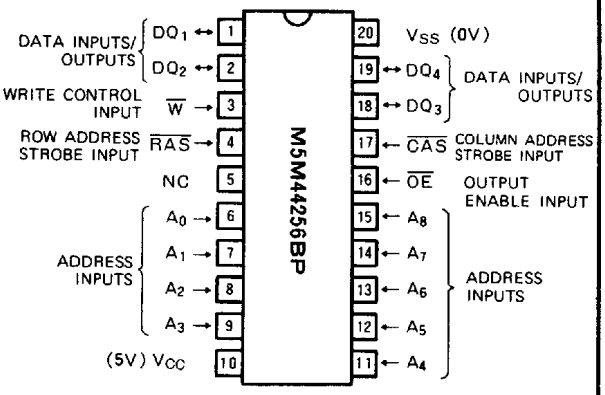
Type name	$\overline{RAS}$ access time (max ns)	$\overline{CAS}$ access time (max ns)	Address access time (max ns)	$\overline{OE}$ access time (max. ns)	Cycle time (min ns)	Power dissipation (typ mW)
M5M44256B-7	70	20	35	20	140	230
M5M44256B-8	80	20	40	20	160	200
M5M44256B-10	100	25	50	25	190	175

- High performance CMOS technology
- Standard 20 pin DIP, 26 pin SOJ, 20 pin ZIP, 24 pin TSOP
- Single 5V±10% supply
- Low stand-by power dissipation
  2.75mW (max) . . . . . CMOS Input level
- Low operating power dissipation
  M5M44256BP, J, L, VP, RV-7 . . . 440mW (max)
  M5M44256BP, J, L, VP, RV-8 . . . 385mW (max)
  M5M44256BP, J, L, VP, RV-10 . . 330mW (max)
- All inputs, outputs TTL compatible and low capacitance
- Tri-state unlatched output
- 512 refresh cycles/8ms
- Early write mode and $\overline{OE}$ control output buffer impedance
- Read-Modify-write, $\overline{RAS}$-only refresh, Fast-page mode capabilities
- $\overline{CAS}$ before $\overline{RAS}$ refresh mode capability
- $\overline{CAS}$ controlled output allows hidden refresh
- Wide $\overline{RAS}$ Low pulse width for
  Fast page mode . . . . . 50μs (max)

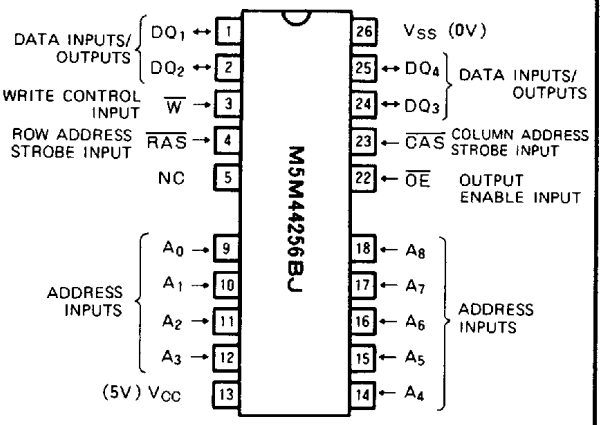
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

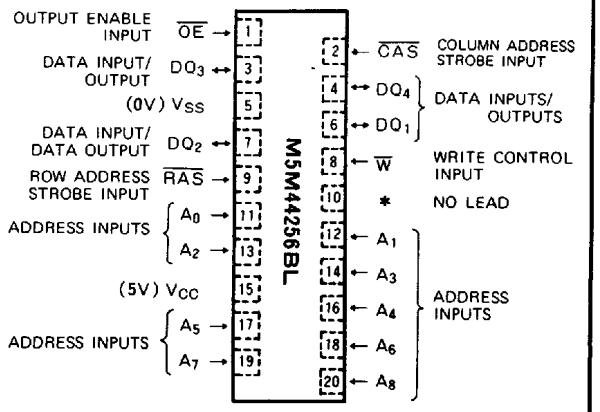
PIN CONFIGURATION (TOP VIEW)



Outline 20P4Y (DIP)



Outline 26P0J (SOJ)

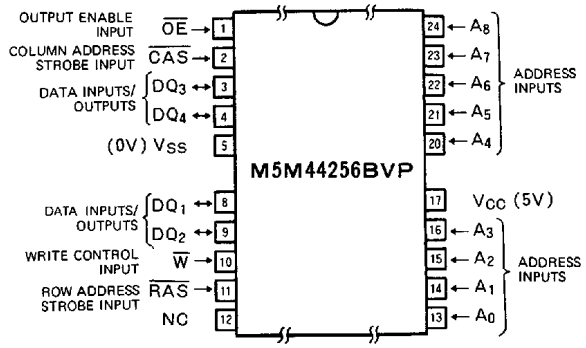


Outline 20P5L-A(ZIP)

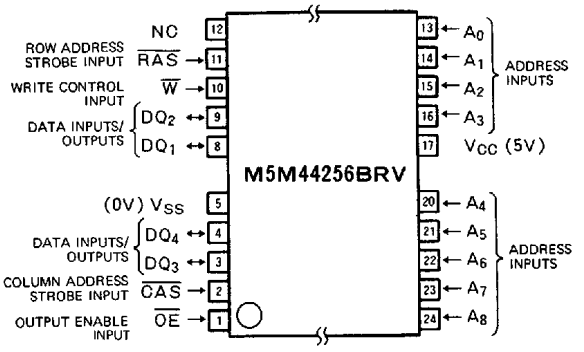
NC NO CONNECTION

FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

PIN CONFIGURATION (TOP VIEW)



Outline 24P3B-L (TSOP)



Outline 24P3B-M (TSOP)

NC NO CONNECTION

FUNCTION

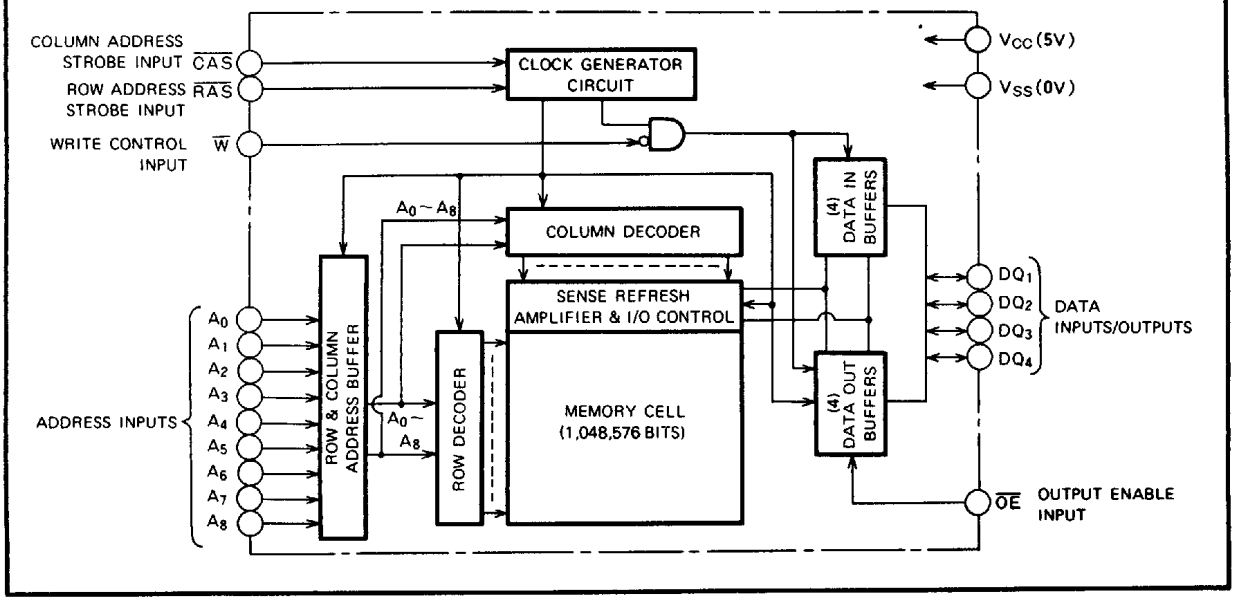
The M5M44256BP, J, L, VP, RV provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Read-Modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$ only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note ACT active, NAC nonactive, DNC don't care, VLD valid, APD applied, OPN open

BLOCK DIAGRAM



FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1～7	V
V_I	Input voltage		−1～7	V
V_O	Output voltage		−1～7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta＝25°C	1000	mW
Topr	Operating temperature		0～70	°C
Tstg	Storage temperature		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−1.0		0.8	V

Note 1 All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, V_{CC}＝5V±10%, V_{SS}＝0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}＝−5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}＝4.2mA	0		0.4	V
I_{OZ}	Off state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦6.5V, Other inputs pins＝0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	M5M44256B-7	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC}＝t_{WC}＝min, output open			80	mA
		M5M44256B-8				70	
		M5M44256B-10				60	
$I_{CC2(AV)}$	Average supply current from V_{CC}, stand-by (Note 6)		$\overline{RAS}$＝$\overline{CAS}$＝V_{IH}, output open			2	mA
			$\overline{RAS}$＝$\overline{CAS}$＝$\overline{OE}$≧V_{CC}−0.5V, output open			0.5	
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	M5M44256B-7	$\overline{RAS}$ cycling, $\overline{CAS}$＝V_{IH}, t_{RC}＝min, output open			80	mA
		M5M44256B-8				70	
		M5M44256B-10				60	
$I_{CC4(AV)}$	Average supply current from V_{CC} Fast-Page-Mode (Note 3, 4)	M5M44256B-7	$\overline{RAS}$＝V_{IL}, $\overline{CAS}$ cycling, t_{PC}＝min, output open			70	mA
		M5M44256B-8				60	
		M5M44256B-10				50	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M44256B-7	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling, t_{RC}＝min, output open			80	mA
		M5M44256B-8				70	
		M5M44256B-10				60	

Note 2. Current flowing into an IC is positive, out is negative
3 $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate
4 $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open

CAPACITANCE (Ta＝0～70°C, V_{CC}＝5V±10%, V_{SS}＝0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs (Note 5)	V_I＝V_{SS}, f＝1MHz, V_I＝25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

Note 5 $C_{I(A)}$ of ZIP is 6pF (max).

SWITCHING CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 6)

Symbol	Parameter		Limits						Unit
			M5M4256B-7		M5M44256B-8		M5M44256B-10		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7, 8)		20		20		25	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7, 9)		70		80		100	ns
t_{CAA}	Column Address access time	(Note 7, 10)		35		40		50	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7, 11)		40		45		55	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		20		20		25	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)	0	20	0	20	0	25	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	(Note 12)	0	20	0	20	0	25	ns

Note 6: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved
Note that $\overline{RAS}$ may be cycled during the initial pause And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods of $\overline{RAS}$ inactivity before proper devise operation is achieved
7 Measured with a load circuit equivalent to 2TTL loads and 100pF
8 Assume that $t_{RCD(max)} \leqq t_{RCD}$ and $t_{ASC} \geqq t_{ASC(max)}$
9 Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$ If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} or t_{RAD} exceeds the value shown.
10 Assume that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$
11 Assume that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$
12 $t_{OFF(max)}$ and $t_{dis(OE)(max)}$ define the time at which the output achieves the high impedance state ($I_{OUT} \leqq \pm 10\mu A$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast Page Mode Cycles)

(T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted, See notes 13, 14)

Symbol	Parameter		Limits						Unit
			M5M44256B-7		M5M44256B-8		M5M44256B-10		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			8		8		8	ms
t_{RP}	$\overline{RAS}$ high pulse width		60		70		80		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	20	50	25	60	25	75	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 16)	10		10		10		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 17)	15	35	20	40	20	50	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 18)	0	10	0	15	0	20	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		15		15		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		15		20		20		ns
t_T	Transition time	(Note 19)	3	50	3	50	3	50	ns

Note 13 The timing requirements are assumed t_T = 5ns
14 $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals
15 $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC} If t_{RCD} is greater than $t_{RCD(max)}$, access time is defined as t_{CAC} and t_{CAA} as shown in notes 8, 10
16 t_{CRP} requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles
17 $t_{RAD(max)}$ is specified as a reference point only If $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$, access time is controlled exclusively by t_{CAA}
18 $t_{ASC(max)}$ is specified as a reference point only If $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}
19 t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M44256B-7		M5M44256B-8		M5M44256B-10		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	140		160		190		ns
t_{RAS}	$\overline{RAS}$ low pulse width	70	10000	80	10000	100	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	20	10000	20	10000	25	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	70		80		100		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	20		20		25		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low	0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (Note 20)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 20)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ setup time	35		40		50		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	0		0		0		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low	20		20		25		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low	70		80		100		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low	0		0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	15		15		20		ns
$t_{h(OECH)}$	$\overline{CAS}$ hold time after $\overline{OE}$ low	20		20		25		ns
$t_{h(OERH)}$	$\overline{RAS}$ hold time after $\overline{OE}$ low	20		20		25		ns

Note 20 Either t_{RCH} or t_{RRH} must be satisfied for a read cycle

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M44256B-7		M5M44256B-8		M5M44256B-10		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	140		160		190		ns
t_{RAS}	$\overline{RAS}$ low pulse width	70	10000	80	10000	100	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	20	10000	20	10000	25	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	70		80		100		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	20		20		25		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 22)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		20		ns
t_{CWL}	$\overline{CAS}$ hold time after write low	20		20		25		ns
t_{RWL}	$\overline{RAS}$ hold time after write low	20		20		25		ns
t_{WP}	Write pulse width	15		15		20		ns
t_{DS}	Data setup time	0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low	15		15		20		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to data	15		15		20		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after write low	15		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M44256B-7		M5M44256B-8		M5M44256B-10		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read-write/read-modify-write cycle time (Note 21)	185		205		245		ns
t_{RAS}	$\overline{RAS}$ low pulse width	115	10000	125	10000	155	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	65	10000	65	10000	80	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	115		125		155		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	65		65		80		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to write low (Note 22)	40		40		50		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to write low (Note 22)	90		100		125		ns
t_{CWL}	$\overline{CAS}$ hold time after write low	20		20		25		ns
t_{RWL}	$\overline{RAS}$ hold time after write low	20		20		25		ns
t_{WP}	Write pulse width	15		15		20		ns
t_{DS}	Data setup time	0		0		0		ns
t_{DH}	Data hold time after write low	15		15		20		ns
t_{AWD}	Delay time, address to write low (Note 22)	55		60		75		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low	20		20		25		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low	70		80		100		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low	0		0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	15		15		20		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after write low	15		15		20		ns

Note 21 t_{RWC} is specified as $t_{RWC(min)} = t_{RAC(max)} + t_{OEHD(min)} + t_{RWL(min)} + t_{RP(min)} + 4t_T$

22 t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, the cycle is a read-modify write cycle and the DQ will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle)

Symbol	Parameter	Limits						Unit
		M5M44256B-7		M5M44256B-8		M5M44256B-10		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Read, Write cycle time	45		50		60		ns
t_{RWPC}	Read-write/read-modify-write cycle time	95		100		115		ns
t_{RAS}	$\overline{RAS}$ low pulse width for Read, write cycle	115	50000	130	50000	160	50000	ns
t_{CAS}	$\overline{CAS}$ low pulse width for read cycle	20	10000	20	10000	25	10000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 23)	10	25	10	25	10	25	ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	20		20		25		ns

Note 23 $t_{CP(max)}$ is specified as a reference point only. If $t_{CP(max)} \leq t_{CP}$, access time is assumed by t_{CAC}.

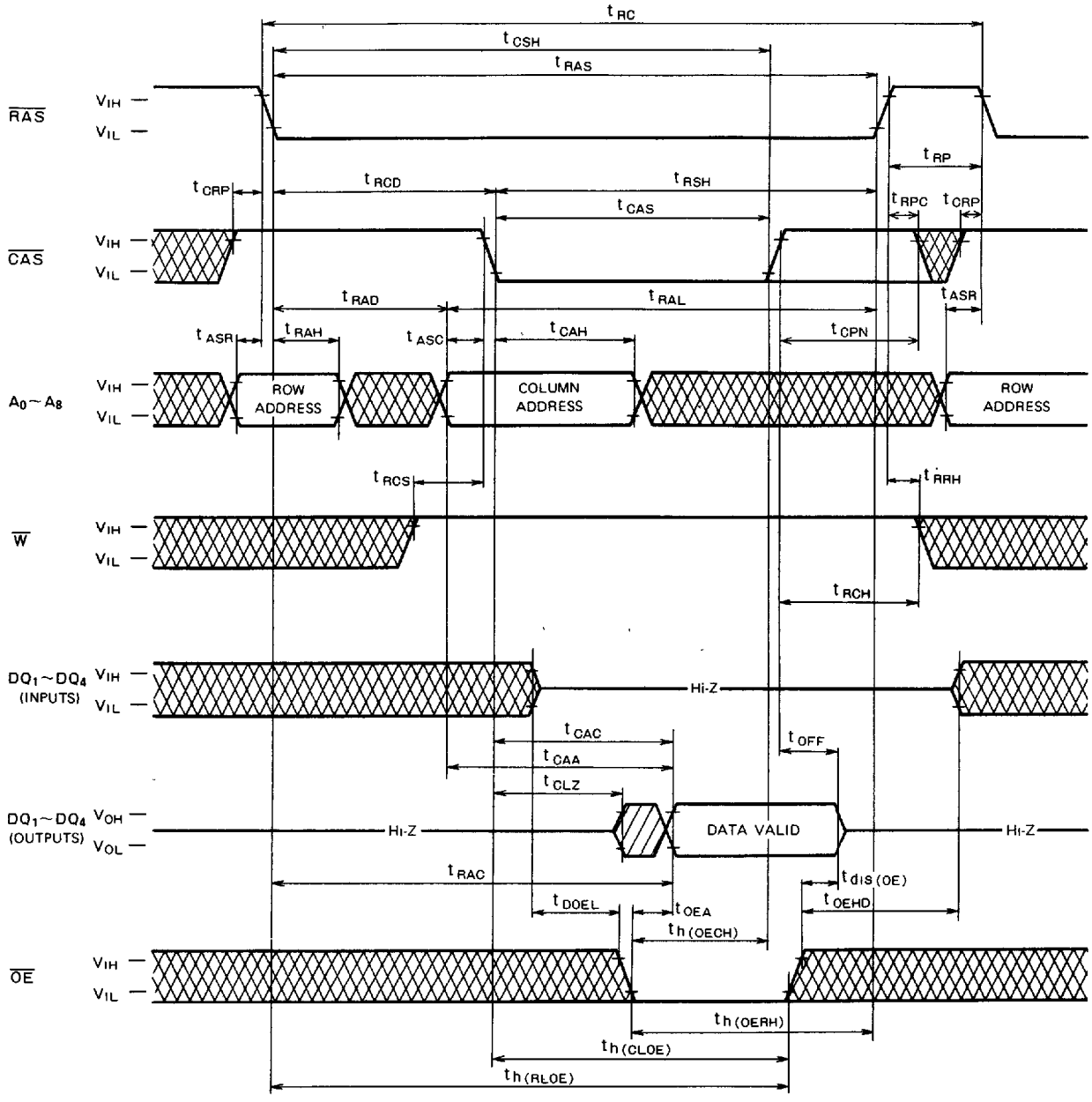
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 24)

Symbol	Parameter	Limits						Unit
		M5M44256B-7		M5M44256B-8		M5M44256B-10		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	15		15		20		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	0		0		0		ns

Note 24 Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 25)

Read Cycle

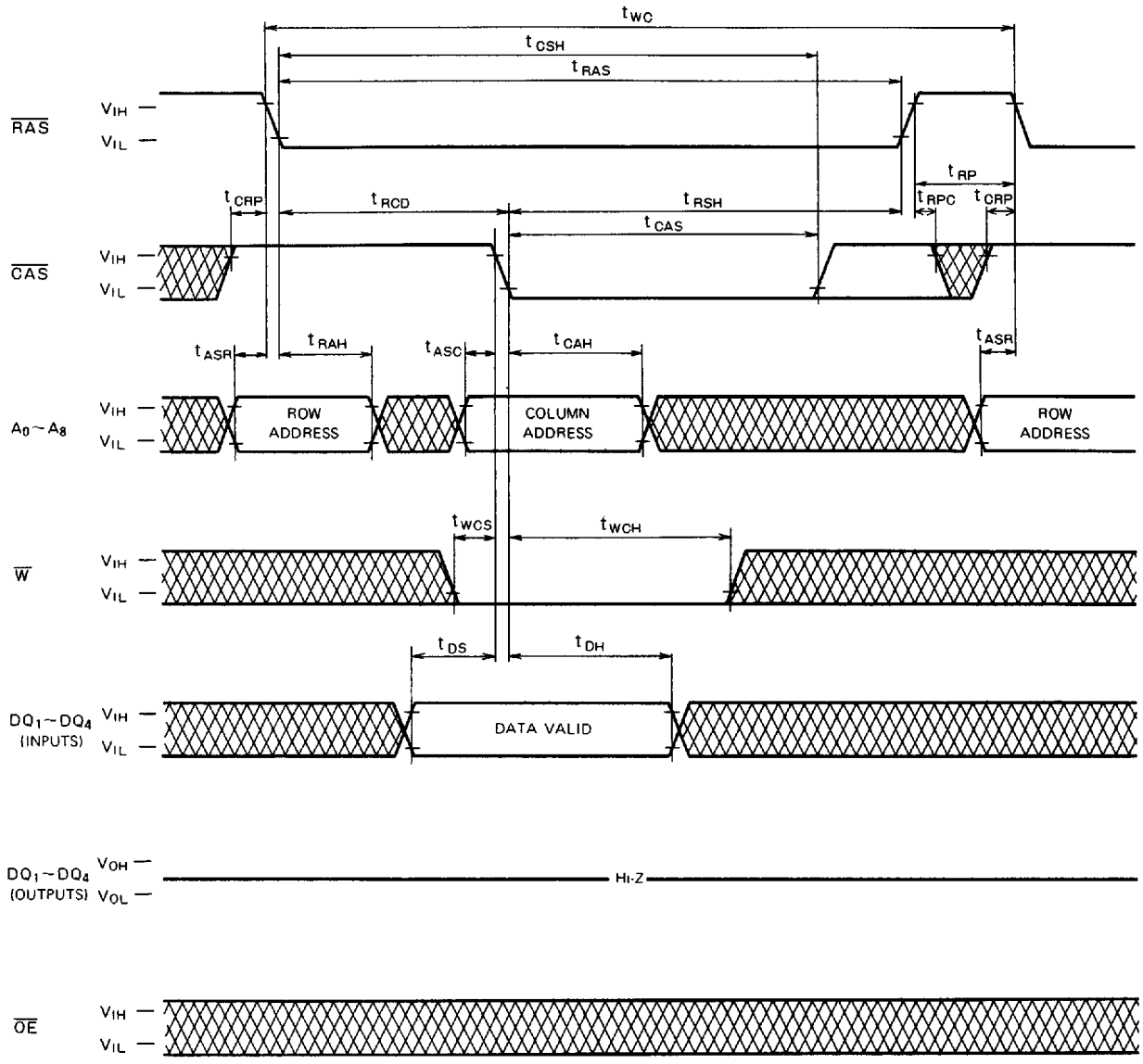


Note 25

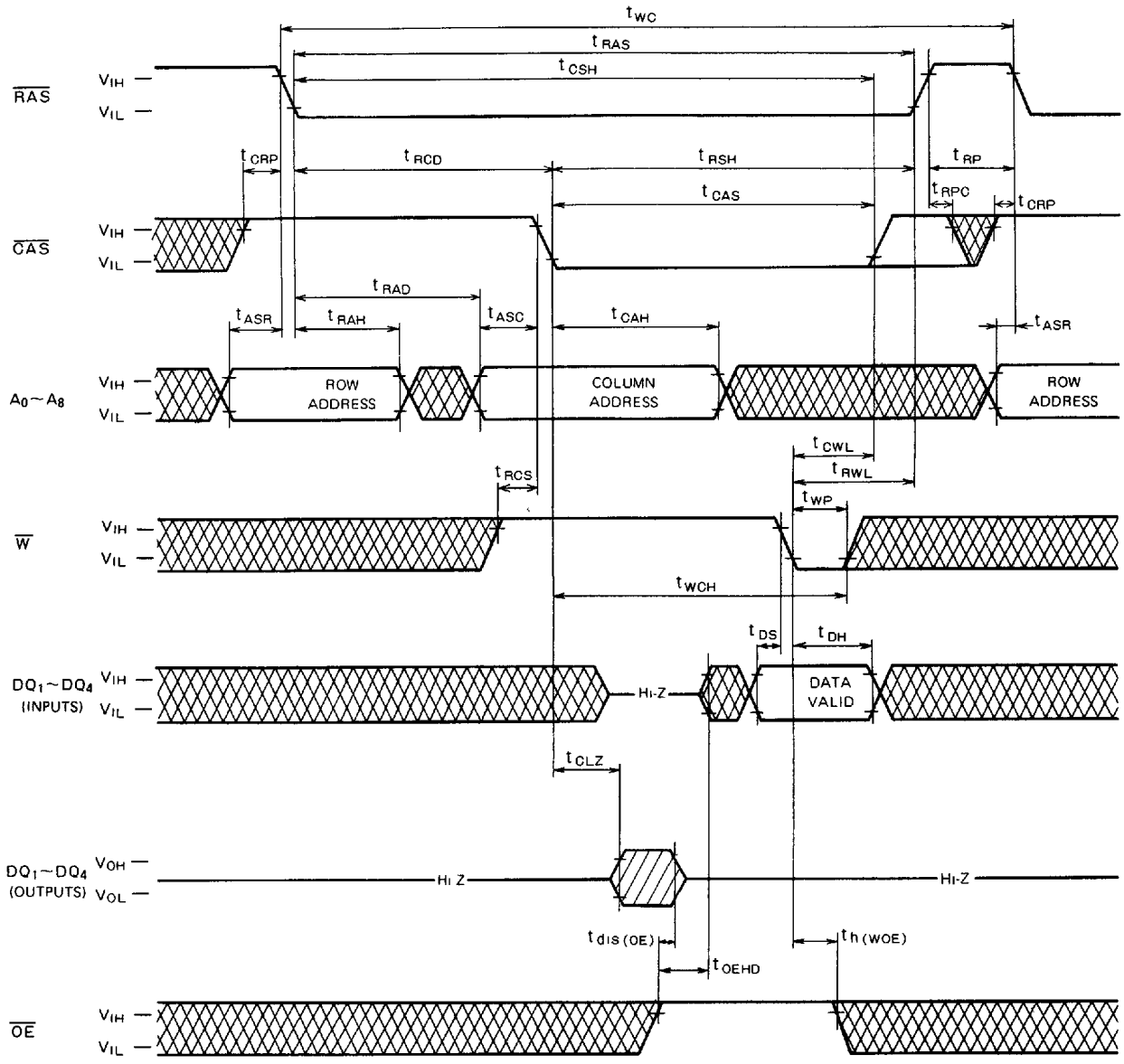
Indicates the don't care input
$V_{IH(min)} \leqq V_{IN} \leqq V_{IH(max)}$ or $V_{IL(min)} \leqq V_{IN} \leqq V_{IL(max)}$

Indicates the invalid output

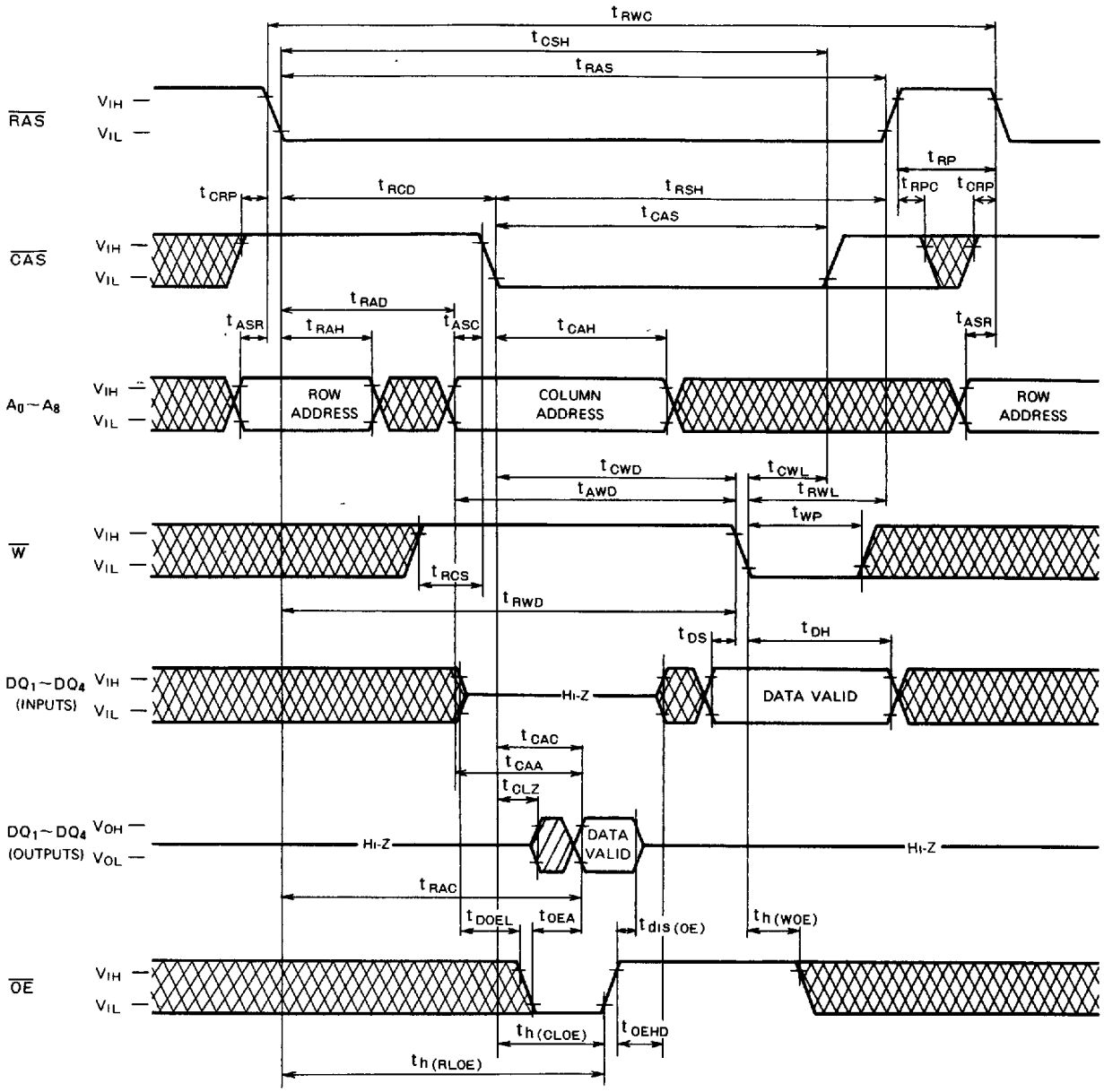
Write Cycle (Early write)



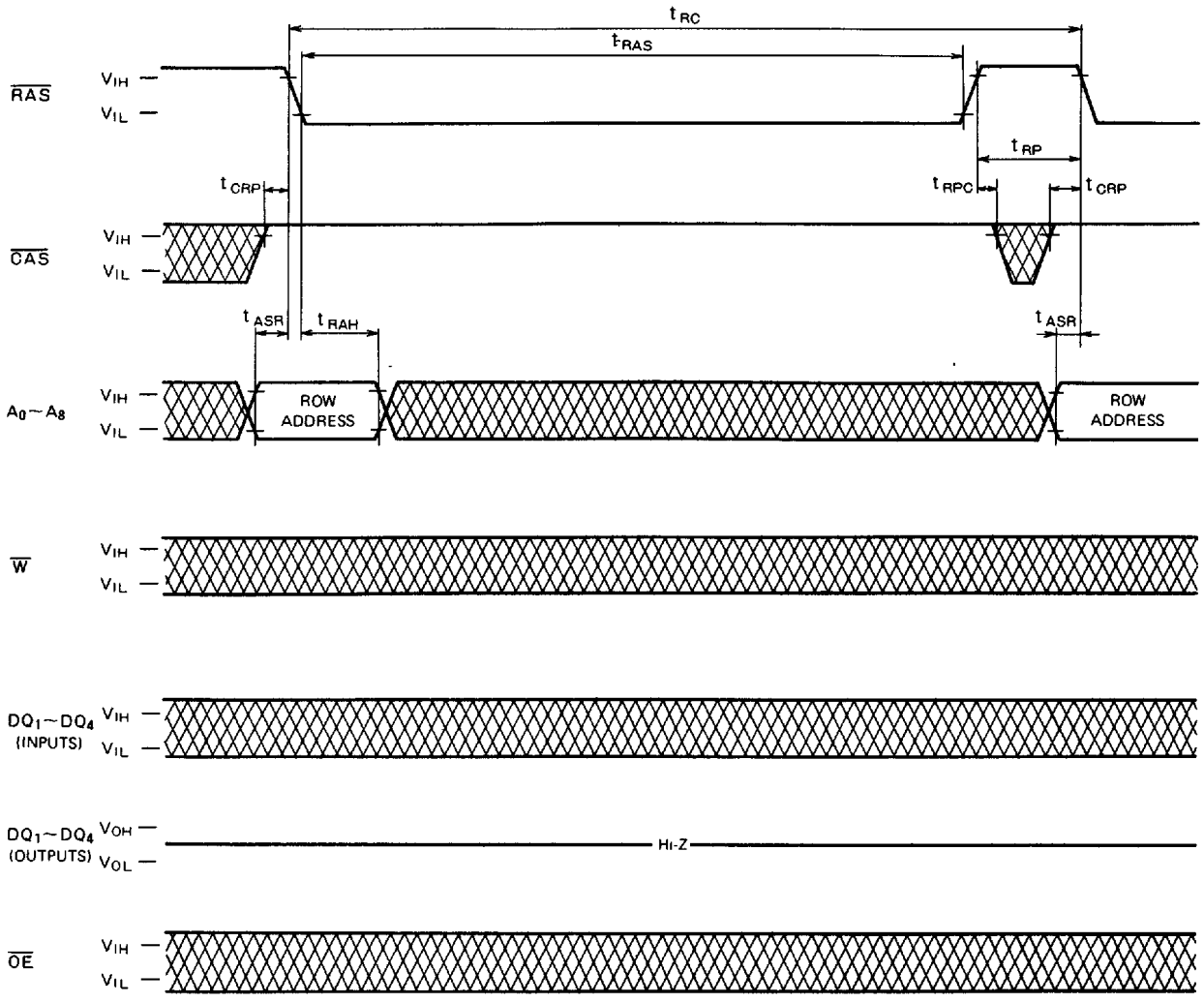
Write Cycle (Delayed Write)



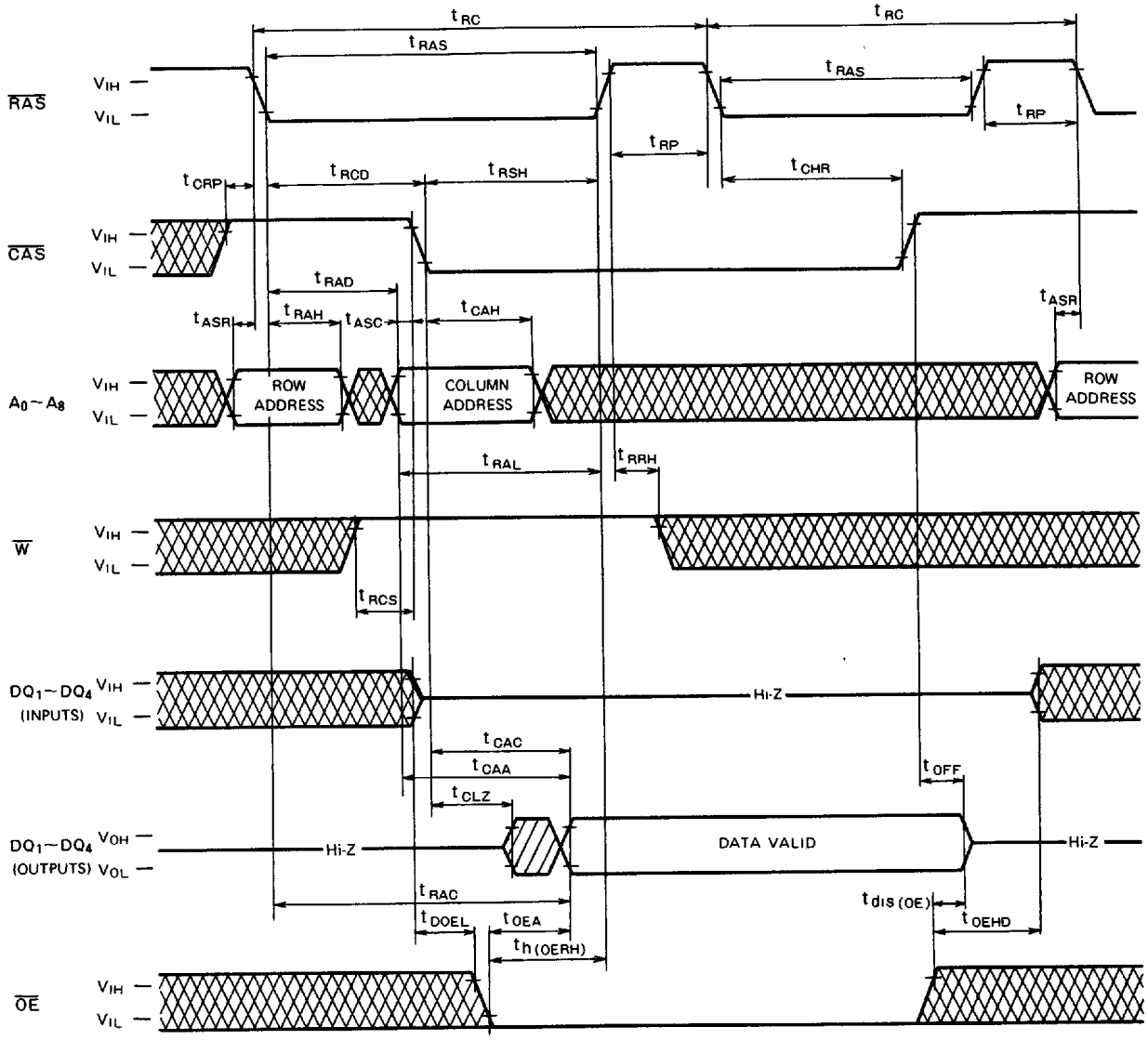
Read-Write, Read-Modify-Write Cycle



$\overline{RAS}$-only Refresh Cycle

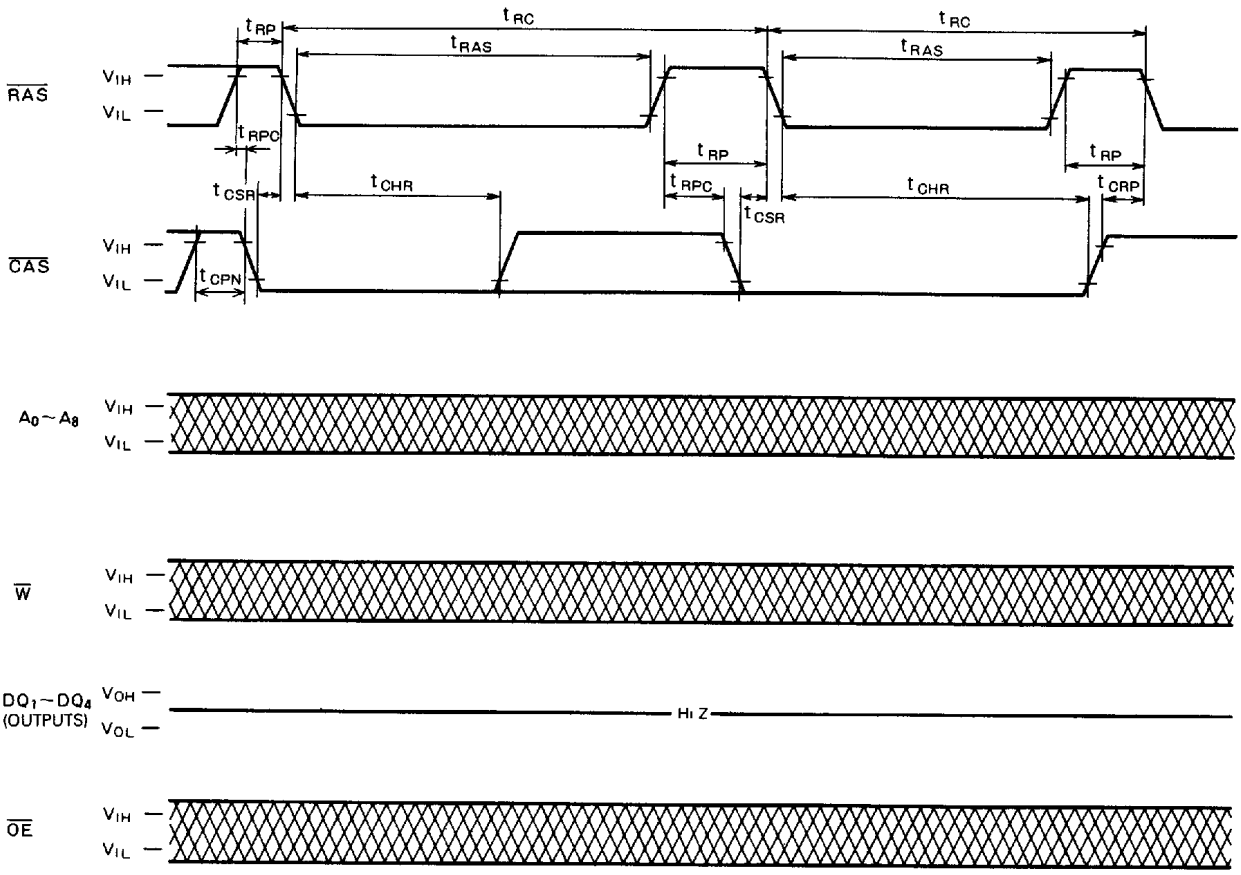


Hidden Refresh Cycle (Read) (Note 26)

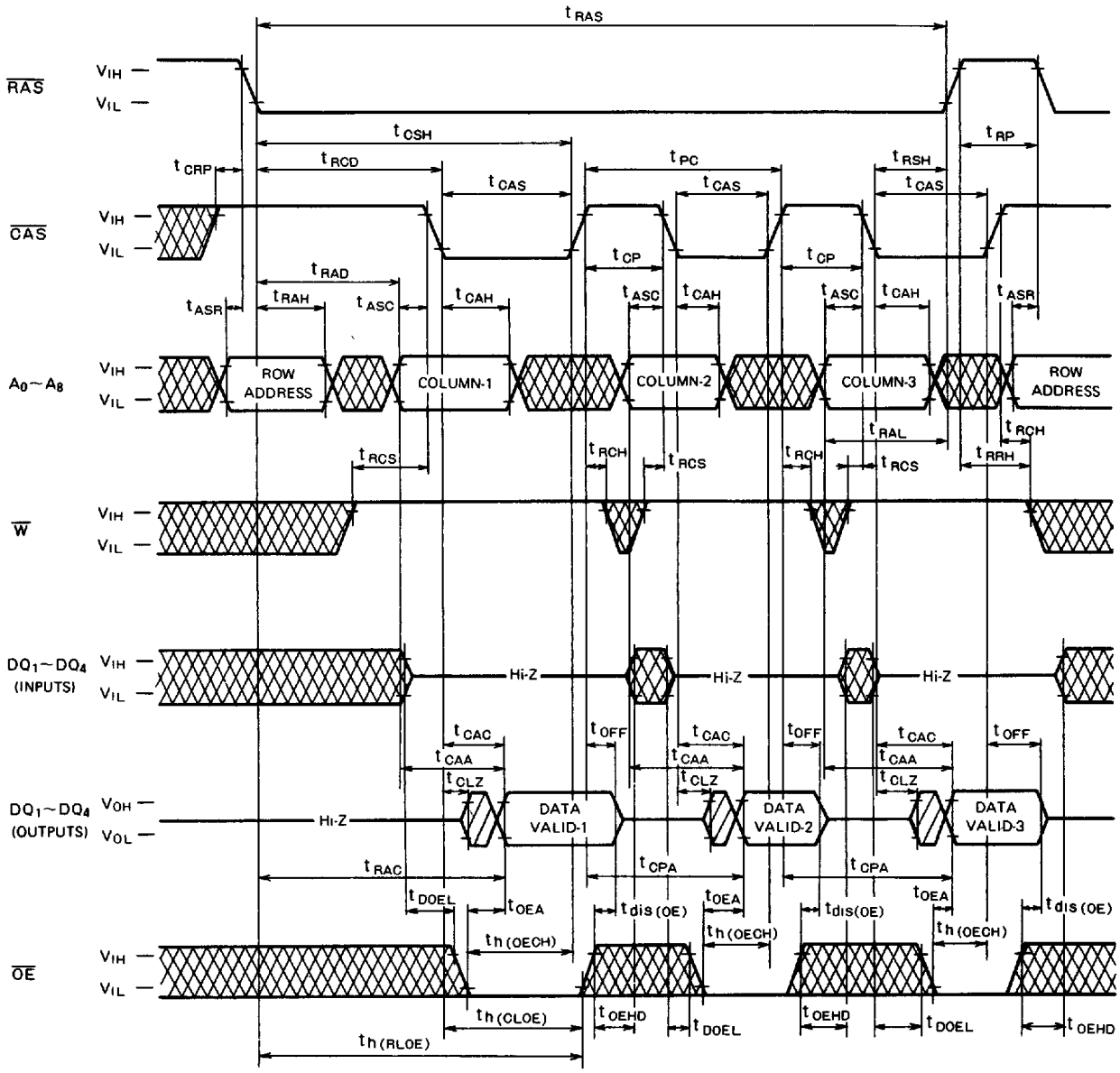


Note 26: Early write, delayed write, read-write or read-modify-write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown before.

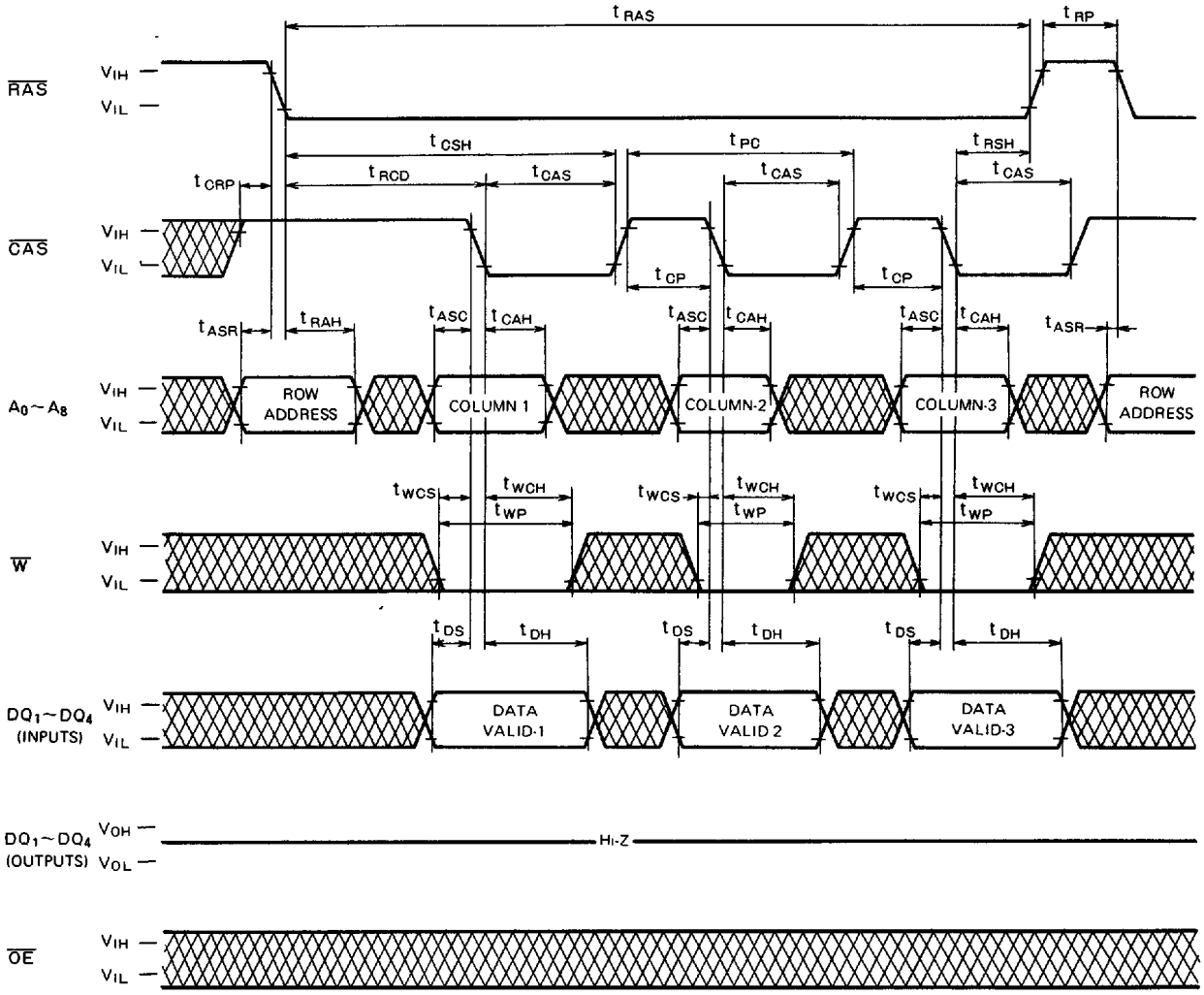
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



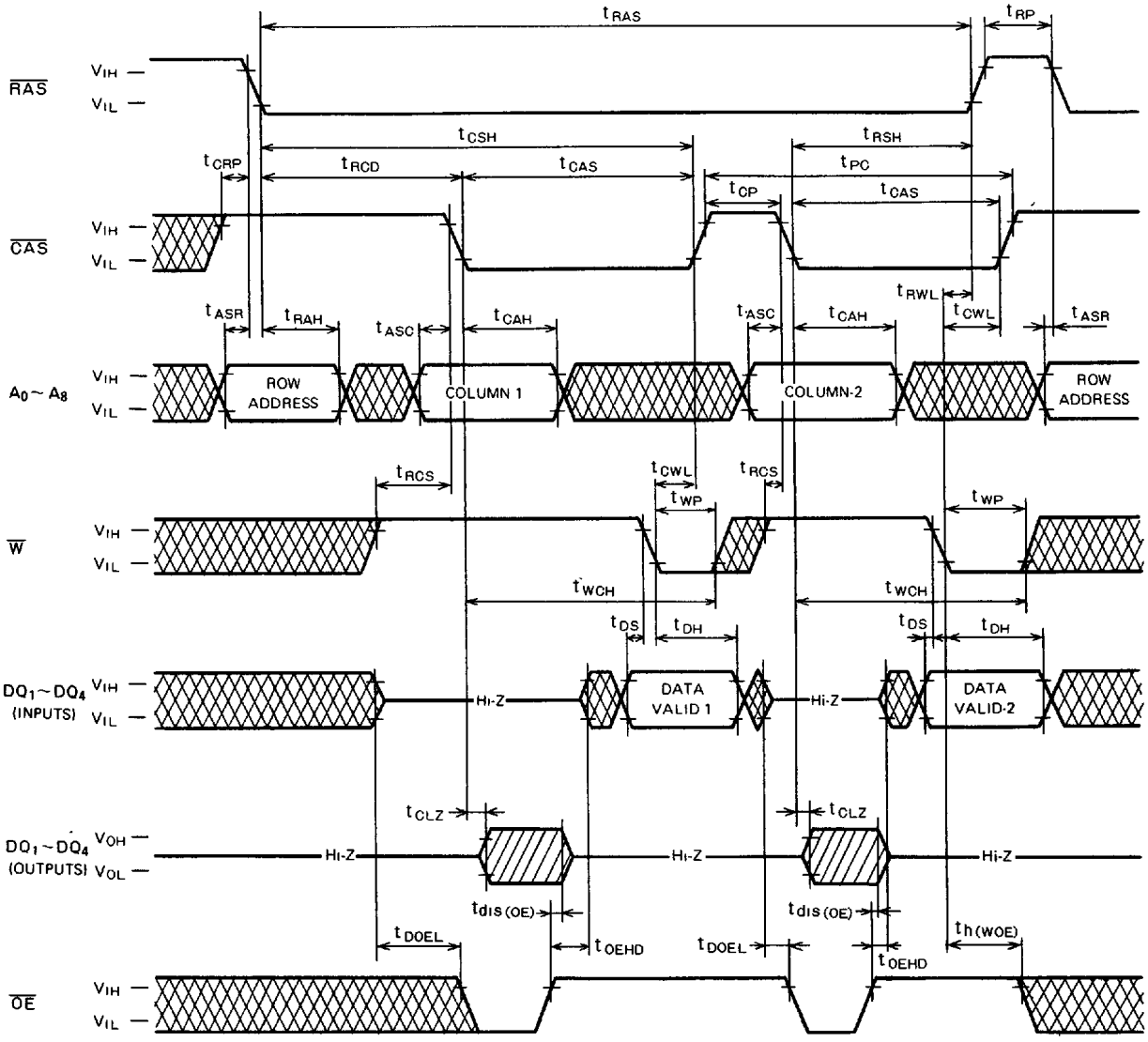
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle (Early Write)



Fast Page Mode Write Cycle (Delayed Write)



Fast Page Mode Read-Write, Read-Modify-Write Cycle