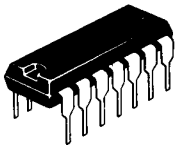


M58655P

1024-BIT(64-WORD BY 16-BIT) ELECTRICALLY ALTERABLE ROM

DESCRIPTION

The M58655P is a serial input/output 1024 bit electrically erasable and reprogrammable ROM organized as 64 words of 16 bits, and fabricated using MNOS technology. Data and addresses are transferred serially via a one-bit bidirectional bus.

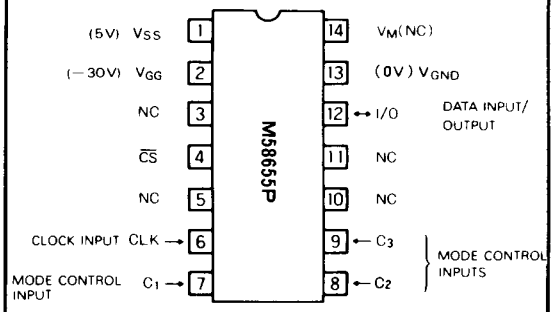
FEATURES

- Word-by-word electrically alterable
- Non-volatile data storage . . . . . 10 years (min)
- Write/erase time . . . . . 20ms word
- Typical power supply voltages . . . . . -30V, +5V
- Number of erase-write cycles . . . . . 10^5 times (min)
- Number of read access unrefreshed. . . 10^9 times (min)
- 5V I/O interface

APPLICATION

Non-volatile channel memories for electronic tuning systems and field-reprogrammable read-only memory systems

PIN CONFIGURATION (TOP VIEW)



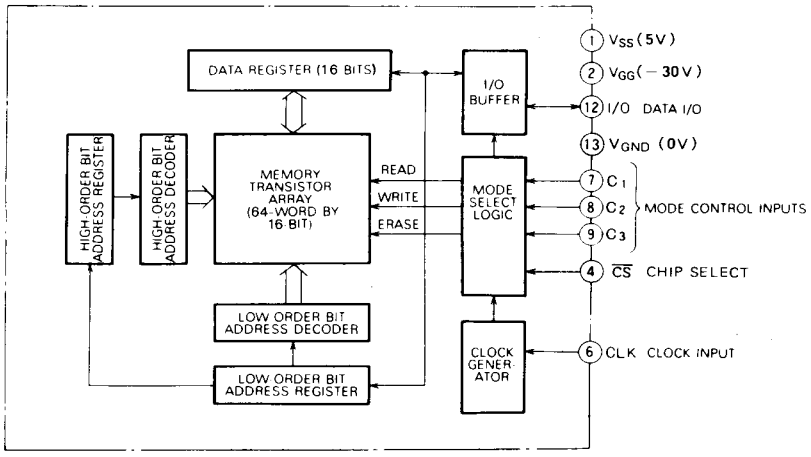
Outline 14P4

NC: NO CONNECTION

FUNCTION

The address is designated by two consecutive one-of-eight coded digits. Seven modes—accept address, accept data, shift data output, erase, write, read, and standby—are all selected by a 3-bit code applied to C_1, C_2, and C_3. Data is stored by internal negative writing pulses that selectively tunnel charges into the SiO_2—Si_3N_4 interface of the gate insulators of the MNOS memory transistors.

BLOCK DIAGRAM



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PIN DESCRIPTION

Pin	Name	Functions
I/O	I/O	In the accept address and accept data modes, used for input. In the shift data output mode, used for output In the standby, read, erase and write modes, this pin is in a floating state
V_M	Test	Used for testing purposes only. It should be left unconnected during normal operation
V_{SS}	Chip substrate voltage	Normally connected to +5V.
V_{GG}	Power supply voltage	Normally connected to −30V.
CLK	Clock input	Required for all operating modes, when $\overline{CS}$ is low.
C_1 C_3	Mode control input	Used to select the operation mode
V_{GND}	Ground voltage	Connected to ground (0V)
$\overline{CS}$	Chip select	Used for chip selection in "L"

OPERATION MODES

C_1	C_2	C_3	Functions
H	H	H	Standby mode. The contents of the address registers and the data register remain unchanged. The output buffer is held in the floating state
H	H	L	Not used
H	L	H	Erase mode. The word stored at the addressed location is erased. The data bits after erasing are all low level
H	L	L	Accept address mode. Data presented at the I/O pin is shifted into the address registers one bit with each clock pulse. The address is designated by two one-of-eight-coded digits. 64-word address is assigned in this mode.
L	H	H	Read mode. The addressed word is read from the memory into the data register.
L	H	L	Shift data output mode. The output driver is enabled and the contents of the data register are shifted to the I/O pin one bit with each clock pulse.
L	L	H	Write mode. The data contained in the data register is written into the location designated by the address registers.
L	L	L	Accept data mode. The data register accepts serial data from the I/O pin one bit with each clock pulse. The address registers remain unchanged.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{GG}	Supply voltage	With respect to V_{SS}	0.3 ~ −40	V
V_I	Input voltage		0.3 ~ −20	V
V_O	Output voltage		0.3 ~ −20	V
T_{stg}	Storage temperature		−40 ~ 125	℃
T_{opr}	Operating temperature		−10 ~ 70	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −10 ~ 70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{GG} V_{SS}	Supply voltage	−32.2	−35	−37.8	V
V_{SS} V_{GND}	Supply voltage	4.75	5	6	V
V_{IH}	High-level input voltage	V_{SS} − 1		V_{SS} + 0.3	V
V_{IL}	Low-level input voltage	V_{SS} − 6.5		V_{SS} − 4.25	V

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ELECTRICAL CHARACTERISTICS (T_a = −10~70°C, V_{GG}-V_{SS} = −35V ± 8%, V_{SS}-V_{GND} = 5V $^{+20\%}_{-5\%}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		$V_{SS}-1$		$V_{SS}+0.3$	V
V_{IL}	Low-level input voltage		$V_{SS}-6.5$		$V_{SS}-4.25$	V
I_{IL}	Low-level input current CLK, C1, C2, C3, I/O	$V_I-V_{SS}=-6.5V$	−10		+10	μA
R_I	Input pull-up resistance, $\overline{CS}$			30		kΩ
I_{OZL}	Off-state output current, low-level voltage applied	$V_O-V_{SS}=-6.5V$	−10		+10	μA
V_{OH}	High-level output voltage	$I_{OH}=-200\mu A$	$V_{SS}-1$			V
V_{OL}	Low-level output voltage	$I_{OL}=80\mu A$			$V_{GND}+0.5$	V
I_{GG}	Supply current from V_{GG}	$I_O=0\mu A$		5.5	8.8	mA

Note 1: Typical values are at Ta = 25°C and V_{GG}-V_{SS} = −35V.

TIMING REQUIREMENTS (T_a = −10~70°C, V_{GG}-V_{SS} = −35V ± 8%, V_{SS}-V_{GND} = 5V $^{+20\%}_{-5\%}$, unless otherwise noted)

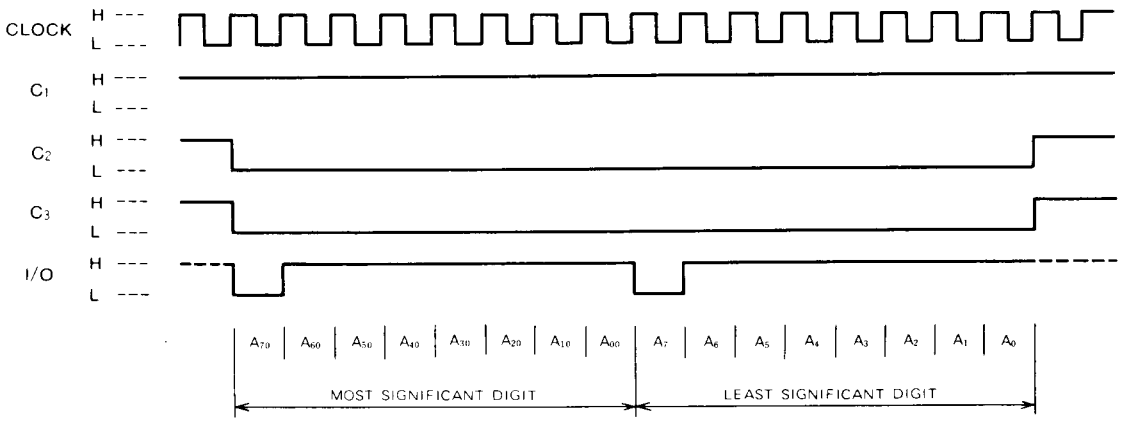
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$T_{L(\phi)}$	Negative clock pulse width		30			μs
$T_{H(\phi)}$	Positive clock pulse width		33			μs
$T_{(\phi)}$	Clock period				300	μs
t_W	Write time		16	20	24	ms
t_E	Erase time		16	20	24	ms
t_r, t_f	Risetime, fall time				1	μs
t_{su}	Control setup time before the fall of the clock pulse		1			μs
t_h	Control hold time after the rise of the clock pulse		0			μs
t_{ss}	Clock control setup time before the fall of $\overline{CS}$		1			μs
t_{hs}	Clock control hold time after the rise of $\overline{CS}$		1			μs

SWITCHING CHARACTERISTICS (T_a = −10~70°C, V_{GG} = −35V ± 8%, unless otherwise noted)

Symbol	Parameter	Alternative symbols	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{a(C)}$	Read access time	t_{PW}	C_L = 100pF, $V_{OH}=V_{SS}-2V$, $V_{OL}=V_{GND}+1.5V$			20	μs
t_S	Unpowered nonvolatile data retention time	T_S	$N_{EW}=10^4$, $t_{W(W)}=20ms$, $t_{W(E)}=20ms$	10			Year
		T_S	$N_{EW}=10^5$, $t_{W(W)}=20ms$, $t_{W(E)}=20ms$	1			
N_{EW}	Number of erase/write cycles	N_W		10^5			Times
N_{RA}	Number pF read access unrefreshed	N_{RA}		10^9			Times
t_{dv}	Data valid time	t_{PW}				20	μs

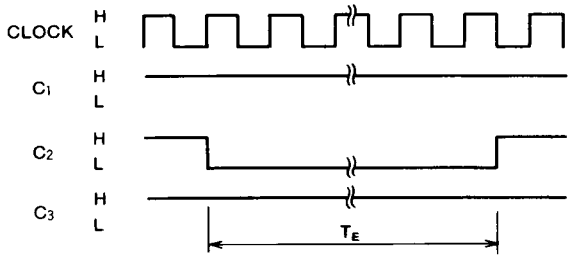
TIMING DIAGRAM

Accept Address Mode (16 clocks) $\overline{CS}$: L

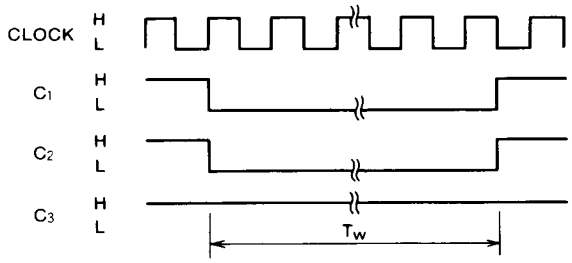


Note 2 The addresses from A_{00} to A_{77} are designated by two one-of-eight coded digits. The above figure shows designation of address A_{77}.

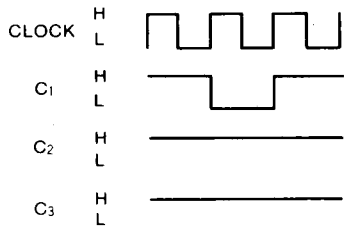
Erase Mode $\overline{CS}$: L



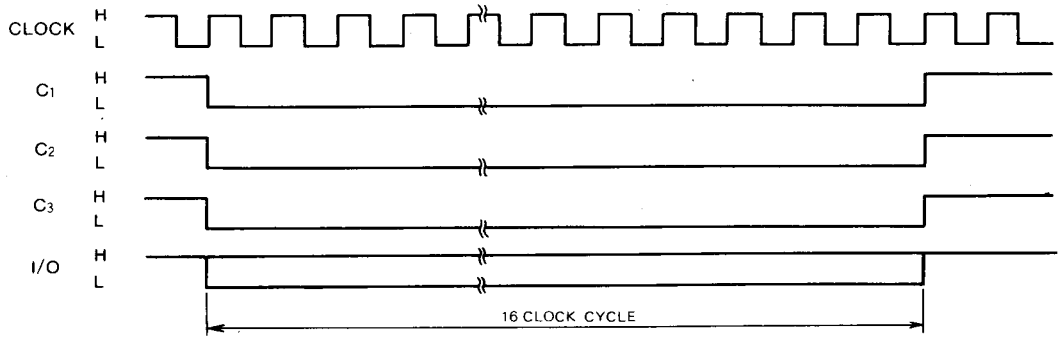
Write Mode $\overline{CS}$: L



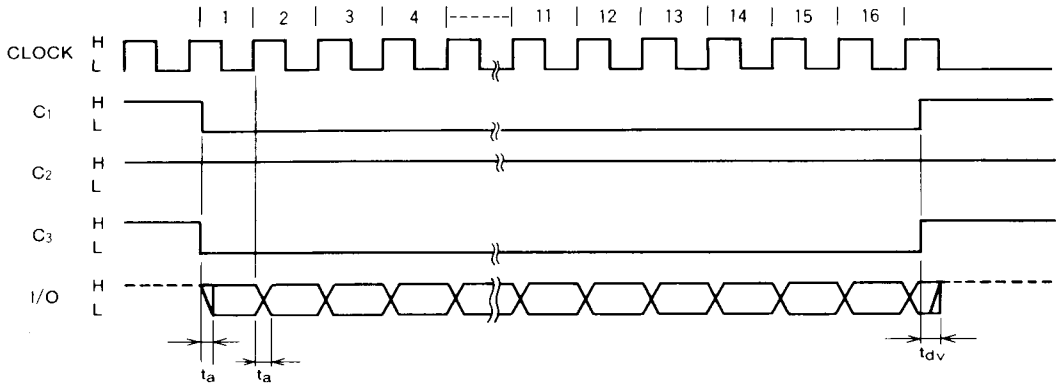
Read Mode (1 clock) $\overline{CS}$: L



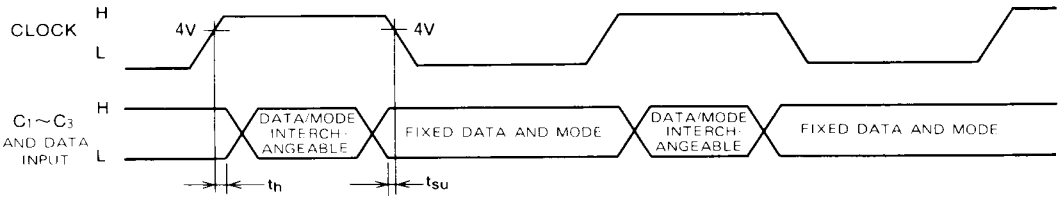
Accept Data (16 clocks) $\overline{CS}$: L



Shift Data Output Mode (16 clocks) $\overline{CS}$: L

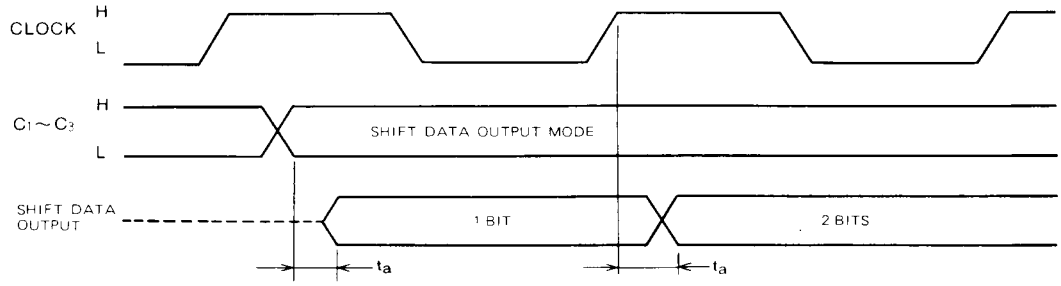


Timing of clock, C_1, C_2, C_3, and data input



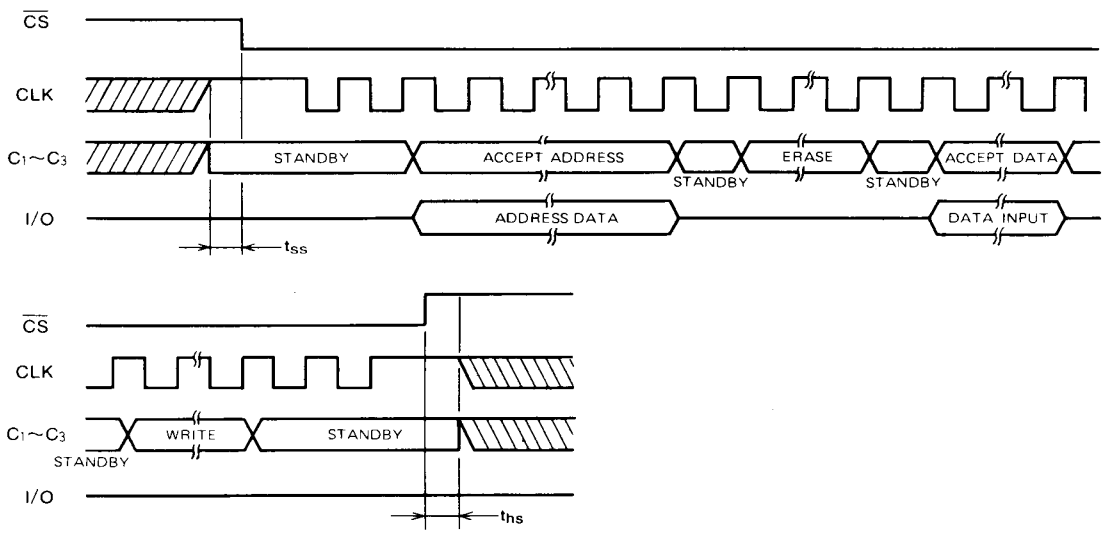
Note 3 $C_1 \sim C_3$ and accept data are interchnageable while the clock is set high.

Timing of clock, C_1, C_2, C_3, and data input



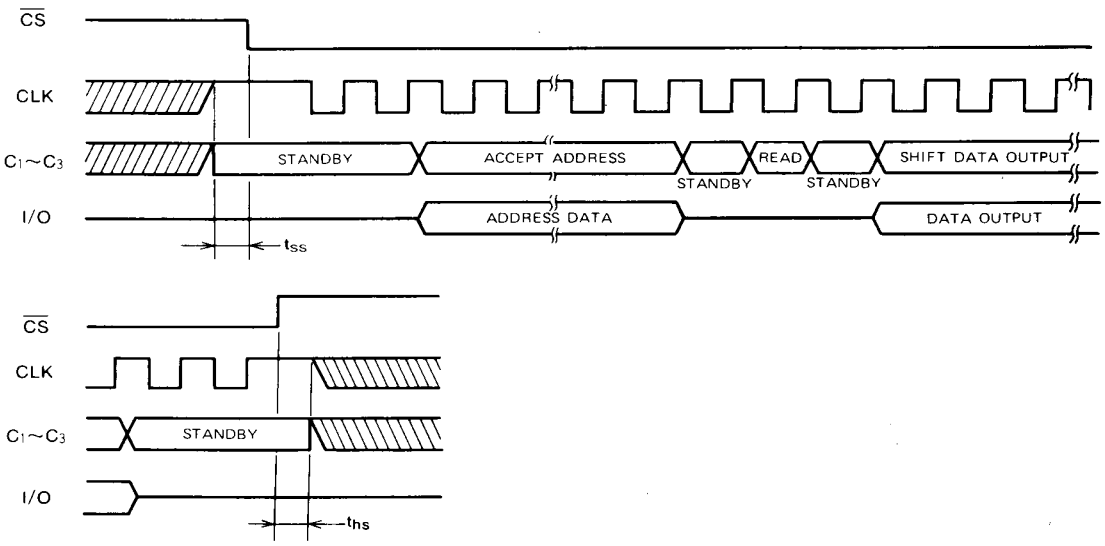
Operation flowchart

Rewriting flowchart



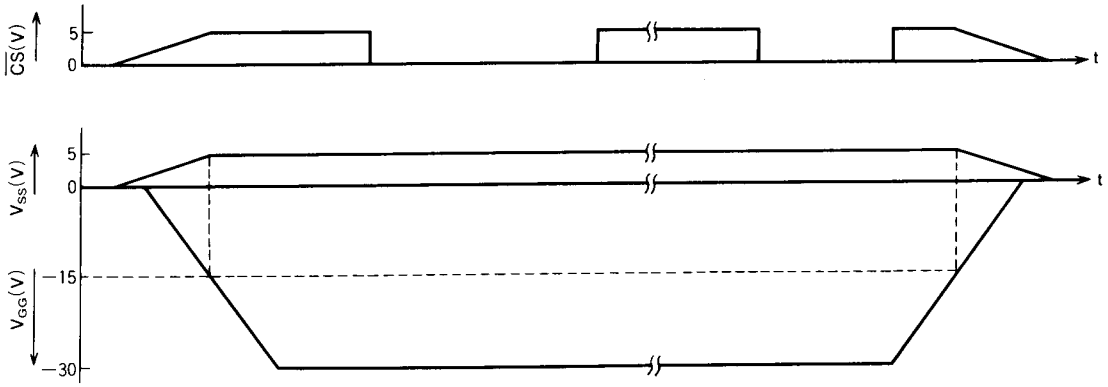
Note 4. One or more clock are required for standby between modes.
5. Set $\overline{CS}$ to the low level after the lapse of t_{ss} and CLK has been set high and $C_1 \sim C_3$ have been set to the standby mode.
6. Keep CLK to the high level and $C_1 \sim C_3$ to "standby" from the time when $\overline{CS}$ is set high to the lapse of t_{hs}.

Read Flowchart



Power-on/off Conditions

With power-on, V_{GG} is applied after V_{SS} has been applied. With power-off, V_{SS} is cut after V_{GG} has been cut. For power-on and off, hold $\overline{CS}$ in V_{SS} or floating state. The recommended timing chart for power-on and off is as follows.



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