# CY7C185

## 8K x 8 Static RAM

### Features

- **High speed**
  - **— 15 ns**
- **Fast $t_{DOE}$**
- **Low active power**
  - **— 715 mW**
- **Low standby power**
  - **— 220 mW**
- **CMOS for optimum speed/power**
- **Easy memory expansion with $\overline{CE}_1$, $CE_2$, and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**

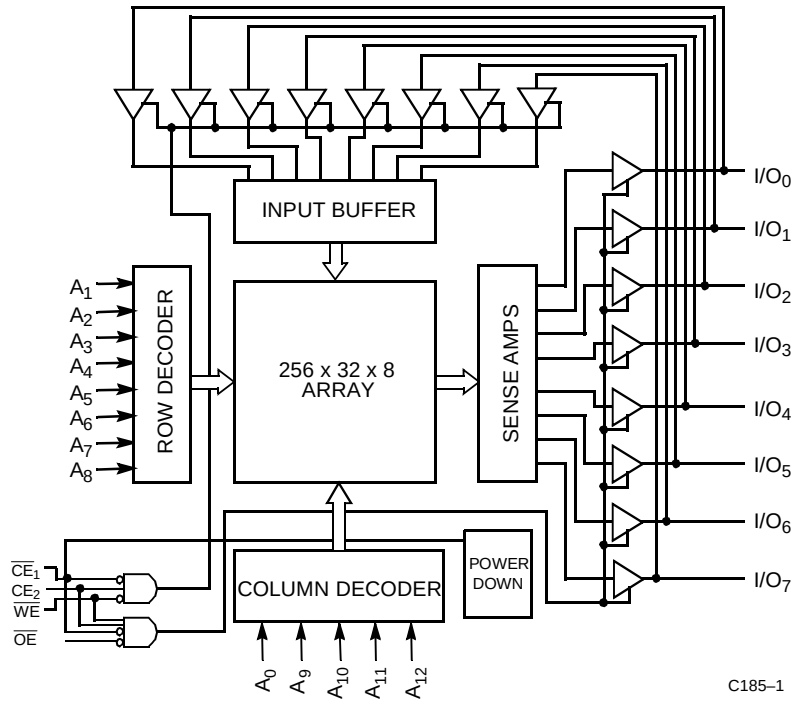
### Functional Description

The CY7C185 is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable ($CE_2$), and active LOW output enable ($\overline{OE}$) and three-state drivers. This device has an automatic power-down feature ($\overline{CE}_1$ or $CE_2$), reducing the power consumption by 70% when deselected. The CY7C185 is in a standard 300-mil-wide DIP, SOJ, or SOIC package.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}_1$ and $\overline{WE}$ inputs are both LOW and $CE_2$ is HIGH, data on the eight data input/output pins ($I/O_0$ through $I/O_7$) is written into the memory location addressed by the address present on the address pins ($A_0$ through $A_{12}$). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}_1$ and $\overline{OE}$ active LOW, $CE_2$ active HIGH, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

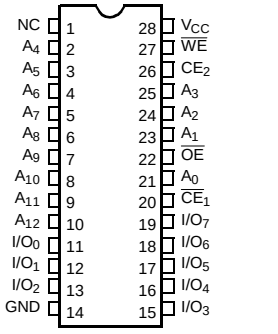
The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH. A die coat is used to insure alpha immunity.

### Logic Block Diagram




### Pin Configurations

**DIP/SOJ/SOIC**
**Top View**




### Selection Guide[1]

| | 7C185–15 | 7C185–20 | 7C185–25 | 7C185–35 |
|---|---|---|---|---|
| Maximum Access Time (ns) | 15 | 20 | 25 | 35 |
| Maximum Operating Current (mA) | 130 | 110 | 100 | 100 |
| Maximum Standby Current (mA) | 40/15 | 20/15 | 20/15 | 20/15 |

**Note:**
1. For military specifications, see the CY7C185A datasheet.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... –0.5V to +7.0V

DC Input Voltage[2] ..... –0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 5V ± 10% |
| Industrial | –40°C to +85°C | 5V ± 10% |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | 7C185–15 | | 7C185–20 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = –4.0 mA | 2.4 | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 8.0 mA | | 0.4 | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.2 | $V_{CC}$ + 0.3V | 2.2 | $V_{CC}$ + 0.3V | V |
| $V_{IL}$ | Input LOW Voltage[2] | | –0.5 | 0.8 | –0.5 | 0.8 | V |
| $I_{IX}$ | Input Load Current | GND ≤ $V_I$ ≤ $V_{CC}$ | –5 | +5 | –5 | +5 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$, Output Disabled | –5 | +5 | –5 | +5 | µA |
| $I_{OS}$ | Output Short Circuit Current[3] | $V_{CC}$ = Max., $V_{OUT}$ = GND | | –300 | | –300 | mA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA | | 130 | | 110 | mA |
| $I_{SB1}$ | Automatic Power-Down Current | Max. $V_{CC}$, $\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$ Min. Duty Cycle=100% | 40 | | 20 | | mA |
| $I_{SB2}$ | Automatic Power-Down Current | Max. $V_{CC}$, $\overline{CE}_1 \geq V_{CC}$ – 0.3V, or $CE_2 \leq 0.3V$ $V_{IN} \geq V_{CC}$ – 0.3V or $V_{IN} \leq 0.3V$ | 15 | | 15 | | mA |

**Notes:**

2. Minimum voltage is equal to –3.0V for pulse durations less than 30 ns.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

## Electrical Characteristics Over the Operating Range (continued)

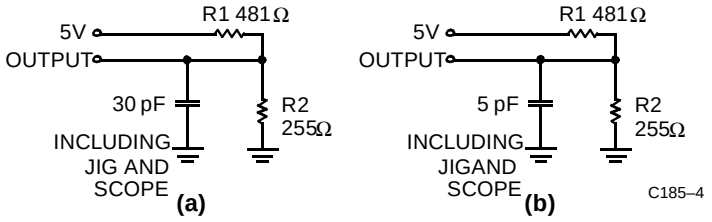
| Parameter | Description | Test Conditions | 7C185–25 | | 7C185-35 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = –4.0 mA | 2.4 | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 8.0 mA | | 0.4 | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.2 | $V_{CC}$ + 0.3V | 2.2 | $V_{CC}$ + 0.3V | V |
| $V_{IL}$ | Input LOW Voltage[2] | | –0.5 | 0.8 | –0.5 | 0.8 | V |
| $I_{IX}$ | Input Load Current | GND ≤ $V_I$ ≤ $V_{CC}$ | –5 | +5 | –5 | +5 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$, Output Disabled | –5 | +5 | –5 | +5 | µA |
| $I_{OS}$ | Output Short Circuit Current[3] | $V_{CC}$ = Max., $V_{OUT}$ = GND | | –300 | | –300 | mA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA | | 100 | | 100 | mA |
| $I_{SB1}$ | Automatic Power-Down Current | Max. $V_{CC}$, $\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$ Min. Duty Cycle=100% | | 20 | | 20 | mA |
| $I_{SB2}$ | Automatic Power-Down Current | Max. $V_{CC}$, $\overline{CE}_1 \geq V_{CC}$ – 0.3V or $CE_2 \leq 0.3V$ $V_{IN} \geq V_{CC}$ – 0.3V or $V_{IN} \leq 0.3V$ | | 15 | | 15 | mA |

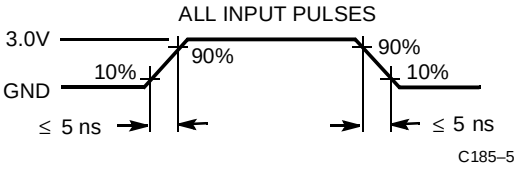
## Capacitance[4]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 5.0V | 7 | pF |
| $C_{OUT}$ | Output Capacitance | | 7 | pF |

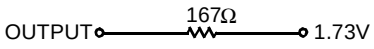
**Note:**
4. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms




Equivalent to: THÉVENIN EQUIVALENT



## Switching Characteristics Over the Operating Range[5]

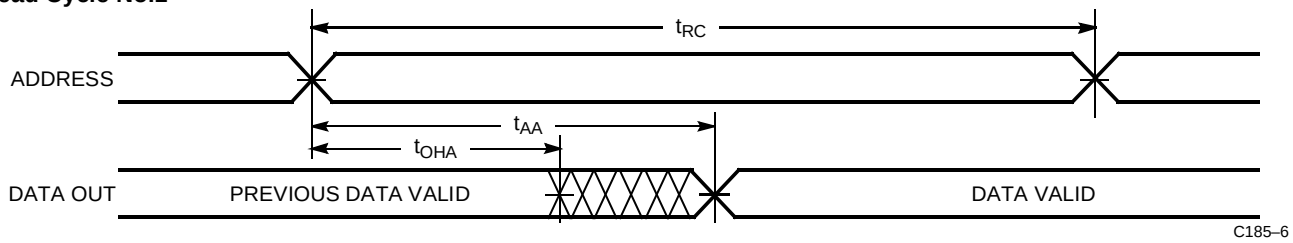
| Parameter | Description | 7C185–15 | | 7C185–20 | | 7C185–25 | | 7C185–35 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **READ CYCLE** | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 15 | | 20 | | 25 | | 35 | | ns |
| $t_{AA}$ | Address to Data Valid | | 15 | | 20 | | 25 | | 35 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 3 | | 5 | | 5 | | 5 | | ns |
| $t_{ACE1}$ | $\overline{CE}_1$ LOW to Data Valid | | 15 | | 20 | | 25 | | 35 | ns |
| $t_{ACE2}$ | $CE_2$ HIGH to Data Valid | | 15 | | 20 | | 25 | | 35 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 8 | | 9 | | 12 | | 15 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z[6] | | 7 | | 8 | | 10 | | 10 | ns |
| $t_{LZCE1}$ | $\overline{CE}_1$ LOW to Low Z[7] | 3 | | 5 | | 5 | | 5 | | ns |
| $t_{LZCE2}$ | $CE_2$ HIGH to Low Z | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{HZCE}$ | $\overline{CE}_1$ HIGH to High Z[6, 7]<br>$CE_2$ LOW to High Z | | 7 | | 8 | | 10 | | 10 | ns |
| $t_{PU}$ | $\overline{CE}_1$ LOW to Power-Up<br>$CE_2$ to HIGH to Power-Up | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{PD}$ | $\overline{CE}_1$ HIGH to Power-Down<br>$CE_2$ LOW to Power-Down | | 15 | | 20 | | 20 | | 20 | ns |
| **WRITE CYCLE**[8] | | | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 15 | | 20 | | 25 | | 35 | | ns |
| $t_{SCE1}$ | $\overline{CE}_1$ LOW to Write End | 12 | | 15 | | 20 | | 20 | | ns |
| $t_{SCE2}$ | $CE_2$ HIGH to Write End | 12 | | 15 | | 20 | | 20 | | ns |
| $t_{AW}$ | Address Set-Up to Write End | 12 | | 15 | | 20 | | 25 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{SA}$ | Address Set-Up to Write Start | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 12 | | 15 | | 15 | | 20 | | ns |
| $t_{SD}$ | Data Set-Up to Write End | 8 | | 10 | | 10 | | 12 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z[6] | | 7 | | 7 | | 7 | | 8 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z | 3 | | 5 | | 5 | | 5 | | ns |

**Notes:**

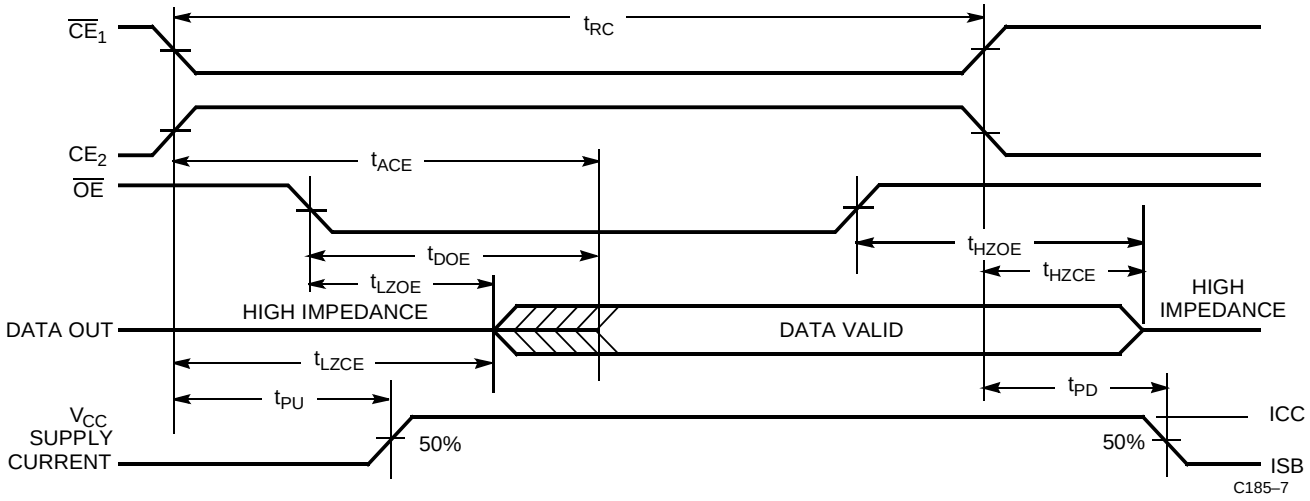
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified $I_{OL}/I_{OH}$ and 30-pF load capacitance.
6. $t_{HZOE}$, $t_{HZCE}$, and $t_{HZWE}$ are specified with $C_L$ = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
7. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE1}$ and $t_{LZCE2}$ for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $CE_2$ HIGH, and $\overline{WE}$ LOW. All 3 signals must be active to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

## Switching Waveforms

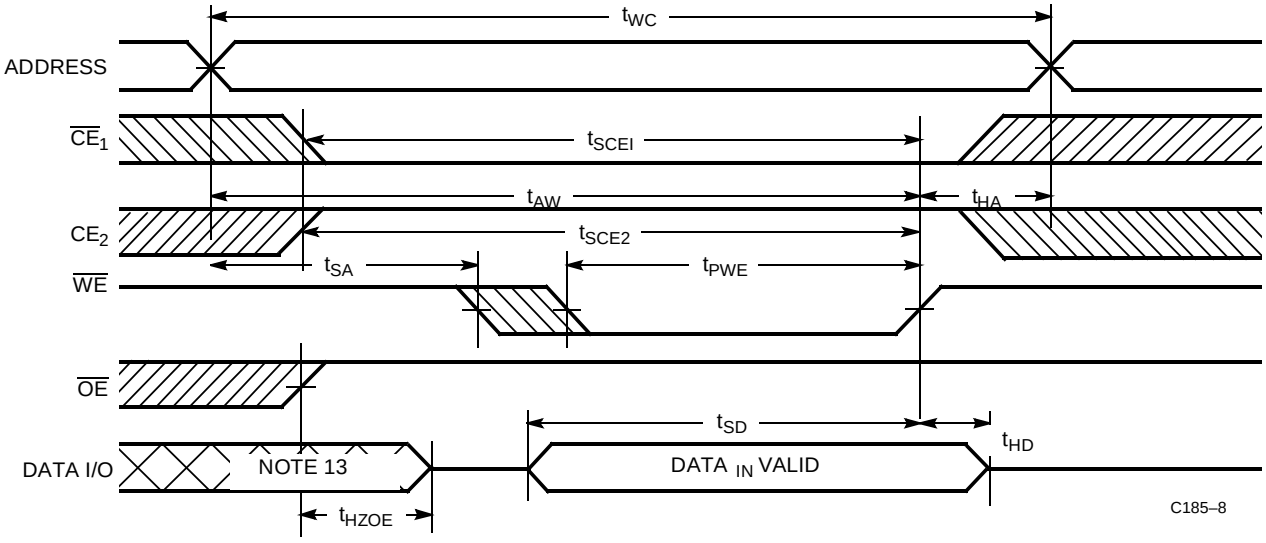
### Read Cycle No.1[9,10]




### Read Cycle No.2[11,12]



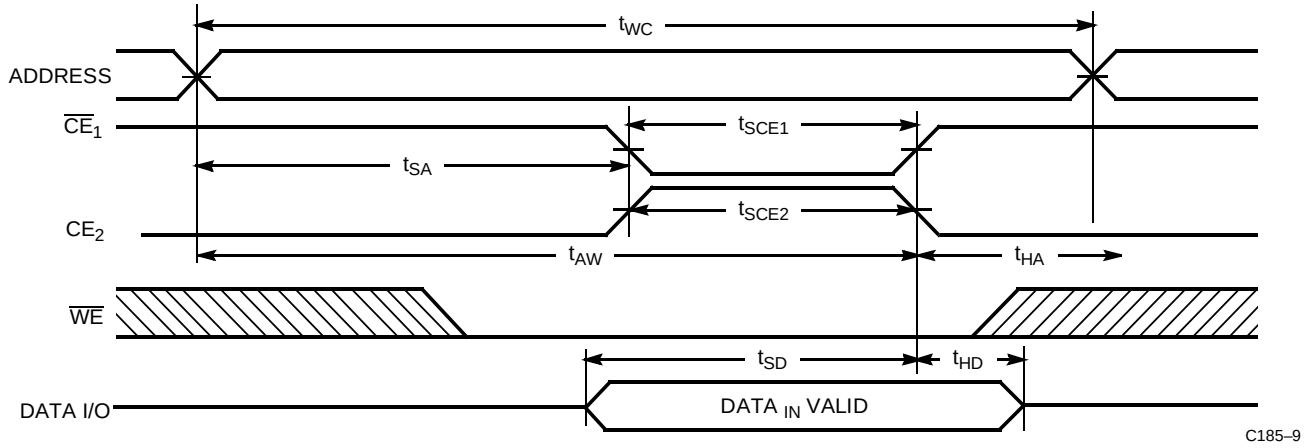

### Write Cycle No. 1 (WE Controlled)[10,12]



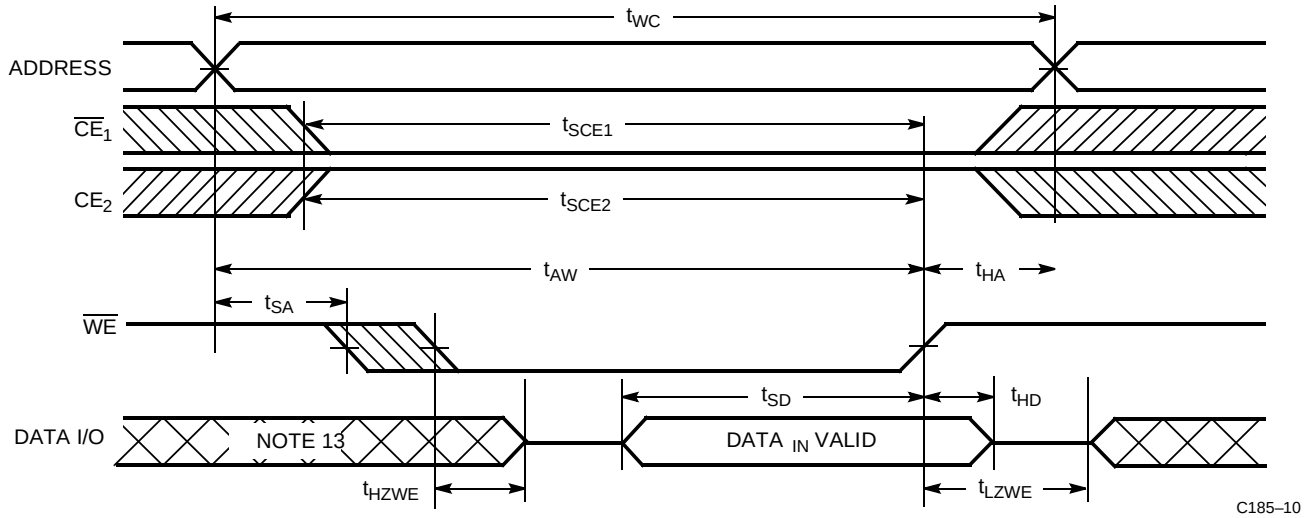

9. Device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = $V_{IL}$. $CE_2$ = $V_{IH}$.
10. $\overline{WE}$ is HIGH for read cycle.
11. Data I/O is High Z if $\overline{OE}$ = $V_{IH}$, $\overline{CE_1}$ = $V_{IH}$, $\overline{WE}$ = $V_{IL}$, or $CE_2$=$V_{IL}$.
12. The internal write time of the memory is defined by the overlap of $\overline{CE_1}$ LOW, $CE_2$ HIGH and $\overline{WE}$ LOW. $\overline{CE_1}$ and $\overline{WE}$ must be LOW and $CE_2$ must be HIGH to initiate write. A write can be terminated by $\overline{CE_1}$ or $\overline{WE}$ going HIGH or $CE_2$ going LOW. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
13. During this period, the I/Os are in the output state and input signals should not be applied.

## Switching Waveforms (continued)

### Write Cycle No. 2 ($\overline{CE}$ Controlled)[12,13,14]




### Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[12,13,14,15]

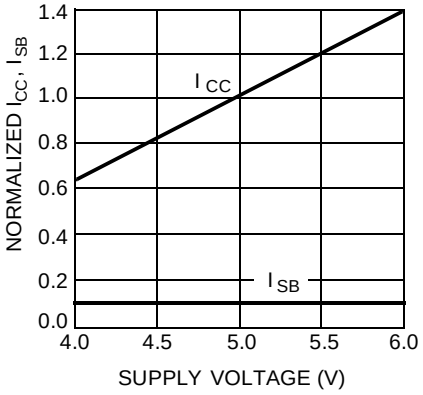



**Notes:**

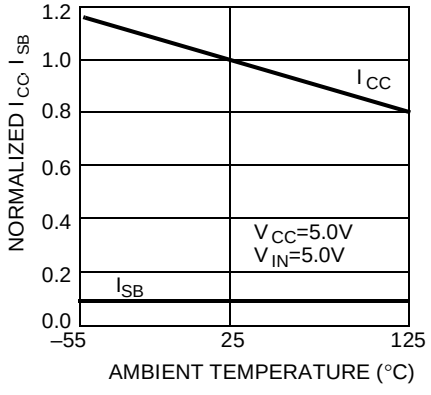
14. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of $t_{HZWE}$ and $t_{SD}$.
15. If $\overline{CE}_1$ goes HIGH or $CE_2$ goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

## Typical DC and AC Characteristics

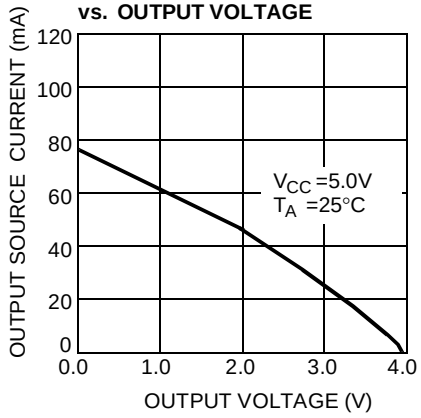
**NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE**



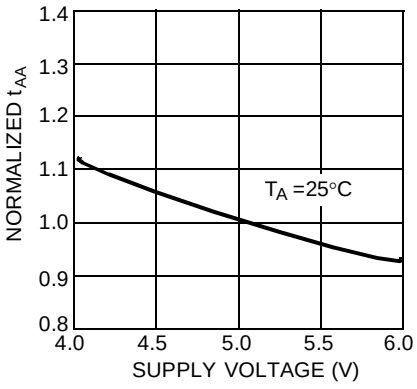

**NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE**



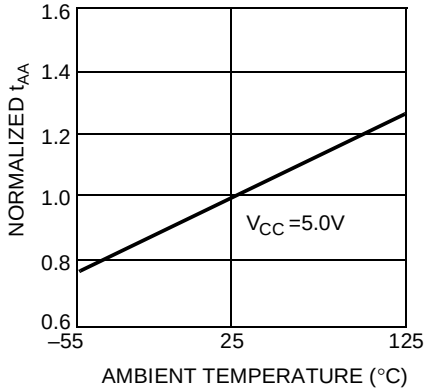

**OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE**



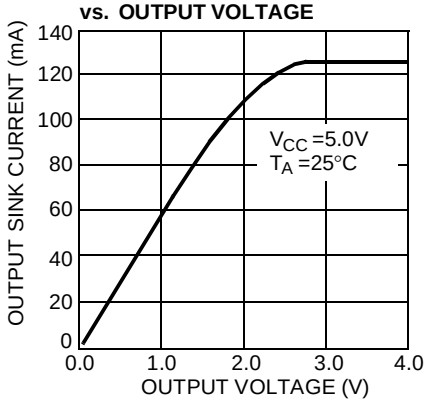

**NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE**



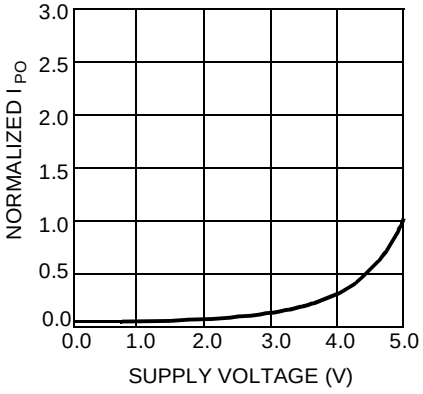

**NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE**



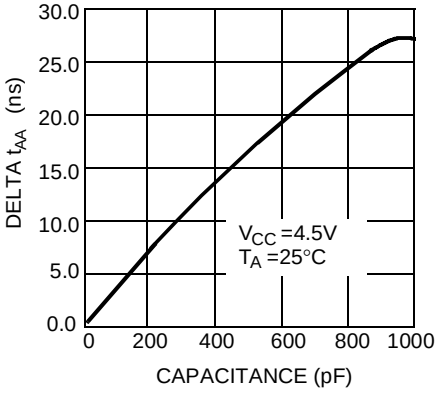

**OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE**



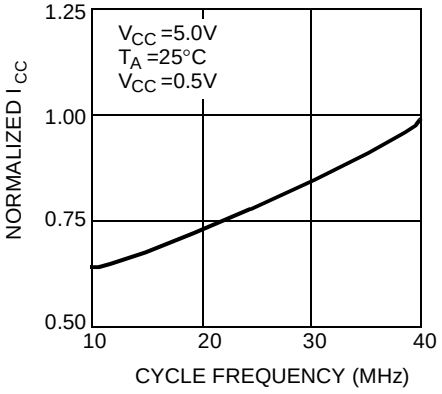

**TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE**




**TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING**




**NORMALIZED $I_{CC}$ vs. CYCLE TIME**



## Truth Table

| $\overline{CE}_1$ | $CE_2$ | $\overline{WE}$ | $\overline{OE}$ | Input/Output | Mode |
|---|---|---|---|---|---|
| H | X | X | X | High Z | Deselect/Power-Down |
| X | L | X | X | High Z | Deselect/Power-Down |
| L | H | H | L | Data Out | Read |
| L | H | L | X | Data In | Write |
| L | H | H | H | High Z | Deselect |

## Address Designators

| Address Name | Address Function | Pin Number |
|---|---|---|
| A4 | X3 | 2 |
| A5 | X4 | 3 |
| A6 | X5 | 4 |
| A7 | X6 | 5 |
| A8 | X7 | 6 |
| A9 | Y1 | 7 |
| A10 | Y4 | 8 |
| A11 | Y3 | 9 |
| A12 | Y0 | 10 |
| A0 | Y2 | 21 |
| A1 | X0 | 23 |
| A2 | X1 | 24 |
| A3 | X2 | 25 |

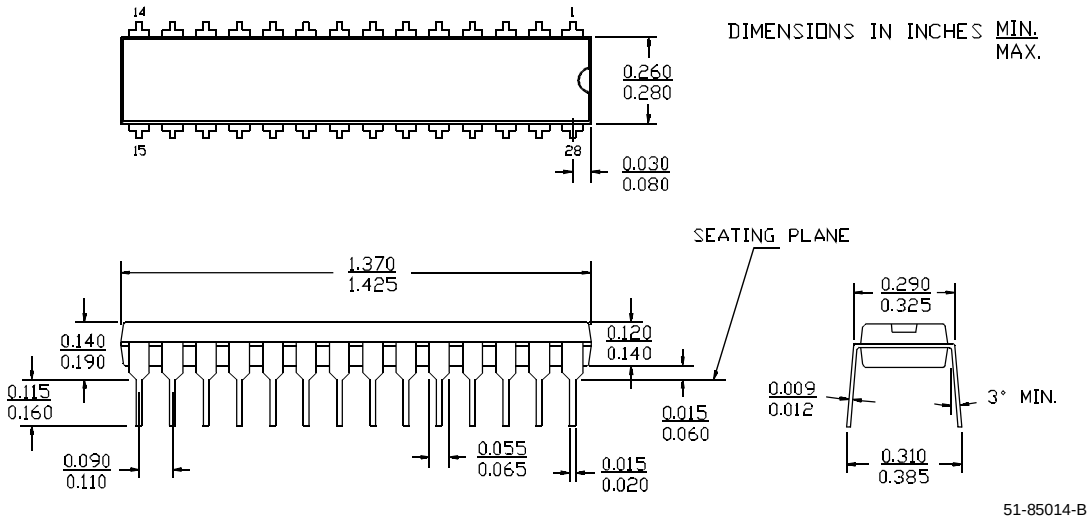
## Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 15 | CY7C185–15PC | P21 | 28-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C185–15SC | S21 | 28-Lead Molded SOIC | |
| | CY7C185–15VC | V21 | 28-Lead Molded SOJ | |
| | CY7C185–15VI | V21 | 28-Lead Molded SOJ | Industrial |
| 20 | CY7C185–20PC | P21 | 28-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C185–20SC | S21 | 28-Lead Molded SOIC | |
| | CY7C185–20VC | V21 | 28-Lead Molded SOJ | |
| | CY7C185–20VI | V21 | 28-Lead Molded SOJ | Industrial |
| 25 | CY7C185–25PC | P21 | 28-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C185–25SC | S21 | 28-Lead Molded SOIC | |
| | CY7C185–25VC | V21 | 28-Lead Molded SOJ | |
| | CY7C185–25VI | V21 | 28-Lead Molded SOJ | Industrial |
| 35 | CY7C185–35PC | P21 | 28-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C185–35SC | S21 | 28-Lead Molded SOIC | |
| | CY7C185–35VC | V21 | 28-Lead Molded SOJ | |
| | CY7C185–35VI | V21 | 28-Lead Molded SOJ | Industrial |

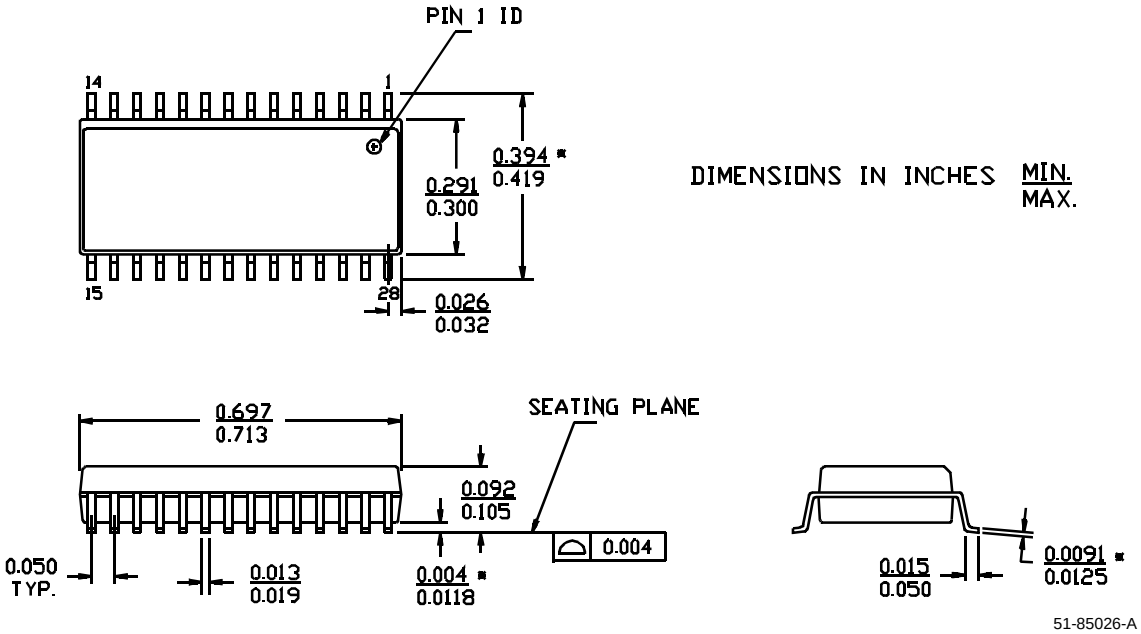
Document #: 38–00037–K

## Package Diagrams

**28-Lead (300-Mil) Molded DIP P21**




**28-Lead (300-Mil) Molded SOIC S21**



## Package Diagrams (continued)

**28-Lead (300-Mil) Molded SOJ V21**