MC145000
MC145001

SERIAL INPUT MULTIPLEXED LCD DRIVERS (MASTER AND SLAVE)

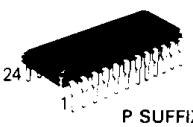
The MC145000 (Master) LCD Driver and the MC145001 (Slave) LCD Driver are CMOS devices designed to drive liquid crystal displays in a multiplexed-by-four configuration. The Master unit generates both frontplane and backplane waveforms, and is capable of independent operation. The Slave unit generates only frontplane waveforms, and is synchronized with the backplanes from the Master unit. Several Slave units may be cascaded from the Master unit to increase the number of LCD segments driven in the system. The maximum number of frontplanes is dependent upon the capacitive loading on the backplane drivers and the drive frequency. The devices use data from a microprocessor or other serial data and clock source to drive one LCD segment per bit.

- Direct Interface to CMOS Microprocessors
- Serial Data Port, Externally Clocked
- Multiplexing-By-Four
- Net dc Drive Component Less Than 50 mV
- Master Drives 48 LCD Segments
- Slave Provides Frontplane Drive for 44 LCD Segments
- Drives Large Segments —Up to one Square Centimeter
- Supply Voltage Range = 3 V to 6 V
- Latch Storage of Input Data
- Low Power Dissipation
- Logic Input Voltage Can Exceed V_{DD}
- Accomodates External Temperature Compensation
- Chip Complexities: MC145000 – 1723 FETs or 431 Equivalent Gates
  MC145001 – 1495 FETs or 374 Equivalent Gates

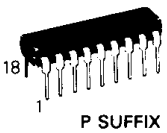
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

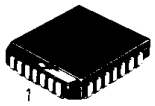
SERIAL INPUT
MULTIPLEXED LCD DRIVERS
(MASTER AND SLAVE)



P SUFFIX
PLASTIC DIP
CASE 709



P SUFFIX
PLASTIC DIP
CASE 707



FN SUFFIX
PLCC
CASE 776

ORDERING INFORMATION

MC14500xP	Plastic DIP
MC14500xFN	PLCC

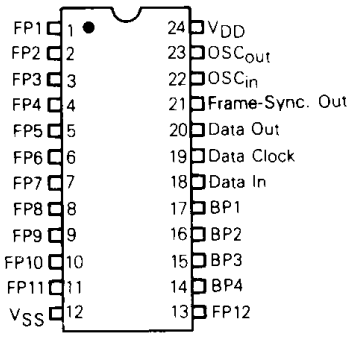
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the ranges $V_{SS} \le V_{out} \le V_{DD}$ and $V_{SS} \le V_{in} \le 15$ V.

Unused inputs must always be tied to an appropriate logic voltage level.

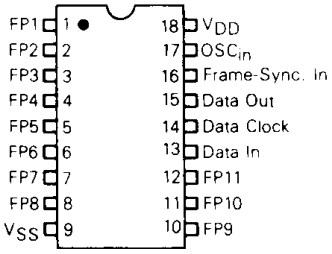
3

PIN ASSIGNMENTS

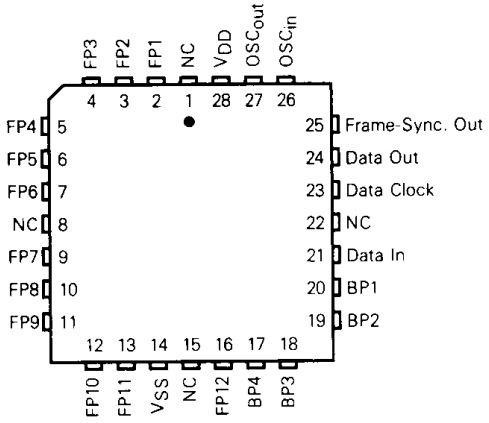
MC145000
Master



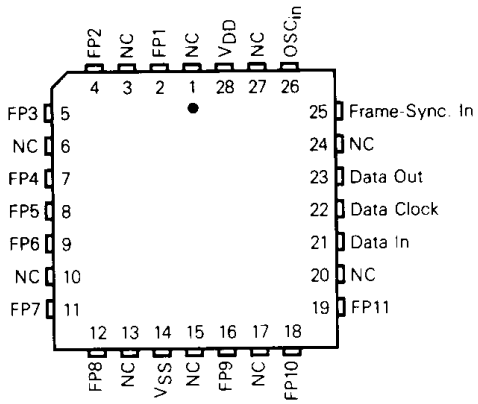
MC145001
Slave



MC145000FN



MC145001FN



Mux-by-4 LCD Manufacturers

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of LCD suppliers.

Supplier	Contact Information
Polytronix, Inc.	Phone: (214) 238-7045 FAX: (214) 644-0805
LXD, Inc.	Phone: (216) 292-3300 FAX: (216) 292-4727
UCE, Inc.	Phone: (203) 838-7500 FAX: (203) 838-2566
Hamlin, Inc.	Phone: (414) 648-1000 FAX: (414) 648-1001

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Characteristic	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +6.5	V
Input Voltage, Data In and Data Clock	V_{in}	−0.5 to 15	V
Input Voltage, OSC_{in} of Master	$V_{in\ osc}$	−0.5 to V_{DD} +0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (Voltages referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Typ#	25°C Max	85°C Min	85°C Max	Unit
RMS Voltage Across a Segment (BPi-FPj) "ON" Segment	V_{ON}	3.0	–	–	–	1.73	–	–	–	V
		6.0	–	–	–	3.46	–	–	–	
"OFF" Segment	V_{OFF}	3.0	–	–	–	1.00	–	–	–	V
		6.0	–	–	–	2.00	–	–	–	
Average DC Offset Voltage	Vdc	3.0	–	30	–	10	30	–	30	mV
		6.0	–	50	–	20	50	–	50	
Input Voltage "0" Level	V_{IL}	3.0	–	0.90	–	1.35	0.90	–	0.90	V
		6.0	–	1.80	–	2.70	1.80	–	1.80	
"1" Level	V_{IH}	3.0	2.10	–	2.10	1.65	–	2.10	–	V
		6.0	4.20	–	4.20	3.30	–	4.20	–	
Output Drive Current – Backplanes										
High-Current State*										
V_O = 2.85 V	I_{BH}	3.0	150	–	75	190	–	35	–	μA
V_O = 1.85 V			220	–	110	200	–	55	–	
V_O = 1.15 V			160	–	80	200	–	40	–	
V_O = 0.15 V			400	–	200	300	–	100	–	
V_O = 5.85 V	I_{BH}	6.0	500	–	250	300	–	125	–	μA
V_O = 3.85 V			1000	–	500	600	–	250	–	
V_O = 2.15 V			800	–	400	500	–	200	–	
V_O = 0.15 V			500	–	250	300	–	125	–	
Low-Current State*										
V_O = 2.85 V	I_{BL}	3.0	140	–	70	80	–	35	–	μA
V_O = 1.85 V			2.4	–	1.2	2.8	–	0.6	–	
V_O = 1.15 V			2.2	–	1.1	2.5	–	0.5	–	
V_O = 0.15 V			400	–	200	330	–	100	–	
V_O = 5.85 V	I_{BL}	6.0	190	–	95	105	–	45	–	μA
V_O = 3.85 V			15	–	7.5	10	–	3.7	–	
V_O = 2.15 V			13	–	6.5	9	–	3.2	–	
V_O = 0.15 V			850	–	425	570	–	210	–	
Output Drive Current – Frontplanes										
High-Current State*										
V_O = 2.85 V	I_{FH}	3.0	80	–	40	60	–	20	–	μA
V_O = 1.85 V			140	–	70	120	–	35	–	
V_O = 1.15 V			180	–	60	100	–	30	–	
V_O = 0.15 V			100	–	50	95	–	25	–	
V_O = 5.85 V	I_{FH}	6.0	140	–	70	90	–	35	–	μA
V_O = 3.85 V			360	–	180	250	–	90	–	
V_O = 2.15 V			400	–	200	240	–	100	–	
V_O = 0.15 V			100	–	50	120	–	25	–	
Low-Current State*										
V_O = 2.85 V	I_{FL}	3.0	60	–	30	40	–	15	–	μA
V_O = 1.85 V			2.8	–	1.4	2.8	–	0.7	–	
V_O = 1.15 V			2.2	–	1.1	2.5	–	0.5	–	
V_O = 0.15 V			100	–	50	100	–	25	–	
V_O = 5.85 V	I_{FL}	6.0	100	–	50	60	–	25	–	μA
V_O = 3.85 V			16	–	8.0	10	–	4.0	–	
V_O = 2.15 V			13	–	6.5	9	–	3.2	–	
V_O = 0.15 V			200	–	100	175	–	50	–	
Input Current	I_{in}	6.0	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Input Capacitance	C_{in}	-	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package) V_{in} = 0 or V_{DD}, I_{out} = 0 μA	I_{DD}	3.0	-	10	–	2.5	15	–	20	μA
		6.0	-	185	–	50	175	–	130	

*For a time ($t \cong 2.56$/osc. freq.) after the backplane or frontplane waveform changes to a new voltage level, the circuit is maintained in the high-current state to allow the load capacitances to charge quickly. Then the circuit is returned to the low-current state until the next voltage level change occurs.

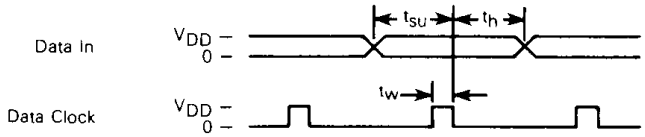
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ#	Max	Unit
Data Clock Frequency	f_{cl}	3.0 6.0	–	12.5 24	7.5 12.5	MHz
Rise and Fall Times – Data clock	t_r, t_f	3.0 6.0	– –	– –	125 10	μs
Setup Time Data In to Data Clock	t_{su}	3.0 6.0	48 16	– –	– –	ns
Hold Time Data In to Data Clock	t_h	3.0 6.0	−5 0	– –	– –	ns
Pulse Width Data Clock	t_w	3.0 6.0	65 40	– –	– –	ns

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING WAVEFORMS



DEVICE OPERATION

Figure 1 shows a block diagram of the Master unit. The unit is composed of two independent circuits: the data input circuit with its associated data clock, and the LCD drive circuit with its associated system clock.

Forty-eight bits of data are serially clocked into the shift register on the falling edges of the external data clock. Data in the shift register is latched into the 48-bit latch at the beginning of each frame period. (As shown in Figure 3, the frame period, t_{frame}, is the time during which all the LCD segments are set to the desired "ON" or "OFF" states.)

The binary data present in the latch determines the appropriate waveform signal to be generated by the frontplane drive circuits, whereas the backplane waveforms are invariant. The frontplane and backplane waveforms, FPn and BPn, are generated using the system clock (which is the oscillator divided by 256) and voltages from the V/3 generator circuit (which divides V_{DD} into one-third increments). As shown in Figure 3, the frontplane and backplane waveforms and the "ON" and "OFF" segment waveforms have periods equal to t_{frame} and frequencies equal to the system clock divided by four.

Twelve frontplane and four backplane drivers are available from the Master unit. The latching of the data at the beginning of each frame period and the carefully balanced voltage-generation circuitry minimize the generation of a net dc component across any LCD segment.

The Slave unit (Figure 2) consists of the same circuitry as the Master unit, with two exceptions: it has no backplane drive circuitry, and its shift register and latch hold 44 bits. Eleven frontplane and no backplane drivers are available from the Slave unit.

LCD DRIVER SYSTEM CONFIGURATIONS

Figure 4 shows a basic LCD Driver system configuration, with one Master and several Slave units. The maximum number of slave units in a system is dictated by the maximum backplane drive capability of the device and by the system data update rate. Data is serially shifted first into the Master unit and then into the following Slave units on the falling edge of the common data clock. The oscillator is common to the Master unit and each of the Slave units. At the beginning of each frame period, t_{frame}, the Master unit generates a frame-sync pulse (Figure 3) which is received by the Slave units. The pulse is to ensure that all Slave unit frontplane drive circuits are synchronized to the Master unit's backplane drive circuits.

A single multiplexed-by-four, 7-segment (plus decimal point) LCD and possible frontplane and backplane connections are shown in Figure 5. When several such displays are used in a system, the four backplanes generated by the Master unit are common to all the LCD digits in the system. The twelve frontplanes of the Master unit are capable of controlling forty-eight LCD segments (6 LCD digits), and the eleven frontplanes of each Slave unit are capable of controlling forty-four LCD segments (5½ LCD digits).

FIGURE 1 – BLOCK DIAGRAM OF THE MC145000 (MASTER) LCD DRIVER

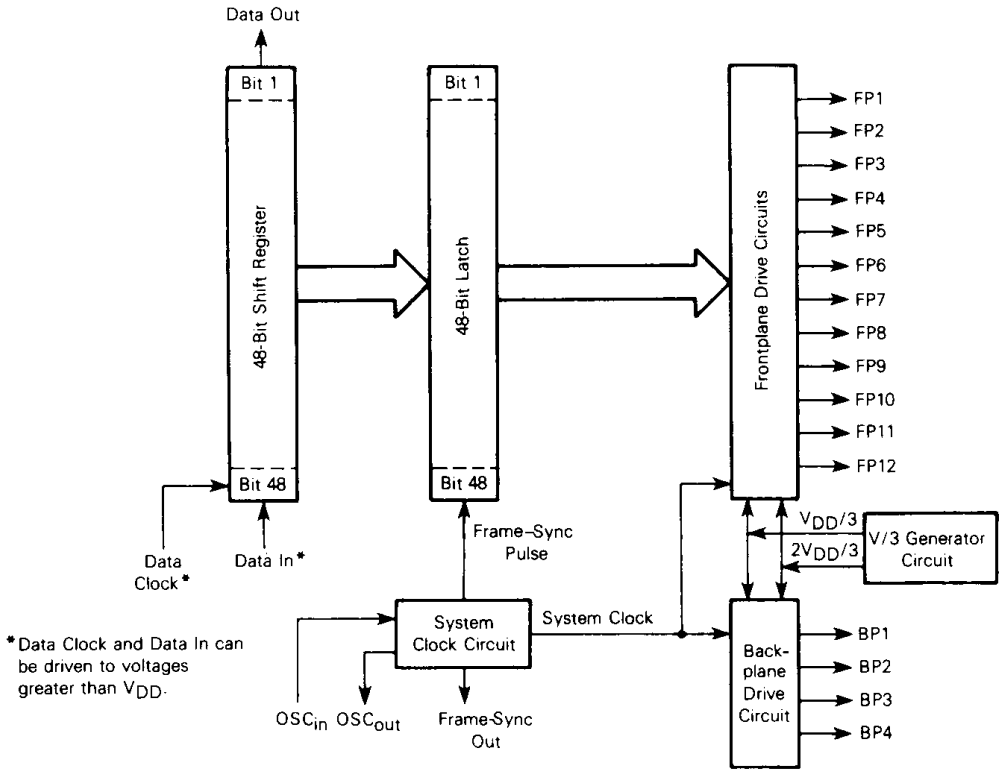


FIGURE 2 – BLOCK DIAGRAM OF THE MC145001 (SLAVE) LCD DRIVER

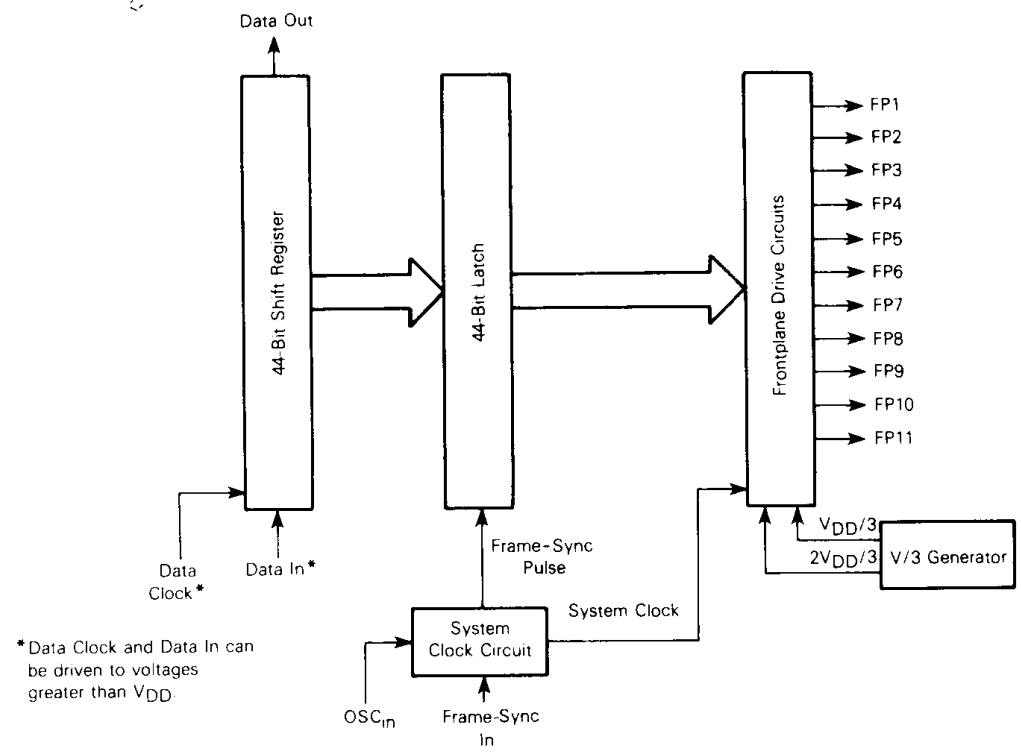


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FIGURE 3 — VOLTAGE WAVEFORMS

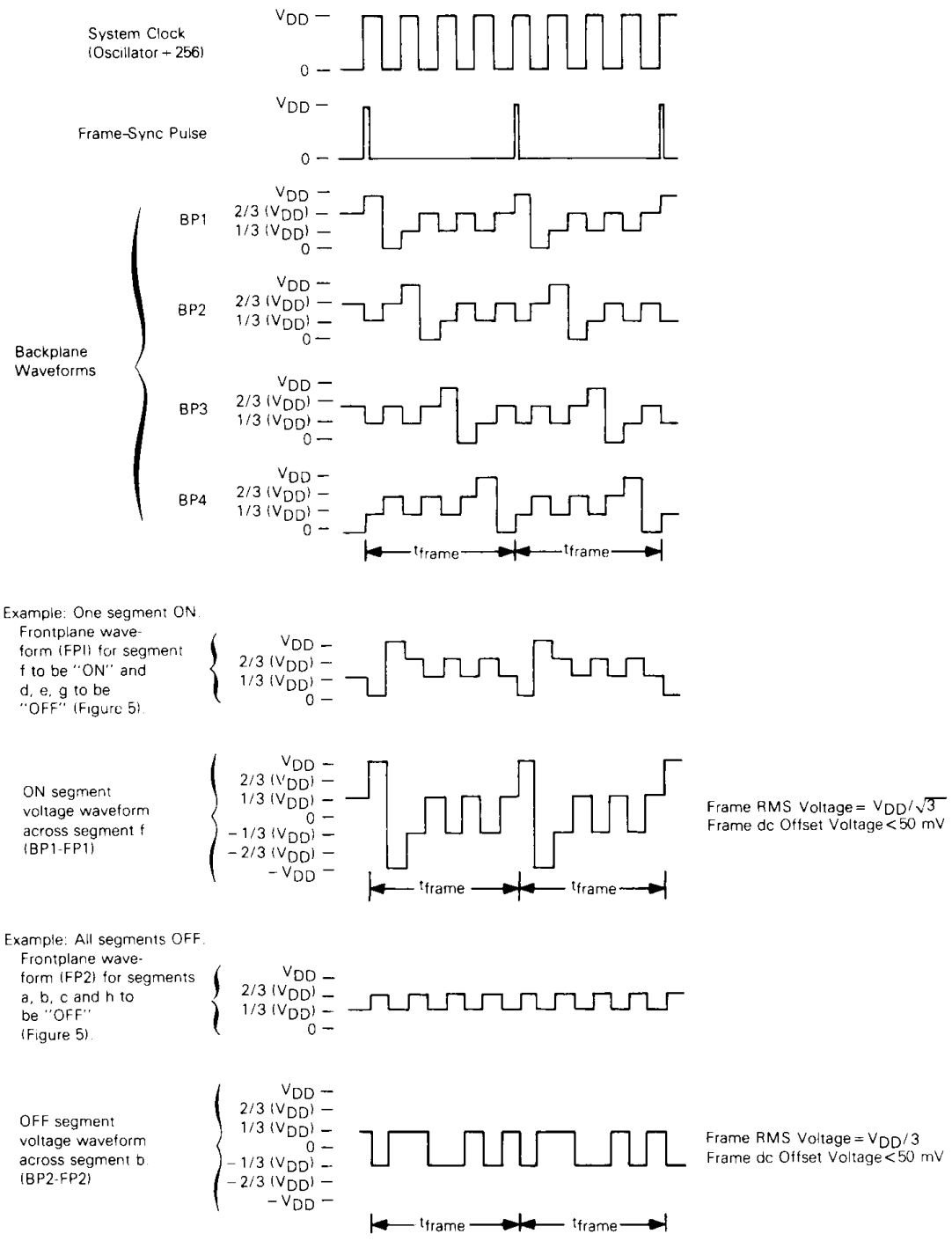


FIGURE 4 — BASIC SYSTEM CONFIGURATION

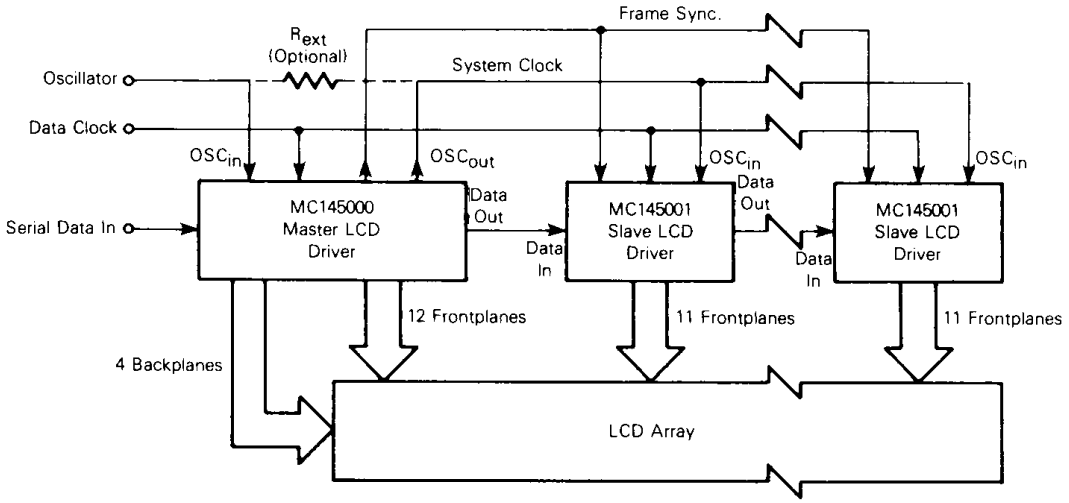
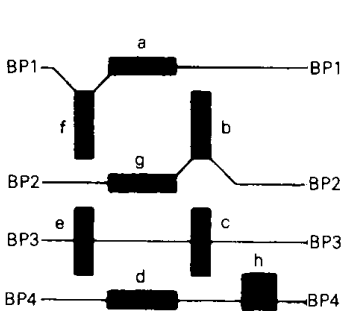
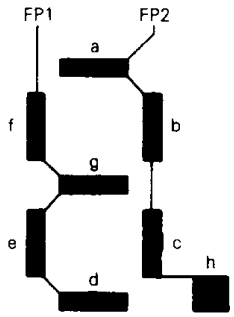


FIGURE 5 — FRONTPLANE AND BACKPLANE CONNECTIONS TO A MULTIPLEXED-BY-FOUR 7-SEGMENT (PLUS DECIMAL POINT) LCD



Typical Backplane Configuration



Typical Frontplane Configuration

SEGMENT TRUTH TABLE*

	FP1	FP2
BP1	f	a
BP2	g	b
BP3	e	c
BP4	d	h

*Because there is no standard for backplane and frontplane connections on multiplexed displays, this truth table may be used only for this example.

PIN DESCRIPTIONS

FRONTPLANE DRIVE OUTPUTS
(Master: FP1-FP12)
(Slave: FP1-FP11)

The frontplane drive waveforms for the LCDs.

BACKPLANE DRIVE OUTPUTS
(Master: BP1-BP4)

The backplane drive waveforms for the LCDs.

DATA IN (Master and Slave)

The serial data input pin. Data is clocked into the shift register on the falling edge of the data clock. A high logic level will cause the corresponding LCD segment to be turned on, and a low logic level will cause the segment to be turned off. This pin can be driven to 15 volts regardless of the value of V_{DD}, thus permitting optimum display drive voltage.

DATA CLOCK (Master and Slave)

The input pin for the external data clock, which controls the shift registers. This pin can be driven to 15 volts regardless of the value of V_{DD}.

DATA OUT (Master and Slave)

The serial data output pin.

FRAME-SYNC OUT (Master)

The output pin for the frame-sync pulse, which is generated by the Master unit at the beginning of each frame period, t_{frame}. From Figure 1, the 48-bit latch is loaded during the positive Frame-Sync Out pulse. Therefore, if the Data Clock is active during this load interval, the display will flicker.

FRAME-SYNC IN (Slave)

The input pin for the frame-sync pulse from the Master unit. The frame-sync pulse synchronizes the Slave frontplane drive waveforms to the Master backplane drive waveforms.

OSC_{in} (Master and Slave)

The input pin to the system clock circuit. The oscillator frequency is either obtained from an external oscillator or generated in the Master unit by connecting an external resistor between the OSC_{in} pin and the OSC_{out} pin. Figure 6 shows the relationship between resistor value and frequency.

OSC_{out} (Master)

The output pin of the system clock circuit. This pin is connected to the OSC_{in} input of each Slave unit.

V_{DD} (Master and Slave)

The positive supply voltage.

V_{SS} (Master and Slave)

The negative supply (or ground) voltage.

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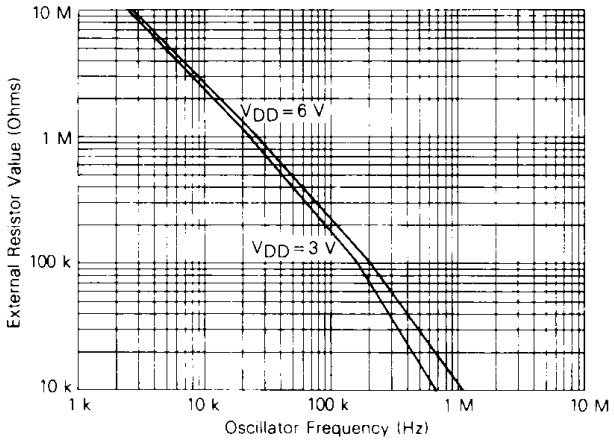
FIGURE 6 – TYPICAL OSCILLATOR FREQUENCY vs EXTERNAL RESISTOR VALUE



APPLICATIONS

The following examples are presented to give the user further insight into the operation and organization of the Master and Slave LCD Drivers.

An LCD segment is turned either on or off depending upon the RMS value of the voltage across it. This voltage is equal to the backplane voltage waveform minus the frontplane voltage waveform. As previously stated, the backplane waveforms are invariant (see Figure 3). Figure 10 shows one period of every possible frontplane waveform.

For a detailed explanation of the operation of liquid crystal materials and multiplexed displays, refer to a brochure entitled "Multiplexed Liquid Crystal Displays," by Gregory A. Zaker, General Electric Company, Liquid XTAL Displays Operation, 24500 Highpoint Road, Cleveland, Ohio 44122.

Example 1: Many applications (e.g., meters, gasoline pumps, pinball machines, and automobile dashboard displays) require that, for each display update, an entirely new set of data must be shifted into the Master and cascaded Slave units. The correspondence between the frontplane-backplane intersections at the LCD segments and the data bit locations in the 48-bit latch of the Master (or 44-bit latch of the Slave) is necessary information to the system designer. In Figure 1, it is shown that data is serially shifted first into the 48th-bit location of the shift register of the Master. Thus, after 48 data bits have been shifted in, the first bit to be entered has been shifted into bit-location one, the second bit into bit-location two, and so on. Table 1 shows the bit location in the latch that controls the corresponding frontplane-backplane intersection. For example, the information stored in the 26th-bit location of the latch controls the LCD segment at the intersection of FP7 and BP3. The voltage waveform across that segment is equal to (BP3 minus FP7). The same table, but with the column for FP12 deleted, describes the operation of the Slave unit.

In applications of this type, all the necessary data to completely update the display are serially shifted into the Master and succeeding Slave units within a frame period. Typically, a microprocessor is used to accomplish this.

Example 2: Many keyboard-entry applications, such as calculators, require that the most significant digit be entered and displayed first. Then as each succeeding digit is entered, the previously entered digits must shift to the left. It is, therefore, neither necessary nor desirable to enter a completely new set of data for each display change. Figure 7 shows a representation of a system consisting of one Master and three Slave units and displaying 20 LCD digits. If each digit has the frontplane-backplane configuration shown in Figure 5, the relationship between frontplanes, backplanes, and LCD segments in the display is shown in Table 2.

Digits (or alphanumeric characters) are entered, most-significant digit first, by using a keyboard and a decoder external to the MC145000. Data is entered into the Master and cascaded Slave units according to the following format:

1) Initially, all registers and latches must be cleared by entering 160 zero data bits. This turns off all 160 segments of the display.

2) Entering the most-significant digit from the keyboard causes the appropriate eight bits to be serially shifted into the Master unit. These eight bits control LCD segments a through h of digit 1, and cause the desired digit to be displayed in the least-significant digit location.

3) Entering the second-most-significant digit from the keyboard causes eight more bits to be serially shifted into the Master unit. These eight bits now control LCD segments a through h of digit 1, and the previously entered eight bits now control segments a through h of digit 2. Thus the two digits are displayed in the proper locations.

4) Entering the remaining 18 digits from the keyboard fills the 20-digit display. Entering an extra digit will cause the first digit entered to be shifted off the display.

Example 3: In addition to controlling 7-segment (plus decimal point) digital displays, the MC145000 and MC145001 may be used to control displays using 5 × 7 dot matrices. A Master and three Slave units can drive 180 LCD segments, and therefore are capable of controlling five 5 × 7 dot matrices (175 segments). Two control schemes are presented in Figures 8 and 9; one using a single Master unit, and one using two Master units.

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TABLE 1 — THE BIT LOCATIONS, IN THE LATCH, THAT CONTROL THE LCD SEGMENTS LOCATED AT EACH FRONTPLANE-BACKPLANE INTERSECTION

BACKPLANES	FRONTPLANES											
	FP1	FP2	FP3	FP4	FP5	FP6	FP7	FP8	FP9	FP10	FP11	FP12
BP1	4	8	12	16	20	24	28	32	36	40	44	48
BP2	3	7	11	15	19	23	27	31	35	39	43	47
BP3	2	6	10	14	18	22	26	30	34	38	42	46
BP4	1	5	9	13	17	21	25	29	33	37	41	45

FIGURE 7 — A 20-DIGIT DISPLAY (EQUIVALENT TO A 4 × 40 ARRAY)

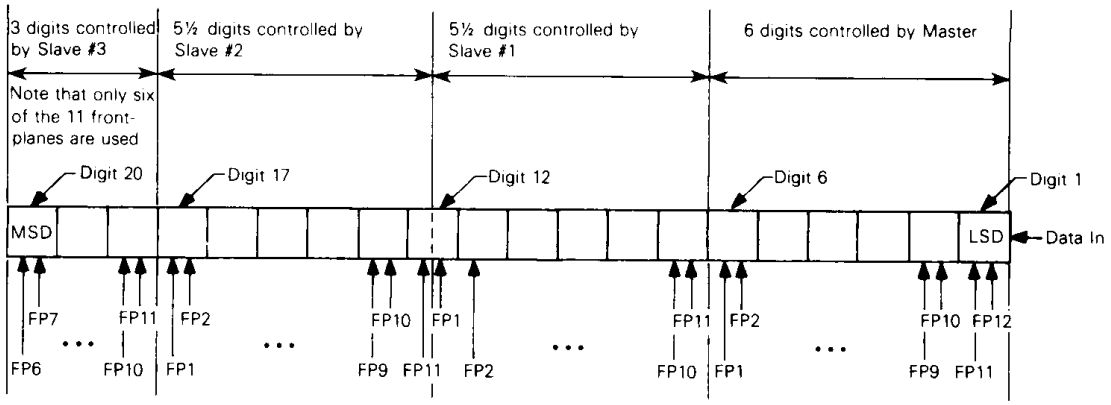

TABLE 2 — THE RELATIONSHIP BETWEEN FRONTPLANE-BACKPLANE INTERSECTIONS AND LCD SEGMENTS FOR THE SYSTEM CONFIGURATION OF FIGURE 7

	Master							Slave #1				Slave #2						Slave #3				
	FP12	FP11	FP10	FP9	• • •	FP2	FP1	FP11	FP10	• • •	FP1	FP11	FP10	FP9	• • •	FP2	FP1	FP11	FP10	• • •	FP7	FP6
BP1	a1	f1	a2	f2		a6	f6	a7	f7		a12	f12	a13	f13		a17	f17	a18	f18		a20	f20
BP2	b1	g1	b2	g2		b6	g6	b7	g7		b12	g12	b13	g13		b17	g17	b18	g18		b20	g20
BP3	c1	e1	c2	e2		c6	e6	c7	e7		c12	e12	c13	e13		c17	e17	c18	e18		c20	e20
BP4	h1	d1	h2	d2		h6	d6	h7	d7		h12	d12	h13	d13		h17	d17	h18	d18		h20	d20
	digit 1		digit 2		• • •	digit 6		digit 7		• • •	digit 12	digit 13			• • •	digit 17		digit 18		• • •	digit 20	

FIGURE 8 — EXAMPLE OF A 5 × 7 DOT MATRIX DISPLAY SYSTEM CONTROLLED BY ONE MASTER AND THREE SLAVE UNITS

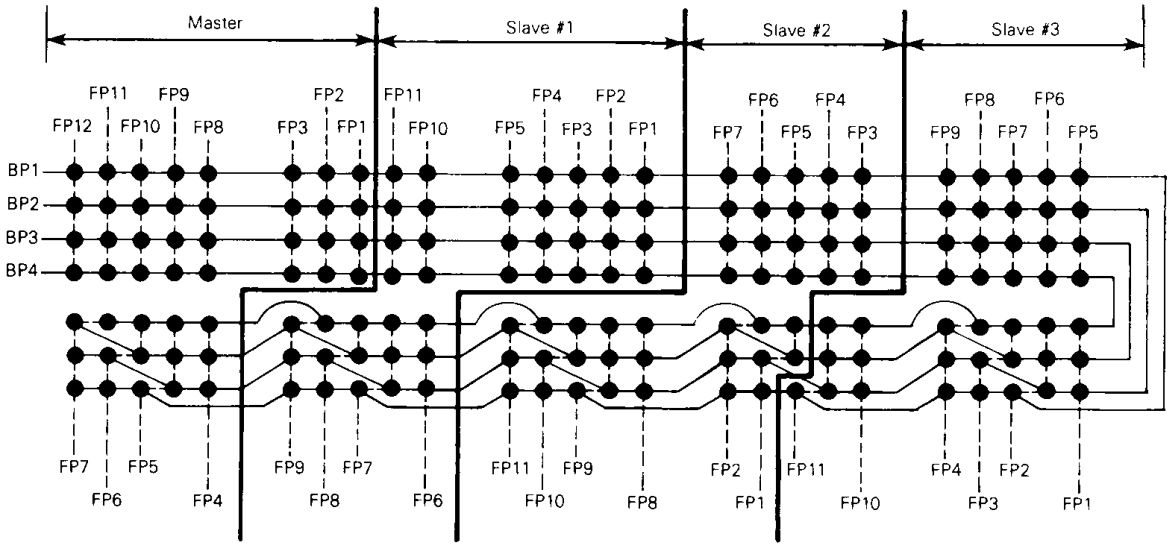

FIGURE 9 — EXAMPLE OF A 5 × 7 DOT MATRIX DISPLAY SYSTEM CONTROLLED BY TWO MASTER AND TWO SLAVE UNITS

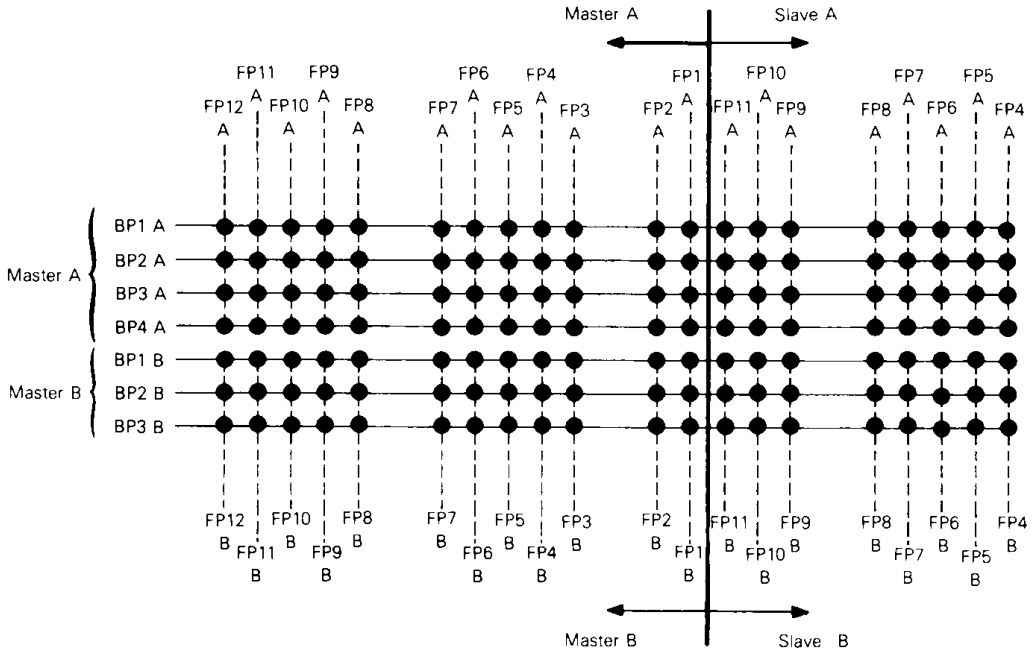

FIGURE 10 — POSSIBLE FRONTPLANE WAVEFORMS