SL11RIDE™
USB to IDE/ATAPI Solution
Data Sheet

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1.0 Conventions

1,2,3,4	Numbers without annotation are decimal
Dh, 1Fh, 39h	Hexadecimal numbers are followed by an “h”
0101b, 010101b	Binary numbers are followed by a “b”
bRequest, n	Words in *italics* indicated terms defined by USB Specification or by this Specification

2.0 Definitions

I2C	Two-wire Serial flash EEPROM interface
SL11RIDE	The SL11R-IDE is 16-bit RISC USB processor, which provides USB to ATAPI/IDE interface on a single chip
USB	**U**niversal **S**erial **B**us
QTOOLS	Utilities tools for ScanLogic 16-bit RISC USB processor
CF	Compact Flash

3.0 References

[ref 1] AT Attachment with Packet Interface Extension (ATA/ATAPI-5)

4.0 General Description

4.1 Overview

The SL11RIDE is a low-cost, high-speed Universal Serial Bus RISC-based Controller board. It contains a 16-bit RISC processor with built-in SL11RIDE ROM to greatly reduce firmware development efforts. Its serial flash EEPROM interface offers low-cost storage for USB device configuration and customer product specific functions. New functions can be programmed into the I^2C by downloading them from a USB Host PC. This unique architecture provides the ability to upgrade products, in the field, without changing the peripheral hardware.

4.2 Features of SL11RIDE

- Two-wire serial EEPROM (I2C) interface port, with SL11RIDE ROM firmware support, to allow on board flash EEPROM programming
- Supports 12-MHz/48-MHz external crystal or clock
- 6Kx8 internal Mask ROM with built-in BIOS
- Supports up to the maximum USB transfer rate of 12 Mbits/sec
- Power source requires only 3.3V, and it can be powered via a USB host PC or a Hub
- Resume, Suspend, and Low-power modes are available
- Includes the necessary firmware to function as a USB to IDE/ATAPI controller

4.3 Applications

Cypress offers a Developer’s Kit with all its product lines. These Developer’s Kits include: ATAPI/IDE firmware, multiple peripheral Mini-port class drivers for Windows98/2000, MAC 8.6 or higher available object code, a complete ATAPI/IDE solution reference design, and a demo board.

The SL11RIDE offers solutions for interfacing USB to IDE/ATAPI peripheral products including HDD, CD-ROM, CD-R/RW, ZIP drives, LS120, MO drives, Compact Flash, Disk on Chip, Tape drives, Smart Media cards, ORB, and CLIK, and MicroDrives.

4.4 Low Power Consumption

The SL11RIDE offers various power consumption modes. The maximum power consumption at 48-MHz operation, including USB, is less then 30 mA, but on the average it consumes around 10 mA.

The following are measurements taken under different setups of the SL11RIDE:

Idle Mode:	2.0 mA (USB is on, CPU runs at 48 MHz)
During Reset:	3.0 mA (Reset is held LOW)
Post Reset:	12.5 mA typical at 48 MHz

Max at 4 MHz CPU speed: 4.0 mA (USB is on)

Max at 32 MHz CPU speed: 25.0 mA (USB is on)

Max at 48 MHz CPU speed: 30.0 mA (USB is on)

4.5 Functions for Suspend, Resume, and Low-Power modes

The SL11RIDE's CPU supports suspend, resume, and CPU low power mode. The SL11RIDE BIOS assigns USBPU for the USB DATA+ line pull-up, which simulates USB cable removal or insertion while USB power is still applied to the board.

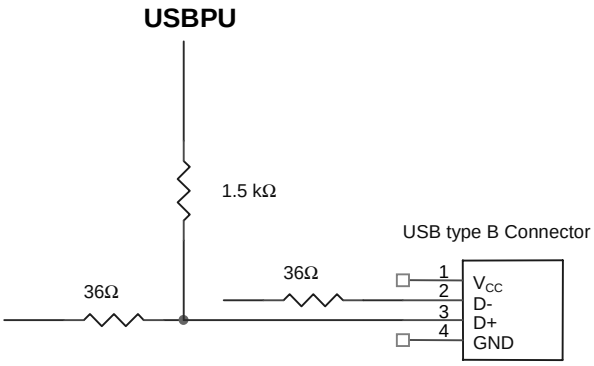


Figure 4-1. USBPU Pull-up Connection Example

4.6 PLL Clock Generator

A 48-MHz external crystal can be used with the SL11RIDE. Two pins, X1 and X2, are provided to connect a low-cost crystal circuit to the device. Circuitry is provided to generate the internal clock requirements of the device. If an external 48-MHz clock is available in the application, it may be used instead of the crystal circuit by connecting directly to the X1 input pin.

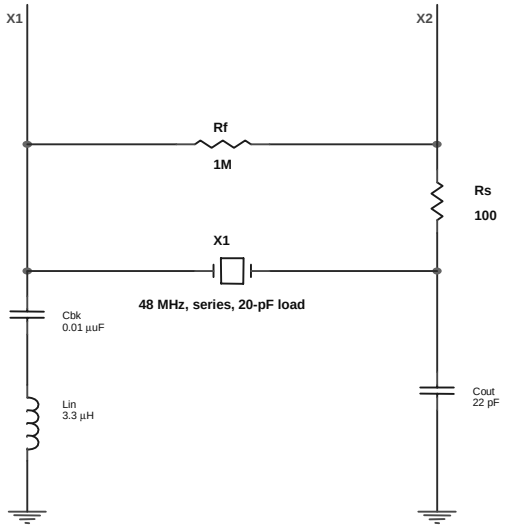


Figure 4-2. Full-Speed 48-MHz Crystal Circuit

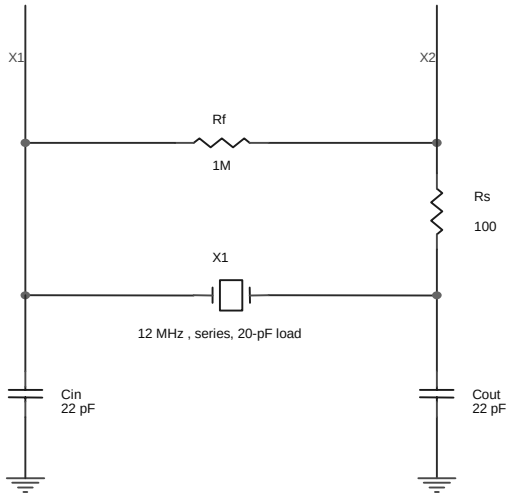


Figure 4-3. 12-MHz Crystal Circuits

Note: You need to set bit C2 =1 from configuration address (0xC006). See section 10.8 for CPU speed control.

4.7 Serial I²C Interface

The SL11RIDE provides an interface to an external serial flash EEPROM. A variety of serial EEPROM formats can be supported. Currently the SL11RIDE firmware supports the two-wire serial flash EEPROM type. It can be used for field product upgrades if needed.

The recommended serial EEPROM device is a two-wire Serial CMOS EEPROM (AT24LCXX Device Family). Currently, the SL11RIDE allows writing to EEPROM, up to 2 KBytes, using a 16-Kbit I²C device (i.e. AT24LC16B/SN).

The USB vendor/device configuration can be programmed and stored into the external EEPROM device. On power-up, the contents of the EEPROM will be downloaded into RAM. The advantage of the EEPROM interface is both cost and space saving compared with using an external 8-bit PROM/EPROM.

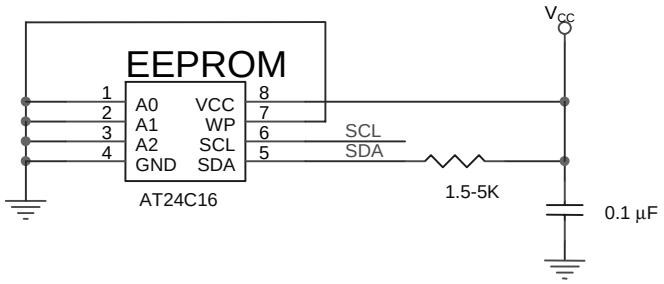


Figure 4-4. I²C 2-Kbyte Connection

Note: You can choose either a 3.3V or a 5.0V EEPROM.

5.0 Software

The SL11RIDE software is *USB Specification* and *USB Mass Storage Class Bulk-Only Transport* version 1.0 compliant in the final release. In the meantime, it will try to track changes to the *USB Mass Storage Class Bulk-Only Transport* as closely as possible. The interface to the host PC is USB, which allows true Plug-and-Play (PnP). The requirement for Operating System (OS) on the host PC side is Win98/2000 or MAC.

5.1 Overview

This document provides a complete outline description of the SL11RIDE firmware and host mini-port driver under Win98/2000, which supports *Bulk Only Transport* between host PC and SL11RIDE. See *Figure 5-1* for details.

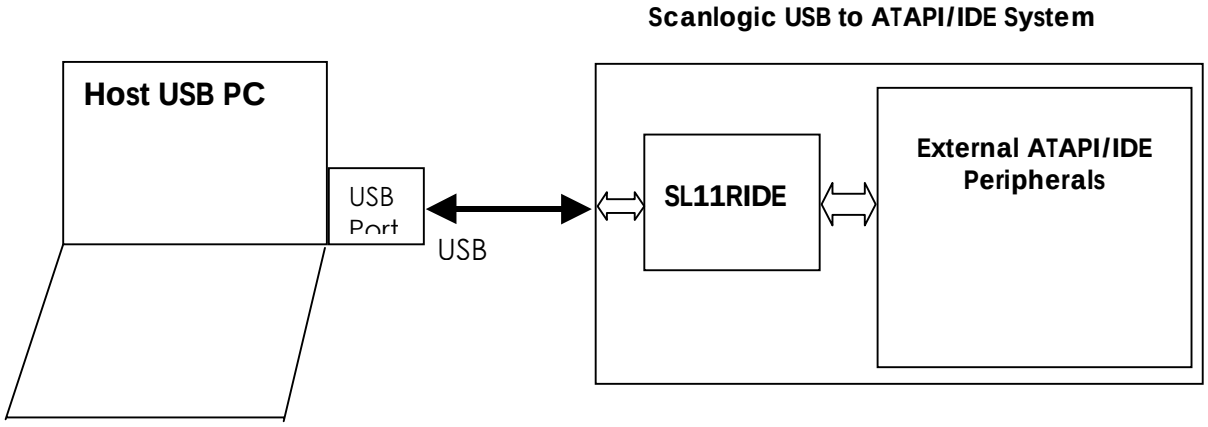


Figure 5-1. General Views

5.2 ATAPI/IDE Firmware

SL11RIDE's firmware supports both ATAPI and IDE devices. The firmware is *USB Mass Storage Class* compliant, which supports multiple Operating Systems such as Windows®98/2000 and Mac.

5.3 Windows® Host Drivers

The WDM and MPD device drivers operate under Windows 98. Win2000 doesn't need any special drivers. See *Table 5-1* for more detail.

Table 5-1. Windows Host Software OS Compatibility

Operation System	USB	Note
Windows98	÷	First Edition from Microsoft
Windows98SE	√	Second Edition from Microsoft
Window2000	÷	WIN2000 beta from Microsoft
Windows NT	--	NT 4.0 does not support USB

5.4 Mac Host Drivers

Cypress does not support end-user firmware updates under the Mac OS. OEM customers must download firmware from MS-DOS.

Table 5-2. Mac Host Software OS Compatibility

Operating System	USB	Note
G3: OS8.6, OS9	÷	G3
iMAC: OS8.6, OS9	--	iMAC
Laptop: OS8.6, OS9	--	G3 Laptop

5.5 Multi Port Driver Support

Currently SL11RIDE mini-port driver is a multi-device driver for ATAPI/IDE peripherals. This driver supports up to 7 ATAPI/IDE devices, which connect via a USB Hub. See *Figure 5-2* for details.

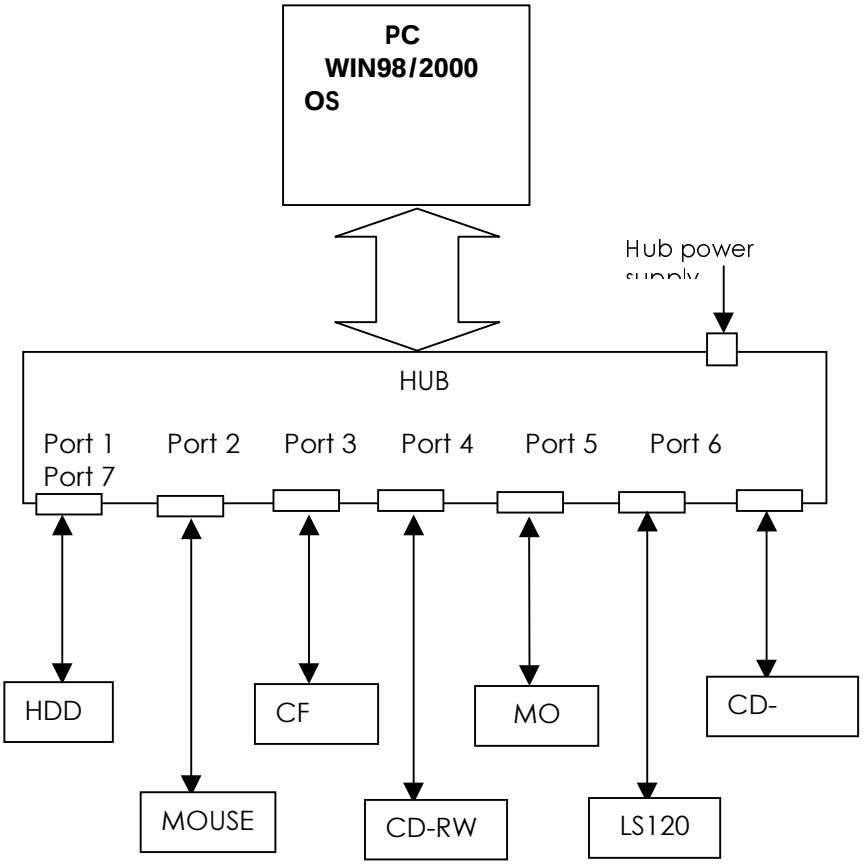


Figure 5-2. Multi-portable Drivers

Note:

- These devices must be self-powered since the Hub cannot provide enough current to each ATAPI/IDE device.
- We recommend that a PC for this configuration be at least a 300-MHz Pentium® II with 64 Mbyte RAM

6.0 Firmware Download

6.1 How to Update the SL11RIDE Firmware

The firmware on the EEPROM doesn't have to be changed after it is downloaded for the first time. If it needs to be changed during testing or for future firmware updates, this can be done from a PC using the USB port. The need to change firmware to switch between an ATAPI device and an IDE device will be removed in a future release.

6.2 The QTUI2C Program

6.2.1 Overview

The QTUI2C program is used to program the I^2C EEPROM that is externally connected to the SL11RIDE chip. This allows programming the I^2C with data alone, such as the USB data descriptors. The SL11RIDE will scan the I^2C for a valid signature before attempting to load the code and/or data to the internal/external RAM.

To program the file, the input filename without the extension is required. The QTUI2C will create a file "MAKEENH.BIN" based on the Object input file. This "MAKEENH.BIN" file will contain the fix-up (.bin) information and it will have a proper format that is defined on the SL11RIDE BIOS specification.

6.2.2 Usage

QTUI2C <filename | filename.bin>

Where:

<Filename> is the output file without extension.

<filename.bin> is the output file with (.**bin**) extension.

Note:

This program is only used when the I^2C is connected to the SL11RIDE chip.

Under Windows, if the EEPROM already has a version of the SL11RIDE firmware programmed, it will be necessary to remove the Bulk-Only hard disk controller from the Device Manager before this program can be used.

After this program completes, at any subsequent boot up, the SL11RIDE firmware will automatically scan the I^2C and load the code from the I^2C into internal/external RAM. However, if the I^2C was corrupted, it sometimes causes an unexpected error on USB communication ports.

6.2.3 How to use QTUI2C.EXE

The QTOOLS utilities are in directory C:\Program Files\ScanLogic\USB2IDE\bin.

- qtui2c zero.bin ; You need to erase all program from I^2C each time you download a new program.
- qtui2c cidexxx.bin ; Program ATAPI and IDE firmware into I^2C

7.0 Mass Production Download EEPROM (I^2C)

7.1 ToHex

7.1.1 Overview

This program converts the Binary output file (. **bin**) to the INTEL HEX format. This INTEL HEX format will be used for programming the PROM on the DATAIO.

7.1.2 Usage

TOHEX <infilespec.bin> <outfilespec [HEX]> [offset, default=0x0000] [h|l]

Where:

Infilespec.bin	is the Binary output file produced by the QTASM
Outfilespec.hex	is the INTEL HEX output file produced by the TOHEX program
Offset	is valid from 0x0000 to 0xFFFF. Default is 0x0000.
[h|l]	'h' is selected HIGH PROM output file. 'l' is selected LOW PROM output file. Without this input the default INTEL HEX output file will be stored into the single 8-bit PROM.

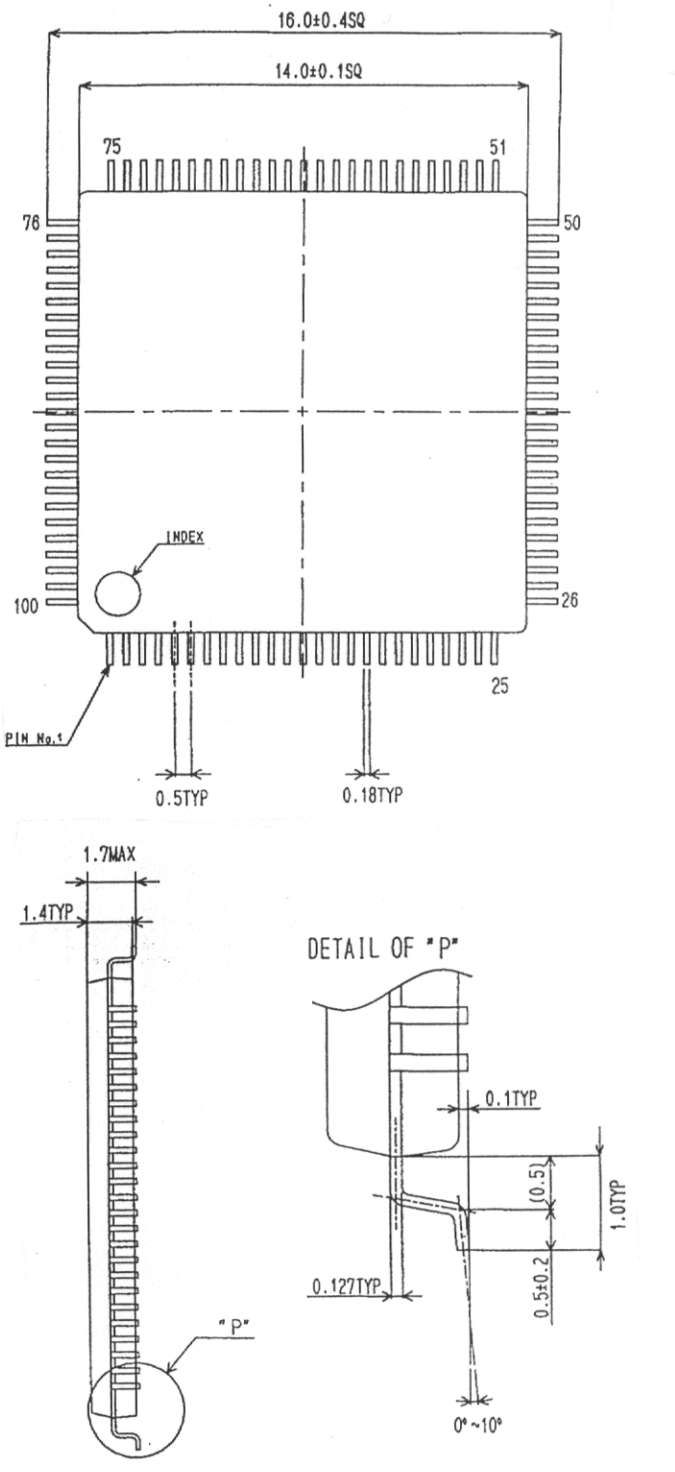
7.1.3 Example

TOHEX cidexxx.bin cidexxx.hex

; Create INTEL HEX format for ATAPI device

8.0 Physical Connection

8.1 SL11RIDE Chip Dimension



The SL11RIDE's Package type is 100 PQFP.

8.2 SL11RIDE Pin Assignment and Description

Pin Assignment and Description

Pin Name	GPIO name	Pin No.	Pin Type	SL11RIDE Pin Description
V_{DD}		1	Power	+3.3 VDC supply[1]
GND		14	GND	Digital ground
X1		15	Input	External 48-MHz Crystal or Clock input[2]
X2		16	Output	External crystal output. Not connect if X1 is used for clock input
V_{DD}		17	Power	+3.3 VDC supply[1]
GND		40	GND	Digital ground
TEST		44	Input	NC—No Connection, MFG test only[3]
nRESET		48	Input	Master Reset. SL11RIDE Device active LOW reset input
VDD		50	Power	+3.3 VDC supply[1]
VDD		51	Power	+3.3 VDC supply[1]
SCL	GPIO31	60	Bidir	Serial Flash EEPROM clock
SDA	GPIO30	61	Bidir	Serial Flash EPROM data[4]
USBPU	GPIO29	62	Bidir	USB turn on/off D+ pull-up resistor
TXD	GPIO28	63	Output	UART TXD
GND		64	GND	Digital ground
GND		65	GND	Digital ground
RXD	GPIO27	66	Input	UART RXD
PWC	GPIO26	67	Bidir	Power control[5]
INTRQ/ HW_RESET/ RB	GPIO25	68	Bidir	Interrupt triggers in the SL11RIDE processor, or define for Hardware Reset for CF[6]
DASP/ WP	GPIO24	69	Bidir	Device Active Present, or define for Write Protect for Smart Media[6]
IOWD	GPIO23	70	Bidir	IOWD—Write uses to indicate IDE write data transfer
CS0	GPIO22	71	Bidir	Chip Select 0
CS1	GPIO21	72	Bidir	Chip Select 1 or user defines Smart media card detect
IORD	GPIO20	73	Bidir	IORD uses to indicate IDE read data transfer
C_DET	GPIO19	74	Bidir	C_DET uses to detect CF
VDD	75	75	Power	+3.3 VDC Supply[1]
A2	GPIO18	76	Bidir	Address bit 2
A1	GPIO17	77	Bidir	Address bit 1
A0	GPIO16	78	Bidir	Address bit 0
GND	79	79	GND	Digital ground.
D15	GPIO15	80	Bidir	DATA port bit 15
D14	GPIO14	81	Bidir	DATA port bit 14
D13	GPIO13	82	Bidir	DATA port bit 13
D12	GPIO12	83	Bidir	DATA port bit 12
D 11	GPIO11	84	Bidir	DATA port bit 11

Pin Assignment and Description (continued)

Pin Name	GPIO name	Pin No.	Pin Type	SL11RIDE Pin Description
D10	GPIO10	85	Bidir	DATA port bit 10
D9	GPIO9	86	Bidir	DATA port bit 9
VDD1	87	87	Power	USB +3.3 VDC Supply[1]
DATA+	88	88	Bidir	USB Differential DATA Signal High Side.
DATA-	89	89	Bidir	USB Differential DATA Signal Low Side.
USB_GND	90	90	GND	USB Digital Ground.
D8	GPIO8	91	Bidir	DATA port bit 8
D7	GPIO7	92	Bidir	DATA port bit 7
D6	GPIO6	93	Bidir	DATA port bit 6
D5	GPIO5	94	Bidir	DATA port bit 5
D4	GPIO4	95	Bidir	DATA port bit 4
D3	GPIO3	96	Bidir	DATA port bit 3
D2	GPIO2	97	Bidir	DATA port bit 2
D1	GPIO1	98	Bidir	DATA port bit 1
D0	GPIO0	99	Bidir	DATA port bit 0
VDD	100	100	Power	+3.3 VDC Supply[1]

Notes:

1. All +3.3VDC must use a 0.1-µF bypass capacitor and these capacitors must be placed near the SL11RIDE chip.
2. 48-MHz Crystal or oscillator has to use a capacitor 0.1 µF to filter output signals. It must be placed at least ¾" from 3.3V, 5.0V or a USB connector
3. All pins not shown (NC pins and reserved pins) should not be connected or used for other purposes.
4. This signal requires a 1- to 5-kΩ pull-up.
5. GPIO26: This signal can be used for device low power mode. It will turn off or disable external powers to the peripheral in suspend mode. Once USB power is resumed, external power can be enabled again
6. GPIO25 can be used as INTRQ/HW_RESET/RB and GPIO24 can be used as DASP/WP signals. These signals are used for CF and Smart Media to exchange media cards or insert/remove media while power is still supplied to the board.

8.2.1 0SL11RIDE 40 Pin Interface Signals

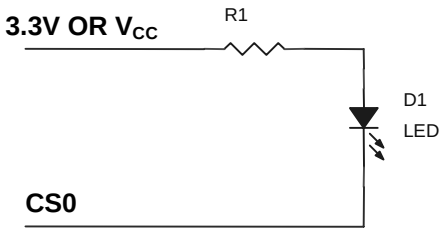
Table 8-1. 40-pin Connector Interface Signals

SL11RIDE Signal	IDE Signal	Pin	Pin	IDE Signal	SL11RIDE Signal
RESET	RESET	1	2	GND	GND
D7	DD7	3	4	DD8	D8
D6	DD6	5	6	DD9	D9
D5	DD5	7	8	DD10	D10
D4	DD4	9	10	DD11	D11
D3	DD3	11	12	DD12	D12
D2	DD2	13	14	DD13	D13
D1	DD1	15	16	DD14	D14
D0	DD0	17	18	DD15	D15
GND	GND	19	20	Key	(See Note 8)
PU[7]	DMARQ	21	22	GND	GND
IOWD	DIOW	23	24	GND	GND
IORD	DIOR	25	26	GND	GND
PU[7]	IORDY	27	28	CSEL	PD[9]
PU[7]	DMACK	29	30	GND	GND
INTRQ	INTRQ	31	32	IOCS16	PU
A1	DA1	33	34	PDIAG	PU
A0	DA0	35	36	DA2	A2
CS0	CS0	37	38	CS1	CS1
DASP	DASP	39	40	GND	GND

Notes:
7. PU: These signals need 10 kΩ pull-up.
8. The Key pin must be not be connected.
9. PD: CSEL connects to GND for default Master and Slave modes.

8.2.2 Access LED Control

The CS0 uses LED access control. You can define the value of R1.



8.3 Package Markings

YYWW = Date code

XXXX = Product code

9.0 Electrical Specification

9.1 Absolute Maximum Ratings

This section lists the absolute maximum ratings of the SL11RIDE. Stresses above those listed can cause permanent damage to the device. Exposure to maximum rated conditions for extended periods can affect device operation and reliability.

Storage Temperature	–40°C to 125°C
Power Supply Voltage (V_{DD})	3.3V±10%
Power Supply Voltage (V_{DD1})	3.3V±10%

9.2 Recommended Operating Conditions

Parameter	Min.	Typical	Max
Power Supply Voltage, V_{DD}	3.0V	3.3V	3.6V
Power Supply Voltage, V_{DD1}	3.0V		3.6V
Operating Temperature	0°C		65°C

9.3 Crystal Requirements (XTAL1, XTAL2)

Crystal Requirements, (XTAL1, XTAL2)	Min.	Typical	Max.
Operating Temperature Range	0°C		65°C
Series Resonant Frequency		48 MHz	
Frequency Drift over Temperature			±20 ppm
Temperature Stability			±100 ppm
Accuracy of Adjustment			±30 ppm
Mode of Vibration 3rd Overtone			
Series Resistance			100Ω
Load Capacitance			20 pF
Shunt Capacitance	3 pF		7 pF
Driver Level	20 µW		5 mW

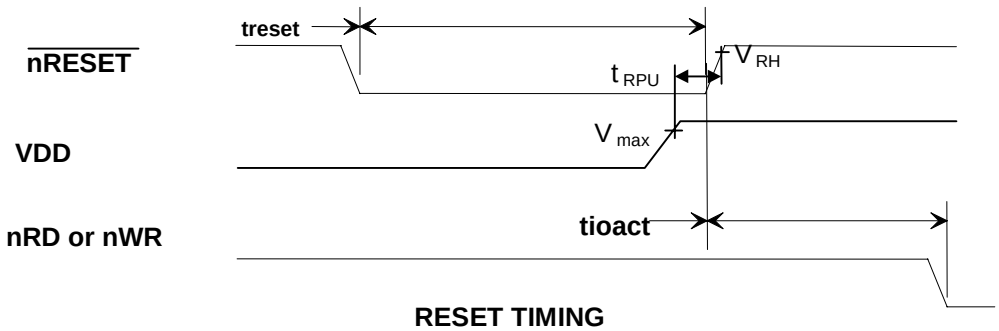
9.4 SL11RIDE USB Transceiver Characteristics

Parameter	Description	Min.	Typical[10]	Max.
V_{IHYS}	Hysteresis On Input (Data+, Data–)	0.1V		200 mV
V_{USBIH}	USB Input Voltage HIGH		1.5V	2.0V
V_{USBIL}	USB Input Voltage LOW	0.8V	1.3V	
V_{USBOH}	USB Output Voltage HIGH	2.2V		
V_{USBOL}	USB Output Voltage LOW			0.7V
Z_{USBH}[11]	Output Impedance HIGH STATE	24Ω		43Ω
Z_{USBL}[11]	Output Impedance LOW STATE	24Ω		43Ω
I_{USB}	Transceiver Supply p-p Current (3.3V)			< 220 µA

Notes:
10. All typical values are V_{DD2} = 3.3 V and T_{AMB}= 25°C.
11. Z_{USBX} Impedance Values includes an external resistor of 24 -- 43 Ohms ± 1%

9.5 SL11RIDE Reset Timing

The nRESET signal from the SL11RIDE chip resets the disk drive. It forces an initialization to occur identical to that after power-up.



RESET TIMING

Parameter	Description	Min.	Typical	Max.
V_{CC}	Operating Voltage Range			5.5V
t_{RPU}	Time Reset Pull up	150 ms		
V_{max}	Voltage reach max	V_{DD} – 0.7V		
V_{RH}	Voltage Reset High	3.0V		
treset	nRESET Pulse width	16 clocks		
tioact	nRESET high to nRD	16 clocks		

Note: Clock is 48 MHz nominal.

9.6 Reset Circuit

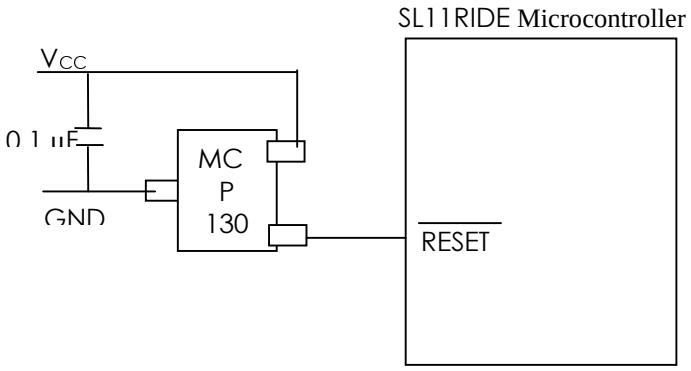


Figure 9-1. Reset Circuit Sample

9.7 SL11RIDE PIO Read/Write Cycle

At power-up and during Read/Write Cycles, the SL11RIDE uses PIO mode 2 timing for the data transfer from/to device. See chapter 10 in the section 10.2.2 of [ref 1] AT Attachment with Packet Interface Extension (ATA/ATAPI-5) for more detail.

10.0 Appendix

This is a pin translation of SL11RIDE signals to 36, 44, 50, and 68 of the Storage Device Class, which is based on the latest AT Attachment specification and Compact Flash Specification Version 1.4.

These signals connect directly to the ATAPI/IDE devices. If you intend to design for a long IDE cable, then you have to use RC Termination. See [ref 1] AT Attachment with Packet Interface Extension (ATA/ATAPI-5).

10.1 SL11RIDE Pin Translation: 36-Pin–40-Pin Signals

Table 10-1. 36-pin to 40-pin Interface Signals

SL11RIDE Signal	36-Pin Signal	36-Pin	Translates	40-Pin
GND	GND	1	→	2
nRESET	RESET	2	→	1
D8	D8	3	→	4
D7	D7	4	→	3
D9	D9	5	→	6
D6	D6	6	→	5
D10	D10	7	→	8

Table 10-1. 36-pin to 40-pin Interface Signals (continued)

SL11RIDE Signal	36-Pin Signal	36-Pin	Translates	40-Pin
D5	D5	8	→	7
D11	D11	9	→	10
D4	D4	10	→	9
D12	D12	11	→	12
D3	D3	12	→	11
D13	D13	13	→	14
D2	D2	14	→	13
D14	D14	15	→	16
D1	D1	16	→	15
D15	D15	17	→	18
D0	D0	18	→	35
PU[7]	DMARQ	19		NC
IOWD	IOWR	20	→	23
IORD	IORD	21	→	25
PU[7]	IORDY	22	→	27
PU[7]	DMACK	23		NC
INTRQ	IRQ	24	→	31
PU[7]	IOCS16	25	→	32
A1	A1	26	→	33
GND	GND	27	→	19
A0	A0	28	→	35
A2	A2	29	→	36
CS0	CS0	30	→	37
CS1	CS1	31	→	38
GND	GND	32	→	22
V_{CC}	+5V	33		VCC
GND	GND	34	→	24
V_{CC}	+5V	35	→	VCC
GND	GND	36	→	26

10.2 SL11RIDE Pin Translation: 40-Pin–44-Pin Signals

Table 10-2. SL11RIDE Pin Translation: 40-Pin–44-Pin Signals

IDE Signal	Pin	Pin	IDE Signal
	A	B	(See Note 12)
	C	D	(See Note 12)
	E	F	(See Note 12)
nRESET	1	2	GND
DD7	3	4	DD8

Table 10-2. SL11RIDE Pin Translation: 40-Pin–44-Pin Signals (continued)

IDE Signal	Pin	Pin	IDE Signal
DD6	5	6	DD9
DD5	7	8	DD10
DD4	9	10	DD11
DD3	11	12	DD12
DD2	13	14	DD13
DD1	15	16	DD14
DD0	17	18	DD15
GND	19	20	Key[13]
DMARQ[15]	21	22	GND
IOWD	23	24	GND
IORD	25	26	GND
IORDY[15]	27	28	CSEL[14]
DMACK[15]	29	30	GND
INTRQ	31	32	IOCS16[15]
DA1	33	34	PDIAG[15]
DA0	35	36	DA2
CS0	37	38	CS1
DASP	39	40	GND
+5V	41	42	+5V
GND	43	44	TYPE

Notes:
12. A—F: Pins that are additional to those of the 40-pin connector.
13. The Key pin must be not connected.
14. CSEL connect to GND for default Master and Slave modes.
15. These signals need a 10k pull-up.

10.3 SL11RIDE Pin Translation: 40-Pin–50-Pin SLIM Connector

The SLIM connector is a new connector that is used for CD-ROM, CD-RW, and ZIP drives.

Table 10-3. SL11RIDE Pin Translation: 40-Pin–50-Pin SLIM Signals

SL11RIDE Signals	SLIM Signals	Pin	Pin	SLIM Signals	SL11RIDE Signals
NC	LOUT	1	2	ROUT	NC
GND	AGND	3	4	NC	NC
nRESET	RESET	5	6	DD8	D8
D7	DD7	7	8	DD9	D9
D6	DD6	9	10	DD10	D10
D5	DD5	11	12	DD11	D11
D4	DD4	13	14	DD12	D12
D3	DD3	15	16	DD13	D13
D2	DD2	17	18	DD14	D14
D1	DD1	19	20	DD15	D15
D0	DD0	21	22	DMARQ	PU[7]

Table 10-3. SL11RIDE Pin Translation: 40-Pin–50-Pin SLIM Signals (continued)

SL11RIDE Signals	SLIM Signals	Pin	Pin	SLIM Signals	SL11RIDE Signals
GND	GND	23	24	DIOR–	IORD
IOWD	DIOW	25	26	GND	GND
PU[7]	IORDY	27	28	DMACK	PU[7]
INTRQ	INTRQ	29	30	IOCS16	PU[7]
A1	DA1	31	32	PDIAG	PU[7]
A0	DA0	33	34	DA2	A2
CS0	CS0	35	36	CS1–	CS1
DASP	DASP	37	38	+5V	V_{CC}
V_{CC}	+5V	39	40	+5V	V_{CC}
V_{CC}	+5V	41	42	+5V	V_{CC}
GND	GND	43	44	GND	GND
GND	GND	45	46	GND	GND
PD[16]	CSEL	47	48	GND	GND
NC	Reserved	49	50	Reserved	NC

Note:
16. PD: CSEL connect to GND for Master and Slave mode

10.4 CLIK 50-Pin Connect with SL11RIDE

The CLIK can connect directly to the SL11RIDE chip for integration solution or can interface with the SL11RIDE via a PCMCIA card.

Note:

- User can define STATUS LED.

10.5 SL11RIDE Pin Translation: 40-Pin–50-Pin CF Card Signals

Table 10-4. SL11RIDE Pin Translation: 40-Pin–50-Pin Signals

SL11RIDE Pin	CLIK Signal	Pin	Pin	CLIK Signal	SL11RIDE Pin
V_{CC}	V_{CC}	1	2	GND	GND
V_{CC}	5V	3	4	GND	GND
nRESET	HRSTD	5	6	X	X
D7	HDD7	7	8	HDD8	D8
D6	HDD6	9	10-	HDD9	D9
D5	HDD5	11	12	HDD10	D10
D4	HDD4	13	14	HDD11	D11
D3	HDD3	15	16	HDD12	D12
D2	HDD2	17	18	HDD13	D13
D1	HDD1	19	20	HDD14	D14
D0	HDD0	21	22	HDD15	D15
GND	GND	23	24	KEYED	NC
PU	DREOO	25	26	GND	GND
IOWD	IOWI	27	28	GND	GND

Table 10-4. SL11RIDE Pin Translation: 40-Pin–50-Pin Signals (continued)

SL11RIDE Pin	CLIK Signal	Pin	Pin	CLIK Signal	SL11RIDE Pin
IORD	IORI	29	30	GND	GND
PU	IOCHROYI	31	32	CESEL	GND with 22Ω
PU	DACK1	33	34	GND	GND
INTRQ	IA01	35	36	IOCSI61	PU
A1	HA10	37	38	POIAG	PU
A0	HA00	39	40	HA20	A2
CS0	HCS00	41	42	HCS10	CS1
DASP	DASPI	43	44	GND	GND
VCC	VCC	45	46	GND	GND
GND with 22Ω	TXD	47	48	RXD	GND with 22Ω
GND with 22 Ω	ATA MODE	49	50	STATUS LED	Note 7

SL11RIDE Signals	CF Signals	Pin	Pin	CF Signals	SL11RIDE Signals
GND	GND	1	2	D3	D3
D4	D4	3	4	D5	D5
D6	D6	5	6	D7	D7
CS0	CE1	7	8	A10	GND
GND	OE	9	10	A9	GND
GND	A8	11	12	A7	GND
PVCC[17]	VCC	13	14	A6	GND
GND	A5	15	16	A4	GND
GND	A3	17	18	A2	A2
A1	A1	19	20	A0	A0
D0	D0	21	22	D1	D1
D2	D2	23	24	IOSI16	PU[7]
GND	CD2	25	26	CD1	C_DET
D11	D11	27	28	D12	D12
D13	D13	29	30	D14	D14
D15	D15	31	32	CE2	PU[7]
GND	VS1	33	34	IORD	IORD
IOWD	IOWR	35	36	WE	PVCC[17]
PU[7]	IREQ	37	38	VCC	PVCC[17]
PD[14]	CSEL	39	40	VS2	GND
PWC_RESET	RESET	41	42	WAIT	PU[7]
Not Connect	INPACK	43	44	REG	PU[7]
PU[7]	BVD2	45	46	BVD1	PU[7]
D8	D8	47	48	D9	D9
D10	D10	49	50	GND	GND

Notes:
17. PVCC= 5VDC from power switch

10.6 Fast EPP Pin Assignment and Description

Table 10-5. Fast EPP Pin Assignment and Description

Pin Name	Pin No.	GPIO Pins	Pin Type	GPIO & Fast EPP Pin Chip Revision 1.1
V_{DD}	1		Power	+3.3 VDC Supply
D0	2		Bidir	External Memory Data Bus, Data0
D1	3		Bidir	External Memory Data Bus, Data1
D2	4		Bidir	External Memory Data Bus, Data2
D3	5		Bidir	External Memory Data Bus, Data3
D4	6		Bidir	External Memory Data Bus, Data4
D5	7		Bidir	External Memory Data Bus, Data5
D6	8		Bidir	External Memory Data Bus, Data6
D7	9		Bidir	External Memory Data Bus, Data7
D8	10		Bidir	External Memory Data Bus, Data8
D9	11		Bidir	External Memory Data Bus, Data9
D10	12		Bidir	External Memory Data Bus, Data10
D11	13		Bidir	External Memory Data Bus, Data11
GND	14		GND	Digital ground.
X1	15		Input	External 48-MHz Crystal or Clock Input.
X2	16		Output	External crystal output. No connection when X1 is used for clock input
VDD	17		Power	+3.3 VDC Supply
D12	18		Bidir	External Memory Data Bus, Data12
D13	19		Bidir	External Memory Data Bus, Data13
D14	20		Bidir	External Memory Data Bus, Data14
D15	21		Bidir	External Memory Data Bus, Data15
A20	22		Output	External Memory Address Bus, A20
A19	23		Output	External Memory Address Bus, A19
A18	24		Output	External Memory Address Bus, A18
A17	25		Output	External Memory Address Bus, A17
A16	26		Output	External Memory Address Bus, A16
A15	27		Output	External Memory Address Bus, A15
A14	28		Output	External Memory Address Bus, A14
A13	29		Output	External Memory Address Bus, A13
A12	30		Output	External Memory Address Bus, A12
A11	31		Output	External Memory Address Bus, A11
A10	32		Output	External Memory Address Bus, A10
A9	33		Output	External Memory Address Bus, A9
A8	34		Output	External Memory Address Bus, A8
A7	35		Output	External Memory Address Bus, A7
A6	36		Output	External Memory Address Bus, A6
A5	37		Output	External Memory Address Bus, A5

Table 10-5. Fast EPP Pin Assignment and Description (continued)

Pin Name	Pin No.	GPIO Pins	Pin Type	GPIO & Fast EPP Pin Chip Revision 1.1
A4	38		Output	External Memory Address Bus, A4
A3	39		Output	External Memory Address Bus, A3
GND	40		GND	Digital ground
A2	41		Output	External Memory Address Bus, A2
A1	42		Output	External Memory Address Bus, A1
A0	43		Output	External Memory Address Bus, A0
TEST	44		Input	No Connection, MFG test only
nWRL	45		Output	Active LOW, Write to lower bank of External SRAM
nWRH	46		Output	Active LOW, Write to upper bank of External SRAM
nRD	47		Output	Active LOW, Read from External SRAM or ROM
nRESET	48		Input	Master Reset. SL11R Device active low reset input.
nRAS	49		Output	Active LOW, DRAM Row Address Select
V_{DD}	50		Power	+3.3 VDC Supply
V_{DD}	51		Power	+3.3 VDC Supply
nCASL	52		Output	Active LOW, DRAM Column Low Address Select
nCASH	53		Output	Active LOW, DRAM Column High Address Select
nDRAMOE	54		Output	Active LOW, DRAM Output Enable
nDRAMWR	55		Output	Active LOW, DRAM Write
nXRAMSEL	56		Output	Active LOW, select external SRAM (16 bit)
nXROMSEL	57		Output	Active LOW, select external ROM
nXMEMSEL	58		Output	Active LOW, select external Memory bus, external SRAM, DRAM, ROM or any memory mapped device
X_PCLK	59		Bidir	See register 0xC006 for more information
SECLK	60	GPIO31	Bidir	SECLK, Serial EEPROM clock, or GPIO31
SEDO	61	GPIO30	Bidir	SEDO, Serial flash EPROM Data, or GPIO30 This pin requires a 5-kΩ pull-up.
GPIO29	62	GPIO29	Bidir	GPIO29
UART_TXD	63	GPIO28	Output	UART Transmit Data (out), or GPIO28
GND	64		GND	Digital ground
GND	65		GND	Digital ground
UART_RXD	66	GPIO27	Input	UART Receive Data (in), or GPIO27
nENS	67	GPIO26	Output	Serial EPROM control signal
CLKS	68	GPIO25	Output	Serial EPROM Clock
nDTSRB	69	GPIO24	Output	EPP Data Strobe
nASTRB	70	GPIO23	Output	EPP Address Strobe
nWRITE	71	GPIO22	Output	EPP Write Strobe
P9	72	GPIO21	Output	P Register
P5	73	GPIO20	Output	P Register or PWR_OFF
P4	74	GPIO19	Output	P Register

Table 10-5. Fast EPP Pin Assignment and Description (continued)

Pin Name	Pin No.	GPIO Pins	Pin Type	GPIO & Fast EPP Pin Chip Revision 1.1
VDD	75		Power	+3.3 VDC Supply
P3	76	GPIO18	Output	P Register or USB_PU (USB DATA+ pull up)
P2	77	GPIO17	Output	P Register
P1	78	GPIO16	Output	P Register
GND	79		GND	Digital ground
P6	80	GPIO15	Output	P Register
P7	81	GPIO14	Output	P Register
P8	82	GPIO13	Output	P Register
GPIO12	83	GPIO12	Bidir	GPIO12
DATAS	84	GPIO11	Bidir	DATA Strobe for Serial EPROM
VREQ	85	GPIO10	Input	TBD
WAIT	86	GPIO9	Bidir	EPP WAIT signal
V_{DD1}	87		Power	USB +3.3 VDC Supply.
DATA+	88		Bidir	USB Differential DATA Signal High Side
DATA–	89		Bidir	USB Differential DATA Signal Low Side
GND1	90		GND	USB Digital Ground
INTR	91	GPIO8	Input	EPP INTR pin
SD7	92	GPIO7	Bidir	EPP Data bit 7
SD6	93	GPIO6	Bidir	EPP Data bit 6
SD5	94	GPIO5	Bidir	EPP Data bit 5
SD4	95	GPIO4	Bidir	EPP Data bit 4
SD3	96	GPIO3	Bidir	EPP Data bit 3
SD2	97	GPIO2	Bidir	EPP Data bit 2
SD1	98	GPIO1	Bidir	EPP Data bit 1
SD0	99	GPIO0	Bidir	EPP Data bit 0
VDD	100		Power	+3.3 VDC Supply

10.7 Design ATAPI/IDE Device Behaves Like Floppy Disk Drive

This design applies to small and low power consumption ATAPI/IDE devices such as Compact Flash, CLIK, MicroDrives, and Smart Media cards. This is an advantage for users to exchange media cards (i.e. MP3) from the SL11RIDE board without plugging or unplugging the USB cable.

This requires three free GPIO signals:

- GPIO 19-CD_DET: Card Detect
- GPIO 25-PWC_RESET: Power Hardware Reset
- GPIO 26-PWC: Power Control

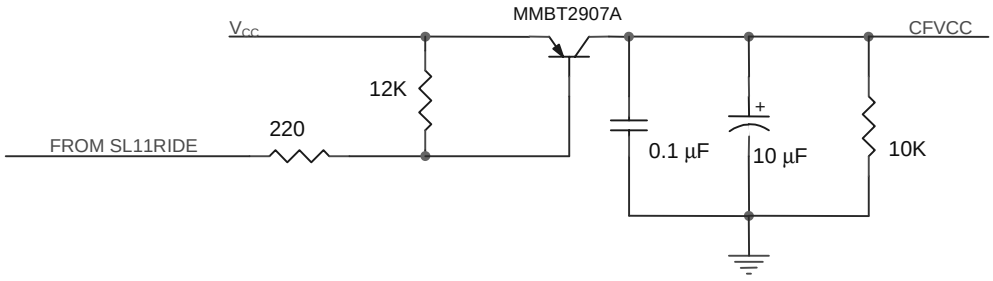


Figure 10-1. Compact Flash Design Note

Table 10-6. Power Switch Operation

Power switch operation	PWC Signal	PVCC Output
	High	OFF
	Low	ON

Table 10-7. Compact Flash Design

Name	Description
V_{CC}	+5V from USB Power or external power
R_{PU}	10-kΩ pull-up resistor
R_{PURS}	10-kΩ pull-up resistor
R_{RS}	1-kΩ series resistor (This depends on transistor requirement)
CD_DET	Card detection uses to detect card present or not. It need 10k pull-up to +3.3VDC.
PWC_RESET	Hardware Reset to the card after power on
PWC	Power control use to turn power on/off when the card insert/remove
PVCC	Power supply to Compact Flash. It must provide enough current and voltage to the card.

10.8 CPU Speed Control

10.8.1 Speed Control Register (0xC008: R/W)

The Speed Control Register allows the SL11R processor to operate at a number of speed selections. A four-bit divider (SPD3-0 + 1) selects the speed as shown below. Speed will also depend on the clock multiplier. See Configuration Register (0xC006: R/W) for more information.

D15-D4	D3	D2	D1	D0
0	SPD3	SPD2	SPD1	SPD0

D3-D0 SPD3-SPD0 Speed selection bits

SPD3-0	SL11R Speed
0000	48.00 MHz.
0001	24.00 MHz.
0010	16.00 MHz.
0011	12.00 MHz.
0100	09.60 MHz.
0101	08.00 MHz.
0110	06.86 MHz.
0111	06.00 MHz.
1000	05.33 MHz.
1001	04.80 MHz.
1010	04.36 MHz.
1011	04.00 MHz.
1100	03.69 MHz.
1101	03.42 MHz.
1110	03.20 MHz.
1111	03.00 MHz.

D15-D4 Reserved should be set to all zeros.

Note:

Upon reset, the lowest speed is selected for low power operation. The SL11R BIOS will configure the clock to 24 MHz as part of its initialization.

11.0 Revision History

Document Title: SL11RIDE USB to IDE/ATAPI Solution Document Number: 38-08007				
REV.	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
**	110566	12/14/01	BHA	Converted to Cypress Format from ScanLogic