

*4M x 16bit CMOS Dynamic RAM with Fast Page Mode*

**DESCRIPTION**

This is a family of 4,194,304 x 16 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time (-45, -5 or -6), power consumption(Normal or Low power) are optional features of this family. All of this family have  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh,  $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 4Mx16 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.

**FEATURES**

• **Part Identification**

- KM416V4000B/B-L(3.3V, 8K Ref.)
- KM416V4100B/B-L(3.3V, 4K Ref.)

• **Active Power Dissipation**

Unit : mW

Speed	8K	4K
-45	360	468
-5	324	432
-6	288	396

• **Refresh Cycles**

Part NO.	Refresh cycle	Refresh time	
		Normal	L-ver
KM416V4000B*	8K	64ms	128ms
KM416V4100B	4K		

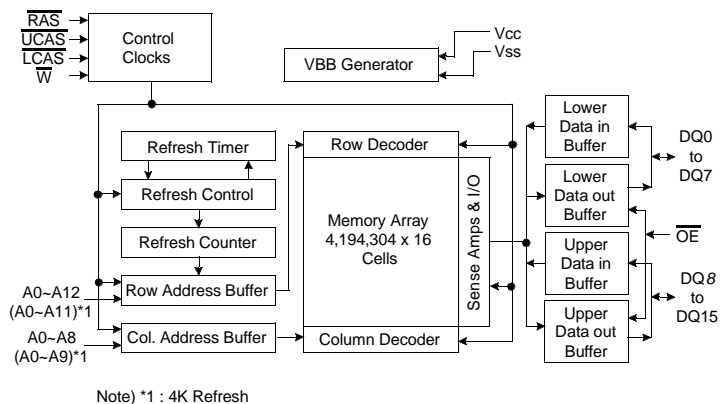
- \* Access mode &  $\overline{\text{RAS}}$  only refresh mode  
 : 8K cycle/64ms(Normal), 8K cycle/128ms(L-ver.)  
 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  & Hidden refresh mode  
 : 4K cycle/64ms(Normal), 4K cycle/128ms(L-ver.)

• **Performance Range**

Speed	t <sub>RAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>	t <sub>PC</sub>
-45	45ns	12ns	80ns	31ns
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns

- Fast Page Mode operation
- $2\overline{\text{CAS}}$  Byte/Word Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- Fast parallel test mode capability
- LVTTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic TSOP(II) packages
- +3.3V±0.3V power supply

**FUNCTIONAL BLOCK DIAGRAM**

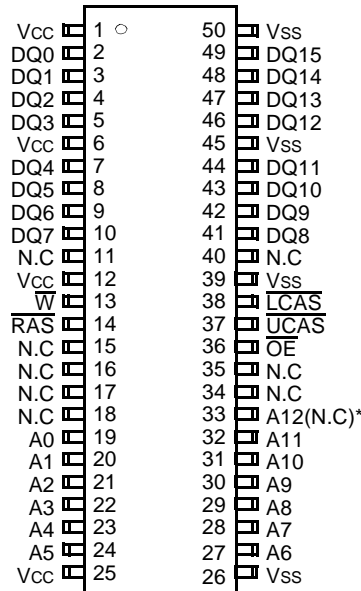


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PIN CONFIGURATION (Top Views)

•KM416V40(1)00BS



(400mil TSOP(II))

\*(N.C) : N.C for 4K Refresh Product

Pin Name	Pin function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 - 15	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power(+3.3V)
N.C	No Connection

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V <sub>IN</sub> ,V <sub>OUT</sub>	-0.5 to +6.5	V
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.5 to +4.6	V
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Power Dissipation	P <sub>D</sub>	1	W
Short Circuit Output Current	I <sub>OS</sub>	50	mA

\* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS** (Voltage referenced to Vss, T<sub>A</sub>= 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.0	-	+5.5* <sup>1</sup>	V
Input Low Voltage	V <sub>IL</sub>	-0.3* <sup>2</sup>	-	0.8	V

\*1 : 6.5V at pulse width ≤15ns which is measured at Vcc

\*2 : -1.3 at pulse width ≤15ns which is measured at Vss

**DC AND OPERATING CHARACTERISTICS** (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V <sub>IN</sub> ≤V <sub>CC</sub> +0.3V, all other pins not under test=0 Volt)	I <sub>I(L)</sub>	-5	5	uA
Output Leakage Current (Data out is disabled, 0V≤V <sub>OUT</sub> ≤V <sub>CC</sub> )	I <sub>O(L)</sub>	-5	5	uA
Output High Voltage Level(I <sub>OH</sub> =-2mA)	V <sub>OH</sub>	2.4	-	V
Output Low Voltage Level(I <sub>OL</sub> =2mA)	V <sub>OL</sub>	-	0.4	V



## DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max		Units
			KM416V4000B	KM416V4100B	
Icc1	Don't care	-45	100	130	mA
		-5	90	120	mA
		-6	80	110	mA
Icc2	Normal L	Don't care	2	2	mA
			2	2	mA
Icc3	Don't care	-45	100	130	mA
		-5	90	120	mA
		-6	80	110	mA
Icc4	Don't care	-45	70	80	mA
		-5	60	70	mA
		-6	50	60	mA
Icc5	Normal L	Don't care	500	500	uA
			300	300	uA
Icc6	Don't care	-45	100	130	mA
		-5	90	120	mA
		-6	80	110	mA
Icc7	L	Don't care	400	400	uA
IccS	L	Don't care	400	400	uA

Icc1\* : Operating Current ( $\overline{RAS}$  and  $\overline{UCAS}$ ,  $\overline{LCAS}$ , Address cycling @trc=min.)

Icc2 : Standby Current ( $\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{IH}$ )

Icc3\* :  $\overline{RAS}$ -only Refresh Current ( $\overline{UCAS}=\overline{LCAS}=V_{IH}$ ,  $\overline{RAS}$ , Address cycling @trc=min.)

Icc4\* : Fast Page Mode Current ( $\overline{RAS}=V_{IL}$ ,  $\overline{UCAS}$  or  $\overline{LCAS}$ , Address cycling @tpc=min.)

Icc5 : Standby Current ( $\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{CC}-0.2V$ )

Icc6\* :  $\overline{CAS}$ -Before- $\overline{RAS}$  Refresh Current ( $\overline{RAS}$  and  $\overline{UCAS}$  or  $\overline{LCAS}$  cycling @trc=min)

Icc7 : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage( $V_{IH}$ )= $V_{CC}-0.2V$ , Input low voltage( $V_{IL}$ )= $0.2V$ ,  $\overline{UCAS}$ ,  $\overline{LCAS}=\overline{CAS}$ -before- $\overline{RAS}$  cycling or  $0.2V$ ,

$\overline{W}$ ,  $\overline{OE}=V_{IH}$ , Address=Don't care DQ=Open, Trc=31.25us

IccS : Self Refresh Current

$\overline{RAS}=\overline{UCAS}=\overline{LCAS}=0.2V$ ,  $\overline{W}=\overline{OE}=A0 \sim A12(A11)=V_{CC}-0.2V$  or  $0.2V$ , DQ0 ~ DQ15= $V_{CC}-0.2V$ ,  $0.2V$  or Open

**\*Note :** Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1, Icc3 and Icc6, address can be changed maximum once while  $\overline{RAS}=V_{IL}$ . In Icc4, address can be changed maximum once within one fast page mode cycle time, tpc.

# KM416V4000B, KM416V4100B

# CMOS DRAM

## CAPACITANCE (TA=25°C, VCC=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A12]	CIN1	-	5	pF
Input capacitance [ $\overline{\text{RAS}}$ , $\overline{\text{UCAS}}$ , $\overline{\text{LCAS}}$ , $\overline{\text{W}}$ , $\overline{\text{OE}}$ ]	CIN2	-	7	pF
Output capacitance [DQ0 - DQ15]	CDQ	-	7	pF

## AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, See note 1,2)

Test condition : VCC=3.3V±0.3V, Vih/Vil=2.2/0.7V, Voh/Vol=2.0/0.8V

Parameter	Symbol	-45		-5		-6		Units	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	80		90		110		ns	
Read-modify-write cycle time	trwc	115		133		153		ns	
Access time from $\overline{\text{RAS}}$	trac		45		50		60	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tcac		12		13		15	ns	3,4,5
Access time from column address	tAA		23		25		30	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	13	0	13	ns	6
Transition time (rise and fall)	tr	1	50	1	50	1	50	ns	2
$\overline{\text{RAS}}$ precharge time	trp	25		30		40		ns	
$\overline{\text{RAS}}$ pulse width	trAS	45	10K	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	trSH	12		13		15		ns	
$\overline{\text{CAS}}$ hold time	tCSH	45		50		60		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	12	10K	13	10K	15	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	trCD	18	33	20	37	20	45	ns	4
$\overline{\text{RAS}}$ to column address delay time	trAD	13	22	15	25	15	30	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	trCP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	trAH	8		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	13
Column address hold time	tCAH	8		10		10		ns	13
Column address to $\overline{\text{RAS}}$ lead time	trAL	23		25		30		ns	
Read command set-up time	trCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	trCH	0		0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	trRH	0		0		0		ns	8
Write command hold time	twCH	8		10		10		ns	
Write command pulse width	tWP	8		10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	trWL	13		15		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	tcWL	12		13		15		ns	16
Data set-up time	tDS	0		0		0		ns	9,19
Data hold time	tDH	10		10		10		ns	9,19



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-45		-5		-6		Units	Note
		Min	Max	Min	Max	Min	Max		
Refresh period (Normal)	tREF		64		64		64	ms	
Refresh period (L-ver)	tREF		128		128		128	ms	
Write command set-up time	twCS	0		0		0		ns	7
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tcWD	32		36		38		ns	7,15
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	trWD	67		73		83		ns	7
Column address to $\overline{\text{W}}$ delay time	tawD	43		48		53		ns	7
$\overline{\text{CAS}}$ precharge $\overline{\text{W}}$ delay time	tcpWD	48		53		60		ns	
$\overline{\text{CAS}}$ set-up time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	5		5		5		ns	17
$\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		10		ns	18
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	trPC	5		5		5		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		26		30		35	ns	3
Fast Page mode cycle time	tPC	31		35		40		ns	
Fast Page mode read-modify-write cycle time	tPRWC	70		76		85		ns	
$\overline{\text{CAS}}$ precharge time (Fast page cycle)	tCP	9		10		10		ns	14
$\overline{\text{RAS}}$ pulse width (Fast page cycle)	trASP	45	200K	50	200K	60	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	trHCP	28		30		35		ns	
$\overline{\text{OE}}$ access time	toEA		12		13		15	ns	
$\overline{\text{OE}}$ to data delay	toED	12		13		13		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	toEZ	0	13	0	13	0	13	ns	6
$\overline{\text{OE}}$ command hold time	toEH	12		13		15		ns	
Write command set-up time (Test mode in)	twTS	10		10		10		ns	11
Write command hold time (Test mode in)	twTH	15		15		15		ns	11
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time ( $\overline{\text{C}}$ -B- $\overline{\text{R}}$ refresh)	tWRP	10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time ( $\overline{\text{C}}$ -B- $\overline{\text{R}}$ refresh)	tWRH	10		10		10		ns	
$\overline{\text{RAS}}$ pulse width ( $\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	trASS	100		100		100		us	20,21,22
$\overline{\text{RAS}}$ precharge time ( $\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	trPS	80		90		110		ns	20,21,22
$\overline{\text{CAS}}$ hold time ( $\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	tCHS	-50		-50		-50		ns	20,21,22

**TEST MODE CYCLE**

( Note 11 )

Parameter	Symbol	-45		-5		-6		Units	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t <sub>RC</sub>	85		95		115		ns	
Read-modify-write cycle time	t <sub>RWC</sub>	120		138		160		ns	
Access time from $\overline{\text{RAS}}$	t <sub>RAC</sub>		50		55		65	ns	3,4,10,12
Access time from $\overline{\text{CAS}}$	t <sub>CAC</sub>		17		18		20	ns	3,4,5,12
Access time from column address	t <sub>AA</sub>		28		30		35	ns	3,10,12
$\overline{\text{RAS}}$ pulse width	t <sub>RAS</sub>	50	10K	55	10K	65	10K	ns	
$\overline{\text{CAS}}$ pulse width	t <sub>CAS</sub>	17	10K	18	10K	20	10K	ns	
$\overline{\text{RAS}}$ hold time	t <sub>RSH</sub>	17		18		20		ns	
$\overline{\text{CAS}}$ hold time	t <sub>CSH</sub>	50		55		65		ns	
Column Address to $\overline{\text{RAS}}$ lead time	t <sub>RAL</sub>	28		30		35		ns	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t <sub>CWD</sub>	37		41		43		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t <sub>RWD</sub>	72		78		88		ns	7
Column Address to $\overline{\text{W}}$ delay time	t <sub>AWD</sub>	48		53		58		ns	7
Fast Page mode cycle time	t <sub>PC</sub>	36		40		45		ns	
Fast Page mode read-modify-write cycle time	t <sub>PRWC</sub>	75		81		90		ns	
$\overline{\text{RAS}}$ pulse width (Fast page cycle)	t <sub>RASP</sub>	50	200K	55	200K	65	200K	ns	
Access time from $\overline{\text{CAS}}$ precharge	t <sub>CPA</sub>		31		35		40	ns	3
$\overline{\text{OE}}$ access time	t <sub>OEA</sub>		17		18		20	ns	
$\overline{\text{OE}}$ to data delay	t <sub>OED</sub>	17		18		18		ns	
$\overline{\text{OE}}$ command hold time	t <sub>OEH</sub>	17		18		20		ns	



**NOTES**

1. An initial pause of 200 $\mu$ s is required after power-up followed by any 8  $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles before proper device operation is achieved.
2.  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL load and 100pF.
4. Operation within the  $t_{\text{RCD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met,  $t_{\text{RCD}}(\text{max})$  is specified as a reference point only. If  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ .
5. Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ .
6.  $t_{\text{OFF}}(\text{min})$  and  $t_{\text{OEZ}}(\text{max})$  define the time at which the output achieves the open circuit condition and are not referenced  $V_{OH}$  or  $V_{OL}$ .
7.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$  and  $t_{\text{AWD}}$  are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ , the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ ,  $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$  and  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ , then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycle.
9. These parameters are referenced to  $\overline{\text{CAS}}$  falling edge in early write cycles and to  $\overline{\text{W}}$  falling edge in read-modify-write cycles. Operation within the  $t_{\text{RAD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met.  $t_{\text{RAD}}(\text{max})$  is specified as a reference point only.
10. If  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{max})$  limit, then access time is controlled by  $t_{\text{AA}}$ . These specifications are applied in the test mode.
11. In test mode read cycle, the value of  $t_{\text{RAC}}$ ,  $t_{\text{AA}}$ ,  $t_{\text{CAC}}$  is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
- 12.

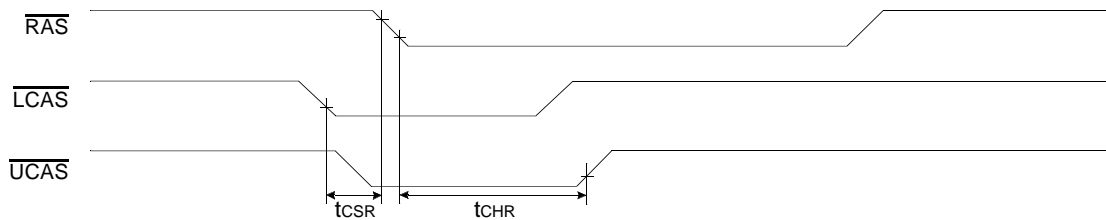
**KM416V40(1)00B Truth Table**

$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	DQ0 - DQ7	DQ8-DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

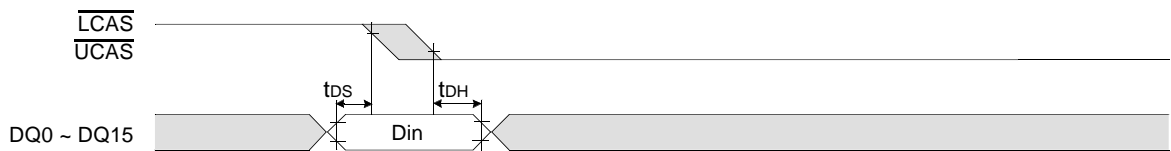




- 13. t<sub>ASC</sub>, t<sub>CAH</sub> are referenced to the earlier  $\overline{\text{CAS}}$  falling edge.
- 14. t<sub>CP</sub> is specified from the later  $\overline{\text{CAS}}$  rising edge in the previous cycle to the earlier  $\overline{\text{CAS}}$  falling edge in the next cycle.
- 15. t<sub>CWD</sub> is referenced to the later  $\overline{\text{CAS}}$  falling edge at word read-modify-write cycle.
- 16. t<sub>CWL</sub> is specified from  $\overline{\text{W}}$  falling edge to the earlier  $\overline{\text{CAS}}$  rising edge.
- 17. t<sub>CSR</sub> is referenced to the earlier  $\overline{\text{CAS}}$  falling edge before  $\overline{\text{RAS}}$  transition low.
- 18. t<sub>CHR</sub> is referenced to the later  $\overline{\text{CAS}}$  rising edge after  $\overline{\text{RAS}}$  transition low.

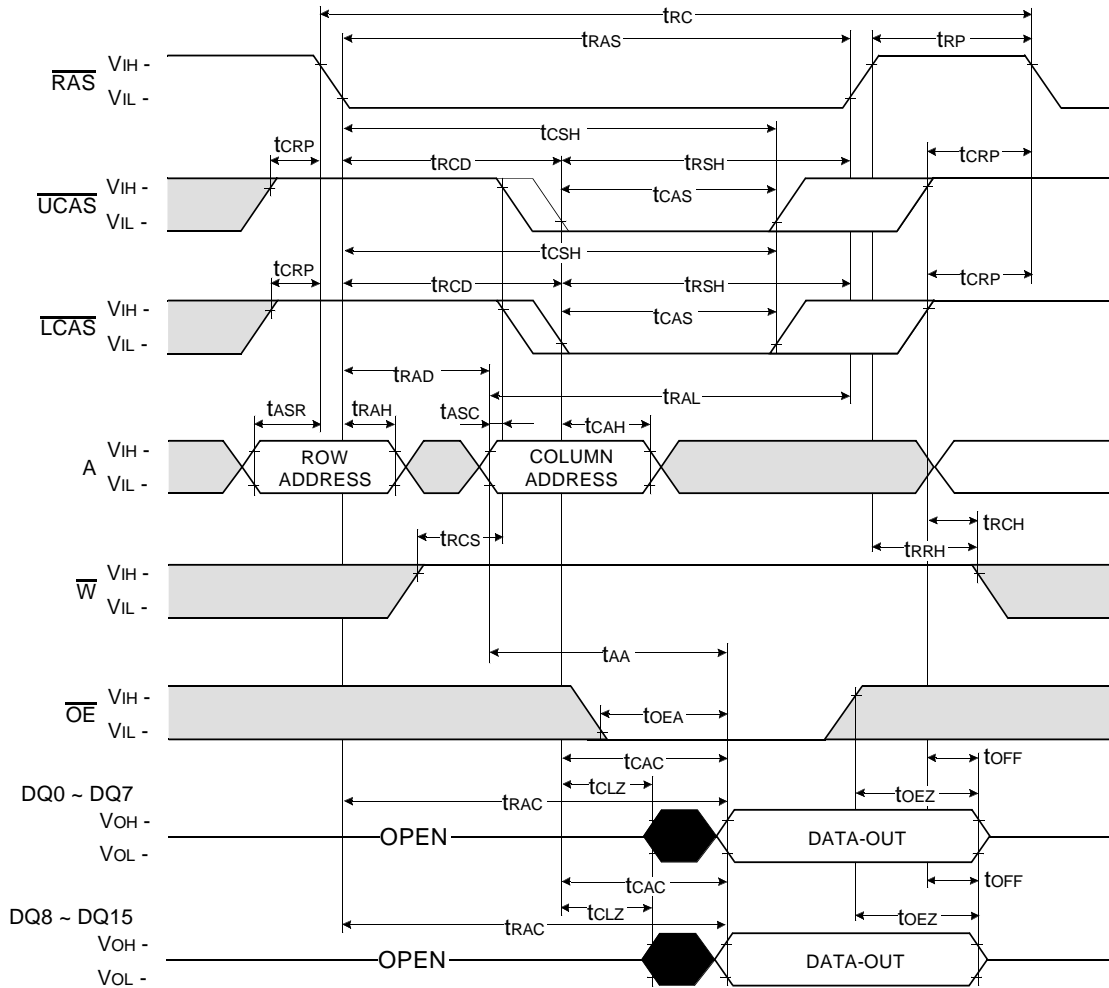


- 19. t<sub>DS</sub> is specified for the earlier  $\overline{\text{CAS}}$  falling edge and t<sub>DH</sub> is specified by the later  $\overline{\text{CAS}}$  falling edge.



- 20. If t<sub>RASS</sub> ≥ 100us, then  $\overline{\text{RAS}}$  precharge time must use t<sub>RPS</sub> instead of t<sub>RP</sub>.
- 21. For  $\overline{\text{RAS}}$ -only refresh and burst  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh mode, 4096(4K/8K) cycles of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.
- 22. For distributed  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  with 15.6us interval  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

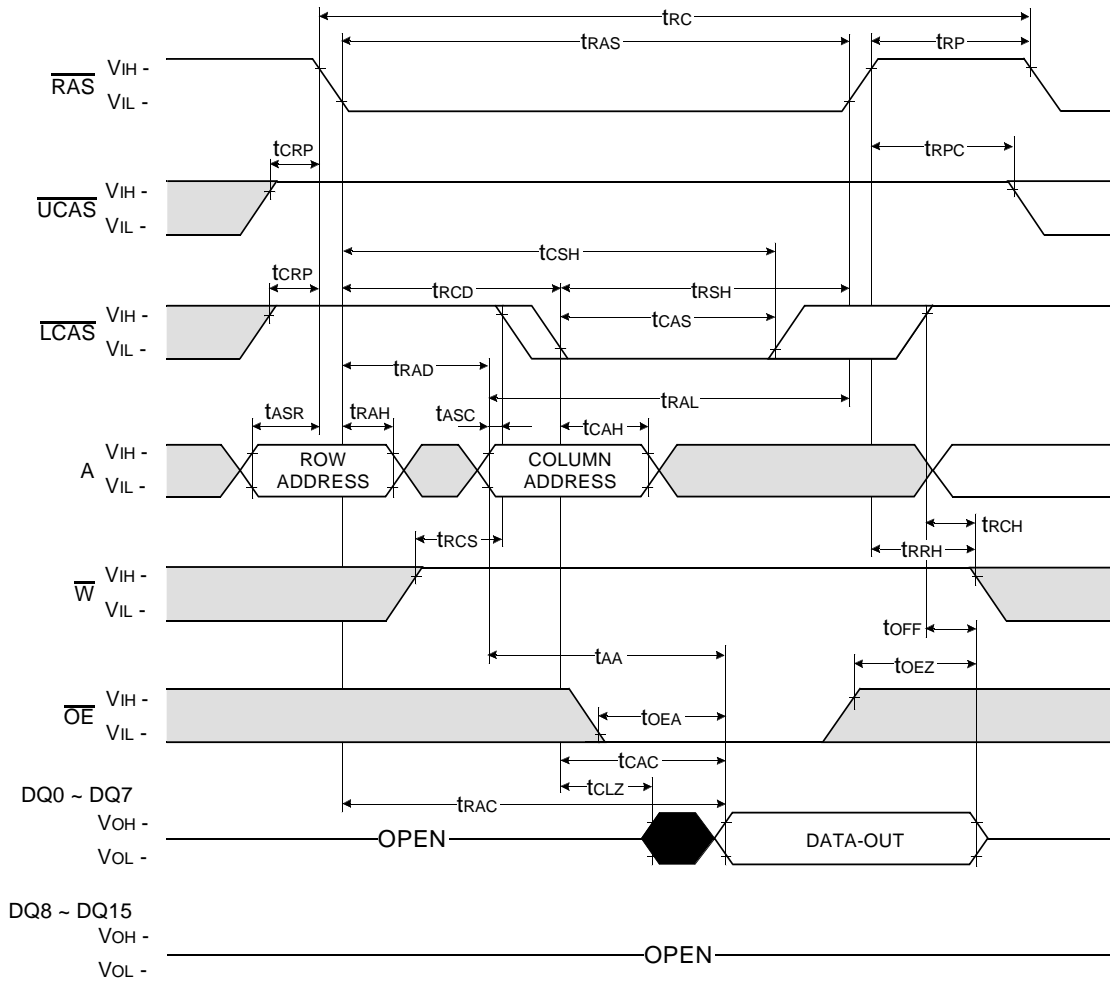
WORD READ CYCLE



Don't care  
 Undefined

LOWER BYTE READ CYCLE

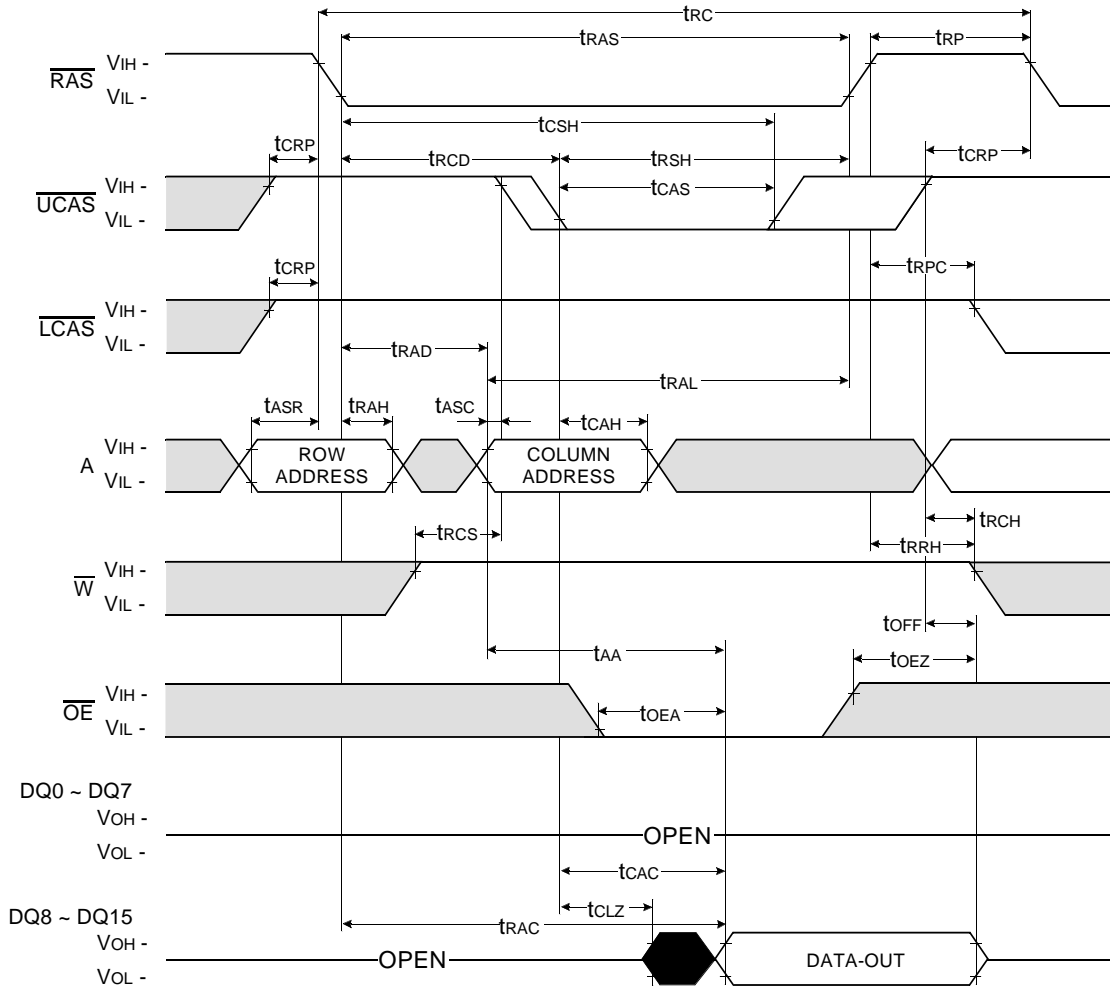
NOTE : DIN = OPEN



Don't care  
 Undefined

UPPER BYTE READ CYCLE

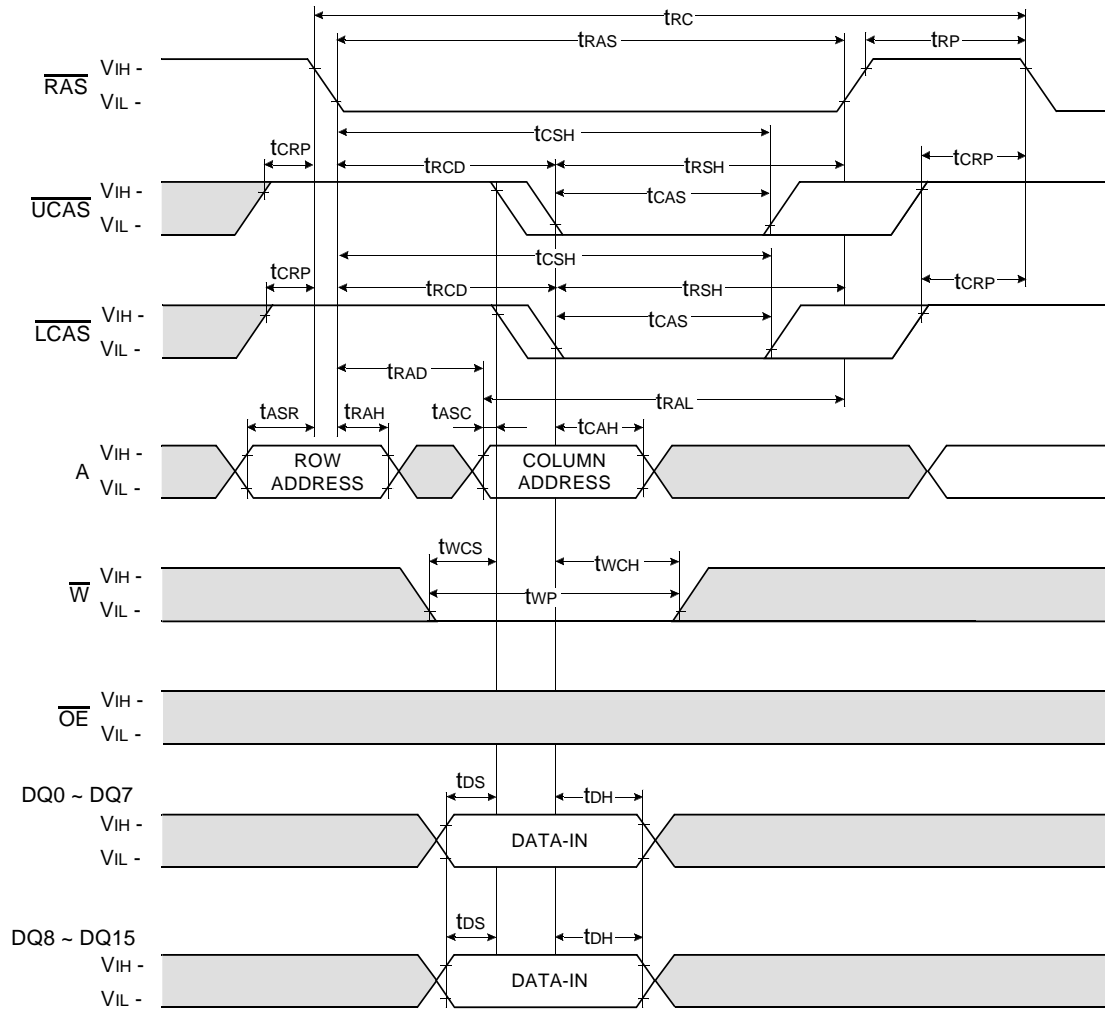
NOTE : DIN = OPEN



Don't care  
 Undefined

WORD WRITE CYCLE ( EARLY WRITE )

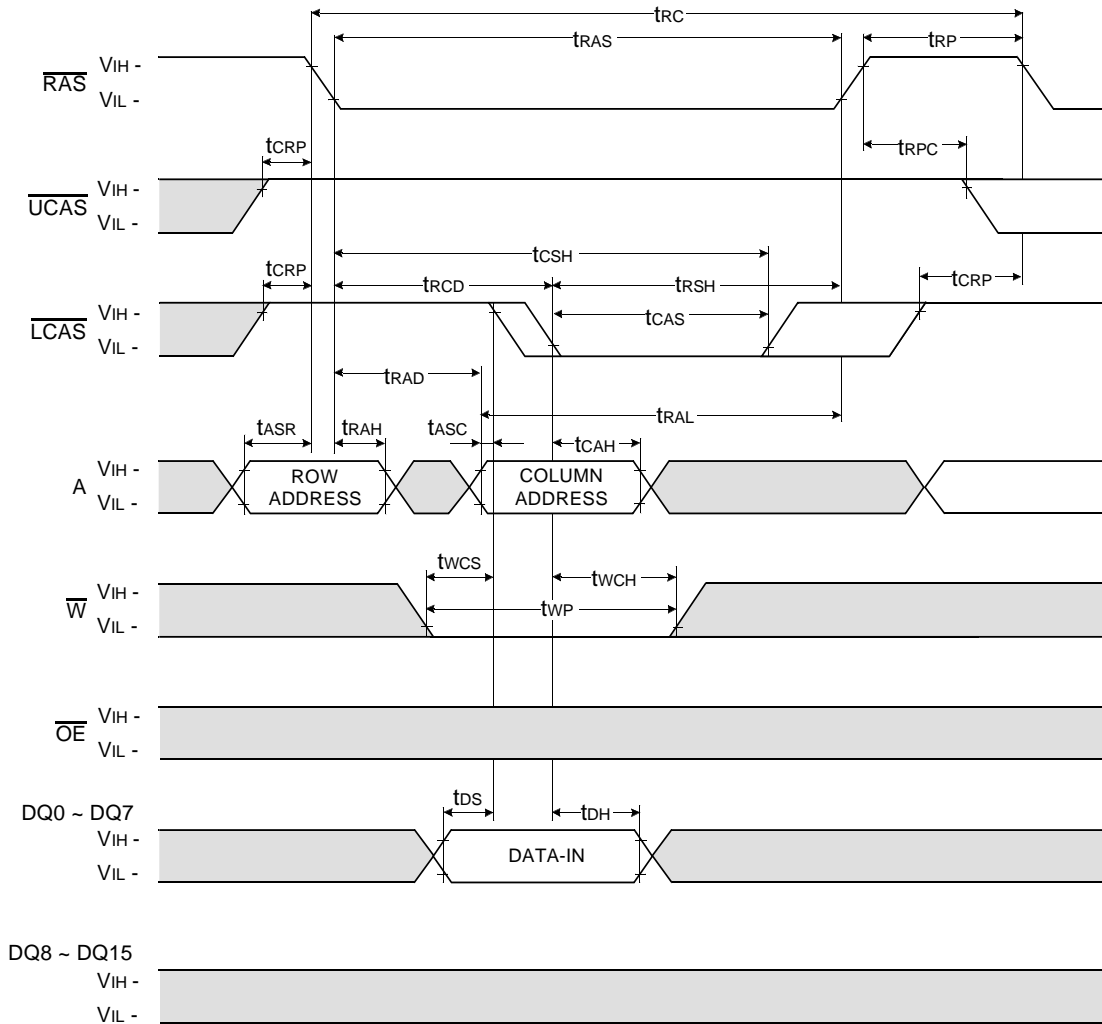
NOTE : DOUT = OPEN



Don't care  
 Undefined

LOWER BYTE WRITE CYCLE ( EARLY WRITE )

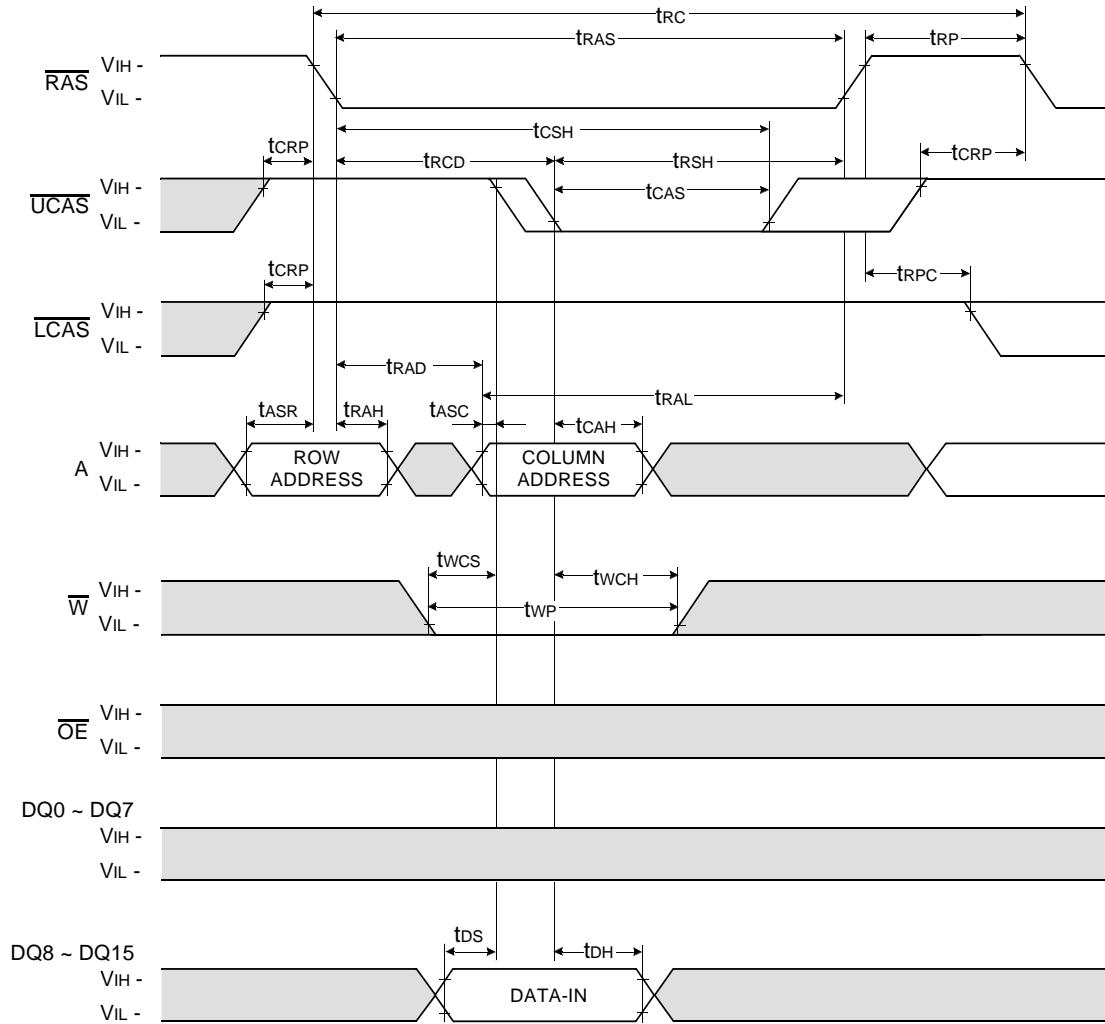
NOTE : DOUT = OPEN



□ Don't care  
■ Undefined

UPPER BYTE WRITE CYCLE ( EARLY WRITE )

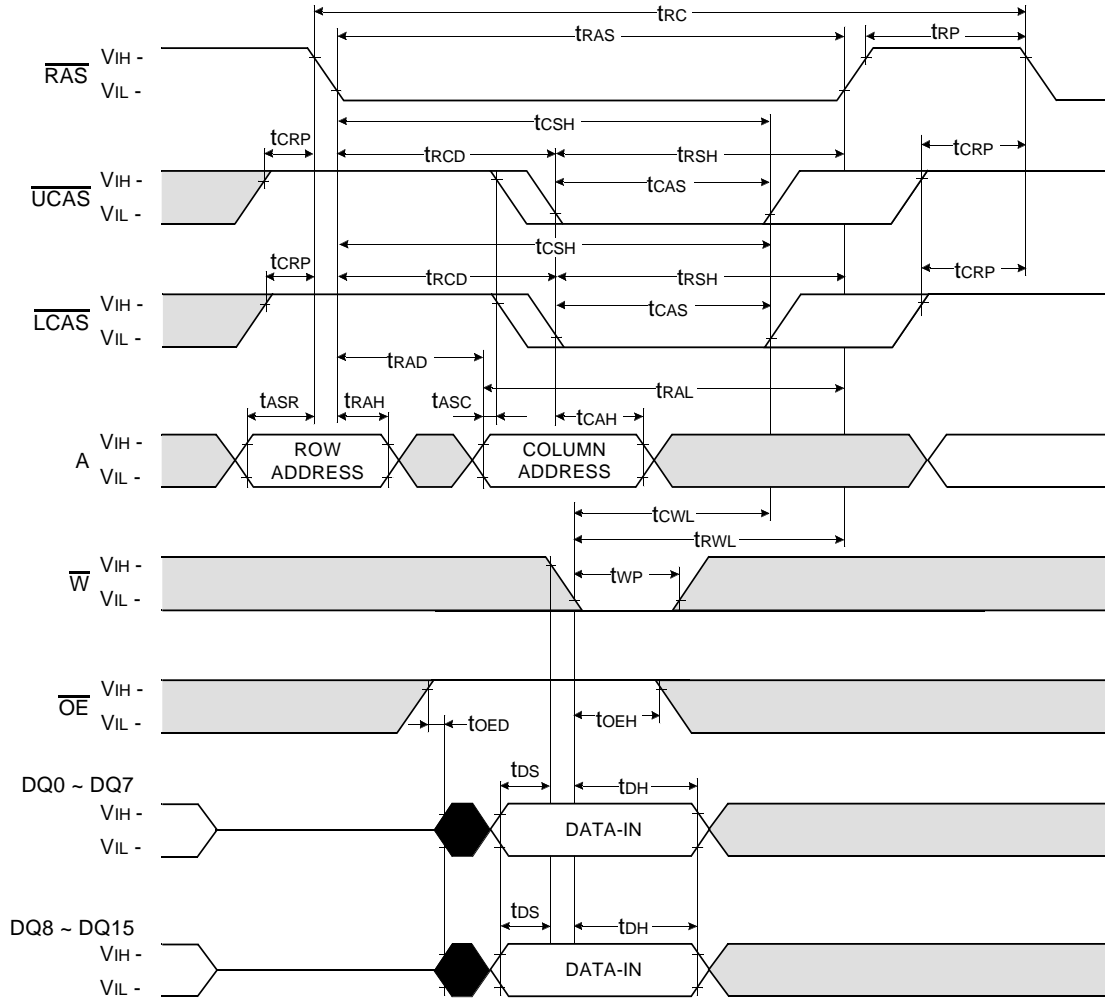
NOTE : DOUT = OPEN



Don't care  
 Undefined

WORD WRITE CYCLE (  $\overline{OE}$  CONTROLLED WRITE )

NOTE : DOUT = OPEN

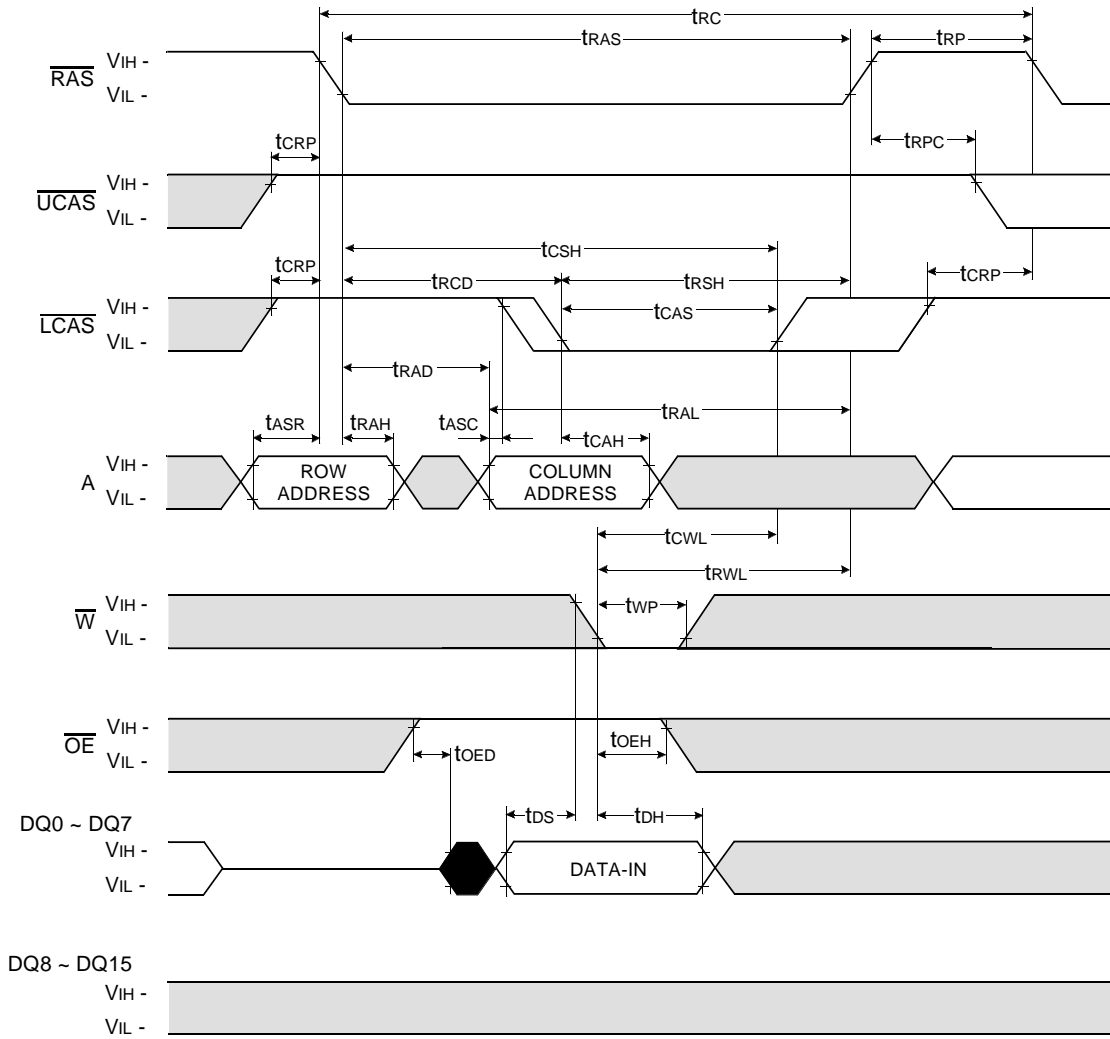


Don't care  
 Undefined



LOWER BYTE WRITE CYCLE (  $\overline{OE}$  CONTROLLED WRITE )

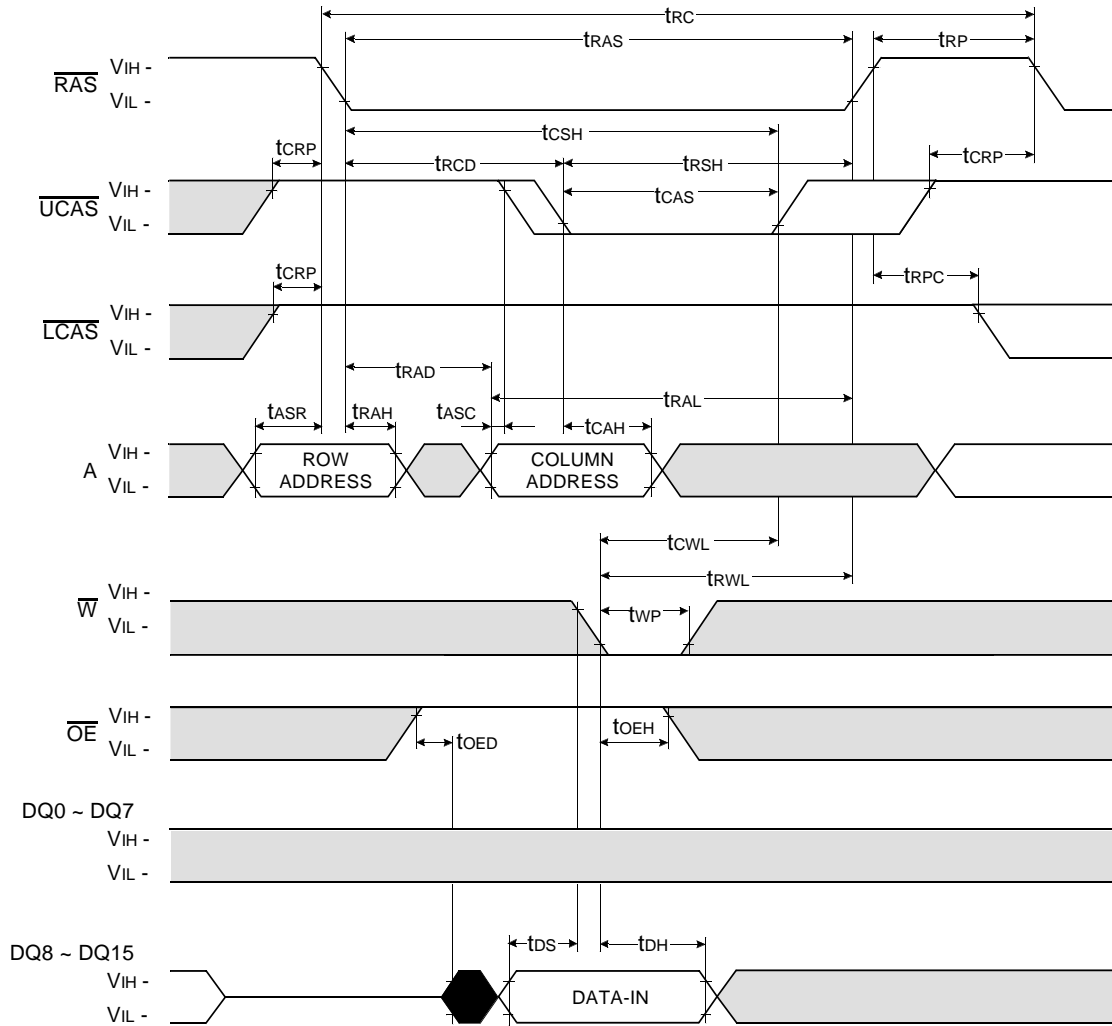
NOTE : DOUT = OPEN



Don't care  
 Undefined

UPPER BYTE WRITE CYCLE (  $\overline{OE}$  CONTROLLED WRITE )

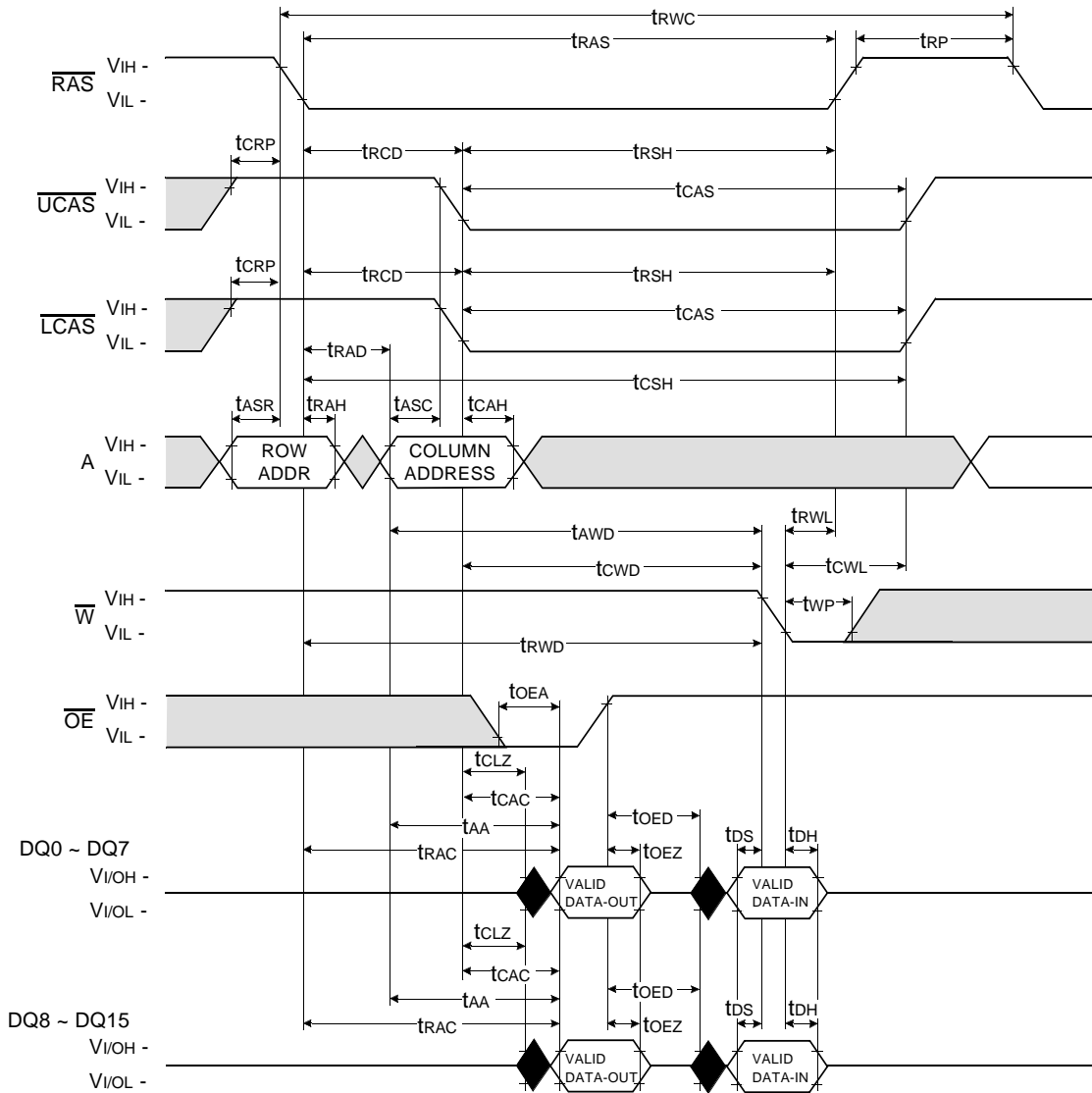
NOTE : DOUT = OPEN



Don't care

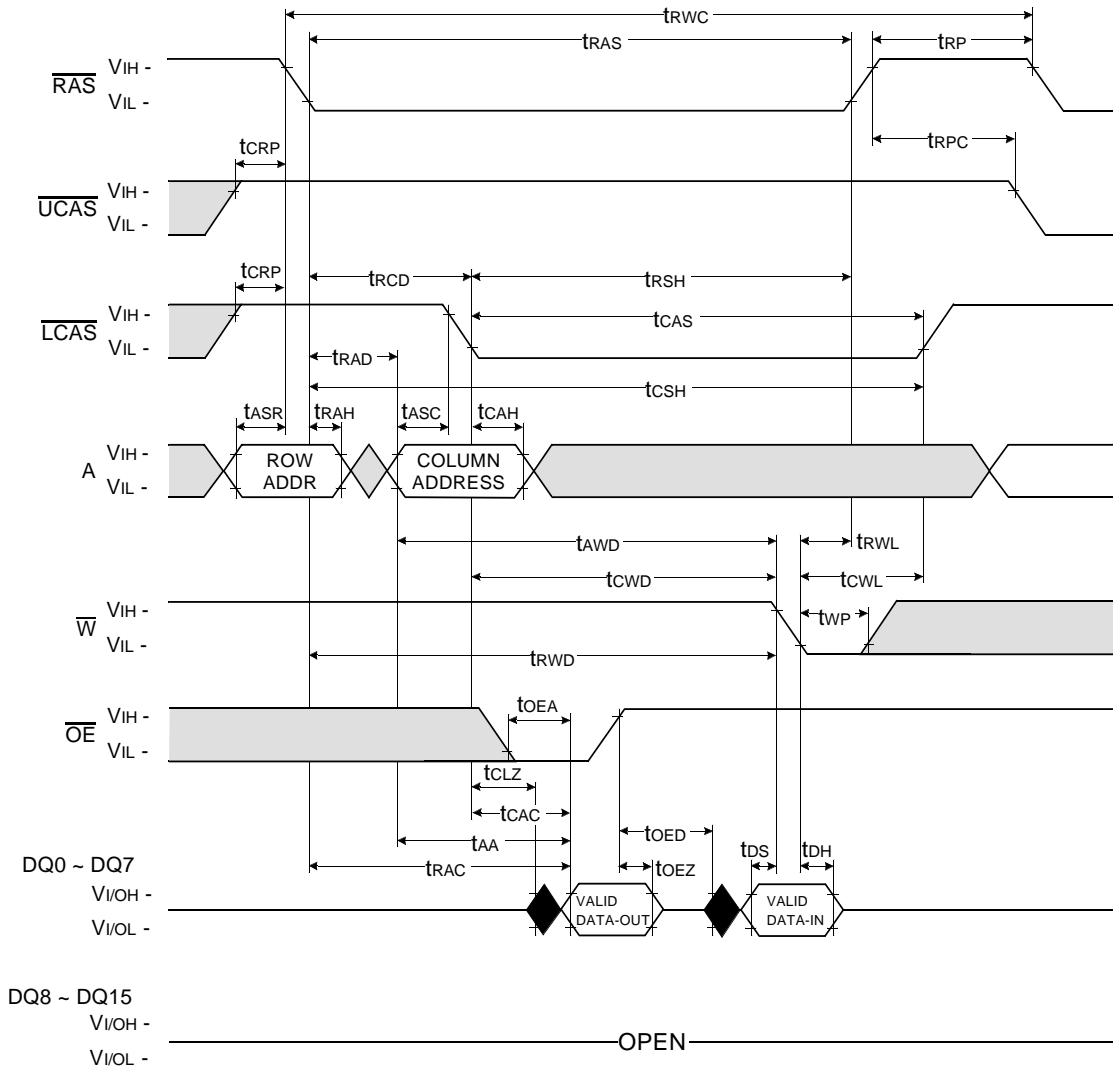
Undefined

WORD READ - MODIFY - WRITE CYCLE



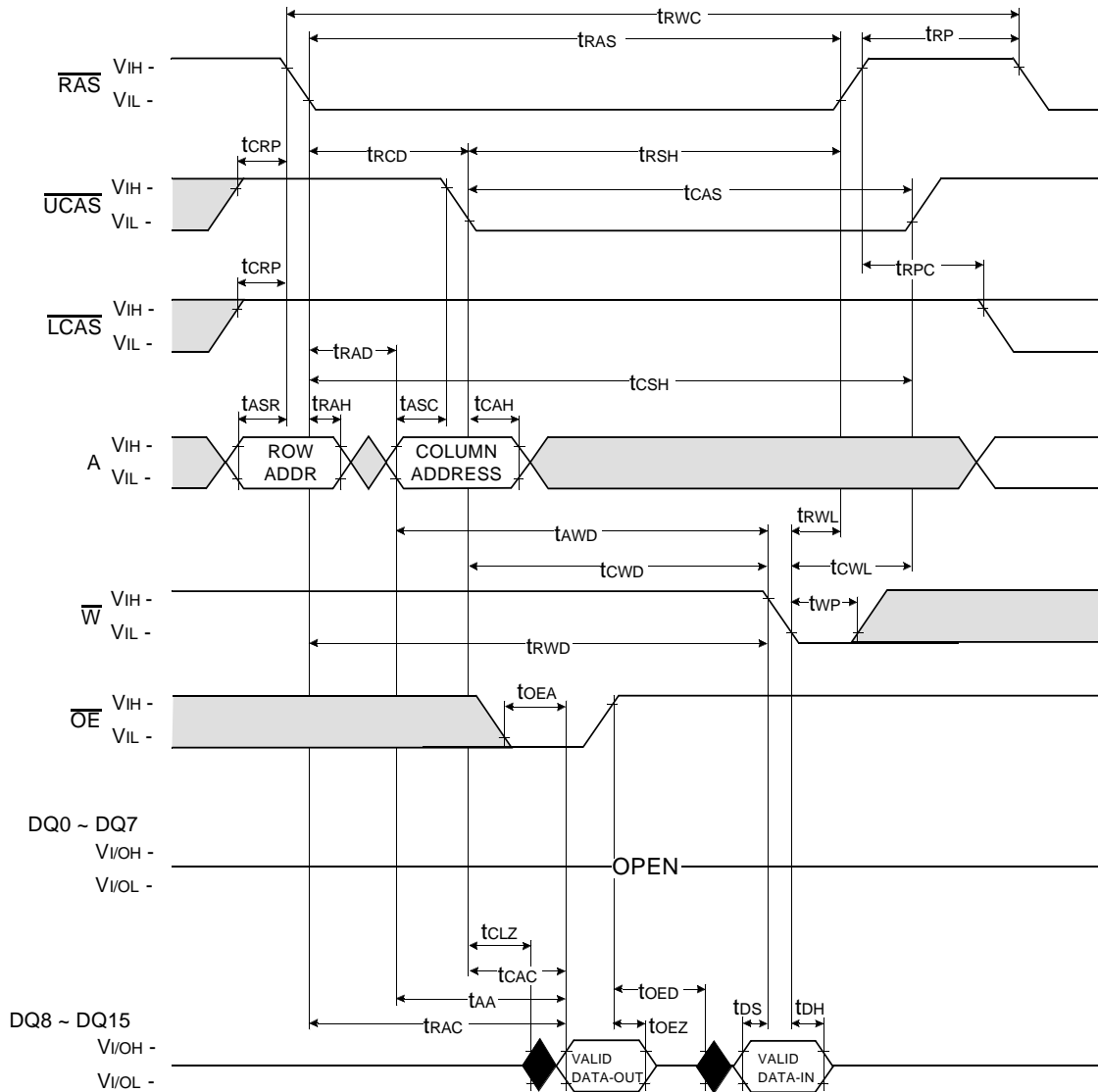
Don't care  
 Undefined

LOWER-BYTE READ - MODIFY - WRITE CYCLE



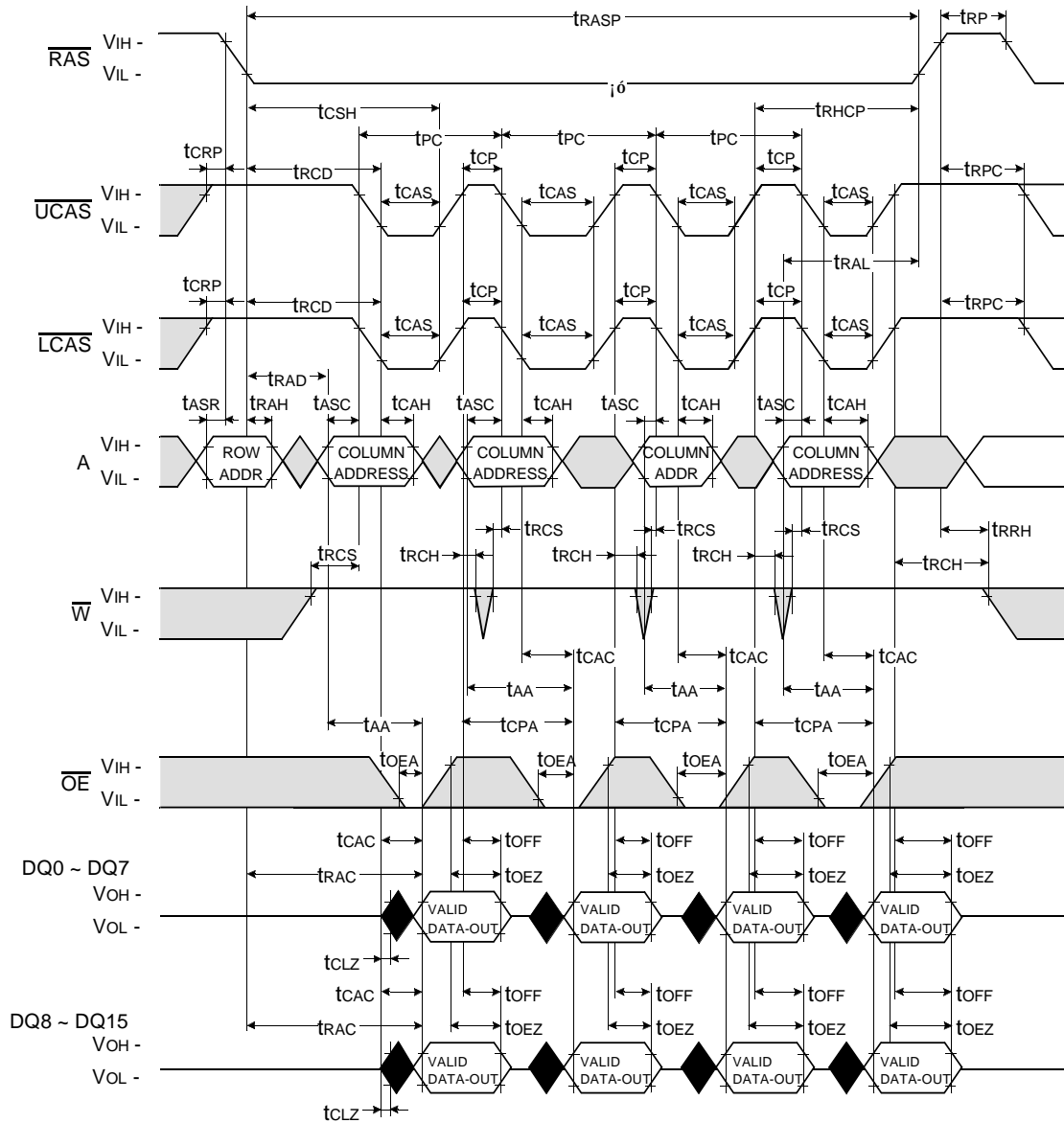
Don't care  
 Undefined

UPPER-BYTE READ - MODIFY - WRITE CYCLE



Don't care  
 Undefined

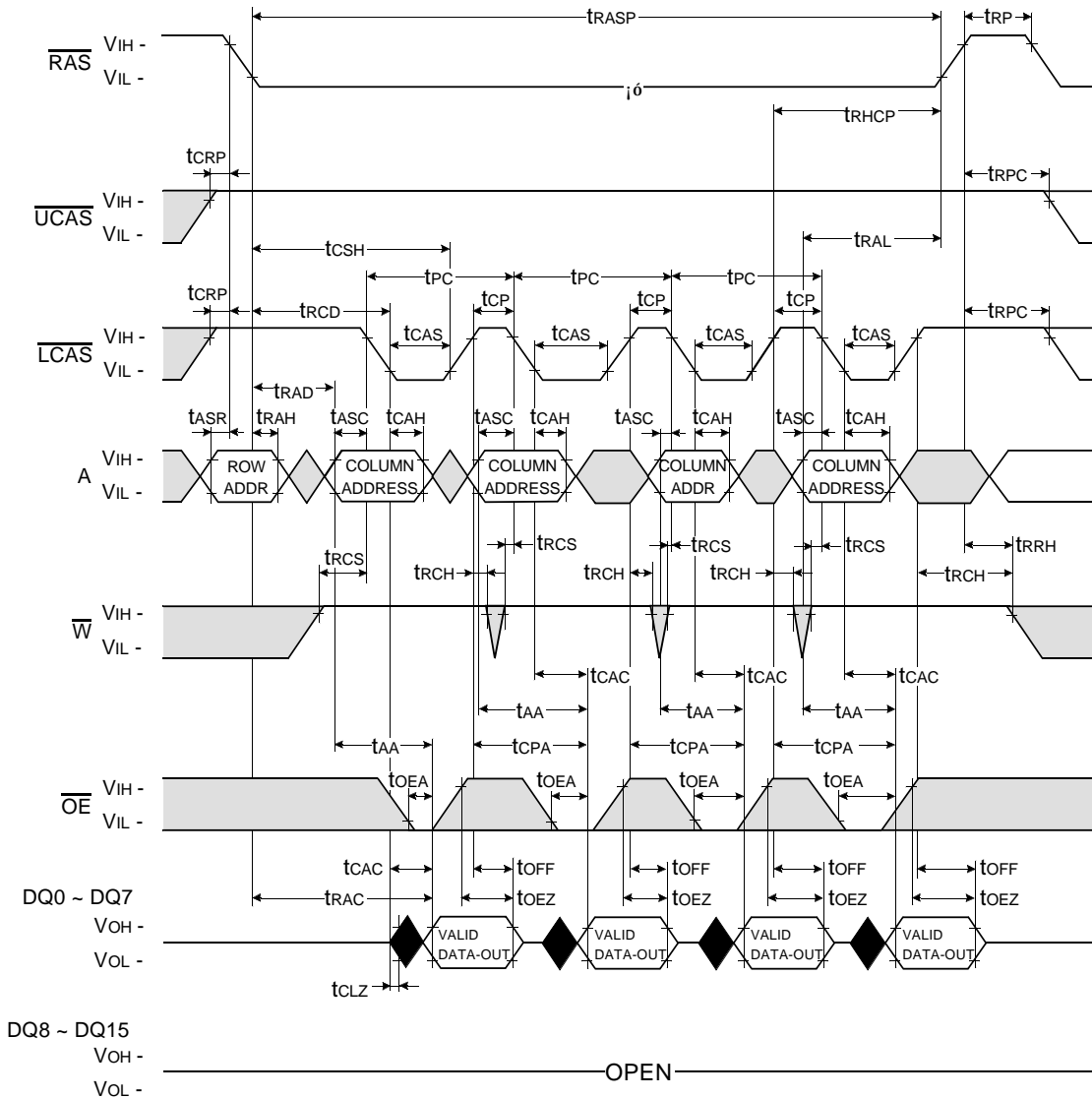
FAST PAGE MODE WORD READ CYCLE



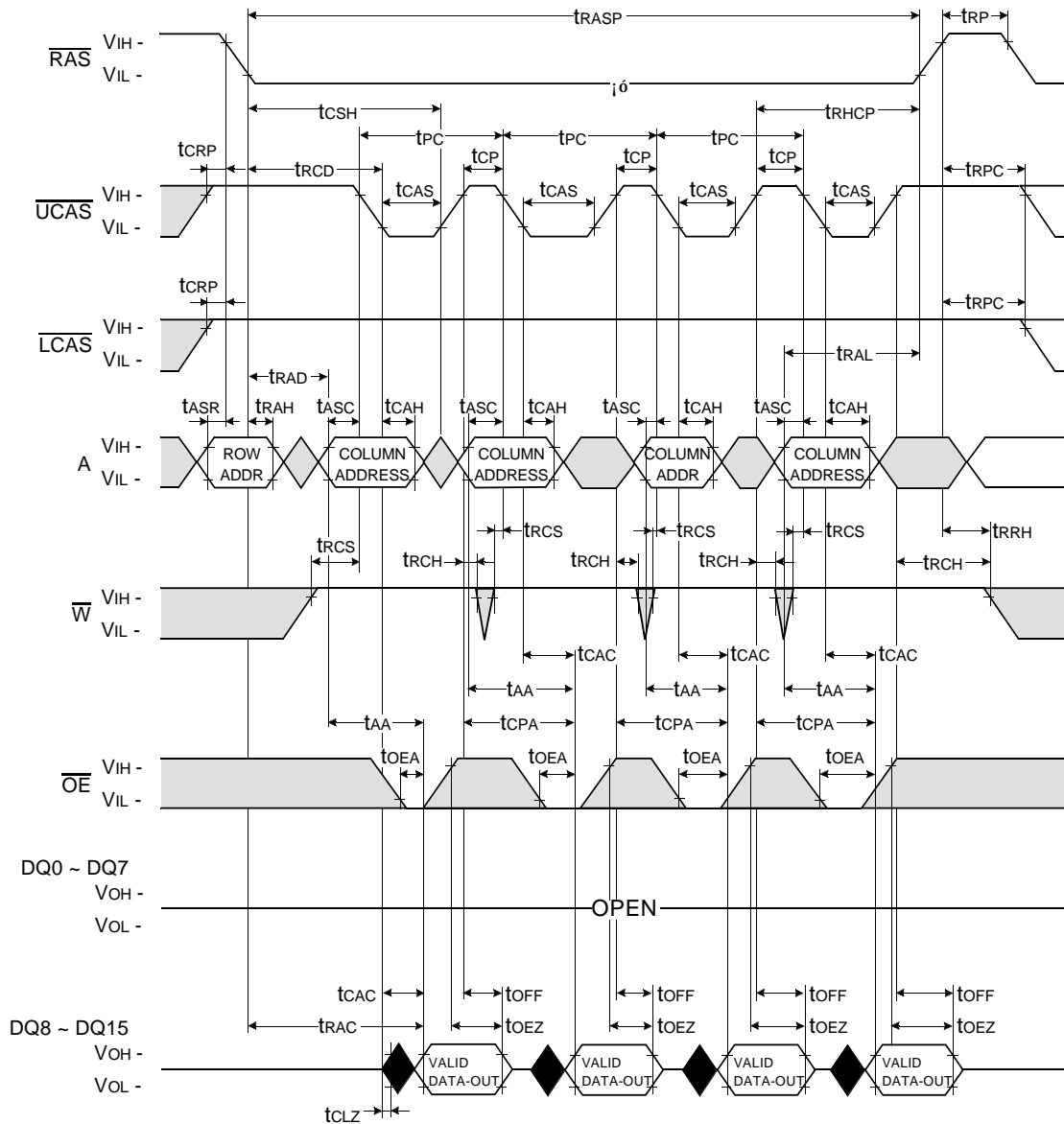
Don't care  
Undefined



FAST PAGE MODE LOWER BYTE READ CYCLE



FAST PAGE MODE UPPER BYTE READ CYCLE



Don't care  
 Undefined

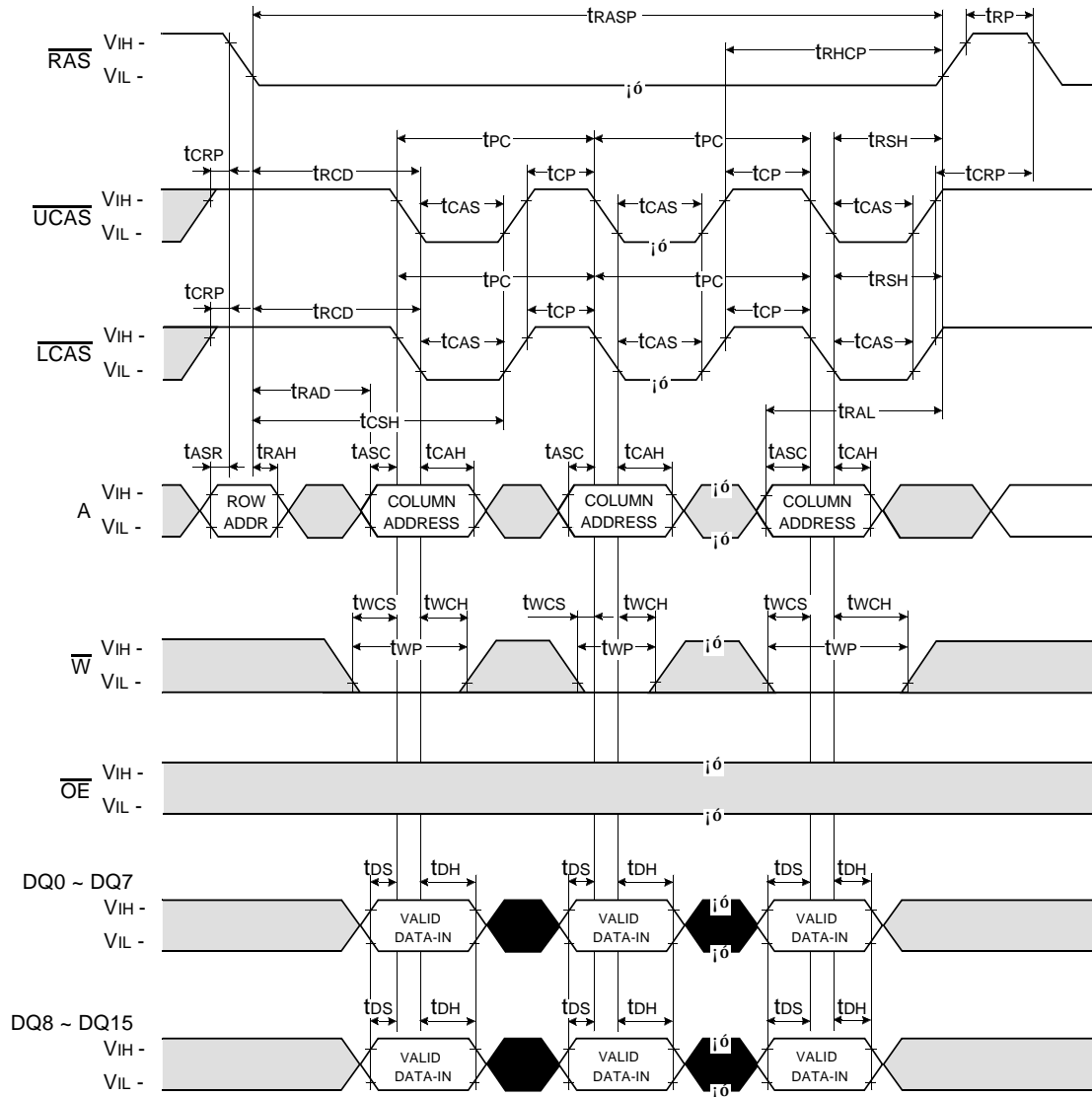


ELECTRONICS



FAST PAGE MODE WORD WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN



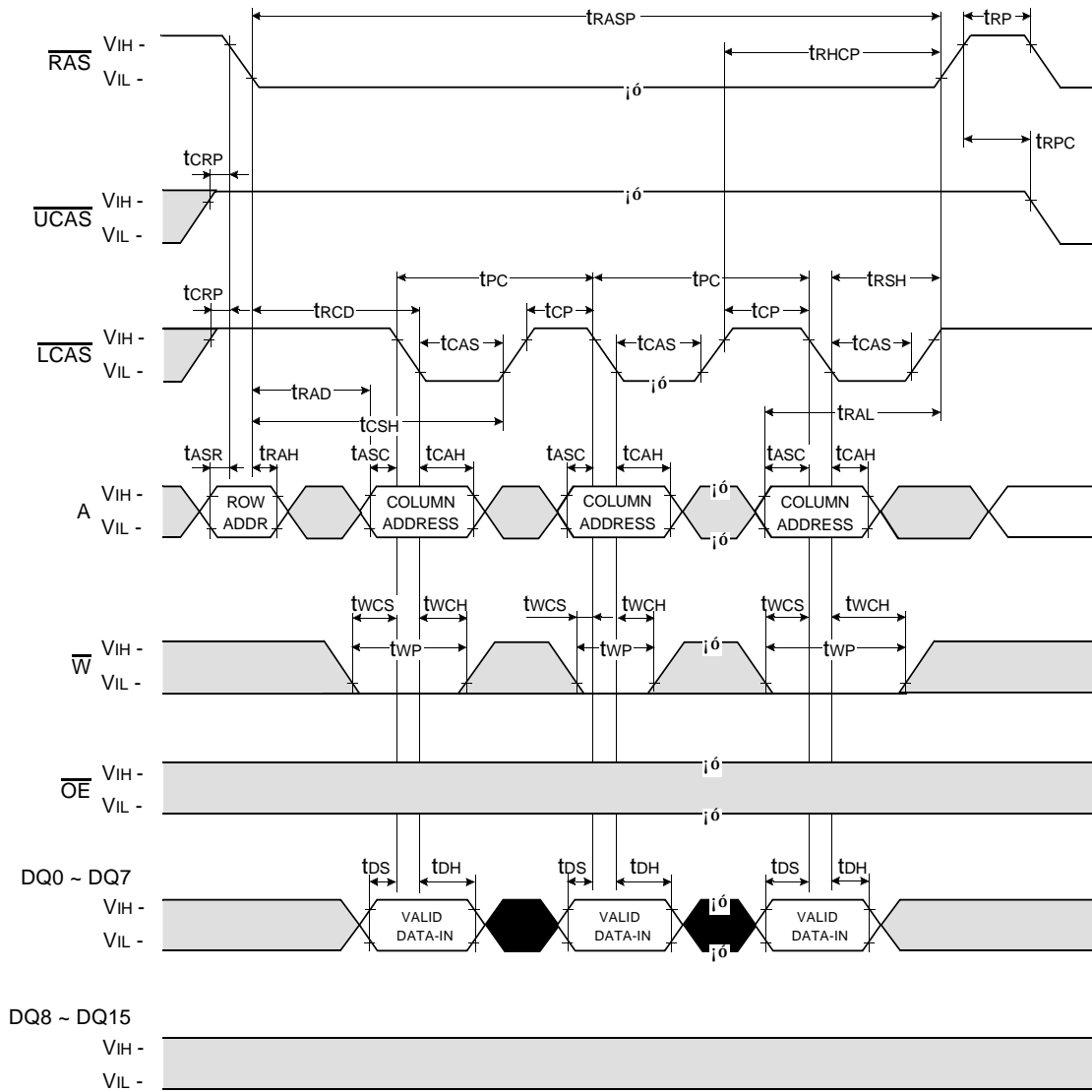
□ Don't care  
 ■ Undefined



ELECTRONICS

**FAST PAGE MODE LOWER BYTE WRITE CYCLE ( EARLY WRITE )**

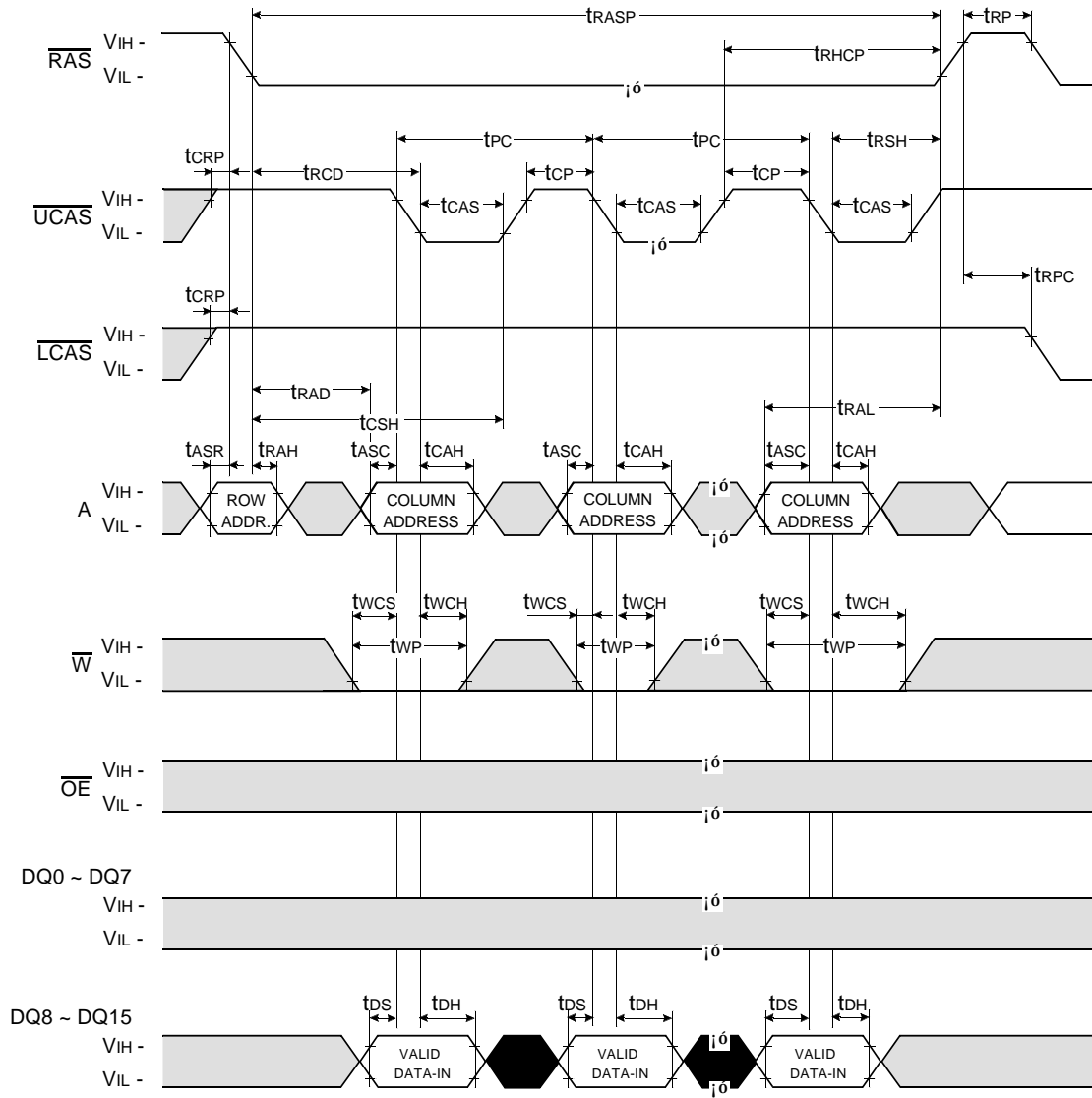
NOTE : DOUT = OPEN



Don't care  
 Undefined

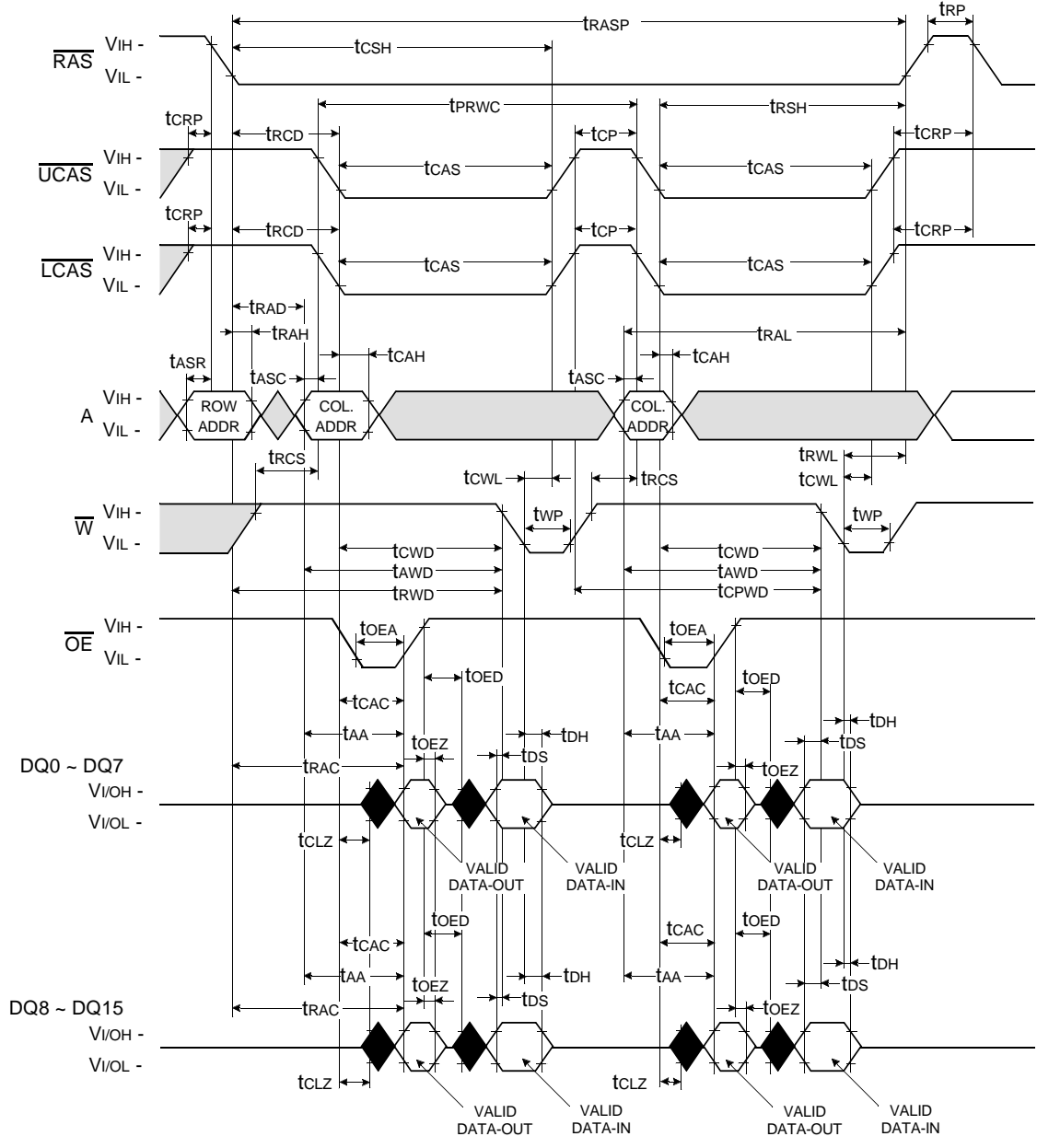
FAST PAGE MODE UPPER BYTE WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN



□ Don't care  
 ■ Undefined

FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

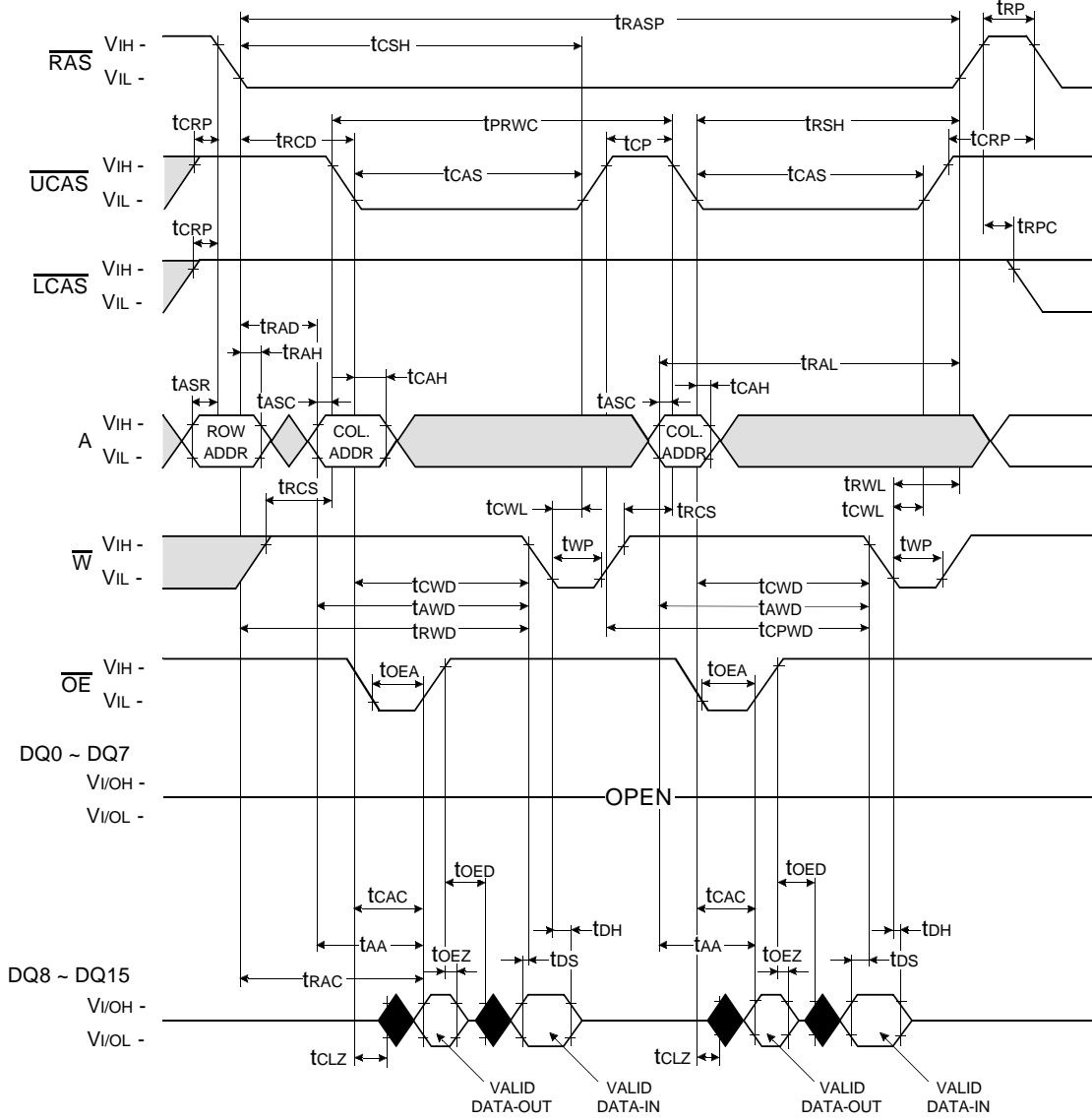


- Don't care
- Undefined





FAST PAGE MODE UPPER BYTE READ - MODIFY - WRITE CYCLE

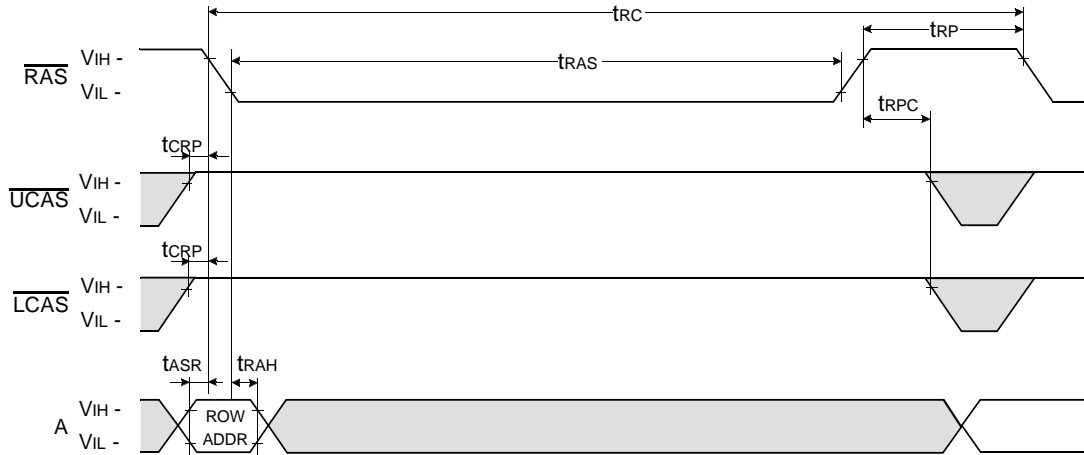


Don't care  
 Undefined

**$\overline{\text{RAS}}$  - ONLY REFRESH CYCLE**

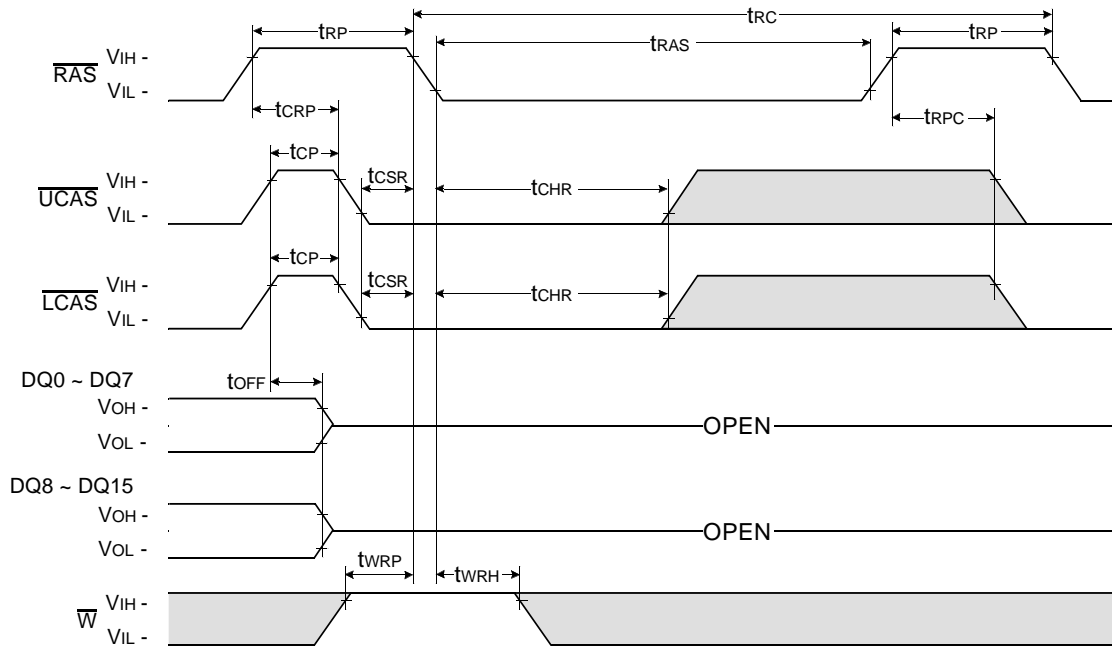
NOTE :  $\overline{\text{W}}$ ,  $\overline{\text{OE}}$ ,  $\text{DIN}$  = Don't care

$\text{DOUT}$  = OPEN



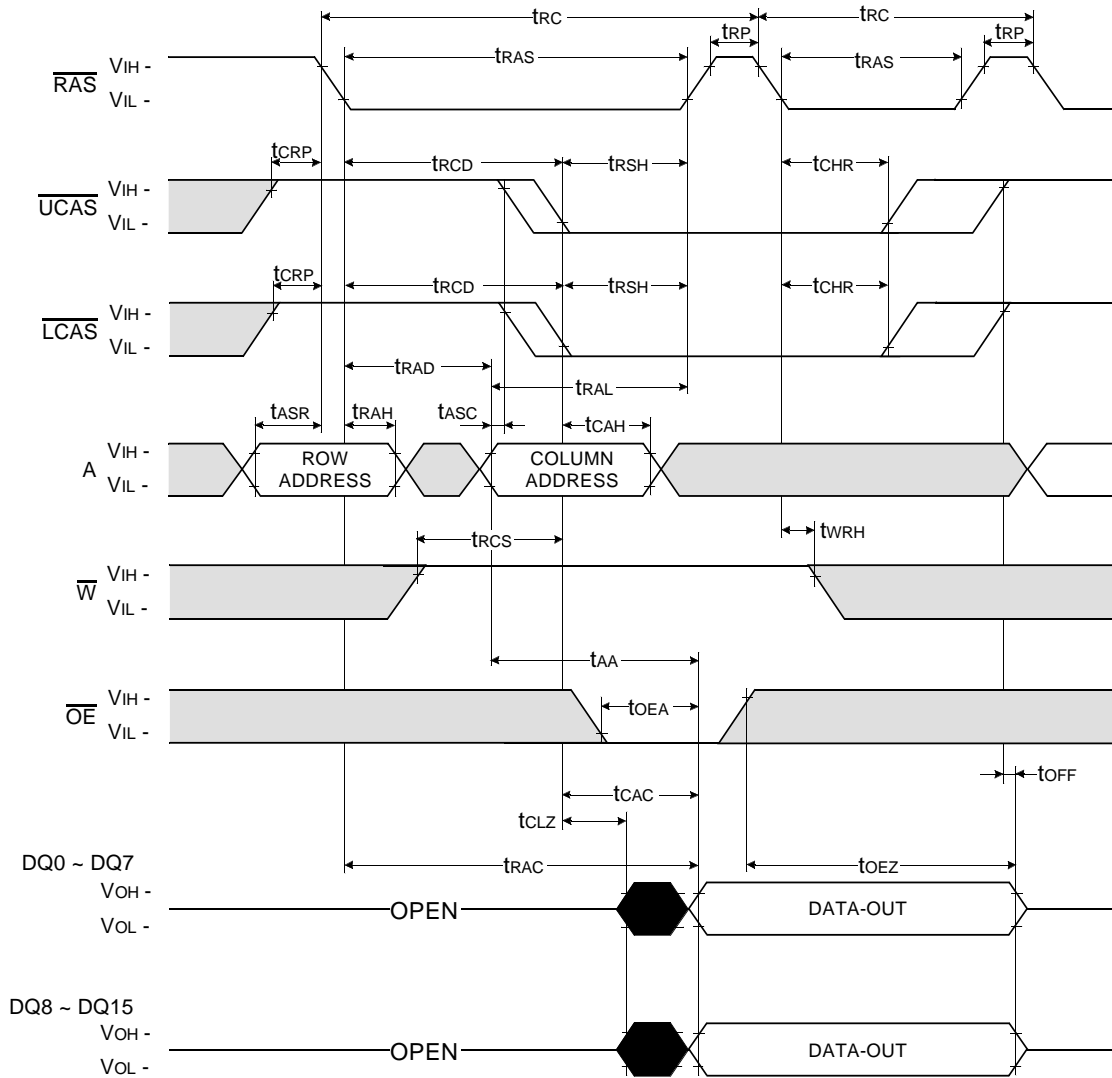
**$\overline{\text{CAS}}$  - BEFORE -  $\overline{\text{RAS}}$  REFRESH CYCLE**

NOTE :  $\overline{\text{OE}}$ ,  $\text{A}$  = Don't care



□ Don't care  
 ■ Undefined

HIDDEN REFRESH CYCLE ( READ )

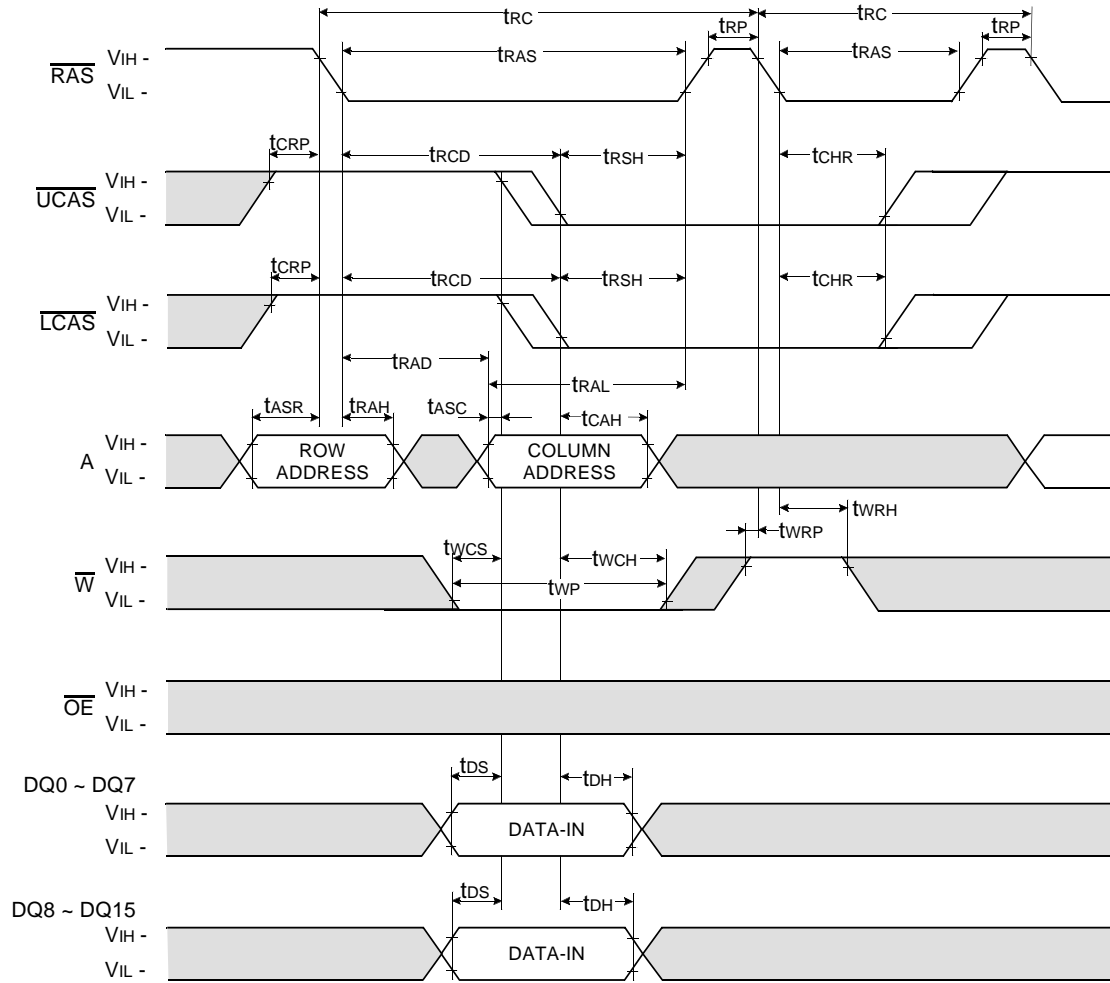


Don't care  
 Undefined



HIDDEN REFRESH CYCLE ( WRITE )

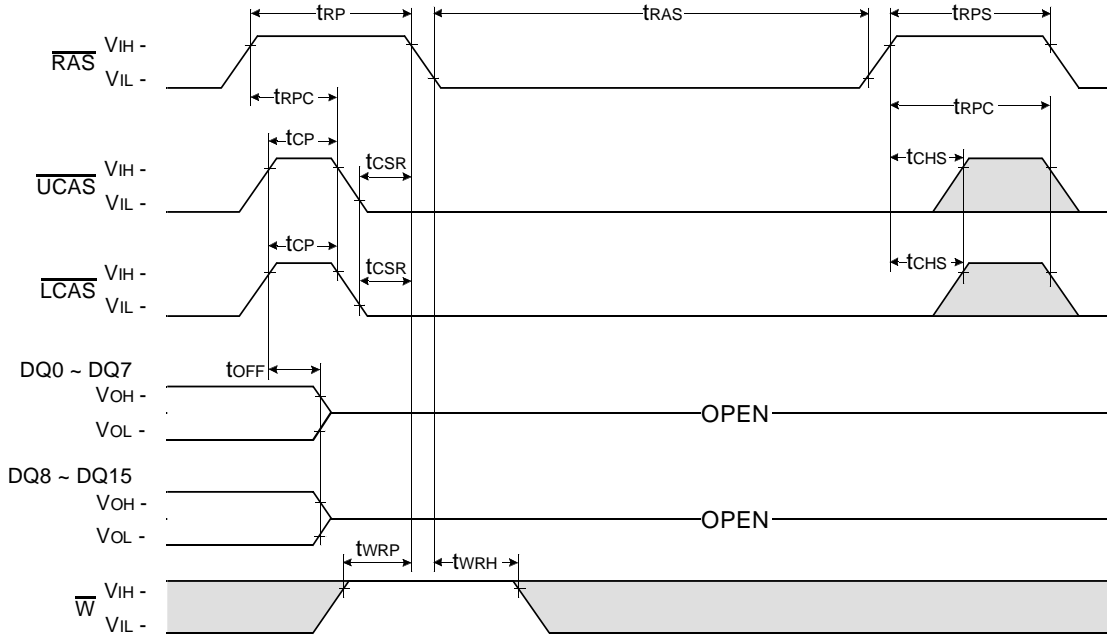
NOTE : DOUT = OPEN



Don't care  
 Undefined

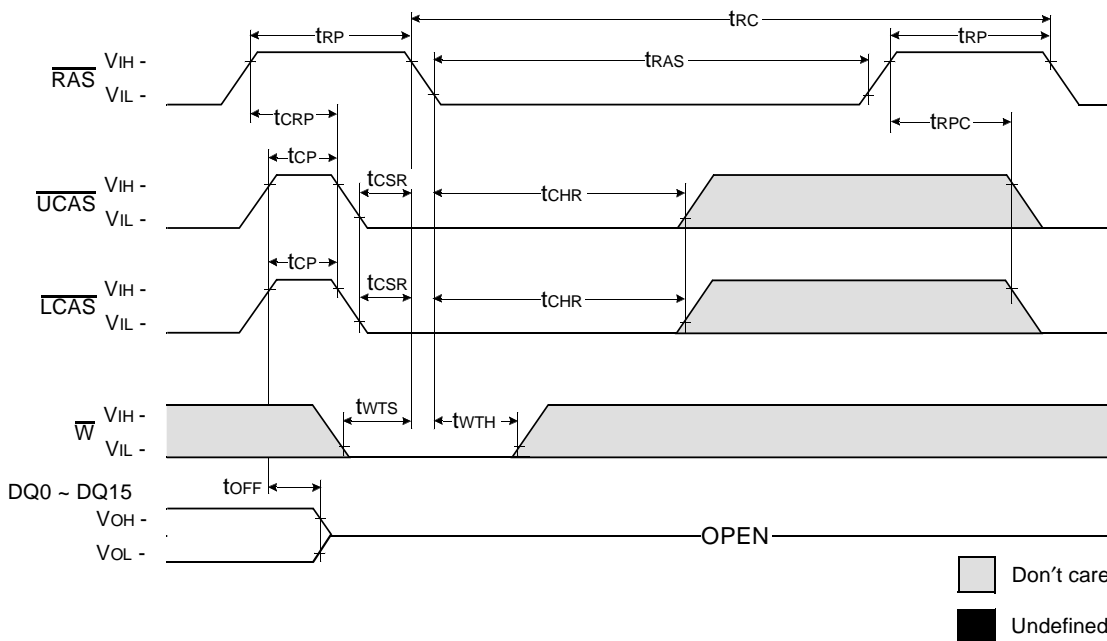
**$\overline{\text{CAS}}$  - BEFORE -  $\overline{\text{RAS}}$  SELF REFRESH CYCLE**

NOTE :  $\overline{\text{OE}}$ , A = Don't care



**TEST MODE IN CYCLE**

NOTE :  $\overline{\text{OE}}$ , A = Don't care



Don't care  
 Undefined

PACKAGE DIMENSION

