3.3 V, Full Duplex, 840 μA 20 Mbps, EIA RS-485 Transceiver

ADM3491

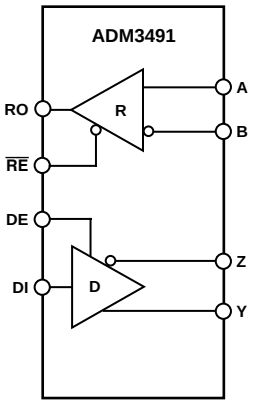
FEATURES

Operates with +3.3 V Supply
EIA RS-422 and RS-485 Compliant Over Full CM Range
19 kΩ Input Impedance
Up to 50 Transceivers on Bus
20 Mbps Data Rate
Short Circuit Protection
Specified Over Full Temperature Range
Thermal Shutdown
Interoperable with 5 V Logic
840 μA Supply Current
2 nA Shutdown Current
Also Available in TSSOP Package
Meets IEC1000-4-4 (>1 kV)
8 ns Skew
Upgrade for MAX 3491, SN75ALS180

APPLICATIONS

Telecommunications
DTE-DCE Interface
Packet Switching
Local Area Networks
Data Concentration
Data Multiplexers
Integrated Services Digital Network (ISDN)
AppleTalk
Industrial Controls

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADM3491 is a low power differential line transceiver designed to operate using a single +3.3 V power supply. Low power consumption coupled with a shutdown mode make it ideal for power sensitive applications. It is suitable for communication on multipoint bus transmission lines.

It is intended for balanced data transmission and complies with both EIA Standards RS-485 and RS-422. It contains a differential line driver and a differential line receiver, making it suitable for full duplex data transfer.

The input impedance is 19 kΩ allowing up to 50 transceivers to be connected on the bus.

Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit. This feature forces the driver output into a high impedance state if, during fault conditions, a significant temperature increase is detected in the internal driver circuitry.

The receiver contains a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating).

The ADM3491 is fabricated on BiCMOS, an advanced mixed technology process combining low power CMOS with fast switching bipolar technology.

The ADM3491 is fully specified over the industrial temperature range and is available in DIP and SOIC packages as well as a new space saving TSSOP package.

REV. 0

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ADM3491—SPECIFICATIONS (V_{CC} = +3.3 V ± 0.3 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
DRIVER					
Differential Output Voltage, V_{OD}	2.0			V	R_L = 100 Ω, Figure 1, V_{CC} > 3.1 V
	1.5			V	R_L = 54 Ω, Figure 1
	1.5			V	R_L = 60 Ω, Figure 2, –7 V < V_{TST} < +12 V
$\Delta\|V_{OD}\|$ for Complementary Output States			0.2	V	R = 54 Ω or 100 Ω, Figure 1
Common-Mode Output Voltage V_{OC}			3	V	R = 54 Ω or 100 Ω, Figure 1
$\Delta\|V_{OC}\|$ for Complementary Output States			0.2	V	R = 54 Ω or 100 Ω, Figure 1
CMOS Input Logic Threshold Low, V_{INL}			0.8	V	
CMOS Input Logic Threshold High, V_{INH}	2.0			V	
Logic Input Current (DE, DI, RE)			±1.0	µA	
Output Leakage (Y, Z) Current			±3	µA	V_O = –7 V or +12 V, V_{CC} = 0 V or 3.6 V
Output Short Circuit Current			±250	mA	V_O = –7 V or +12 V
RECEIVER					
Differential Input Threshold Voltage, V_{TH}	–0.2		+0.2	V	–7 V < V_{CM} < +12 V
Input Voltage Hysteresis, ΔV_{TH}		50		mV	V_{CM} = 0 V
Input Resistance	12	19		kΩ	–7 V < V_{CM} < +12 V
Input Current (A, B)			+1	mA	V_{IN} = +12 V
			–0.8	mA	V_{IN} = –7 V
Logic Enable Input Current ($\overline{RE}$)			±1	µA	
Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = +2.5 mA
Output Voltage High, V_{OH}	V_{CC} –0.4 V			V	I_{OUT} = –1.5 mA
Short Circuit Output Current			±60	mA	V_{OUT} = GND or V_{CC}
Three-State Output Leakage Current			±1.0	µA	V_{CC} = 3.6 V, 0 V < V_{OUT} < V_{CC}
POWER SUPPLY CURRENT					
I_{CC}					Outputs Unloaded,
		0.84	1.2	mA	DE = V_{CC}, $\overline{RE}$ = 0 V
		0.84	1.2	mA	DE = 0 V, $\overline{RE}$ = 0 V
Supply Current in Shutdown		0.002	1	µA	DE = 0 V, $\overline{RE}$ = V_{CC}

Specifications subject to change without notice.

TIMING SPECIFICATIONS (V_{CC} = +3.3 V, T_A = +25°C)

Parameter	Min	Typ	Max	Units	Test Conditions/ Comments
DRIVER					
Differential Output Delay T_{DD}	1		35	ns	R_L = 60 Ω, C_{L1} = C_{L2} = 15 pF, Figure 5
Differential Output Transition Time	1	8	15	ns	R_L = 60 Ω, C_{L1} = C_{L2} = 15 pF, Figure 5
Propagation Delay Input to Output T_{PLH}, T_{PHL}	7	22	35	ns	R_L = 27 Ω, C_{L1} = C_{L2} = 15 pF, Figure 6
Driver O/P to O/P T_{SKEW}			8	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 15 pF, Figure 6
ENABLE/DISABLE					
Driver Enable to Output Valid		45	90	ns	R_L = 110 Ω, C_L = 50 pF, Figure 3
Driver Disable Timing		40	80	ns	R_L = 110 Ω, C_L = 50 pF, Figure 3
Driver Enable from Shutdown		650	110	ns	R_L = 110 Ω, C_L = 15 pF, Figure 3
RECEIVER					
Time to Shutdown	80	190	300	ns	
Propagation Delay Input to Output T_{PLH}, T_{PHL}	25	65	90	ns	C_L = 15 pF, Figure 8
Skew T_{PLH}–T_{PHL}			10	ns	C_L = 15 pF, Figure 8
Receiver Enable T_{EN}		25	50	ns	C_L = 15 pF, Figure 4
Receiver Disable T_{DEN}		25	45	ns	C_L = 15 pF, Figure 4
Receiver Enable from Shutdown			500	ns	C_L = 15 pF, Figure 4

TIMING SPECIFICATIONS (V_{CC} = +3.3 V ± 0.3 V, T_A = T_{MIN} to T_{MAX})

Parameter	Min	Typ	Max	Units	Test Conditions/ Comments
DRIVER					
Differential Output Delay T_{DD}	1		70	ns	R_L = 60 Ω, C_{L1} = C_{L2} = 15 pF, Figure 5
Differential Output Transition Time	2	8	15	ns	R_L = 60 Ω, C_{L1} = C_{L2} = 15 pF, Figure 5
Propagation Delay Input to Output T_{PLH}, T_{PHL}	7	22	70	ns	R_L = 27 Ω, C_{L1} = C_{L2} = 15 pF, Figure 6
Driver O/P to O/P T_{SKEW}			10	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 15 pF, Figure 6
ENABLE/DISABLE					
Driver Enable to Output Valid		45	110	ns	R_L = 110 Ω, C_L = 50 pF, Figure 3
Driver Disable Timing		40	110	ns	R_L = 110 Ω, C_L = 50 pF, Figure 3
Driver Enable from Shutdown		650	110	ns	R_L = 110 Ω, C_L = 15 pF, Figure 3
RECEIVER					
Time to Shutdown	50	190	500	ns	
Propagation Delay Input to Output T_{PLH}, T_{PHL}	25	65	115	ns	C_L = 15 pF, Figure 8
Skew T_{PLH}–T_{PHL}			20	ns	C_L = 15 pF, Figure 8
Receiver Enable T_{EN}		25	50	ns	C_L = 15 pF, Figure 4
Receiver Disable T_{DEN}		25	50	ns	C_L = 15 pF, Figure 4
Receiver Enable from Shutdown			600	ns	C_L = 15 pF, Figure 4

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{CC} . . . . . +7 V
Inputs
  Driver Input (DI) . . . . . –0.3 V to V_{CC} + 0.3 V
  Control Inputs (DE, $\overline{RE}$) . . . . . –0.3 V to V_{CC} + 0.3 V
  Receiver Inputs (A, B) . . . . . –7.5 V to +12.5 V
Outputs
  Driver Outputs . . . . . –7.5 V to +12.5 V
  Receiver Output . . . . . –0.5 V to V_{CC} +0.5 V
Power Dissipation 14-Lead DIP . . . . . 800 mW
  θ_{JA}, Thermal Impedance . . . . . 140°C/W
Power Dissipation 14-Lead SOIC . . . . . 650 mW
  θ_{JA}, Thermal Impedance . . . . . 115°C/W
Power Dissipation 16-Lead TSSOP . . . . . 500 mW
  θ_{JA}, Thermal Impedance . . . . . 158 °C/W
Operating Temperature Range
  Industrial (A Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
  Vapor Phase (60 sec) . . . . . +215°C
  Infrared (15 sec) . . . . . +220°C
ESD Rating . . . . . >2 kV
EFT Rating (IEC1000-4-4) . . . . . >1 kV

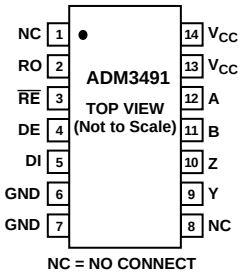
*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

ORDERING GUIDE

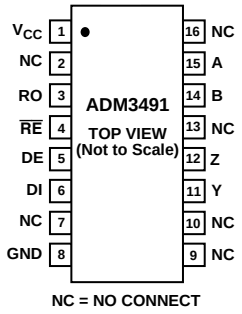
Model	Temperature Range	Package Description	Package Options
ADM3491AN	–40°C to +85°C	Plastic DIP	N-14
ADM3491AR	–40°C to +85°C	Small Outline (SOIC)	R-14
ADM3491ARU	–40°C to +85°C	Thin Shrink Small Outline (TSSOP)	RU-16

PIN CONFIGURATION

DIP/SOIC



TSSOP



PIN FUNCTION DESCRIPTIONS

Mnemonic Pin	DIP/ SOIC	TSSOP	Function
NC	1, 8	2, 7, 9, 10, 13, 16	No Connect.
RO	2	3	Receiver Output. High when A > B by 200 mV or Low when A < B by 200 mV.
$\overline{RE}$	3	4	Receiver Output Enable. With $\overline{RE}$ low, the receiver output RO is enabled. With $\overline{RE}$ high, the output goes high impedance. If $\overline{RE}$ is high and DE low, the ADM3491 enters a shutdown state.
DE	4	5	Driver Output Enable. A high level enables the driver differential outputs, Y and Z. A low level places it in a high impedance state.
DI	5	6	Driver Input. When the driver is enabled, a logic Low on DI forces Y low and Z high while a logic high on DI forces Y high and Z low.
GND	6, 7	8	Ground Connection, 0 V.
Y	9	11	Noninverting Driver Output Y.
Z	10	12	Inverting Driver Output Z.
B	11	14	Inverting Receiver Input B.
A	12	15	Noninverting Receiver Input A.
V_{CC}	13, 14	1	Power Supply, 3.3 V ± 0.3 V.

Test Circuits

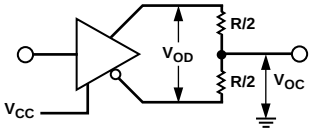


Figure 1. Driver Voltage Measurement Test Circuit

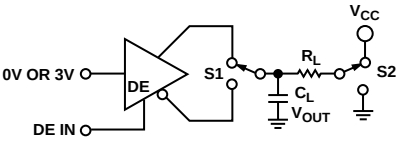


Figure 2. Driver Enable/Disable Test Circuit

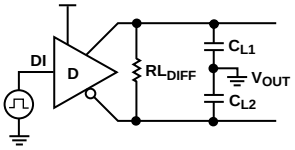


Figure 3. Driver Differential Output Delay Test Circuit

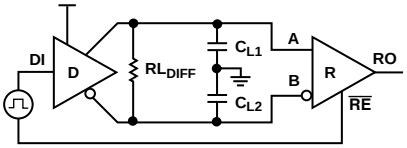


Figure 4. Driver/Receiver Propagation Delay Test Circuit

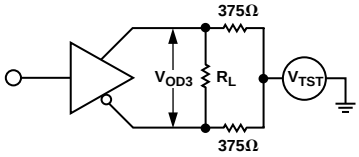


Figure 5. Driver Voltage Measurement Test Circuit 2

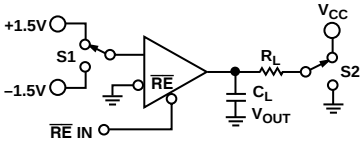


Figure 6. Receiver Enable/Disable Test Circuit

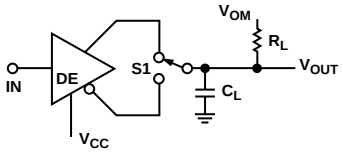


Figure 7. Driver Propagation Delay Test Circuit

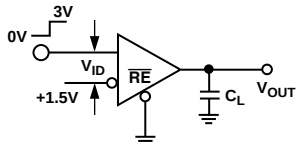


Figure 8. Receiver Propagation Delay Test Circuit

Switching Characteristics

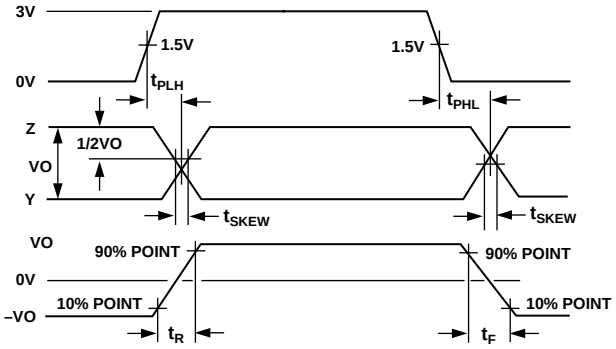


Figure 9. Driver Propagation Delay, Rise/Fall Timing

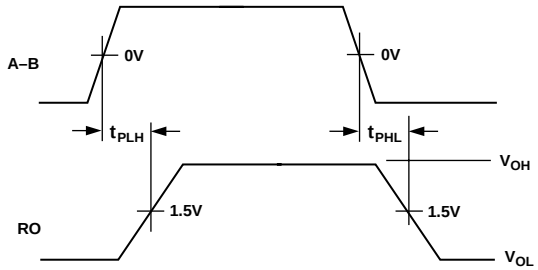


Figure 10. Receiver Propagation Delay

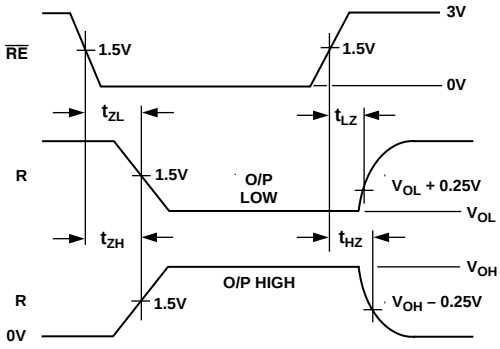


Figure 11. Driver Enable/Disable Timing

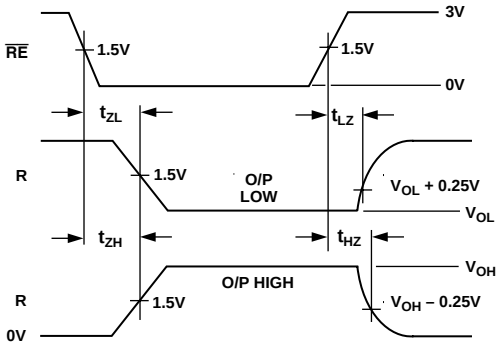


Figure 12. Receiver Enable/Disable Timing

ADM3491–Typical Performance Characteristics

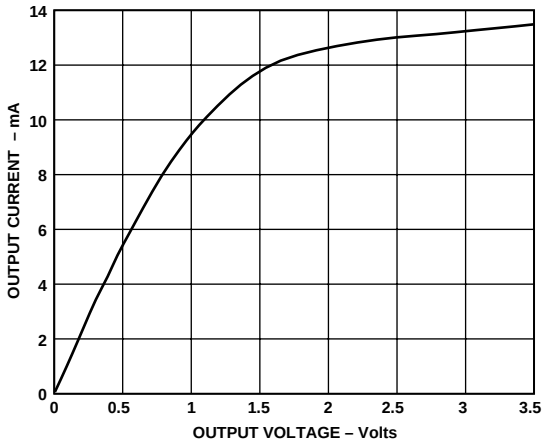


Figure 13. Receiver Output Low Voltage vs. Output Current

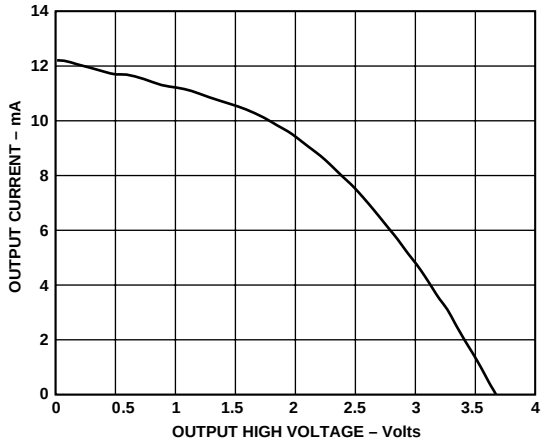


Figure 16. Receiver Output High Voltage vs. Output Current

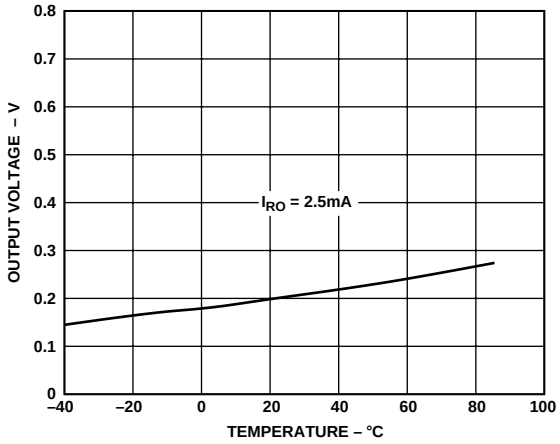


Figure 14. Receiver Output Low Voltage vs. Temperature

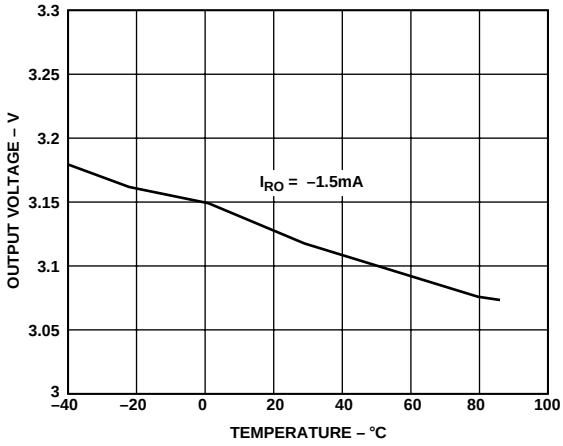


Figure 17. Receiver Output High Voltage vs. Temperature

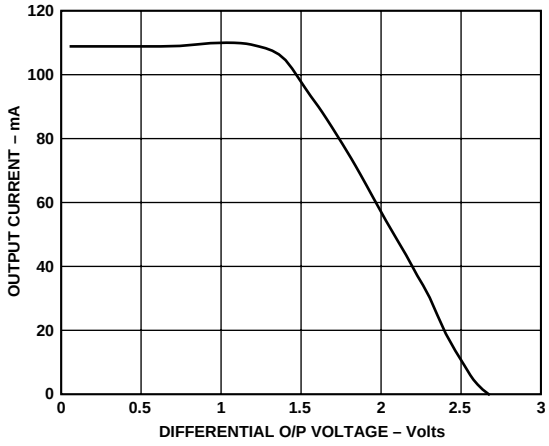


Figure 15. Driver Differential Output Voltage vs. Output Current

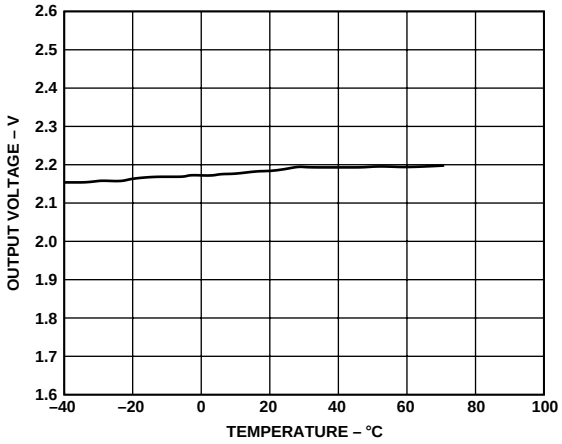


Figure 18. Driver Differential Output Voltage vs. Temperature

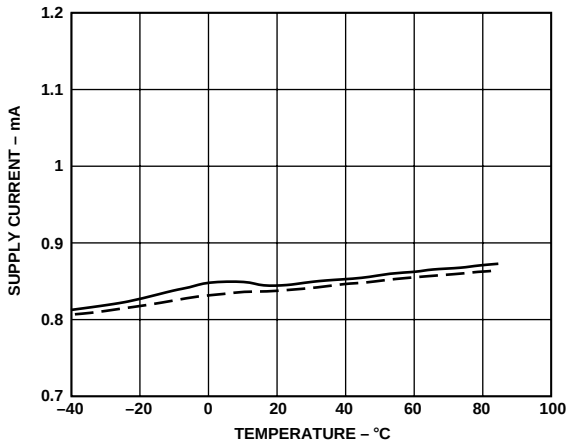


Figure 19. Supply Current vs. Temperature

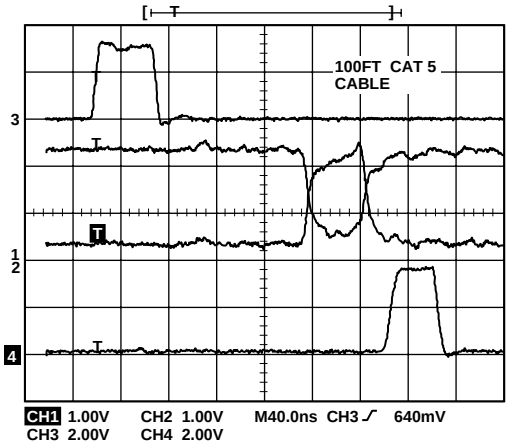


Figure 21. Driving 100 ft. Cable H-L Transition

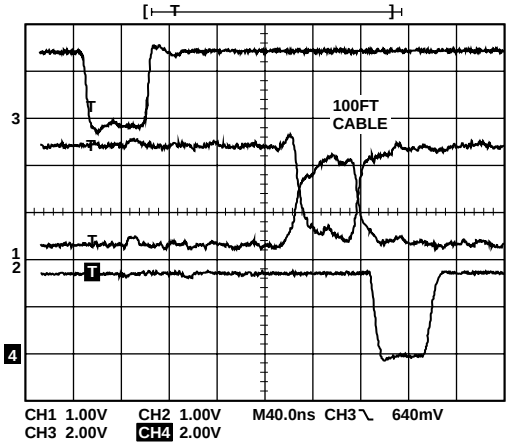


Figure 20. Driving 100 ft. Cable L-H Transition

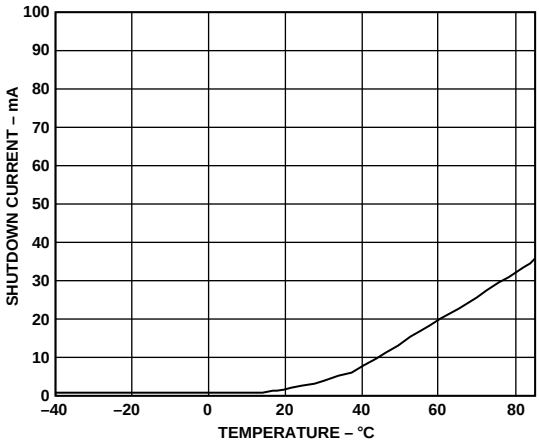


Figure 22. Shutdown Current vs. Temperature

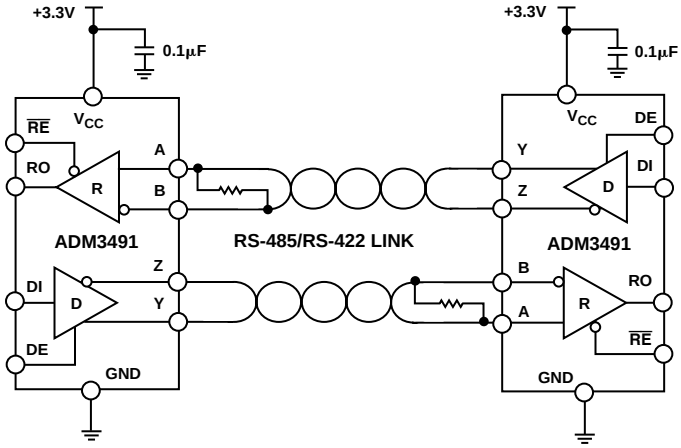


Figure 23. ADM3491 Full-Duplex Data Link

Table I. Transmitting Truth Table

Transmitting				
Inputs			Outputs	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	Hi-Z	Hi-Z
1	0	X	Hi-Z	Hi-Z

Table II. Receiving Truth Table

Receiving			
Inputs			Outputs
$\overline{RE}$	DE	A–B	RO
0	X	> +0.2 V	1
0	X	< –0.2 V	0
0	X	Inputs O/C	1
1	X	X	Hi-Z

APPLICATIONS INFORMATION

Differential Data Transmission

Differential data transmission is used to reliably transmit data at high rates over long distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals which appear as common-mode voltages on the line.

Two main standards are approved by the Electronics Industries Association (EIA) which specify the electrical characteristics of transceivers used in differential data transmission. The RS-422 standard specifies data rates up to 10 MBaud and line lengths up to 4000 ft. A single driver can drive a transmission line with up to 10 receivers.

The RS-485 standard was defined to cater to true multipoint communications. This standard meets or exceeds all the requirements of RS-422, but also allows multiple drivers and receivers to be connected to a single bus. An extended common mode range of –7 V to +12 V is defined.

The most significant difference between RS-422 and RS-485 is the fact that the drivers may be disabled thereby allowing more than one to be connected to a single line. Only one driver should be enabled at a time, but the RS-485 standard contains additional specifications to guarantee device safety in the event of line contention.

Cable and Data Rate

The transmission line of choice for RS-485 communications is a twisted pair. Twisted pair cable tends to cancel common-mode noise and also causes cancellation of the magnetic fields generated by the current flowing through each wire, thereby reducing the effective inductance of the pair.

The ADM3491 is designed for bidirectional data communications on multipoint transmission lines. A typical application showing a multipoint transmission network is illustrated in Figure 23. Only one driver can transmit at a particular time, but multiple receivers may be enabled simultaneously.

As with any transmission line, it is important that reflections are minimized. This may be achieved by terminating the extreme ends of the line using resistors equal to the characteristic impedance of the line. Stub lengths of the main line should also be kept as short as possible. A properly terminated transmission line appears purely resistive to the driver.

Receiver Open-Circuit Fail Safe

The receiver input includes a fail-safe feature that guarantees a logic high on the receiver when the inputs are open circuit or floating.

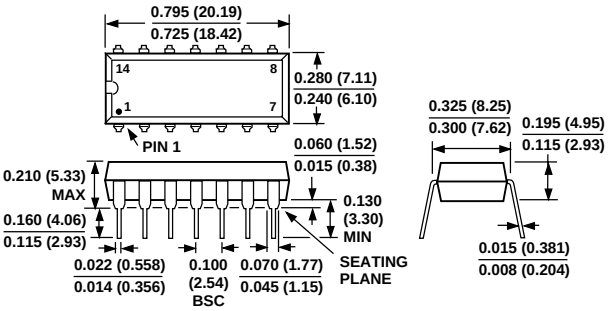
Table III. Comparison of RS-422 and RS-485 Interface Standards

Specification	RS-422	RS-485
Transmission Type	Differential	Differential
Maximum Cable Length	4000 ft.	4000 ft.
Minimum Driver Output Voltage	±2 V	±1.5 V
Driver Load Impedance	100 Ω	54 Ω
Receiver Input Resistance	4 kΩ min	12 kΩ min
Receiver Input Sensitivity	±200 mV	±200 mV
Receiver Input Voltage Range	–7 V to +7 V	–7 V to +12 V

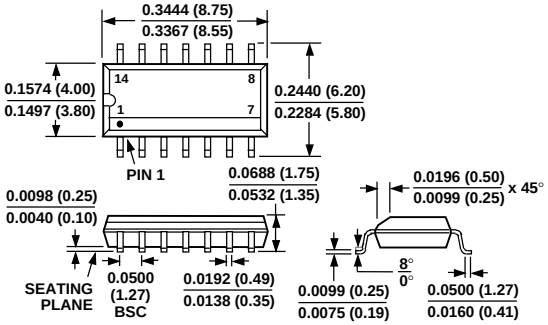
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

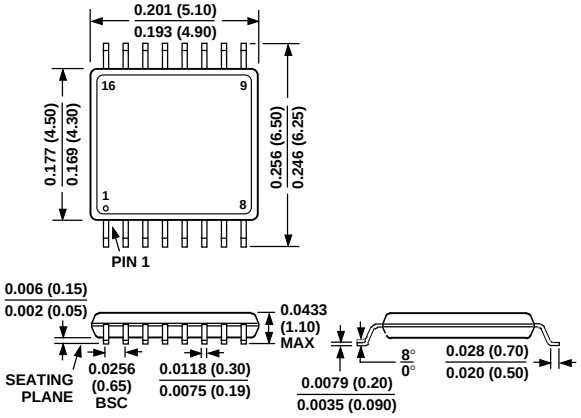
14-Lead Plastic DIP (N-14)



14-Lead Narrow Body Small Outline (SOIC) (R-14)



16-Lead Thin Shrink Small Outline (TSSOP) (RU-16)



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