



# 2.5 $\Omega$ , 1.8 V to 5.5 V, $\pm 2.5$ V Triple/Quad SPDT Switches in Chip Scale Packages

## ADG786/ADG788

### FEATURES

- 1.8 V to 5.5 V Single Supply
- $\pm 2.5$  V Dual Supply
- 2.5  $\Omega$  On Resistance
- 0.5  $\Omega$  On Resistance Flatness
- 100 pA Leakage Currents
- 19 ns Switching Times
- Triple SPDT: ADG786
- Quad SPDT: ADG788
- 20-Lead 4 mm  $\times$  4 mm Chip Scale Packages
- Low Power Consumption
- TTL/CMOS-Compatible Inputs
- For Functionally-Equivalent Devices in 16-Lead TSSOP Packages, See ADG733/ADG734

### APPLICATIONS

- Data Acquisition Systems
- Communication Systems
- Relay Replacement
- Audio and Video Switching
- Battery-Powered Systems

### GENERAL DESCRIPTION

The ADG786 and ADG788 are low voltage, CMOS devices comprising three independently selectable SPDT (single pole, double throw) switches and four independently selectable SPDT switches respectively.

Low power consumption and operating supply range of 1.8 V to 5.5 V and dual  $\pm 2.5$  V make the ADG786 and ADG788 ideal for battery powered, portable instruments and many other applications. All channels exhibit break-before-make switching action preventing momentary shorting when switching channels. An  $\overline{EN}$  input on the ADG786 is used to enable or disable the device. When disabled, all channels are switched OFF.

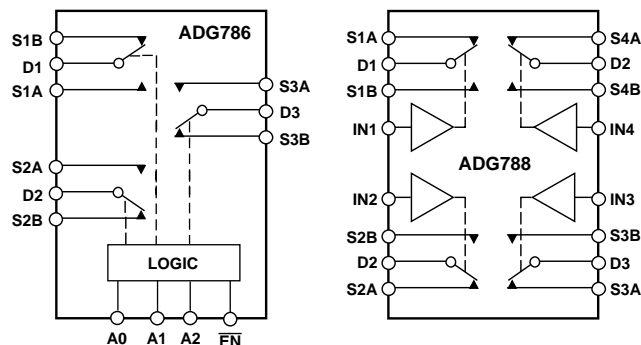
These multiplexers are designed on an enhanced submicron process that provides low power dissipation yet gives high switching speed, very low on resistance, high signal bandwidths and low leakage currents. On resistance is in the region of a few ohms, is closely matched between switches and very flat over the full signal range. These parts can operate equally well in either direction and have an input signal range which extends to the supplies.

The ADG786 and ADG788 are available in small 20-lead chip scale packages.

REV. 0

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### FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

### PRODUCT HIGHLIGHTS

1. Small 20-Lead 4 mm  $\times$  4 mm Chip Scale Packages (CSP).
2. Single/Dual Supply Operation. The ADG786 and ADG788 are fully specified and guaranteed with 3 V  $\pm$  10% and 5 V  $\pm$  10% single supply rails, and  $\pm 2.5$  V  $\pm$  10% dual supply rails.
3. Low On Resistance (2.5  $\Omega$  typical).
4. Low Power Consumption ( $< 0.01$   $\mu$ W).
5. Guaranteed Break-Before-Make Switching Action.

# ADG786/ADG788–SPECIFICATIONS<sup>1</sup> ( $V_{DD} = 5\text{ V} \pm 10\%$ , $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$ , unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
<b>ANALOG SWITCH</b>				
Analogue Signal Range		0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	2.5		$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = 10\text{ mA}$ ; Test Circuit 1
	4.5	5.0	$\Omega$ max	
On-Resistance Match between Channels ( $\Delta R_{ON}$ )		0.1	$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = 10\text{ mA}$
		0.4	$\Omega$ max	
On-Resistance Flatness ( $R_{FLAT(ON)}$ )	0.5		$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = 10\text{ mA}$
		1.2	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>				
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$		nA typ	$V_{DD} = 5.5\text{ V}$ $V_D = 4.5\text{ V}/1\text{ V}$ , $V_S = 1\text{ V}/4.5\text{ V}$ ; Test Circuit 2
	$\pm 0.1$	$\pm 0.3$	nA max	
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$		nA typ	$V_D = V_S = 1\text{ V}$ , or $4.5\text{ V}$ ; Test Circuit 3
	$\pm 0.1$	$\pm 0.5$	nA max	
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005		$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		$\pm 0.1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	4		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
$t_{ON}$	19		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_{S1A} = 3\text{ V}$ , $V_{S1B} = 0\text{ V}$ , Test Circuit 4
		34	ns max	
$t_{OFF}$	7		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 3\text{ V}$ , Test Circuit 4
		12	ns max	
ADG786 $t_{ON}(\overline{EN})$	20		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 3\text{ V}$ , Test Circuit 5
		40	ns max	
$t_{OFF}(\overline{EN})$	7		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 3\text{ V}$ , Test Circuit 5
		12	ns max	
Break-Before-Make Time Delay, $t_D$	13		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 3\text{ V}$ , Test Circuit 6
		1	ns min	
Charge Injection	$\pm 3$		pC typ	$V_S = 2\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; Test Circuit 7
Off Isolation	-72		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 8
Channel-to-Channel Crosstalk	-67		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 9
-3 dB Bandwidth	160		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , Test Circuit 10
$C_S$ (OFF)	11		pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	34		pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.001		$\mu\text{A}$ typ	$V_{DD} = 5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V
		1.0	$\mu\text{A}$ max	

## NOTES

<sup>1</sup>Temperature range is as follows: B Version: -40°C to +85°C.

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# SPECIFICATIONS<sup>1</sup>

( $V_{DD} = 3\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
<b>ANALOG SWITCH</b>				
Analog Signal Range		0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	6		$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = 10\text{ mA}$ ; Test Circuit 1
	11	12	$\Omega$ max	
On-Resistance Match between Channels ( $\Delta R_{ON}$ )		0.1	$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = 10\text{ mA}$
		0.5	$\Omega$ max	
On-Resistance Flatness ( $R_{FLAT(ON)}$ )		3	$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = 10\text{ mA}$
<b>LEAKAGE CURRENTS</b>				
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$		nA typ	$V_{DD} = 3.3\text{ V}$ ; $V_S = 3\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/3\text{ V}$ ; Test Circuit 2
	$\pm 0.1$	$\pm 0.3$	nA max	
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$		nA typ	$V_S = V_D = 1\text{ V}$ or $3\text{ V}$ ; Test Circuit 3
	$\pm 0.1$	$\pm 0.5$	nA max	
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.0	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005		$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		$\pm 0.1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	4		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
$t_{ON}$	28		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_{S1A} = 2\text{ V}$ , $V_{S1B} = 0\text{ V}$ , Test Circuit 4
		55	ns max	
$t_{OFF}$	9		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 2\text{ V}$ , Test Circuit 4
		16	ns max	
ADG786 $t_{ON}(\overline{EN})$	29		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 2\text{ V}$ , Test Circuit 5
		60	ns max	
$t_{OFF}(\overline{EN})$	9		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 2\text{ V}$ , Test Circuit 5
		16	ns max	
Break-Before-Make Time Delay, $t_D$	22		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 2\text{ V}$ , Test Circuit 6
		1	ns min	
Charge Injection	$\pm 3$		pC typ	$V_S = 1\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; Test Circuit 7
Off Isolation	-72		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 8
Channel-to-Channel Crosstalk	-67		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 9
-3 dB Bandwidth	160		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , Test Circuit 10
$C_S$ (OFF)	11		pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	34		pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.001		$\mu\text{A}$ typ	$V_{DD} = 3.3\text{ V}$ ; Digital Inputs = 0 V or 3.3 V
		1.0	$\mu\text{A}$ max	

## NOTES

<sup>1</sup>Temperature ranges are as follows: B Version: -40°C to +85°C.

<sup>2</sup>Guaranteed by design, not subject to production test.

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# ADG786/ADG788–SPECIFICATIONS<sup>1</sup>

**DUAL SUPPLY** ( $V_{DD} = +2.5\text{ V} \pm 10\%$ ,  $V_{SS} = -2.5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
<b>ANALOG SWITCH</b>				
Analog Signal Range		$V_{SS}$ to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	2.5		$\Omega$ typ	$V_S = V_{SS}$ to $V_{DD}$ , $I_{DS} = 10\text{ mA}$ ; Test Circuit 1
	4.5	5.0	$\Omega$ max	
On-Resistance Match between Channels ( $\Delta R_{ON}$ )		0.1	$\Omega$ typ	$V_S = V_{SS}$ to $V_{DD}$ , $I_{DS} = 10\text{ mA}$
		0.4	$\Omega$ max	
On-Resistance Flatness ( $R_{FLAT(ON)}$ )	0.5		$\Omega$ typ	$V_S = V_{SS}$ to $V_{DD}$ , $I_{DS} = 10\text{ mA}$
		1.2	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>				
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$		nA typ	$V_{DD} = +2.75\text{ V}$ , $V_{SS} = -2.75\text{ V}$ $V_S = +2.25\text{ V}/-1.25\text{ V}$ , $V_D = -1.25\text{ V}/+2.25\text{ V}$ ; Test Circuit 2
	$\pm 0.1$	$\pm 0.3$	nA max	
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$		nA typ	$V_S = V_D = +2.25\text{ V}/-1.25\text{ V}$ , Test Circuit 3
	$\pm 0.1$	$\pm 0.5$	nA max	
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		1.7	V min	
Input Low Voltage, $V_{INL}$		0.7	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005		$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		$\pm 0.1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	4		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
$t_{ON}$	21	35	ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_{S1A} = 1.5\text{ V}$ , $V_{S1B} = 0\text{ V}$ , Test Circuit 4
			ns max	
$t_{OFF}$	10	16	ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 1.5\text{ V}$ , Test Circuit 4
			ns max	
ADG786 $t_{ON}(\overline{EN})$	21	40	ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 1.5\text{ V}$ , Test Circuit 5
			ns max	
$t_{OFF}(\overline{EN})$	10	16	ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 1.5\text{ V}$ , Test Circuit 5
			ns max	
Break-Before-Make Time Delay, $t_D$	13	1	ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 1.5\text{ V}$ , Test Circuit 6
			ns min	
Charge Injection	$\pm 5$		pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; Test Circuit 7
Off Isolation	-72		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 8
Channel-to-Channel Crosstalk	-67		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 9
-3 dB Bandwidth	160		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , Test Circuit 10
$C_S$ (OFF)	11		pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	34		pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.001		$\mu\text{A}$ typ	$V_{DD} = +2.75\text{ V}$ Digital Inputs = 0 V or 2.75 V
		1.0	$\mu\text{A}$ max	
$I_{SS}$	0.001		$\mu\text{A}$ typ	$V_{SS} = -2.75\text{ V}$ Digital Inputs = 0 V or 2.75 V
		1.0	$\mu\text{A}$ max	

## NOTES

<sup>1</sup>Temperature range is as follows: B Version: -40°C to +85°C.

<sup>2</sup>Guaranteed by design, not subject to production test.

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## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = 25°C unless otherwise noted)

V <sub>DD</sub> to V <sub>SS</sub> .....	7 V
V <sub>DD</sub> to GND .....	-0.3 V to +7 V
V <sub>SS</sub> to GND .....	+0.3 V to -3.5 V
Analog Inputs <sup>2</sup> .....	V <sub>SS</sub> - 0.3 V to V <sub>DD</sub> + 0.3 V or 30 mA, Whichever Occurs First
Digital Inputs <sup>2</sup> .....	-0.3 V to V <sub>DD</sub> + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D .....	100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D .....	30 mA
Operating Temperature Range	
Industrial (A, B Versions) .....	-40°C to +85°C

Storage Temperature Range .....	-65°C to +150°C
Junction Temperature .....	150°C
20 Lead CSP, θ <sub>JA</sub> Thermal Impedance .....	32°C/W
Lead Temperature, Soldering (10 sec) .....	300°C
IR Reflow, Peak Temperature .....	220°C

### NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

<sup>2</sup>Overtolerances at A, EN, IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

## CAUTION

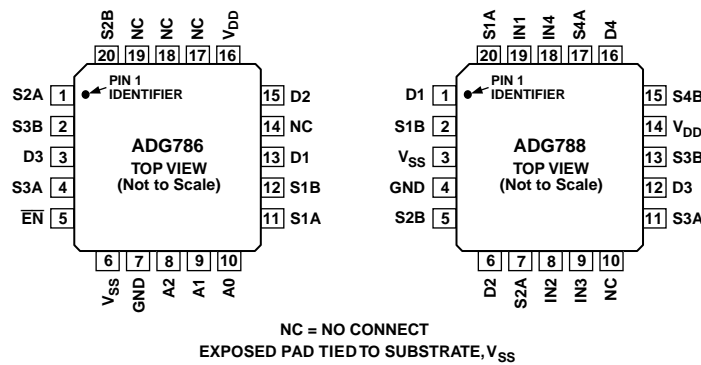
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG786/ADG788 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG786BCP	-40°C to +85°C	Chip Scale Package (CSP)	CP-20
ADG788BCP	-40°C to +85°C	Chip Scale Package (CSP)	CP-20

## PIN CONFIGURATIONS



# ADG786/ADG788

**Table I. ADG786 Truth Table**

A2	A1	A0	$\overline{\text{EN}}$	ON Switch
X	X	X	1	None
0	0	0	0	D1-S1A, D2-S2A, D3-S3A
0	0	1	0	D1-S1B, D2-S2A, D3-S3A
0	1	0	0	D1-S1A, D2-S2B, D3-S3A
0	1	1	0	D1-S1B, D2-S2B, D3-S3A
1	0	0	0	D1-S1A, D2-S2A, D3-S3B
1	0	1	0	D1-S1B, D2-S2A, D3-S3B
1	1	0	0	D1-S1A, D2-S2B, D3-S3B
1	1	1	0	D1-S1B, D2-S2B, D3-S3B

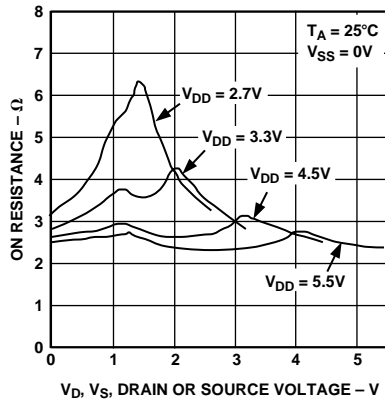
**Table II. ADG788 Truth Table**

Logic	Switch A	Switch B
0	OFF	ON
1	ON	OFF

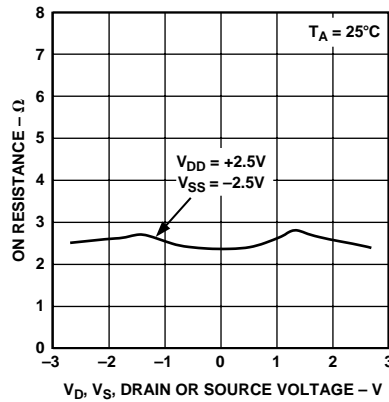
## TERMINOLOGY

$V_{DD}$	Most Positive Power Supply Potential
$V_{SS}$	Most Negative Power Supply in a Dual Supply Application. In single supply applications, this should be tied to ground close to the device.
$I_{DD}$	Positive Supply Current
$I_{SS}$	Negative Supply Current
GND	Ground (0 V) Reference
S	Source Terminal. May be an input or output
D	Drain Terminal. May be an input or output
IN	Logic Control Input
$V_D (V_S)$	Analog Voltage on Terminals D, S
$R_{ON}$	Ohmic Resistance between D and S
$\Delta R_{ON}$	On Resistance Match between Any Two Channels, i.e., $R_{ONmax} - R_{ONmin}$ .
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
$I_S$ (OFF)	Source Leakage Current with the Switch "OFF"
$I_D, I_S$ (ON)	Channel Leakage Current with the Switch "ON"
$V_{INL}$	Maximum Input Voltage for Logic "0"
$V_{INH}$	Minimum Input Voltage for Logic "1"
$I_{INL} (I_{INH})$	Input Current of the Digital Input
$C_S$ (OFF)	"OFF" Switch Source Capacitance. Measured with reference to ground.
$C_D, C_S$ (ON)	"ON" Switch Capacitance. Measured with reference to ground.
$C_{IN}$	Digital Input Capacitance
$t_{ON}$	Delay time measured between the 50% and 90% points of the digital inputs and the switch "ON" condition.
$t_{OFF}$	Delay time measured between the 50% and 90% points of the digital input and the switch "OFF" condition.
$t_{ON}(\overline{\text{EN}})$	Delay time between the 50% and 90% points of the $\overline{\text{EN}}$ digital input and the switch "ON" condition.
$t_{OFF}(\overline{\text{EN}})$	Delay time between the 50% and 90% points of the $\overline{\text{EN}}$ digital input and the switch "OFF" condition.
$t_{OPEN}$	"OFF" time measured between the 80% points of both switches when switching from one address state to another.
Charge	A measure of the glitch impulse transferred Injection from the digital input to the analog output during switching.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
On Response	The Frequency Response of the "ON" Switch
Insertion Loss	The Loss Due to the ON Resistance of the Switch.

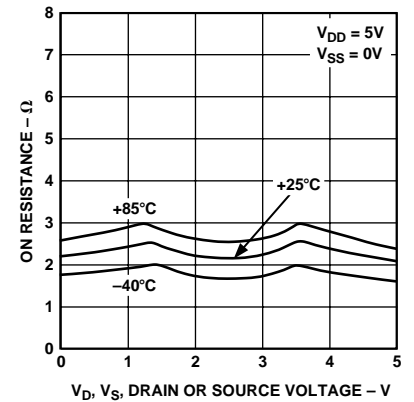
# Typical Performance Characteristics–ADG786/ADG788



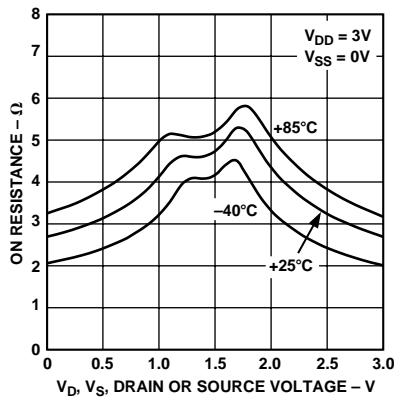
TPC 1. On Resistance as a Function of  $V_D(V_S)$  for Single Supply



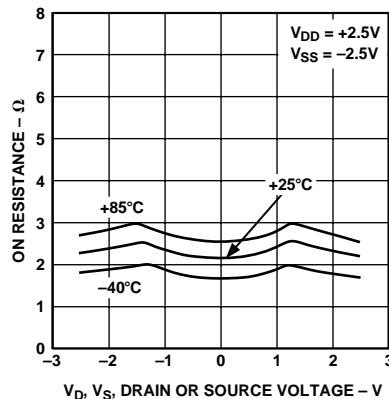
TPC 2. On Resistance as a Function of  $V_D(V_S)$  for Dual Supply



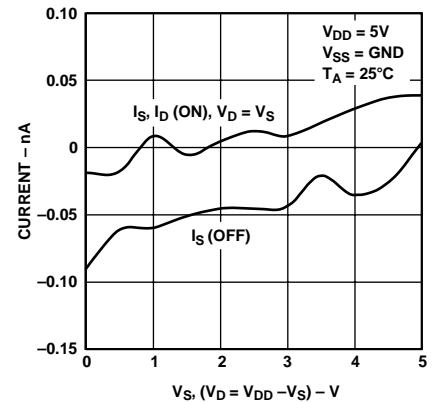
TPC 3. On Resistance as a Function of  $V_D(V_S)$  for Different Temperatures, Single Supply



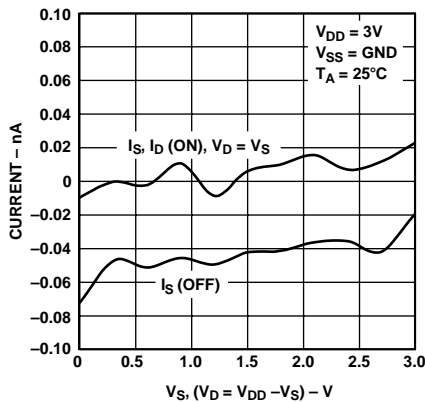
TPC 4. On Resistance as a Function of  $V_D(V_S)$  for Different Temperatures, Single Supply



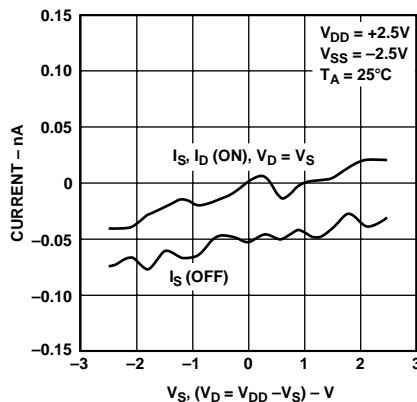
TPC 5. On Resistance as a Function of  $V_D(V_S)$  for Different Temperatures, Dual Supply



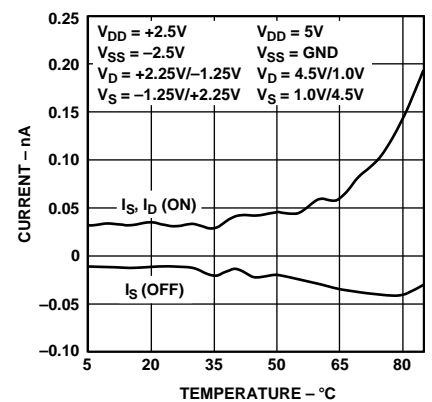
TPC 6. Leakage Currents as a Function of  $V_D(V_S)$



TPC 7. Leakage Currents as a Function of  $V_D(V_S)$

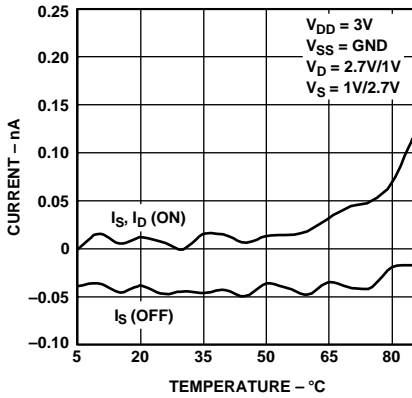


TPC 8. Leakage Currents as a Function of  $V_D(V_S)$

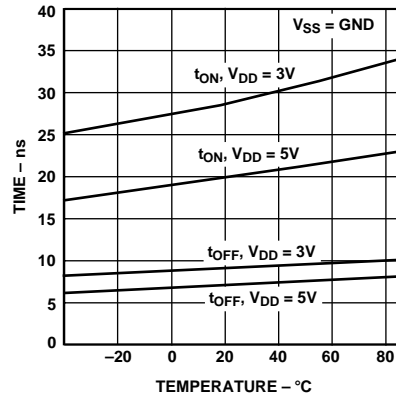


TPC 9. Leakage Currents as a Function of Temperature

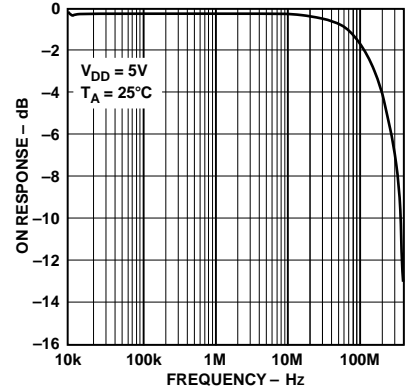
# ADG786/ADG788



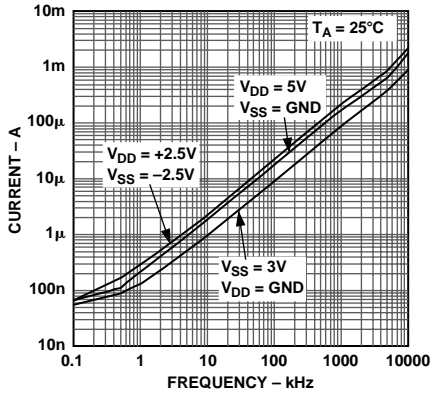
TPC 10. Leakage Currents as a Function of Temperature



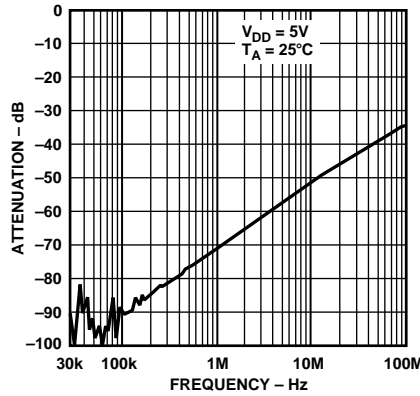
TPC 11.  $t_{ON}/t_{OFF}$  Times vs. Temperature



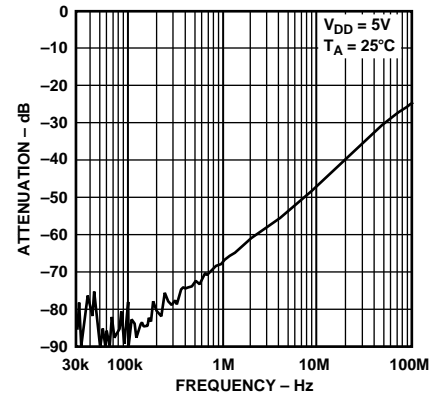
TPC 12. On Response vs. Frequency



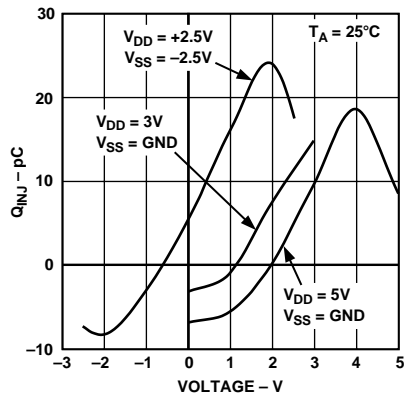
TPC 13. Input Current,  $I_{DD}$  vs. Switching Frequency



TPC 14. Off Isolation vs. Frequency



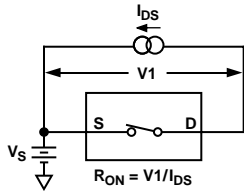
TPC 15. Crosstalk vs. Frequency



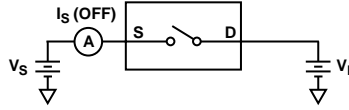
TPC 16. Charge Injection vs. Source Voltage



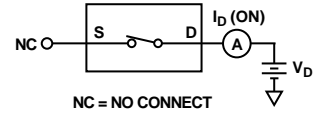
# Test Circuits



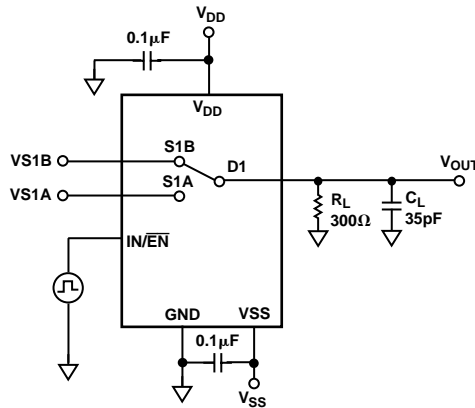
Test Circuit 1. On Resistance



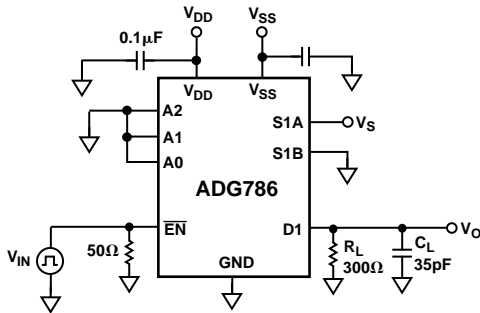
Test Circuit 2.  $I_S$  (OFF)



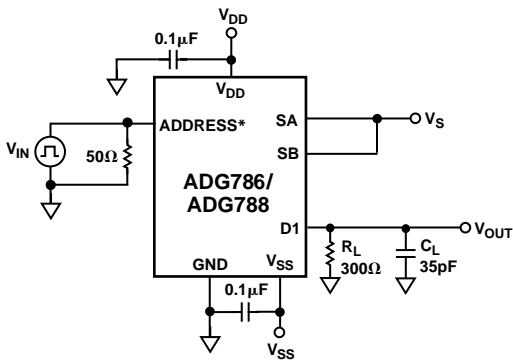
Test Circuit 3.  $I_D$  (ON)



Test Circuit 4. Switching Times,  $t_{ON}$ ,  $t_{OFF}$



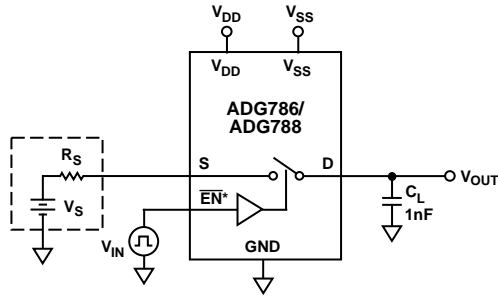
Test Circuit 5. Enable Delay,  $t_{ON}(\overline{EN})$ ,  $t_{OFF}(\overline{EN})$



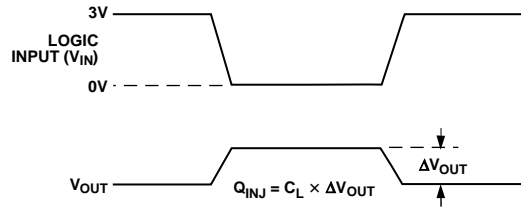
\*A0, A1, A2 for ADG786, IN1-4 for ADG788

Test Circuit 6. Break-Before-Make Delay,  $t_{OPEN}$

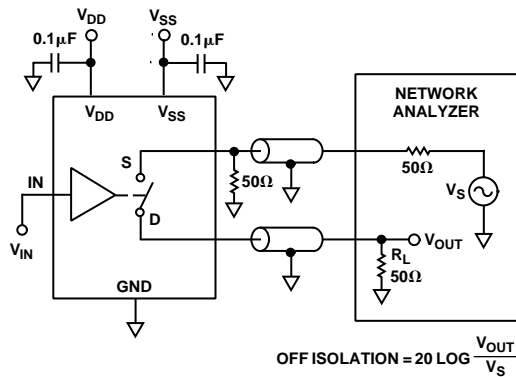
# ADG786/ADG788



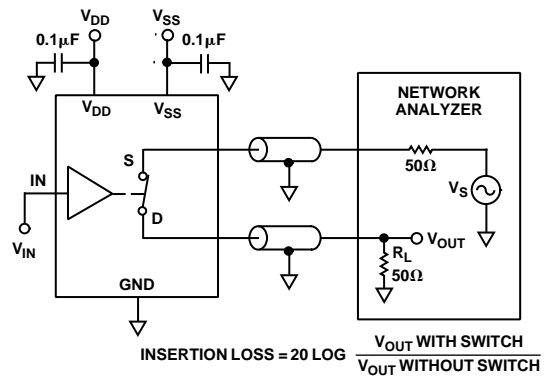
\* IN1-4 for ADG734



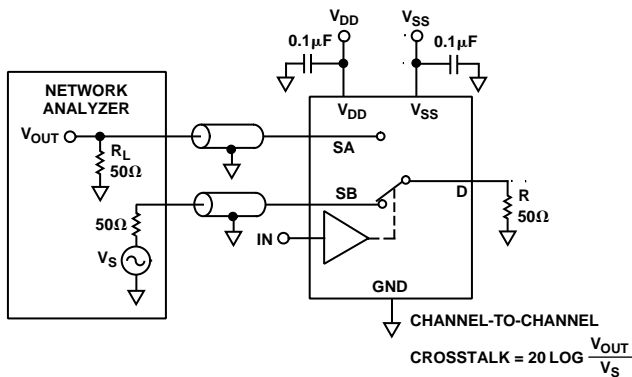
Test Circuit 7. Charge Injection



Test Circuit 8. OFF Isolation



Test Circuit 10. Bandwidth



Test Circuit 9. Channel-to-Channel Crosstalk

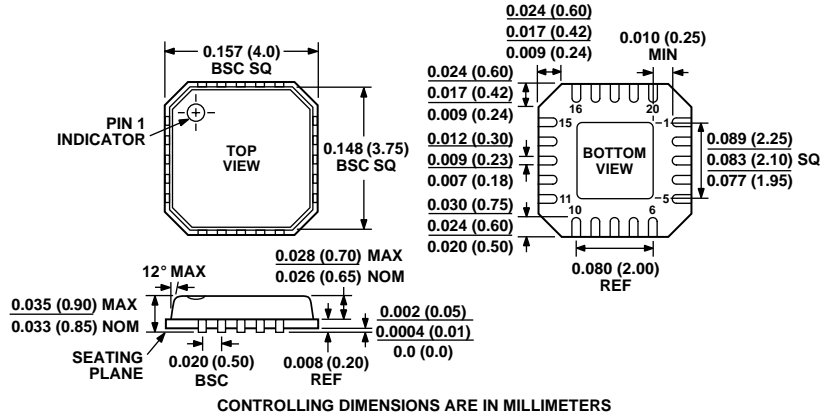
## Power Supply Sequencing

When using CMOS devices, care must be taken to ensure correct power supply sequencing. Incorrect sequencing can result in the device being subjected to stresses beyond those maximum ratings listed in the data sheet. Digital and analog inputs should be applied to the device after supplies and ground. In dual supply applications, if digital and analog inputs may be applied prior to  $V_{DD}$  and  $V_{SS}$  supplies, the addition of a Schottky diode connected between  $V_{SS}$  and GND will ensure that the device powers on correctly. For single supply applications,  $V_{SS}$  should be tied to GND as close to the device as possible.

**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

**20-Lead Chip Select Package  
(CP-20)**







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