

3-phase Brushless Motor Driver

Overview

The LB1694N is a 3-phase brushless motor driver IC that is ideal for driving DC fan motors in air conditioners, hot-water supply systems, and the like.

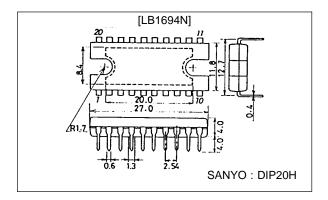
Features

- · 3-phase brushless motor driver.
- Withstand voltage: 45 V; output current: 2.5 A.
- Current limiter built in.
- Low-voltage protector circuit built in.
- Thermal shutdown protector built in.
- Hall amplifier with hysteresis built in.
- FG output function.

Package Dimensions

unit: mm

3037A-DIP20H



Specifications

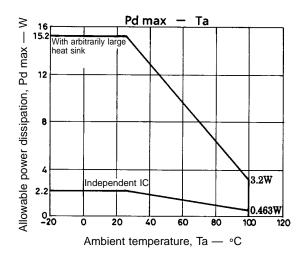
Absolute Maximum Ratings at Ta = 25 °C

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|---------------------|----------------------------------|-------------|------|
| Maximum supply voltage | V _{CC} max | | 10 | V |
| Maximum supply voltage | V _M max | | 45 | V |
| Output current | IO | | 2.5 | Α |
| Allowable newer discinction | Pd max1 | Independent IC | 2.2 | W |
| Allowable power dissipation | Pd max2 | With arbitrarily large heat sink | 15.2 | W |
| Operating temperature | Topr | | -20 to +100 | ∘C |
| Storage temperature | Tstg | | -55 to +120 | ∘C |

Allowable Operating Ranges at Ta = 25 °C

| Parameter | Symbol | Conditions | Ratings | Unit |
|--------------------------------|-----------------------|--|------------|------|
| Supply voltage range | V _{CC} | | 4.5 to 5.5 | V |
| Supply voltage range | V _M | | 5 to 42 | V |
| Power cupply veltage rice rate | ΔV _{CC} / Δt | V _{CC} = V _{LVSD} (OFF) point *1 | to 0.04 | V/µs |
| Power supply voltage rise rate | ΔV _M / Δt | V _M = 0 V point*1 | to 0.16 | V/µs |

^{*1} If the supply voltage rise rate is fast when power is applied, through current may flow to output.



Electric Characteristics at Ta = 25 $^{\circ}C,~V_{CC}$ = 5 V, V_{M} = 30 V

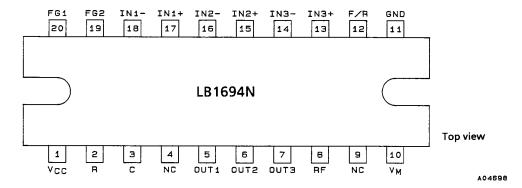
| | Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|--|------------------------|---|------|-----|------------|------|
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | Supply current | Icc | Forward | | 13 | 19 | mA |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | Output saturation voltage | V _{Osat1} | $I_O = 1 A, V_O (sink) + V_O (source)$ | | 2.1 | 3.0 | > |
| Dutput leak current Io(leak) Io(leak) Io μA Hall amplifier | Output saturation voltage | V _{Osat2} | $I_O = 2 A$, $V_O (sink) + V_O (source)$ | | 3.0 | 4.2 | > |
| Input bias current Input bias current Input bias current Input bias current Input voltage range VICM Input voltage L → H VSLH Input voltage H → L VSHL Input voltage Direction voltage VFGL Input voltage Direction voltage VFGL Input voltage Direction voltage VFGL Input voltage VFR1 Input voltage VFR1 Input voltage VFR2 Input voltage VFFR2 Input voltage VFFFR2 Input voltage VFFFR2 Input voltage VFFFR2 Input voltage VFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF | Output leak current | | | | | 100 | μΑ |
| Common-mode input voltage range V_{ICM} 1.5 3.2 V Hysteresis width ΔV_{IN} 21 30 37 mV Input voltage L \rightarrow H V_{SHL} 5 15 25 mV Input voltage H \rightarrow L V_{SHL} -25 -15 -5 mV FG pin (rate pulse output) Input voltage pulse output) Version of the pulse output voltage Version of the pulse output voltage of the pulse output voltage Version of the pulse output voltage of the pulse output voltage output voltage Version of the pulse output voltage outp | Hall amplifier | | | | | | |
| range V_{ICM} 1.5 3.2 V Hysteresis width $ΔV_{IN}$ 21 30 37 mV Input voltage L → H V _{SLH} 5 15 25 mV Input voltage H → L V _{SHL} -25 -15 -5 mV FG pin (rate pulse output) Low level output voltage V _{FGL} I _{FG} = 5 mA 0.4 V Pull-up resistance R _{FG} 0 0.8 V F/R operation Forward V _{FR1} 0 0.8 V F/R operation Reverse V _{FR2} 0 0.42 0.5 0.6 V Current limit operation limiter V _{RF} 0.42 0.5 0.6 V Thermal shutdown operation temperature T _{SD} Design target 120 150 °C Hysteresis width ΔT _{SD} Design target 3.5 3.8 4.1 V Educed voltage protection operation voltage V _{LVSD} 0.4 0.5 0.6 V Hysteresis width ΔV _{LVSD} 0.4 0.5 0.6 V C pin charge current I _{CL} R = 33 kΩ 30 40 55 μA C pin charge start voltage V _{CL} R = 33 kΩ 0.3 0.4 0.5 V C pin charge start voltage V _{CL} R = 33 kΩ 0.3 0.4 0.5 V C pin discharge start voltage V _{CL} R = 33 kΩ 0.3 0.4 0.5 V C pin discharge start voltage V _{CL} R = 33 kΩ 0.3 0.4 0.5 V C pin discharge start voltage V _{CL} R = 33 kΩ 0.3 0.4 0.5 V C pin discharge start voltage V _{CL} R = 33 kΩ 0.3 0.4 0.5 V C pin discharge start voltage V _{CL} R = 33 kΩ 0.3 0.4 0.5 V C pin discharge start voltage V _{CL} R = 33 kΩ 0.3 0.4 0.5 V C pin discharge start voltage V _{CL} R = 33 kΩ 0.3 0.4 0.5 V C pin discharge start voltage V _{CL} R = 33 kΩ 0.3 0.4 0.5 V C pin discharge start voltage V _{CL} R = 33 kΩ 0.3 0.4 0.5 V C pin discharge start voltage V _{CL} R = 33 kΩ 0.3 0.4 0.5 V C pin discharge start voltage V _{CL} R = 33 kΩ 0.4 0.5 0.5 V C putput current neglect time t _{sm} R = 33 kΩ 0.4 0.5 0.5 0.5 V | Input bias current | I _{HB} | | | 1 | 4 | μΑ |
| Input voltage L \rightarrow H V_{SLH} V_{SLH} V_{SHL} $V_$ | | V _{ICM} | | 1.5 | | 3.2 | ٧ |
| Input voltage H → L V _{SHL} -25 -15 -5 mV FG pin (rate pulse output) Low level output voltage V _{FGL} I _{FG} = 5 mA 0.4 V Pull-up resistance R _{FG} 7.5 10 12.5 kΩ F/R operation Forward V _{FR1} 0 0.8 V F/R operation Reverse V _{FR2} 4.2 5.0 V Current limit operation limiter V _{RF} 0.42 0.5 0.6 V Thermal shutdown operation temperature T _{SD} Design target 120 150 °C Hysteresis width ΔT _{SD} Design target 3.5 3.8 4.1 V Reduced voltage protection operation voltage V _{LVSD} 3.5 3.8 4.1 V Reduced voltage protection release voltage V _{LVSD} (OFF) 4.3 4.5 V Hysteresis width ΔV _{LVSD} 0.4 0.5 0.6 V C pin charge current I _{CL} R = 33 kΩ 30 40 | Hysteresis width | ΔV_{IN} | | 21 | 30 | 37 | mV |
| Input voltage H → L V _{SHL} -25 -15 -5 mV FG pin (rate pulse output) Low level output voltage V _{FGL} I _{FG} = 5 mA 0.4 V Pull-up resistance R _{FG} 7.5 10 12.5 kΩ F/R operation Forward V _{FR1} 0 0.8 V F/R operation Reverse V _{FR2} 4.2 5.0 V Current limit operation limiter V _{RF} 0.42 0.5 0.6 V Thermal shutdown operation temperature T _{SD} Design target 120 150 °C Hysteresis width ΔT _{SD} Design target 3.5 3.8 4.1 V Reduced voltage protection operation voltage V _{LVSD} 3.5 3.8 4.1 V Reduced voltage protection release voltage V _{LVSD} (OFF) 4.3 4.5 V Hysteresis width ΔV _{LVSD} 0.4 0.5 0.6 V C pin charge current I _{CL} R = 33 kΩ 30 40 | Input voltage $L \rightarrow H$ | V _{SLH} | | 5 | 15 | 25 | mV |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | Input voltage $H \rightarrow L$ | V _{SHL} | | -25 | -15 | – 5 | mV |
| Pull-up resistance R _{FG} 7.5 10 12.5 $k\Omega$ F/R operation Forward VFR1 0 0.8 V F/R operation Reverse VFR2 4.2 5.0 V Current limit operation limiter VRF 0.42 0.5 0.6 V Thermal shutdown operation temperature T _{SD} Design target 120 150 °C °C Hysteresis width ΔT _{SD} Design target 30 °C °C °C Reduced voltage protection operation voltage 3.5 3.8 4.1 V V V 4.3 4.5 V <td>FG pin (rate pulse output)</td> <td></td> <td></td> <td>·</td> <td></td> <td></td> <td></td> | FG pin (rate pulse output) | | | · | | | |
| F/R operation Forward V_{FR1} 0 0.8 V_{FR} 0 0.8 V_{FR} 0 0.8 V_{FR} 0 0.8 0 0.8 0 0.8 0 0.8 0 0.8 0 0.8 0 0.8 0 0.8 0 0.8 0 0.8 0 0.8 0 0.8 0 0.8 0 0.8 0 0.8 0 0.8 0 0 0.8 0 0 0.8 0 0 0.8 0 0 0 0 0 0 0 0 0 0 | Low level output voltage | V _{FGL} | I _{FG} = 5 mA | | | 0.4 | V |
| F/R operation Reverse V_{FR2} V_{FR2} V_{FR2} V_{RF} $V_{$ | Pull-up resistance | R _{FG} | | 7.5 | 10 | 12.5 | kΩ |
| F/R operation Reverse V_{FR2} V_{RF} V_{RF | F/R operation Forward | V _{FR1} | | | 0 | 0.8 | V |
| Thermal shutdown operation temperature T_{SD} Design target T_{S | F/R operation Reverse | | | 4.2 | 5.0 | | V |
| The period of t | Current limit operation limiter | V _{RF} | | 0.42 | 0.5 | 0.6 | > |
| Reduced voltage protection operation voltage V_{LVSD} 3.5 3.8 4.1 V Reduced voltage protection release voltage $V_{LVSD(OFF)}$ 4.3 4.5 V Hysteresis width ΔV_{LVSD} 0.4 0.5 0.6 V C pin charge current I_{CL} R = 33 kΩ 30 40 50 μA C pin discharge current I_{CH} R = 33 kΩ 90 120 150 μA C pin charge start voltage V_{CL} R = 33 kΩ 0.3 0.4 0.5 V C pin discharge start voltage V_{CH} R = 33 kΩ 1.5 2.0 2.5 V Output current neglect time I_{SM} R = 33 kΩ, C = 4700 pF 58 68 78 μs | Thermal shutdown operation temperature | T _{SD} | Design target | 120 | 150 | | °C |
| Substitution of the proper action of the proper action voltage VLVSD 3.5 3.8 4.1 V Reduced voltage protection release voltage VLVSD(OFF) 4.3 4.5 V Hysteresis width ΔVLVSD 0.4 0.5 0.6 V C pin charge current I _{CL} R = 33 kΩ 30 40 50 μA C pin discharge current I _{CH} R = 33 kΩ 90 120 150 μA C pin charge start voltage V _{CL} R = 33 kΩ 0.3 0.4 0.5 V C pin discharge start voltage V _{CH} R = 33 kΩ 1.5 2.0 2.5 V Output current neglect time t _{Sm} R = 33 kΩ, C = 4700 pF 58 68 78 μs | Hysteresis width | ΔT _{SD} | Design target | | 30 | | °C |
| release voltage $VLVSD(OFF)$ 4.3 4.5 V Hysteresis width ΔV_{LVSD} 0.4 0.5 0.6 V C pin charge current I_{CL} R = 33 kΩ 30 40 50 μA C pin discharge current I_{CH} R = 33 kΩ 90 120 150 μA C pin charge start voltage I_{CH} R = 33 kΩ 0.3 0.4 0.5 V C pin discharge start voltage I_{CH} R = 33 kΩ 0.3 0.4 0.5 V C pin discharge start voltage I_{CH} R = 33 kΩ 1.5 2.0 2.5 V Output current neglect time I_{SM} R = 33 kΩ, C = 4700 pF 58 68 78 μs | Reduced voltage protection operation voltage | V _{LVSD} | | 3.5 | 3.8 | 4.1 | ٧ |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | Reduced voltage protection release voltage | V _{LVSD(OFF)} | | | 4.3 | 4.5 | ٧ |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | Hysteresis width | ΔV_{LVSD} | | 0.4 | 0.5 | 0.6 | V |
| C pin charge start voltage V_{CL} R = 33 k Ω 0.3 0.4 0.5 V C pin discharge start voltage V_{CH} R = 33 k Ω 1.5 2.0 2.5 V Output current neglect time t_{sm} R = 33 k Ω , C = 4700 pF 58 68 78 μs | C pin charge current | | R = 33 kΩ | 30 | 40 | 50 | μΑ |
| C pin charge start voltage V_{CL} R = 33 k Ω 0.3 0.4 0.5 V C pin discharge start voltage V_{CH} R = 33 k Ω 1.5 2.0 2.5 V Output current neglect time t_{sm} R = 33 k Ω , C = 4700 pF 58 68 78 μs | C pin discharge current | I _{CH} | R = 33 kΩ | 90 | 120 | 150 | μΑ |
| Output current neglect time t_{sm} R = 33 k Ω , C = 4700 pF 58 68 78 μ s | C pin charge start voltage | V _{CL} | R = 33 kΩ | 0.3 | 0.4 | 0.5 | V |
| Output current neglect time t_{sm} R = 33 k Ω , C = 4700 pF 58 68 78 μs | C pin discharge start voltage | V _{CH} | R = 33 kΩ | 1.5 | 2.0 | 2.5 | V |
| Output off time t_{SO} R = 33 k Ω , C = 4700 pF 164 193 222 μ s | Output current neglect time | | R = 33 kΩ, C = 4700 pF | 58 | 68 | 78 | μs |
| | Output off time | t _{so} | R = 33 kΩ, C = 4700 pF | 164 | 193 | 222 | μs |

Truth Table

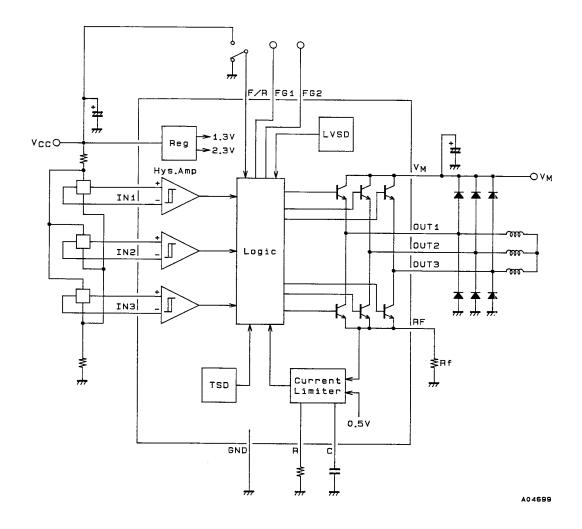
| | Input | | F/R control | Output | FG output | | | | |
|---|-------|-------|-------------|--------|-------------------|-----|-------------|---|---|
| | IN1 | IN2 | IN3 | F/R | $Source \to Sink$ | FG1 | FG2 | | |
| 1 | 1 H L | | Н | L | OUT2 → OUT1 | | | | |
| ' | П | | П | Н | OUT1 → OUT2 | | L | | |
| 2 | Н | | 1 | L | OUT3 → OUT1 | | Н | | |
| | П | | L | Н | OUT1 → OUT3 | | п | | |
| 3 | 2 11 | н | L | L | OUT3 → OUT2 | L | L | | |
| 3 | П | | | Н | OUT2 → OUT3 | | | | |
| 4 | | | Н | ш | L | L | OUT1 → OUT2 | Н | Н |
| 4 | L | L H | | Н | OUT2 → OUT1 | | П | | |
| 5 | 5 L H | | Н | L | OUT1 → OUT3 | Н | | | |
| 3 | L | П | П | Н | OUT3 → OUT1 | | L | | |
| 6 | | | L H | L | OUT2 → OUT3 | Н Н | Н | | |
| 0 | | _ L | | Н | OUT3 → OUT2 |] " | П | | |

| F/R | | | FG output |
|---------|---|--------------|-----------|
| Forward | L | 0.0 to 0.8 V | FG1 |
| Reverse | Н | 4.2 to 5.0 V | FG2 |

Pin Assignment



Block Diagram and Peripheral Circuit Diagram



Pin Functions

| Pin No. | Pin Name | Pin Voltage | Equivalent Circuit Diagram | Pin Function |
|-------------|----------------------|-------------------------------------|--|--|
| 1 | V _{CC} | | | Supplies power to all circuits except output block. |
| 2 | R | | 2000 | Sets the C pin charge/discharge current. |
| 3 | С | | 2.0V 0.4V | Sets the output off time and output current neglect time during current limiter operation. |
| 5 6 7 | OUT1 OUT2 OUT3 | | <u>vec</u> ⊕ ⊕ ⊕ ⊕ −−−−−−−−−−−−−−−−−−−−−−−−−−−−− | Output pin 1 Output pin 2 Output pin 3 |
| 8 | RF | | 9.57 2000 0 | Output current detection pin. By inserting resistor R_f between this pin and GND, the output current is detected as voltage. The output current is limited to a current value set by V_{RF}/R_f (current limit operation). |
| 10 | V _M | | A04701 | Power supply pin providing output. |
| 11 | GND | | | GND for other than output. The minimum potential of output transistor is the RF pin voltage. |
| 12 | F/R | 0.0 V min V _{CC} max | 10kp 20kp 12 10kg M 12 A64792 | Forward/reverse control pin. |
| 17, 18, | IN1+, IN1- | 1.5 V min V _{CC} -1.8 V | <u>vcc</u> | Hall device input pin. Logic "H" represents IN+ > IN |
| 15, 16, | IN2+, IN2- | max | ⊕ } ⊢ | · |
| 13, 14 | IN3+, IN3- | | 13 2000 19 19 19 19 A64703 | |
| 19 20 | FG2 FG1 | | 19@0 404704 | Rate pulse output pin 2. Pull-up resistor built in. Rate pulse output pin 1. Pull-up resistor built in. |

1. Hall input circuit

The Hall input circuit is a differential amplifier with hysteresis (30 mV typ). The operating DC level must be within the common-mode input voltage range (1.5 V to $V_{CC}-1.8$ V). An input level that is at least three times greater than the hysteresis (from 120 to 160 mVp-p) is recommended to be independent of noise, etc. If the handling capability needs to be considered in noise evaluation, etc., connect a capacitor (about 0.01 μ F) between the Hall inputs IN^+ and IN^- .

Protectors

2-1. Reduced voltage protector

If V_{CC} drops below the prescribed voltage (V_{LVSD}), the output transistor on the sink side turns off. This protector prevents malfunction which may occur when V_{CC} is reduced.

2-2. Thermal shutdown protector

If the junction temperature exceeds the prescribed temperature (T_{SD}) , the output transistor on the sink side turns off. This protector prevents the IC from being damaged by heat. Thermal design must be such that no operation is performed in other modes than abnormality.

3. FG output circuit

IN1, IN2, and IN3 Hall input signals are composited and wave shaped to be output. FG1 has the same frequency as for Hall input, while FG2 3-fold as many.

4. Forward/reverse controller

No forward/reverse (F/R) switching is assumed to be performed during motor running period. If F/R switching is performed during motor running period, through current flows to output and ASO needs to be considered. It is recommended that F/R switching be performed when the V_M power supply is off (in motor stop mode).

5. V_{CC} and V_M power supplies

If the supply voltage (V_{CC}, V_M) rise rate is fast when power is applied, through current flows to output and ASO needs to be considered. The supply voltage rise rate must be such that $\Delta V_{CC}/\Delta t = 0.04 \text{ V/\mu}s$ or less and $\Delta V_M/\Delta t = 0.16 \text{ V/\mu}s$ or less. The desirable order of applying power is V_{CC} on first and then V_M on. The desirable order of turning off power supply is V_M off first and then V_{CC} off after motor stop. If, after V_M is turned off, V_{CC} is turned off during motor's inertial running, some types of motors have a possibility that V_M voltage rises, exceeding the withstand voltage.

6. Power supply stabilization capacitor

Great fluctuations in the V_{CC} line may cause the reduced-voltage protector, etc. to malfunction. A capacitor (several μF) needs to be connected to the V_{CC} line (between V_{CC} and GND) for stabilization. Since a large switching current flows in the V_M line, wiring inductance component, etc. fluctuates. Because there are also fluctuations in the GND line, a capacitor needs to be connected to the V_M line (between V_M and GND) for stabilization thus preventing malfunction and keeping the withstand voltage from being exceeded. Especially when the routing of wiring (V_M , V_{CC} , or GND) is long, be sure to connect capacitors with adequate capacity for power line stabilization.

7. Current limiter

The current limiter turns off the sink side output transistor when the output current-set current value (limiter value) is reached. The output current is limited by the limit value. The RF pin is used to detect the output current. The output current is detected as voltage by connecting resistor R_f between RF pin and GND. When the RF pin voltage reaches 0.5 V (typ), the current limiter operates so that the output current is limited to the $0.5/R_f$ -set limiter value.

7-1. Output off time

The current limiter is so designed that current limit function turns on to turn off the sink side output transistor and then turn on the transistor again after off period of a fixed time (output off time) has elapsed. Since the LB1694N uses this output switching method for the current limiter, it is hardly necessary to consider ASO in current limiter operated mode as compared with the output unsaturated current limited one. The output off time depends on charge time of capacitor C connected to the C pin. When the current limiter turns on, C begins charging and the output is kept off until C is charged up to 2 V (typ). When C has been charged up to 2 V, the sink side output turns on again. The C charging current is a constant-regulated current which depends on resistor R connected to the R pin. The C charging current I_{CL} and output off time t_{off} are calculated as follows:

$$I_{CL} = 1.3/R$$
 (R must be set to be 13 k Ω and 100 k Ω .)
 $t_{off} = C/I_{CL} \times 2.0$
 $= 1.53 \times R \times C$

7-2. Output current neglect time

While the current limiter turns on and the sink side output is off, the regeneration current flows through the external diode used for absorbing the regeneration current above the output that was turned off. After the output off time elapses and the sink side output is turned on again, reverse current flows momentarily through the external diode (for the diode's reverse recovery time), causing the current that reaches the limiter value to flow momentarily through the output. Because this current will cause current limiter to turn on again, turning off the output, the average current decreases, causing the torque to be decreased at motor start-up, etc. Therefore, in order to prevent this current from being detected, the current limiter is designed so that the output current is not detected for a fixed period of time after the sink side output is turned on again. This length of time is the output current neglect time. The output current neglect time is determined by the discharge time of the capacitor C connected to the C pin. When current limiter turns on and C charges to 2 V, C begins discharging, and the output current neglect time is the time it takes for C to discharge to the point where the voltage at C is 0.4 V (typ). The C discharge current is a constant current, and is set at about 3 times charge current I_{CL} , As a result, the output current neglect time is about 1/3 of the output off time. The C discharge current I_{CH} and the output current neglect time t_{sm} are determined according to the following equations:

$$\begin{split} I_{CL} & \doteq 1.3/R \times 3 \\ t_{sm} & \doteq C/I_{CL} \times 1.6 \\ & \doteq 0.41 \times R \times C \end{split}$$

Because there is a slope to the time at which the sink side output is turned on again, the reverse current is not very large, even if a rectifier diode (a diode in which the reverse recovery time is not short) is used as the external diode for absorbing the regeneration current in the current limiter.

7-3. Output off time setting

It is necessary to set the output off time to a suitable level for the type of motor being used. (The output off time is set by the external resistors connected to the R pin, and by the external capacitor connected to the C pin.) Fig. 1 shows the current limiter operation waveform.

(1) When the output off time is set short

The output current neglect time is set by a circuit within the IC to about 1/3 of the output off time. Therefore, if the output off time is set to a very short length of time, the output current neglect time may not be adequate. If the output current neglect time is inadequate, the current limiter will turn on in response to reverse current from the external diode used to absorb the regeneration current. (Refer to Section 7-2.) Furthermore, if the output off time is short, the diode reverse current becomes large and ASO must be considered.

(2) When the output off time is set long

If the output off time is set to a very long length of time, the average current decreases, with the result that the torque at motor start-up drops. Depending on the type of motor, it may be impossible to shift from the current limiter operation state to the normal rotation state.

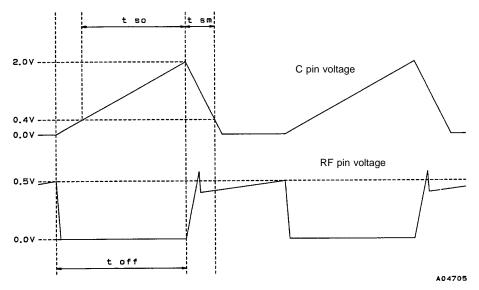


Fig. 1 Current Limiter Operation Waveform

Calculation of the IC's internal power dissipation Pd = (V_{CC} × I_{CC}) + (V_M × I_M) – (power dissipated by the motor coil)

9. Measuring the increase in the IC's temperature

Because the temperature of the IC chip cannot be measured directly, the temperature is normally measured using one of the following methods.

9-1. Measurement using a thermocouple

In order to measure the temperature by using a thermocouple, mount the thermocouple on the fin. Although this method of measurement is simple, if the rate of heat generation has not stabilized, the measurement error is great.

9-2. Measurement using the characteristics of a diode within the IC

It is recommended that the parasitic diode between FG1 and GND be used to measure the temperature of the IC. Set FG1 high (the "off" state), measure the parasitic diode voltage V_F , and calculate the temperature based on the temperature characteristics of the voltage V_F .

(Sanyo's data: $I_F = -1$ mA, V_F temperature characteristics: approximately -2 mV/ $^{\circ}$ C)

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