
HM5212325FBPC-B60

128M LVTTTL interface SDRAM
100 MHz
1-Mword × 32-bit × 4-bank
PC/100 SDRAM

HITACHI

ADE-203-1122C (Z)
Rev. 1.0
May. 12 , 2000

Description

The Hitachi HM5212325FBPC is a 128-Mbit SDRAM organized as 1048576-word × 32-bit × 4-bank. All inputs and outputs are referred to the rising edge of the clock input. It is packaged in standard 90-bump fine pitch BGA.

Features

- Single chip wide bit solution (× 32)
- 3.3 V power supply
- Clock frequency: 100 MHz (max)
- LVTTTL interface
- Extremely small foot print: 0.8 mm pitch
 - Package: FBGA (BP-90)
- 4 banks can operate simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length: 4/8/full page
- 2 variations of burst sequence
 - Sequential (BL = 4/8/full page)
 - Interleave (BL = 4/8)
- Programmable $\overline{\text{CAS}}$ latency: 2/3
- Byte control by DQMB
- Refresh cycles: 4096 refresh cycles/64 ms

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- 2 variations of refresh
 - Auto refresh
 - Self refresh
- Full page burst length capability
 - Sequential burst
 - Burst stop capability

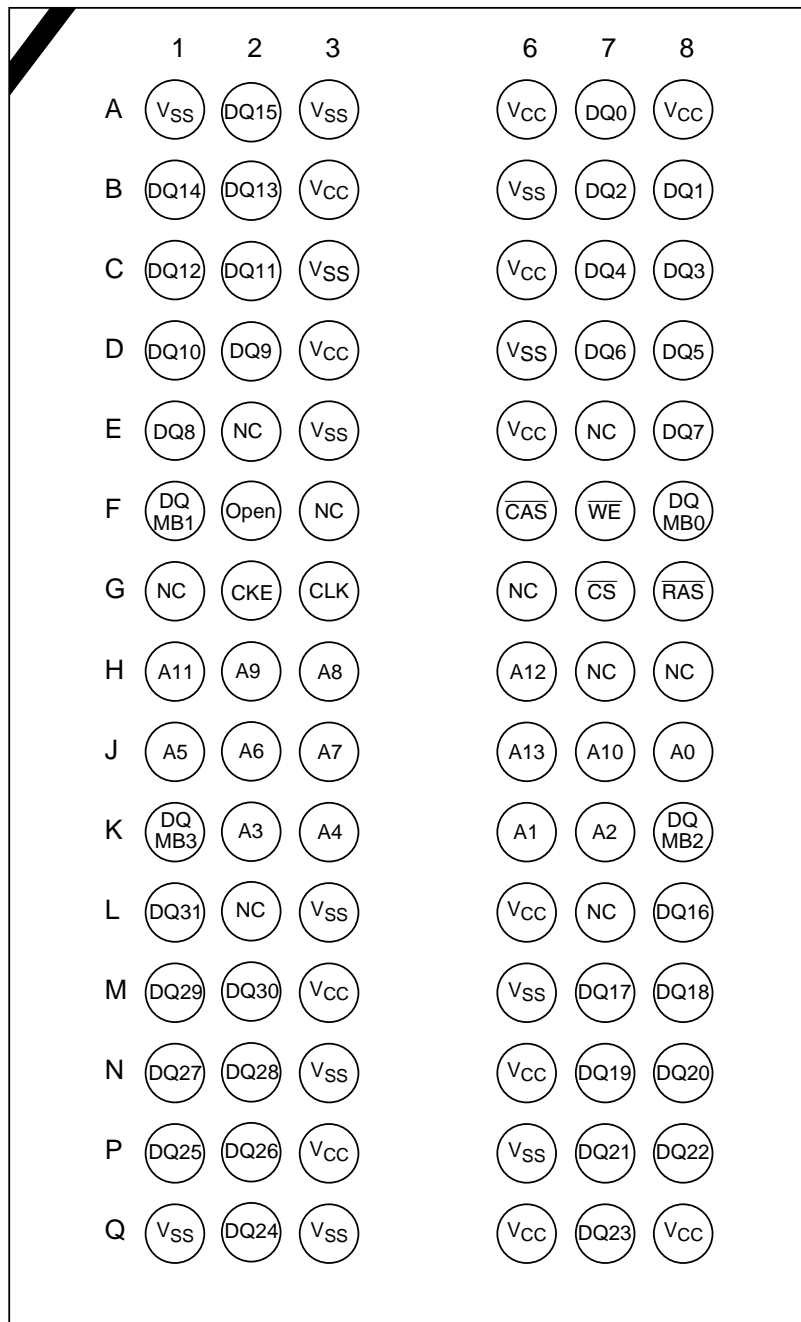
Ordering Information

Type No.	Frequency	$\overline{\text{CAS}}$ latency	Package
HM5212325FBPC-B60*	100 MHz	3	10 mm × 13 mm 90 bump FBGA (BP-90)

Note: 66 MHz operation at $\overline{\text{CAS}}$ latency = 2.

Pin Arrangement

90-bump FBGA



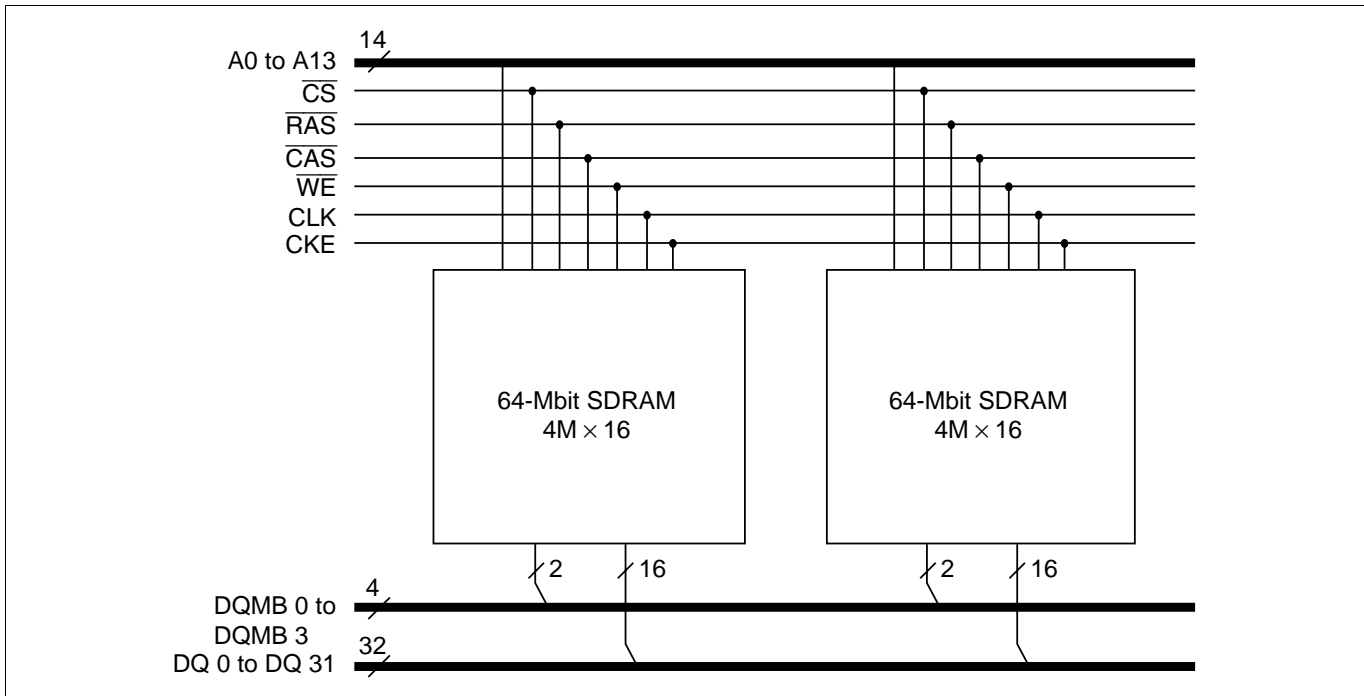
(Top view)

Pin Description

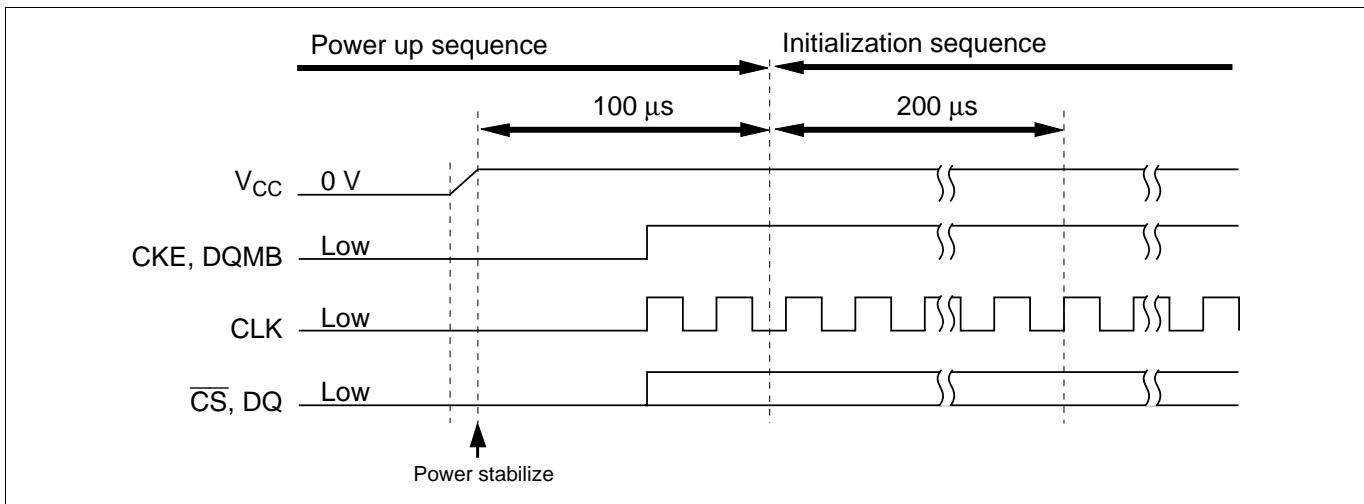
Pin name	Function
A0 to A13	Address input Row address A0 to A11 Column address A0 to A7 Bank select address A12/A13 (BS)
DQ0 to DQ31	Data-input/output
\overline{CS}	Chip select
\overline{RAS}	Row address strobe command
\overline{CAS}	Column address strobe command
\overline{WE}	Write enable
DQMB0 to DQMB3	Byte data mask*1
CLK	Clock input
CKE	Clock enable
V _{CC}	Power supply
V _{SS}	Ground
Open	Open*2

- Note:
1. DQMB0: DQ0 to DQ7
DQMB1: DQ8 to DQ15
DQMB2: DQ16 to DQ23
DQMB3: DQ24 to DQ31
 2. Don't connect. Internally connected with die.

Block Diagram



Power-up Sequence and Initialization Sequence



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	-0.5 to $V_{CC} + 0.5$ (≤ 4.6 (max))	V	1
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{out}	50	mA	
Operating temperature	T_{opr}	0 to +70 (T_j max = 110)	°C	
Storage temperature	T_{stg}	-55 to +125	°C	

Note: 1. Respect to V_{SS} .

DC Operating Conditions ($T_{case} = 0$ to +70°C [T_j max = 110°C])

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage	V_{CC}	3.0	3.6	V	1, 2
	V_{SS}	0	0	V	3
Input high voltage	V_{IH}	2.0	$V_{CC} + 0.3$	V	1, 4
Input low voltage	V_{IL}	-0.3	0.8	V	1, 5

Notes: 1. All voltage referred to V_{SS} .

2. The supply voltage with all V_{CC} pins must be on the same level.

3. The supply voltage with all V_{SS} pins must be on the same level.

4. V_{IH} (max) = $V_{CC} + 2.0$ V for pulse width ≤ 3 ns at V_{CC} .

5. V_{IL} (min) = $V_{SS} - 2.0$ V for pulse width ≤ 3 ns at V_{SS} .

DC Characteristics

 (T_{case} = 0 to +70°C [T_j max = 110°C]), V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

HM5212325F						
-B60						
Parameter	Symbol	Min	Max	Unit	Test conditions	Notes
Operating current ($\overline{\text{CAS}}$ latency = 2)	I _{CC1}	—	100	mA	Burst length = 1 t _{RC} = min	1, 2, 3
	($\overline{\text{CAS}}$ latency = 3)	I _{CC1}	—	110		
Standby current in power down	I _{CC2P}	—	6	mA	CKE = V _{IL} , t _{CK} = 12 ns	6
Standby current in power down (input signal stable)	I _{CC2PS}	—	4	mA	CKE = V _{IL} , t _{CK} = ∞	7
Standby current in non power down	I _{CC2N}	—	32	mA	CKE, $\overline{\text{CS}}$ = V _{IH} , t _{CK} = 12 ns	4
Standby current in non power down (input signal stable)	I _{CC2NS}	—	18	mA	CKE = V _{IH} , t _{CK} = ∞	9
Active standby current in power down	I _{CC3P}	—	8	mA	CKE = V _{IL} , t _{CK} = 12 ns	1, 2, 6
Active standby current in power down (input signal stable)	I _{CC3PS}	—	6	mA	CKE = V _{IL} , t _{CK} = ∞	2, 7
Active standby current in non power down	I _{CC3N}	—	40	mA	CKE, $\overline{\text{CS}}$ = V _{IH} , t _{CK} = 12 ns	1, 2, 4
Active standby current in non power down (input signal stable)	I _{CC3NS}	—	30	mA	CKE = V _{IH} , t _{CK} = ∞	2, 9
Burst operating current ($\overline{\text{CAS}}$ latency = 2)	I _{CC4}	—	110	mA	t _{CK} = min, BL = 4	1, 2, 5
	($\overline{\text{CAS}}$ latency = 3)	I _{CC4}	—	135		
Refresh current	I _{CC5}	—	190	mA	t _{RC} = min	3
Self refresh current	I _{CC6}	—	2	mA	V _{IH} ≥ V _{CC} - 0.2 V V _{IL} ≤ 0.2 V	8
Self refresh current (L-version)	I _{CC6}	—	0.8	mA		
Input leakage current	I _{LI}	-2	2	μA	0 ≤ Vin ≤ V _{CC}	
Output leakage current	I _{LO}	-3	3	μA	0 ≤ Vout ≤ V _{CC} DQ = disable	
Output high voltage	V _{OH}	2.4	—	V	I _{OH} = -4 mA	
Output low voltage	V _{OL}	—	0.4	V	I _{OL} = 4 mA	

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- Notes:
1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
 2. One bank operation.
 3. Input signals are changed once per one clock.
 4. Input signals are changed once per two clocks.
 5. Input signals are changed once per four clocks.
 6. After power down mode, CLK operating current.
 7. After power down mode, no CLK operating current.
 8. After self refresh mode set, self refresh current.
 9. Input signals are V_{IH} or V_{IL} fixed.

Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$)

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance (CLK)	C_{11}	4	8	pF	1, 2, 4
Input capacitance (Input except DQM)	C_{12}	4	8	pF	1, 2, 4
Input capacitance (DQM)	C_{13}	2	5	pF	1, 2, 4
Output capacitance (DQ)	C_O	2	5	pF	1, 2, 3, 4

- Notes:
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. Measurement condition: $f = 1\text{ MHz}$, 1.4 V bias, 200 mV swing.
 3. $DQMB = V_{IH}$ to disable Dout.
 4. This parameter is sampled and not 100% tested.

AC Characteristics

(T_{case} = 0 to +70°C [T_j max = 110°C]), V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

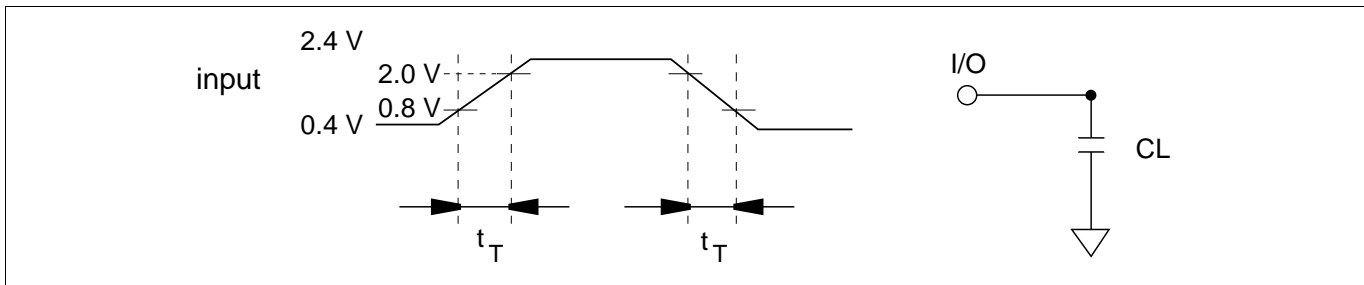
Parameter	HITACHI Symbol	PC/100 Symbol	HM5212325F		Unit	Notes
			Min	Max		
System clock cycle time ($\overline{\text{CAS}}$ latency = 2)	t _{CK}	Tclk	15	—	ns	1
	($\overline{\text{CAS}}$ latency = 3)	t _{CK}	Tclk	10	—	
CLK high pulse width	t _{CKH}	Tch	3	—	ns	1
CLK low pulse width	t _{CKL}	Tcl	3	—	ns	1
Access time from CLK ($\overline{\text{CAS}}$ latency = 2)	t _{AC}	Tac	—	8	ns	1, 2
	($\overline{\text{CAS}}$ latency = 3)	t _{AC}	Tac	6	ns	
Data-out hold time	t _{OH}	Toh	3	—	ns	1, 2
CLK to Data-out low impedance	t _{LZ}		2	—	ns	1, 2, 3
CLK to Data-out high impedance	t _{HZ}		—	6	ns	1, 4
Input setup time	t _{AS} , t _{CS} , t _{DS} , t _{CES}	Tsi	2	—	ns	1, 5, 6
CKE setup time for power down exit	t _{CESP}	Tpde	2	—	ns	1
Input hold time	t _{AH} , t _{CH} , t _{DH} , t _{CEH}	Thi	1	—	ns	1, 5
Ref/Active to Ref/Active command period	t _{RC}	Trc	70	—	ns	1
Active to Precharge command period	t _{RAS}	Tras	50	120000	ns	1
Active command to column command (same bank)	t _{RCD}	Trcd	20	—	ns	1
Precharge to active command period	t _{RP}	Trp	20	—	ns	1
Write recovery or data-in to precharge lead time	t _{DPL}	Tdpl	10	—	ns	1
Active (a) to Active (b) command period	t _{RRD}	Trrd	20	—	ns	1
Transition time (rise and fall)	t _T		1	5	ns	
Refresh period	t _{REF}		—	64	ms	

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- Notes:
1. AC measurement assumes $t_T = 1$ ns. Reference level for timing of input signals is 1.5 V.
 2. Access time is measured at 1.5 V. Load condition is $CL = 50$ pF.
 3. t_{LZ} (min) defines the time at which the outputs achieves the low impedance state.
 4. t_{HZ} (max) defines the time at which the outputs achieves the high impedance state.
 5. t_{CES} define CKE setup time to CLK rising edge except power down exit command.
 6. t_{AS}/t_{AH} : Address, t_{CS}/t_{CH} : \overline{CS} , \overline{RAS} , \overline{CAS} , \overline{WE} , DQM.
 t_{DS}/t_{DH} : Data-in, t_{CES}/t_{CEH} : CKE

Test Conditions

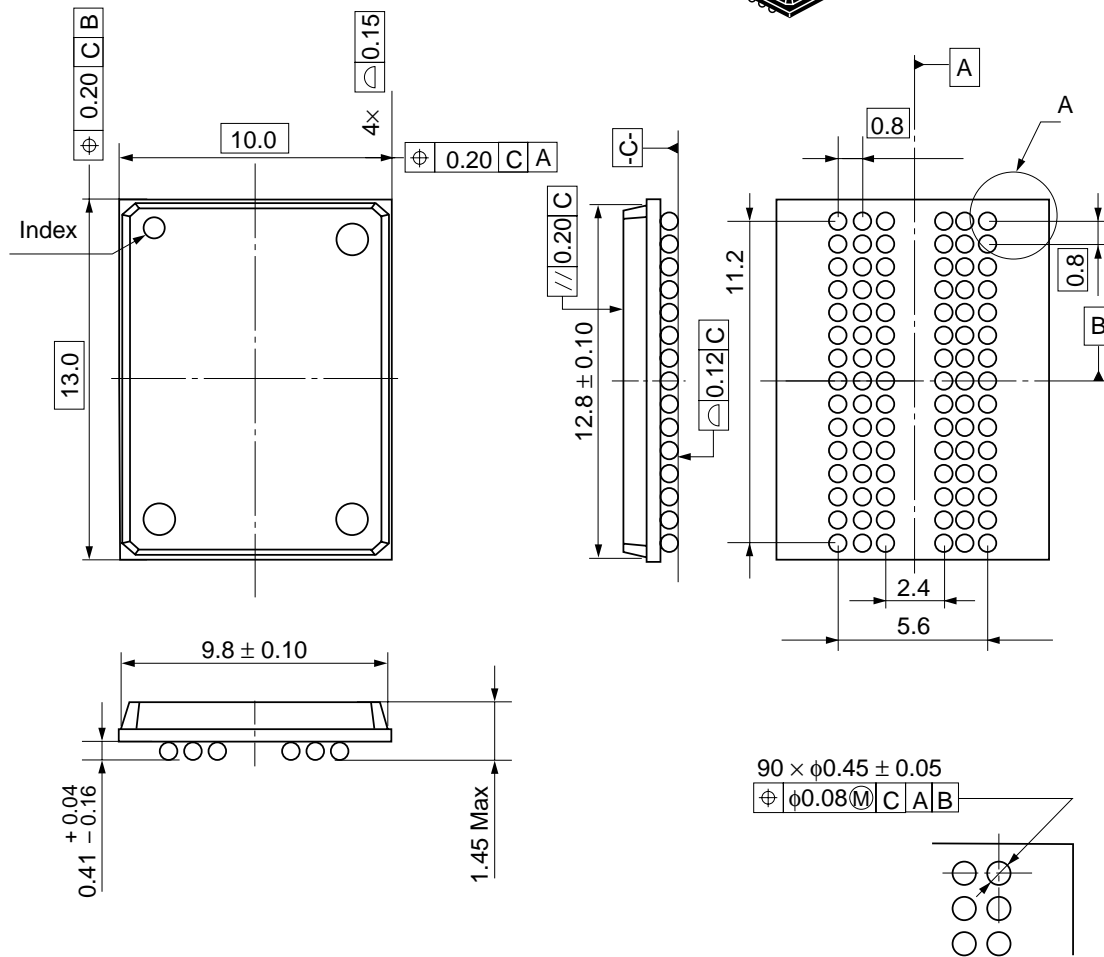
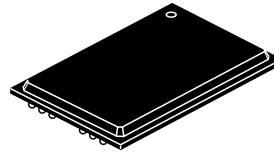
- Input and output timing reference levels: 1.5 V
- Input waveform and output load: See following figures



Package Dimensions

HM5212325FBPC (BP-90)

Unit: mm



Details of the part A

Hitachi Code	BP-90
JEDEC	—
EIAJ	—
Mass (reference value)	0.28 g

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Oct. 25, 1999	Initial issue	S. Hatano	S. Hatano
0.1	Jan. 7, 2000	Correct errors of pin arrangement Correct errors of DC Characteristics I _{LI} : -4/4 to -2/2 μ A I _{LO} : -6/6 to -3/3 μ A Package dimension Change tolerance value	Y. Kagaya	S. Hatano
0.2	Feb. 29, 2000	Capacitance C ₁₁ min: 5 pF to 4 pF C ₁₂ min: 5 pF to 4 pF C ₁₃ min: 2.5 pF to 2 pF C _O min: 3 pF to 2 pF	M. Nishimura	I. Hihara
1.0	May. 12, 2000	Package dimension Change of seated height		