FINAL

Am79C98

Twisted-Pair Ethernet Transceiver (TPEX)

DISTINCTIVE CHARACTERISTICS

- **CMOS device provides compliant operation and low operating current from a single +5 V supply**
- **Power Down mode provides reduced power consumption for battery-powered applications. Reset capability allows use in remote MAU applications.**
- **Pin-selectable twisted-pair receive polarity detection and automatic inversion of the receive signal. Polarity indication output pin can directly drive an LED.**
- **Pin-selectable twisted-pair Link Integrity Test capability conforming to the IEEE 802.3 standard for 10BASE-T. Link status pin can directly drive an LED.**
- **Internal twisted-pair transmitter digital predistortion circuit reduces medium-induced jitter and ensures compliance with the 10BASE-T transmit and receive waveform requirements**
- **Pin-selectable SQE Test (heartbeat) enable**
- **Transmit and receive status indications are available on separate, dedicated pins**
- **AUI loopback, Jabber Control, and SQE Test functions comply with the 10BASE-T standard IEEE Std 802.3i-1990**

GENERAL DESCRIPTION

The Am79C98 Twisted-Pair Ethernet Transceiver (TPEX) is an integrated circuit that implements the medium attachment unit (MAU) functions for the twisted-pair medium, as specified by the IEEE 802.3 standard (Type 10BASE-T). This device provides the necessary electrical and functional interface between the IEEE 802.3 standard attachment unit interface (AUI) and the twisted-pair cable.

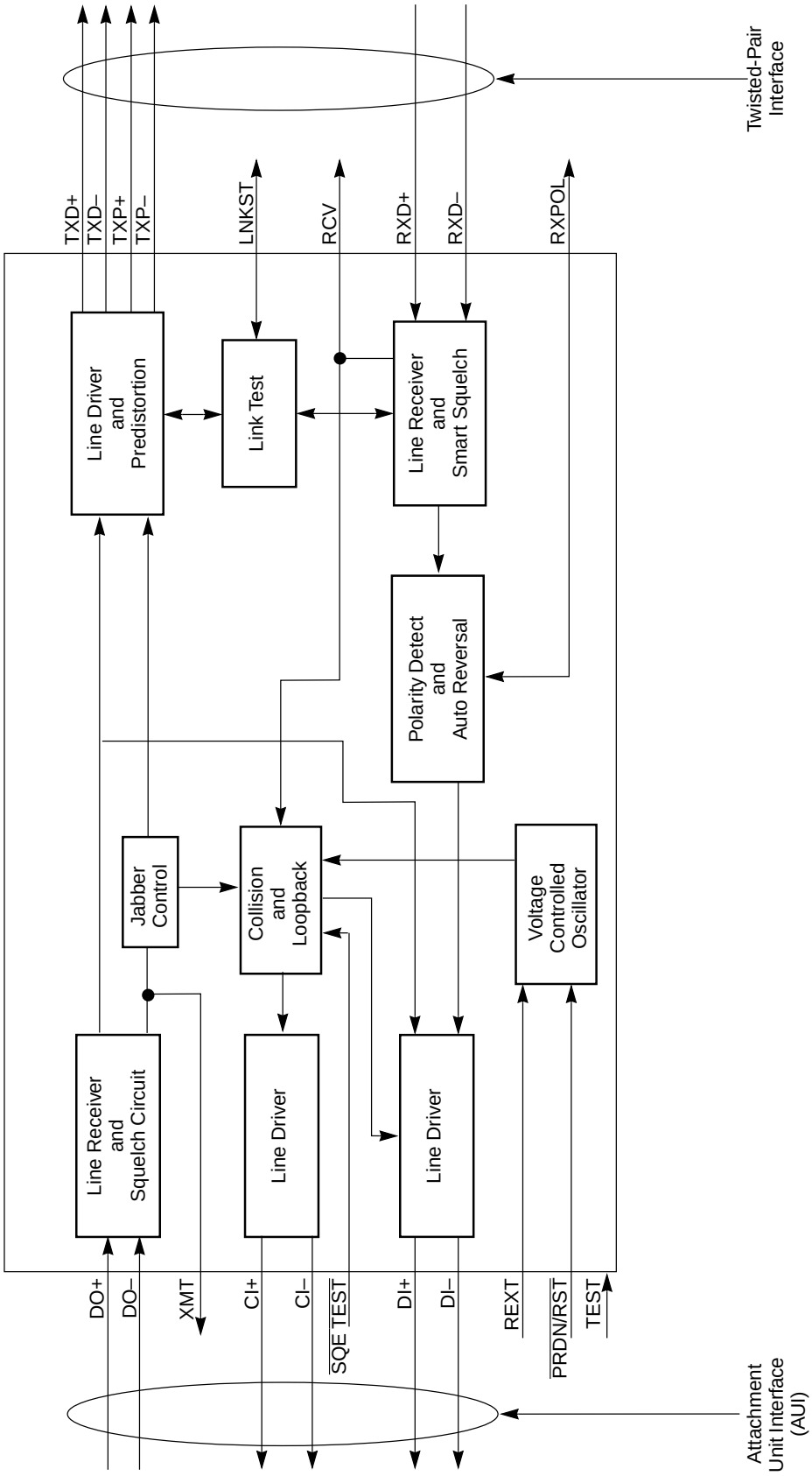
A network based on the 10BASE-T standard can use unshielded twisted-pair cables, providing an economical solution to networking by allowing the use of existing telephone wiring. The Am79C98 provides a minimal component count and cost-effective solution to the design and implementation of 10BASE-T standard networks.

TPEX provides twisted-pair driver and receiver circuits, including on-board transmit digital predistortion, receiver squelch, and an AUI port with pin-selectable SQE Test enable. The device also provides a number of additional features, including pin-selectable Twisted-Pair Receive Polarity Detection and Automatic Polarity Reversal, Link Status indication, Link Test disable function, and transmit and receive status. The Twisted-Pair Polarity and Link Status pins can be used to drive LEDs directly.

The Am79C98 is fabricated in CMOS technology and requires a single +5 V supply. The device is available in 24-pin SKINNYDIP® plastic dual in-line and 28-pin plastic leaded chip carrier (PLCC) packaging.

Publication# **14395** Rev: **D** Amendment/**0**
Issue Date: **May 1994**

BLOCK DIAGRAM



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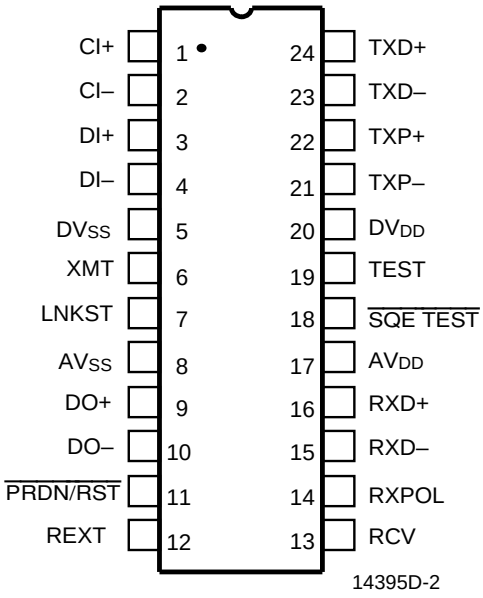
RELATED AMD PRODUCTS

Part No.	Description
Am7996	IEEE-802.3/Ethernet/Cheapernet Tap Transceiver
Am79C100	Twisted-Pair Ethernet Transceiver Plus (TPEX+)
Am79C90	CMOS Local Area Network Controller for Ethernet (C-LANCE)
Am79C900	Integrated Local Area Communications Controller™ (ILACC™)
Am79C940	Media Access Controller for Ethernet (MACE™)
Am79C960	PCnet-ISA Single-Chip Ethernet Controller (for ISA bus)
Am79C961	PCnet-ISA+ Single-Chip Ethernet Controller (with Microsoft® Plug n' Play support)
Am79C965	PCnet-32 Single-Chip Ethernet Controller (for 386DX, 486 and VL buses)
Am79C970	PCnet-PCI Single-Chip Ethernet Controller (for PCI bus)
Am79C974	PCnet-SCSI Combination Ethernet and SCSI Controller for PCI Systems
Am79C981	Integrated Multiport Repeater Plus™ (IMR+™)
Am79C987	Hardware Implemented Management Information Base™ (HIMIB™)

CONNECTION DIAGRAM

Top View

DIP



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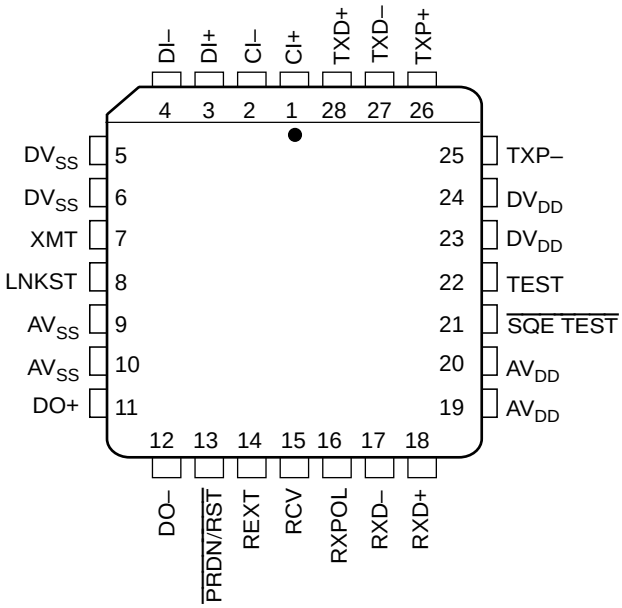
Note:
Pin 1 is marked for orientation

PLCC



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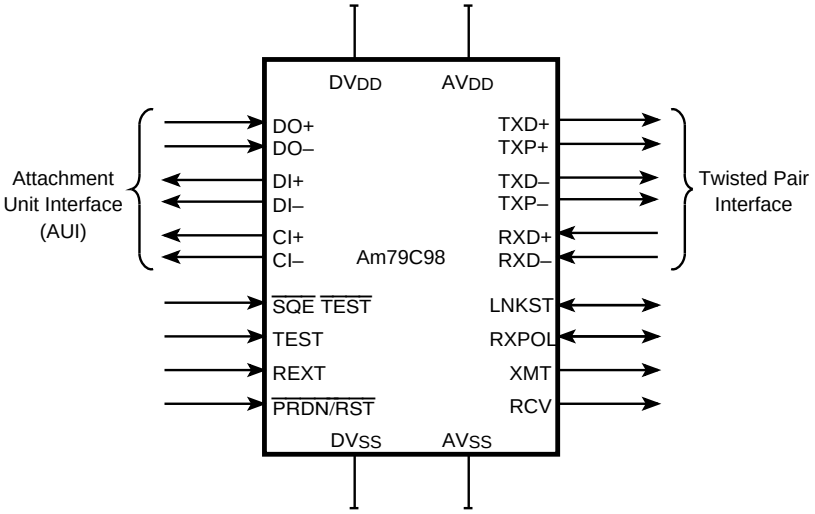
LOGIC SYMBOL



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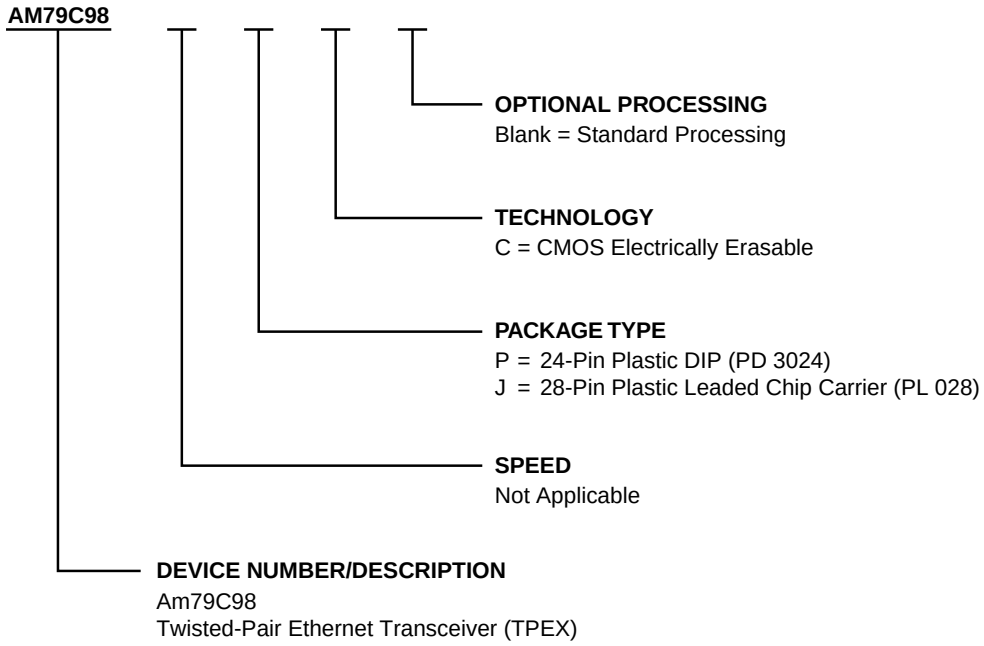
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (valid combination) is formed by a combination of the elements below.



Valid Combinations	
AM79C98	PC, JC

Valid Combinations

Valid combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTION

AV_{DD}

Analog Power

This pin supplies +5 V to analog portions of the TPEX circuitry.

AV_{SS}

Analog Ground

This pin is the ground reference for analog portions of the TPEX circuitry.

CI+, CI–

Control In
Output

AUI port differential driver.

DI+, DI–

Data In
Output

AUI port differential driver.

DO+, DO–

Data Out
Input

AUI port differential receiver.

DV_{DD}

Digital Power

This pin supplies +5 V to digital portions of the TPEX circuitry.

DV_{SS}

Digital Ground

This pin is the ground reference for digital portions of TPEX circuitry.

LNKST

Link Status
Open Drain, Input/Output

When this pin is tied LOW, the internal Link Test Receive function is disabled and the Transmit and Receive functions will remain active irrespective of arriving idle Link Test pulses and data. TPEX continues to generate idle Link Test pulses irrespective of the status of this pin.

As an output, this pin is driven LOW if the link is identified as functional. However, if the link is determined to be nonfunctional, due to missing idle Link Test pulses or data packets, then this pin is not driven. In the LOW output state, the pin is capable of sinking a maximum of 16 mA and can be used to drive an LED.

This pin is internally pulled HIGH when inactive.

$\overline{PRDN/RST}$

Power Down/Reset
Input, Active LOW

Driving this input LOW resets the internal logic of TPEX and places the device in a special Power Down mode. In the Power Down/Reset mode, all output drivers are placed in their inactive state.

RCV

Receive
Output

This pin is driven HIGH while TPEX is receiving data on the RXD pins and is transferring the received signal onto the AUI DI pair. The RCV and XMT pins are simultaneously driven HIGH during collision.

REXT

External Resistor
Input

An external precision resistor is connected between this pin and AV_{DD} in order to provide a voltage reference for the internal voltage-controlled oscillator (VCO).

RXD+, RXD–

Receive Data
Input

10BASE-T port differential receivers.

RXPOL

Receive Polarity
Open Drain, Input/Output

The twisted-pair receiver is capable of detecting a receive signal with reversed polarity (wiring error). The RXPOL pin is normally in the LOW state, indicating correct polarity of the received signal. If the receiver detects reversed polarity, then this pin is not driven (goes HIGH) and the polarity of subsequent packets is inverted. In the LOW output state, this pin can sink up to a maximum of 16 mA and is therefore capable of driving an LED.

This feature can be disabled by strapping this pin LOW. In this case, the Receive Polarity correction circuit is disabled and the internal receive signal remains noninverted, irrespective of the received signal.

This pin is internally pulled HIGH when inactive.

$\overline{SQE\ TEST}$

Signal Quality Test (Heartbeat) Enable
Input, Active LOW

The SQE Test function is enabled by tying this input LOW.

This input is internally pulled HIGH when inactive.

TEST

Test
Input, Active HIGH

This pin should be tied HIGH for normal operation. If this pin is driven LOW, TPEX will enter Loopback Test mode. The type of loopback is determined by the state of the $\overline{\text{SQE TEST}}$ pin. If this pin is in the LOW state (Station MAU), TPEX transfers data independently from DO to the TXD/TXP circuit and from RXD to the DI circuit. If the $\overline{\text{SQE TEST}}$ is in the HIGH state (Repeater MAU), then data on the RXD circuit is transmitted back onto the TXD/TXP circuit and data on the DO circuit is transmitted onto the DI pair.

TXD+, TXD–

Transmit Data
Output

10BASE-T port differential drivers.

TXP+, TXP–

Transmit Predistortion
Output

Transmit waveform predistortion control.

XMT

Transmit
Output

This pin is driven HIGH while TPEX is receiving data on the AUI DO pair and is transmitting data on the TXD/TXP pins. The XMT and RCV pins are simultaneously driven HIGH during collision.

FUNCTIONAL DESCRIPTION

The Twisted-Pair Ethernet Transceiver (TPEX) complies with the requirements specified by the IEEE 802.3 standard for the attachment unit interface (AUI) and the standard for 10BASE-T medium attachment unit (MAU). TPEX also implements a number of features in addition to the IEEE 802.3 standard. An outline of functions implemented by the Am79C98 is given below.

Attachment Unit Interface (DO+/–, DI+/–, CI+/–)

The AUI electrical and functional characteristics comply with those specified by the IEEE 802.3, Sections 7 and 14 (drafted). The AUI pins can be wired directly to the isolation transformer, for a remote MAU application, or to another device (e.g., Am7992 serial interface adapter). The end-of-packet SQE Test function (heartbeat) can be disabled to allow the device to be employed in a repeater application.

Twisted-Pair Transmit Function

Data transmission to the 10BASE-T medium occurs when valid AUI signals appear on the DO+/–differential pair. This data stream is routed to the differential driver circuitry in the TXD+/– pins. The driver circuitry provides necessary electrical driving capability and predistortion control for transmitting signals over maximum-length twisted-pair cable, as specified by the IEEE 802.3 10BASE-T standard. The transmit function meets the propagation delays and jitter specified by the standard. During transmission, the XMT pin is driven HIGH and can be used for status information.

Twisted-Pair Receive Function

The receiver complies with the receiver specifications of the IEEE 802.3 10BASE-T standard, including noise immunity and received signal rejection criteria (“Smart Squelch”). Signals meeting these criteria appearing at the RXD+/– differential input pair are routed to the DI+/– outputs. The receiver function meets the propagation delays and jitter requirements specified by the standard. Receiver squelch level drops to approximately half its threshold value after unsquelch to allow reception of minimum amplitude signals and to offset carrier fade in the event of worst-case signal attenuation and crosstalk noise conditions. During receive, the RCV pin is driven HIGH and can be used for status information.

Link Test Function

The Link Test function is implemented as specified by the IEEE 802.3 10BASE-T standard. During periods of transmit pair inactivity, Link Test pulses will be periodically sent over the twisted-pair medium to allow constant monitoring of medium integrity. When the Link Test function is enabled, the absence of Link Test pulses on the RXD+/– pair will cause the TPEX to go into a Link Fail state. In Link Fail state, data transmission, data reception, and the collision detection functions are disabled, and remain disabled until valid data or >2 consecutive Link Test pulses appear on the RXD+/– pair. During Link Fail, the LNKST pin is internally pulled HIGH. When the link is identified as functional, the LNKST pin is driven LOW and is capable of directly driving a “link OK” LED. In order to interoperate with systems that do not implement Link Test, this function can be disabled by grounding the LNKST pin. When disabled, the driver and receiver functions remain enabled irrespective of the presence or absence of data or Link Test pulses on the RXD+/– pair. The transmitter continues to generate Link Test pulses in the absence of transmit data even if the Link Test function is disabled.

Polarity Detection and Reversal

The TPEX receive function includes the ability to invert the polarity of the signals appearing at the RXD± pair if the polarity of the received signal is reversed (such as in the case of a wiring error). This feature allows data packets received from a reverse-wired RXD± input pair to be corrected in the TPEX prior to transfer to the DTE via the AUI interface (DI±). The polarity detection function is activated following reset or Link Fail, and will reverse the receive polarity based on both the polarity of any previous Link Test pulses and the polarity of subsequent packets with a valid end transmit delimiter (ETD).

When in the Link Fail state, TPEX will recognize Link Test pulses of either positive or negative polarity. Exit from the Link Fail state is caused by the reception of five to six consecutive Link Test pulses of identical polarity. On entry to the Link Pass state, the polarity of the last five Link Test pulses is used to determine the initial receive polarity configuration and the receiver is reconfigured to subsequently recognize only Link Test pulses of the previously established polarity. This link pulse algorithm is employed only until ETD polarity determination is made, as described later in this section.

Positive Link Test pulses are defined as received signals with a positive amplitude greater than 520 mV and a pulse width of 60 ns to 200 ns. This positive excursion may be followed by a negative excursion. This definition is consistent with the expected received signal at a correctly wired receiver when a Link Test pulse that fits the template of Figure 14-12 in the 10BASE-T standard is generated at a transmitter and passed through 100 m of twisted-pair cable.

Negative Link Test pulses are defined as received signals with a negative amplitude greater than 520 mV and a pulse width of 60 ns to 200 ns. This negative excursion may be followed by a positive excursion. This definition is consistent with the expected received signal at a reverse wired receiver when a Link Test pulse that fits the template of Figure 14-12 in the 10BASE-T

standard is generated at a transmitter and passed through 100 m of twisted-pair cable.

The polarity detection/correction algorithm will remain "armed" until two consecutive packets with valid ETD of identical polarity are detected. When "armed," the receiver is capable of changing the initial or previous polarity configuration based on the most recent ETD polarity.

On receipt of the first packet with valid ETD following reset or Link Fail, TPEX will utilize the inferred polarity information to configure its RXD± input, regardless of its previous state. On receipt of a second packet with a valid ETD with correct polarity, the detection/correction algorithm will "lock in" the initial polarity. If the second (or subsequent) packet is not detected as confirming the previous polarity decision, the most recently detected ETD polarity will be used as the new default. Note that packets with invalid ETD have no effect on updating the previous polarity decision. Once two consecutive packets with valid ETD have been received, TPEX will disable the detection/correction algorithm until either a Link Fail condition occurs or $\overline{\text{PRDN/RST}}$ is asserted.

During polarity reversal, the RXPOL pin is internally pulled HIGH. During normal polarity conditions, the RXPOL pin is driven LOW and is capable of directly driving a "Polarity OK" LED using an integrated 16 mA driver. If desired, the polarity reversal function can be disabled by grounding the RXPOL pin.

Twisted-Pair Interface Status

Two outputs (XMT and RCV) indicate whether TPEX is transmitting (AUI to twisted-pair) or receiving (twisted-pair to AUI). Both signals are asserted during a collision. In Link Fail mode, RCV is disabled. In Jabber Detect mode, XMT is disabled. Both signals are active HIGH.

Collision Detect Function

Simultaneous carrier sense (presence of valid data signals) by both the AUI DO+/– pair and the RXD+/– pair constitutes a collision, thereby causing a 10 MHz signal to be asserted on the CI+/– output pair. The CI+/– output meets the drive requirements for the AUI. This 10 MHz signal will remain on the CI+/– pair until one of the two colliding states changes from active to idle. The CI+/– output pair stays HIGH for two bit times at the end of a collision, decreasing to the idle level within eighty bit times after the last LOW-to-HIGH transition. Both the XMT and RCV pins are driven HIGH during collision.

Signal Quality Error (SQE) Test (Heartbeat) Function

When the $\overline{\text{SQE TEST}}$ pin is driven LOW, TPEX will routinely exercise the collision detection circuitry by generating an SQE message at the end of every transmission. This signal is a self-test indication to the DTE that the MAU collision circuitry is functional. An SQE message consists of a 10 MHz signal on the CI+/– pair with a duration of 8 bit times (800 ns). When enabled, an SQE Test will occur at the end of every transmission, starting eight bit times (800 ns) after the last transition of the transmitted signal. For repeater applications, the SQE Test function can be disabled by tying the $\overline{\text{SQE TEST}}$ pin HIGH or by leaving it disconnected.

Jabber Function

The Jabber function inhibits the twisted-pair transmit function of TPEX if the DO+/– circuit is active longer than the time permitted to transmit the maximum-length 802.3/Ethernet data packet (50 ms nominal). This prevents any one node from disrupting the network due to a "stuck on" or faulty transmitter. If this maximum transmit time is exceeded, TPEX transmitter circuitry is disabled and a 10 MHz signal is driven onto the CI+/– pair. Once the transmit data stream is removed from the DO+/– pair of inputs, an "unjab" time of 250 ms to 750 ms will elapse before TPEX removes the 10 MHz signal from the CI+/– pair and re-enables the transmit path.

Power Down

In addition to on-board power-on-reset circuitry, the $\overline{\text{PRDN/RST}}$ pin is used as the master reset for TPEX. $\overline{\text{PRDN/RST}}$ must be driven LOW for a minimum of two microseconds for reset to occur. The $\overline{\text{PRDN/RST}}$ pin can also be used to put the TPEX into an inactive state, causing the device to consume less power. This feature is useful in battery-powered or low-duty-cycle systems. Driving $\overline{\text{PRDN/RST}}$ LOW resets the internal logic of TPEX and places the device into idle mode. In this mode, the twisted-pair driver pins (TXD+/–,TXP+/–) are driven LOW, the AUI pins (CI+/–, DI+/–) are driven HIGH, the LNKST and RXPOL pins are in the inactive state, and XMT and RCV are LOW. TPEX will remain in idle as long as $\overline{\text{PRDN/RST}}$ is asserted. Following the rising edge of the signal on $\overline{\text{PRDN/RST}}$, TPEX will remain in the reset state for 10 µs.

Test Modes

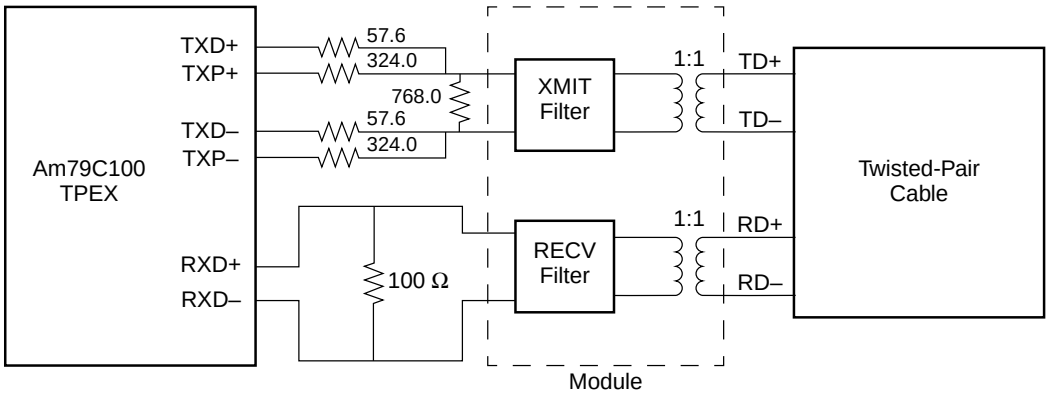
TPEX implements two types of loopback test modes suitable for Station (DTE) or Repeater applications. The Test mode is entered by driving the TEST pin HIGH. The two types of test modes available are:

1. **Station (DTE):** $\overline{\text{SQE TEST}}$ pin LOW. Data on DO+/– pair is transmitted onto the TXD+/– and TXP+/– pairs and data on the RXD+/– input pair is transmitted onto the DI+/– output pair. The jabber function and collision detection functions are disabled.
2. **Repeater:** $\overline{\text{SQE TEST}}$ pin HIGH. Data on DO+/– pair is looped back onto the DI+/– pair and data on the RXD+/– pair is retransmitted on the twisted-pair drivers (TXD+/– and TXP+/– pairs).

In both modes, the jabber circuitry, collision detection, and collision oscillator functions are disabled and the AUI and RXD+/– squelch circuits are active.

TPEX External Components

Figure 1 shows a typical twisted-pair port external components schematic. The resistors used should have a ±1% tolerance to ensure interoperability with 10BASE-T-compliant networks. Filters and pulse transformers are necessary devices that have a major influence on the performance and compliance of a TPEX-based MAU. Specifically, the transmitted waveforms are heavily influenced by filter characteristics and the twisted-pair receivers employ several criteria to continuously monitor the incoming signal's amplitude and timing characteristics to determine when and if to assert the internal carrier sense. For these reasons, it is crucial that the values and tolerances of the external components be as specified. Several manufacturers produce a module that combines the functions of the transmit and receive filters and the pulse transformers into one package.



Note:
The filter/transformer module shown is available from the following manufacturers: Belfuse, TDK, Pulse Engineering, PCA, Valor Electronics, and Nano Pulse.

Figure 1. Typical Twisted-Pair Port External Components

TYPICAL APPLICATIONS

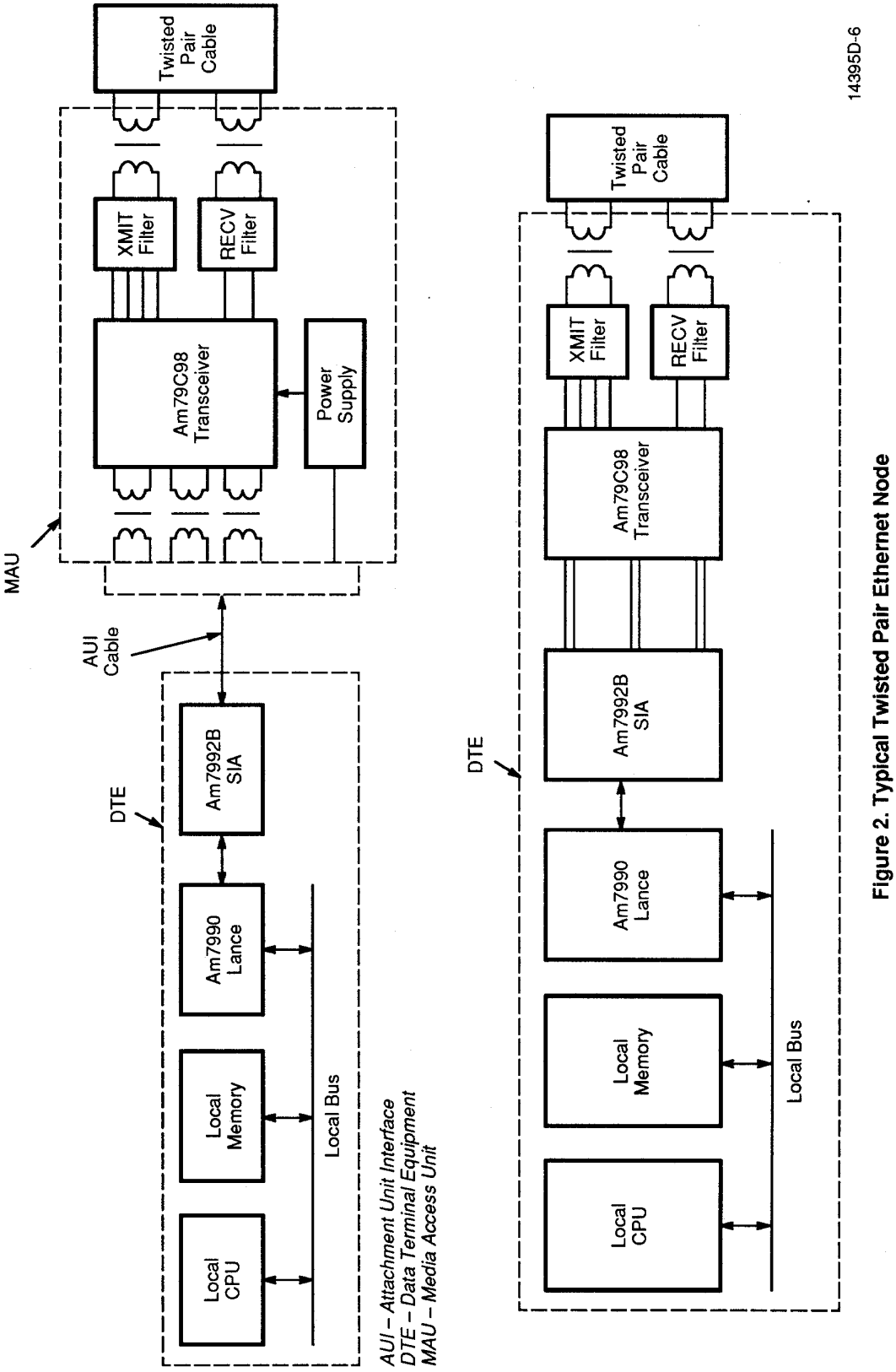


Figure 2. Typical Twisted Pair Ethernet Node

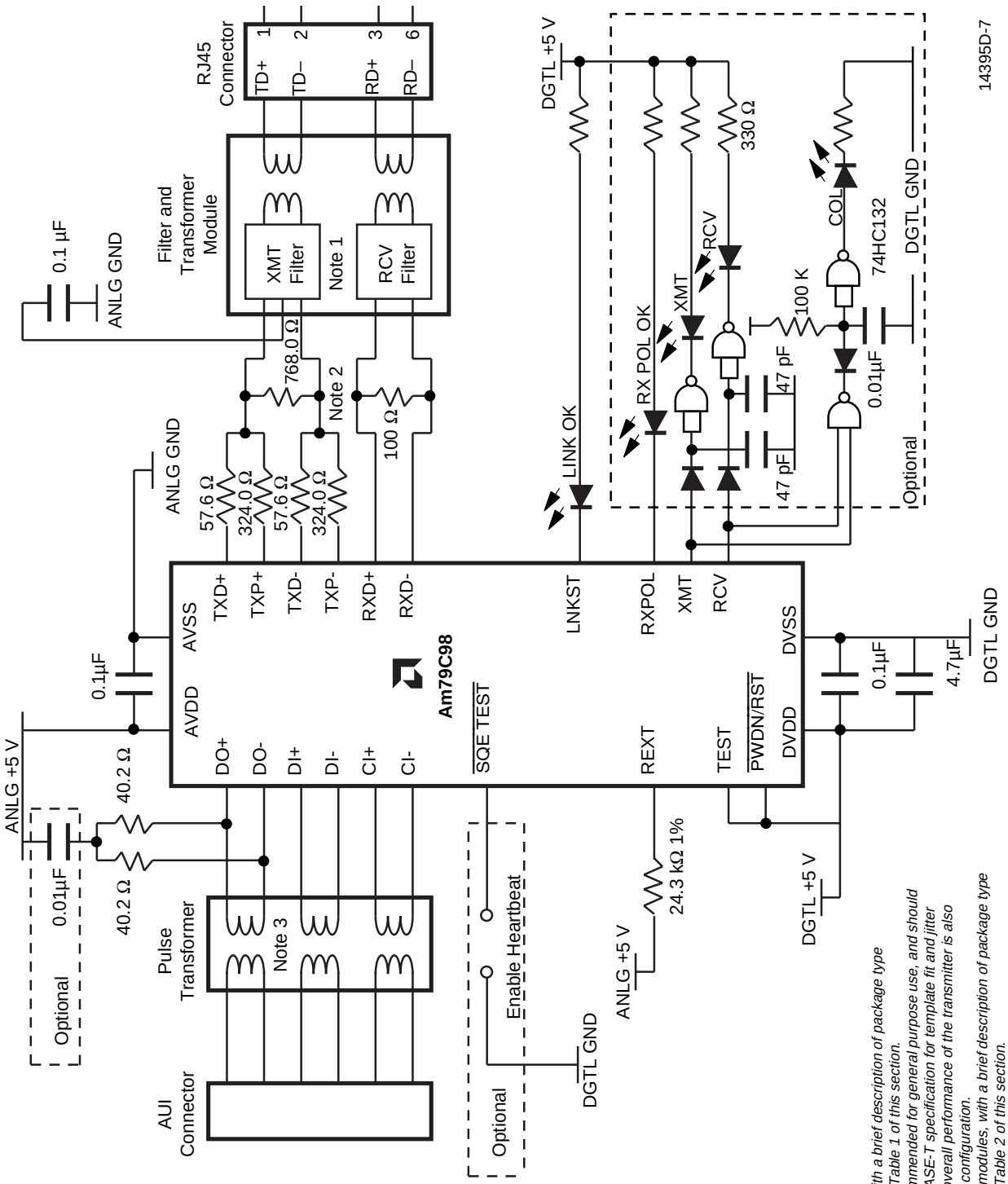


Figure 3. Typical TPEX System Application

Notes:

1. *Compatible filter modules, with a brief description of package type and features are included in Table 1 of this section.*
2. *The resistor values are recommended for general purpose use, and should allow compliance to the 10BASE-T specification for template fit and jitter performance. However, the overall performance of the transmitter is also affected by the transmit filter configuration.*
3. *Compatible AUI transformer modules, with a brief description of package type and features are included in Table 2 of this section.*

Table 1. TPEX Compatible Media Interface Modules

Manufacturer	Part #	Package	Description
Bel Fuse	A556-2006-DE	16-pin 0.3” DIL	Transmit and receive filters and transformers
Bel Fuse	0556-2006-00	14-pin SIP	Transmit and receive filters and transformers
Bel Fuse	0556-2006-01	14-pin SIP	Transmit and receive filters, transformers and common mode chokes
Valor Electronics	PT3877	16-pin 0.3” DIL	Transmit and receive filters and transformers
Valor Electronics	PT3983	8-pin 0.3” DIL	Transmit and receive common mode chokes
Valor Electronics	FL1012	16-pin 0.3” DIL	Transmit and receive filters and transformers, transmit common mode choke
Nano pulse	NP6612	16-pin 0.3” DIL	Transmit and receive filters, transformers and common mode chokes
Nano pulse	NP6581	8-pin 0.3” DIL	Transmit and receive common mode chokes
Nano pulse	NP6696	24-pin 0.6” DIL	Transmit and receive filters, transformers and common mode chokes
TDK	TLA 470	14-pin SIP	Transmit and receive filters and transformers
TDK	HIM3000	24-pin 0.6” DIL	Transmit and receive filters, transformers and common mode chokes
Pulse Engineering	PE65421	16-pin 0.3” DIL	Transmit and receive filters and transformers
Pulse Engineering	SUPRA 1.1	16-pin 0.5” DIL	Transmit and receive filters and transformers, transmit common mode choke
Bel Fuse	0556-6392-00	16-pin 0.5” DIL	Transmit and receive filters, transformers, and common mode chokes

Table 2. Am79C98 TPEX Compatible AUI Transformers

Manufacturer	Part #	Package	Description
Bel Fuse	A553-0506-AB	16-pin 0.3” DIL	50 µH
Valor Electronics	LT6031	16-pin 0.3” DIL	50 µH
TDK	TLA 100-3E	16-pin 0.3” DIL	100 µH
Pulse Engineering	PE64106	16-pin 0.3” DIL	50 µH

ABSOLUTE MAXIMUM RATINGS

Storage Temperature: . . . . . -65°C to +150°C

Ambient Temperature Under Bias: . . . . 0°C to +70°C

Supply Voltage to AV_{SS} or DV_{SS} (AV_{DD}, DV_{DD}): . . . . . –0.3 V to +6 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A): . . . . . 0°C to +70°C

Supply Voltages (AV_{DD}, DV_{DD}): . . . . . +5 V ± 5%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Digital Input Voltage					
V_{IL}	Input LOW Voltage		DV_{SS}-0.5	0.8	V
V_{IH}	Input HIGH Voltage		2.0	0.5 + DV_{DD}	V
Digital Output Voltage					
V_{OL}	Output LOW Voltage	I_{OL1} = 16 mA (Open drain) I_{OL2} = 4.0 mA		0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = -0.4 mA	2.4		V
Digital Input Leakage Current					
I_{ILL}	Input Leakage Current	0 < V_{IN} < DV_{DD} + 0.5 V		10	µA
I_{ILD}	Input Leakage Current (Open drain pins, output inactive)	0 < V_{IN} < DV_{DD} + 0.5 V		500	µA
AUI					
I_{IAXD}	Input Current at DO+, DO-	-1 < Vin < AV_{DD} + 0.5 V	-500	500	µA
V_{AICM}	DO+/- Open Circuit Input Common Mode Voltage (Bias)	I_{IN} = 0 V	AV_{DD} - 3.0	AV_{DD} - 1.0	V
V_{AIDV}	Differential Mode Input Voltage Range (DO+/-)	AV_{DD} = 5 V	-2.5	+2.5	V
V_{ASQ}	DO+/- Squelch Threshold		160	-275	mV
V_{ATH}	DO+ Switching Threshold	(Note 1)	-35	+35	mV
V_{AOD}	Differential Output Voltage |(DI+) - (DI-)| OR |(CI+) - (CI-)|	R_L = 78 Ω	620	1100	mV
V_{AODI}	DI+/- & CI+/- Differential Output Voltage Imbalance	R_L = 78 Ω (Note 1)	-25	+25	mV
V_{AOD}OFF	DI+/- & CI+/- Differential Idle Output Voltage	R_L = 78 Ω	-40	+40	mV
I_{AOD}OFF	DI+/- & CI+/- Differential Idle Output Current	R_L = 78 Ω (Note 1)	-1	1	mA
V_{AOCM}	DI+/- & CI+/- Common Mode Output Voltage	R_L = 78 Ω	2.5	AV_{DD}	V

DC CHARACTERISTICS (continued)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Twisted Pair Interface					
I_{IRXD}	Input Current at RXD+/–	$AV_{SS} < V_{IN} < AV_{DD}$	–500	500	µA
R_{RXD}	RXD+/– Differential Input Resistance	(Note 1)	10		KΩ
V_{TIVB}	RXD+, RXD– Open Circuit Input Voltage (Bias)	I_{IN} = 0 mA	AV_{DD} - 3.0	AV_{DD} - 1.5	V
V_{TIDV}	Differential Mode Input Voltage Range (RXD+/–)	AV_{DD} = +5 V	–3.1	3.1	V
V_{TSQ+}	RXD Positive Squelch Threshold (Peak)	Sinusoid 5 MHz < f< 10 MHz	300	520	mV
$V_{TSQ–}$	RXD Negative Squelch Threshold (Peak)	Sinusoid 5 MHz < f< 10 MHz	–520	–300	mV
V_{THS+}	RXD Post-Squelch Positive Threshold (Peak)	Sinusoid 5 MHz < f< 10 MHz	150	293	mV
$V_{THS–}$	RXD Post-Squelch Negative Threshold (Peak)	Sinusoid 5 MHz < f< 10 MHz	–293	–150	mV
V_{RXDTH}	RXD Switching Threshold	(Note 1)	–60	60	mV
V_{TXH}	TXD+/– and TXP+/– Output HIGH Voltage	(Note 2) DV_{SS} = 0 V	DV_{DD} - 0.6	DV_{DD}	V
V_{TXL}	TXD+/– and TXP+/– Output LOW Voltage	(Note 2) DV_{DD} = +5 V	DV_{SS}	DV_{SS} + 0.6	V
V_{TXI}	TXD+/– and TXP+/– Differential Output Voltage Imbalance		–40	+40	mV
V_{TXOFF}	TXD+/– and TXP+/– Differential Idle Output Voltage	DV_{DD} = +5 V	–40	+40	mV
R_{TX}	TXD+/– and TXP+/– Differential Driver Output Impedance	(Note 1)		40	Ω
I_{IREXT}	Input Current at REXT Pin	R_{EXT} = 24.3K Ω ± 1% AV_{DD} = +5 V		120	µA
Power Supply Current					
I_{DD}	Power Supply Current (Transmitting 10 MHz Data) (Typical TP load)	$\overline{PRDN/RST}$ = HIGH		115	mA
	Power Supply Current (Transmitting 10 MHz Data) (No TP load)	$\overline{PRDN/RST}$ = HIGH		90	mA
I_{DDPRDN}	Power Supply Current in Power Down Mode	$\overline{PRDN/RST}$ = LOW		4	mA

SWITCHING CHARACTERISTICS over COMMERCIAL

Parameter Symbol	Parameter Description		Min	Max	Unit
Transmit Timing					
t_{PWODO}	DO Pulse Width Accept/Reject Threshold	$\|V_{IN}\| > \|V_{ASQ}\|$ (Note 3)	15	35	ns
t_{PWKDO}	DO Pulse Width Maintain/Turn-Off Threshold	$\|V_{IN}\| > \|V_{ASQ}\|$ (Note 4)	105	200	ns
t_{TON}	Transmit Start Up Delay			300	ns
t_{TSD}	Transmit Static Propagation Delay (DO to TXD)			120	ns
t_{DODION}	DO to DI Startup Delay			300	ns
t_{DODISD}	DO to DI Static Propagation Delay			100	ns
t_{TETD}	Transmit End of Transmission		250	450	ns
t_{TR}	Transmitter Rise Time (10% to 90%)			10	ns
t_{TF}	Transmitter Fall Time (90% to 10%)			10	ns
t_{TM}	Transmitter Rise and Fall Time Mismatch			4	ns
t_{THD}	DO L–>H to TXD+ L–>H and TXD- H->L Delay	Steady State (Note 1)	t_{TSD} – 1.0	t_{TSD} + 1.0	ns
t_{TLD}	DO H–>L to TXD+ H–>L and TXD– L–>H Delay	Steady State (Note 1)	t_{TSD} – 1.0	t_{TSD} + 1.0	ns
t_{THDP}	DO L–>H to TXP+ H–>L and TXP- L->H Delay	Steady State (Note 1)	t_{TSD} + 40	t_{TSD} + 60	ns
t_{TLDP}	DO H–>L to TXP+ L–>H and TXP– H->L Delay	Steady State (Note 1)	t_{TSD} + 40	t_{TSD} + 60	ns
t_{XMTON}	XMT Asserted Delay			100	ns
t_{XMTOFF}	XMT De-asserted Delay			300	ns
t_{PERLP}	Idle Signal Period		8	24	ms
t_{PWLP}	Idle Link Test Pulse Width	(Note 1)	75	120	ns
t_{PWPLP}	Predistortion Idle Link Test Pulse Width	(Note 1)	40	60	ns
t_{JA}	Transmit Jabber Activation Time		20	150	ms
t_{JR}	Transmit Jabber Reset Time		250	750	ms
t_{JREC}	Transmit Jabber Recovery Time (Minimum time gap between transmitted packets to prevent jabber activation)		1.0	–	µs

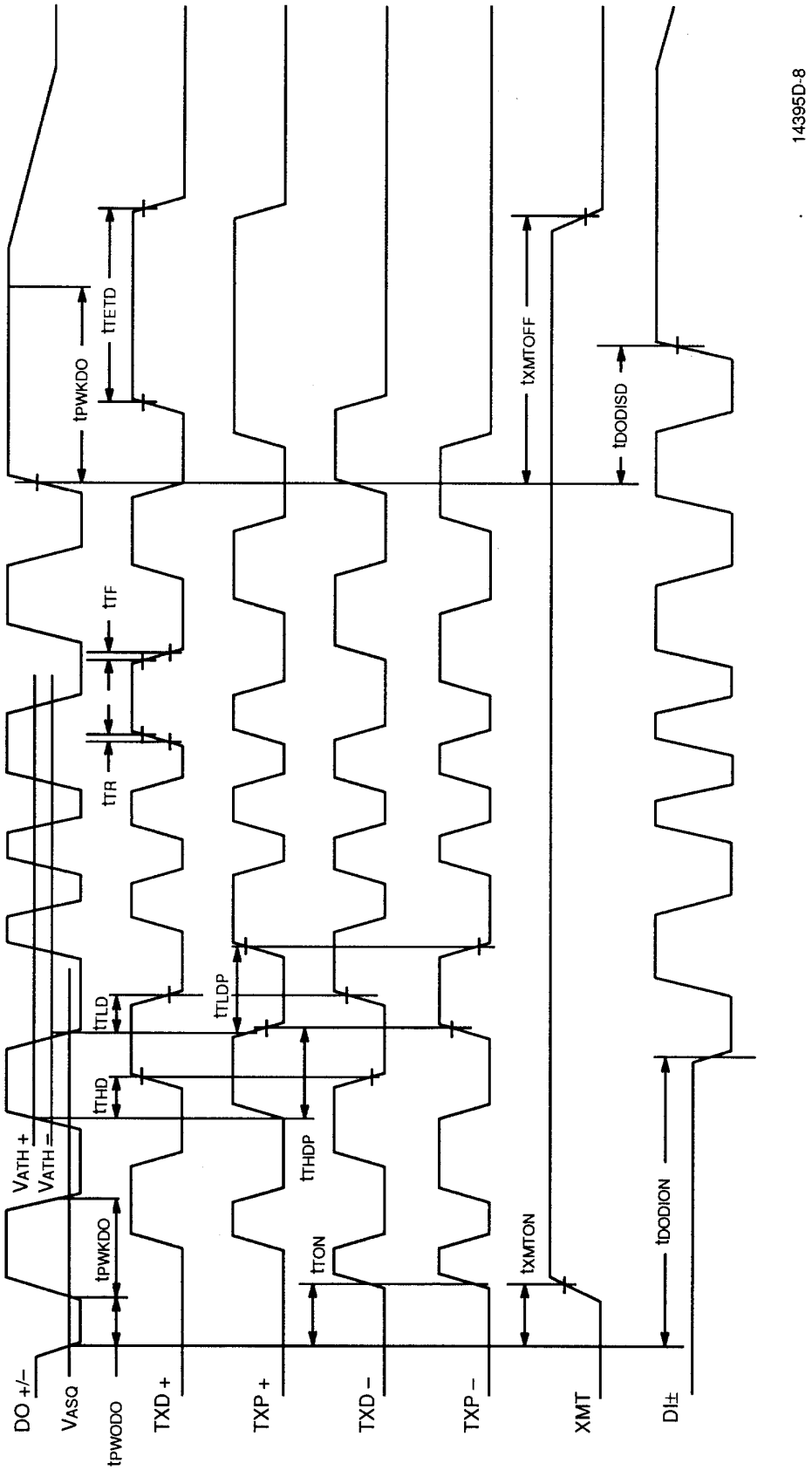
SWITCHING CHARACTERISTICS (continued)

Parameter Symbol	Parameter Description		Min	Max	Unit
Receive Timing					
t_{PWKRD}	RXD Pulse Width Maintain/Turn-Off Threshold	$\|V_{IN}\| > \|V_{THS}\|$ (Note 5)	136	200	ns
t_{RON}	Receiver Start Up Delay (RXD to DI+/–)	5 MHz Sinusoid	200	400	ns
t_{RVB}	First Validly Timed Bit on DI+/– (RXD to DI)			t_{RON} + 100	ns
t_{RSD}	Receiver Static Propagation Delay (RXD to DI)			70	ns
t_{RETD}	DI End of Transmission		200		ns
t_{RHD}	RXD L–>H to DI+ L–>H and DI– H–>L Delay	(Note 1)	t_{RSD} – 2.5	t_{RSD} + 2.5	ns
t_{RLD}	RXD H–>L to DI+ H–>L and DI- L->H Delay	(Note 1)	t_{RSD} – 2.5	t_{RSD} + 2.5	ns
t_{RR}	DI+, DI–, CI+, CI– Rise Time (10% to 90%)			5.0	ns
t_{RF}	DI+, DI–, CI+, CI– Fall Time (10% to 90%)			5.0	ns
t_{RM}	DI+/– & CI+/– Rise and Fall Time Mismatch ($\|t_{RR} – t_{RF}\|$)			2.0	ns
t_{RCVON}	RCV Asserted Delay		t_{RON} – 50	t_{RON} + 100	ns
t_{RCVOFF}	RCV De-asserted Delay			t_{RSD} + 250	ns
Collision Detection and SQE Test					
t_{CON}	Collision Turn-On Delay (CI+/–)			500	ns
t_{COFF}	Collision Turn-Off Delay (CI+/–)			500	ns
t_{PER}	Collision Period (CI+/–)		87	117	ns
t_{CPW}	Collision Output Pulse Width (CI+/-)		40	60	ns
t_{SQED}	SQE Test Delay Time		600	1600	ns
t_{SQEL}	SQE Test Length		500	1500	ns

Notes:

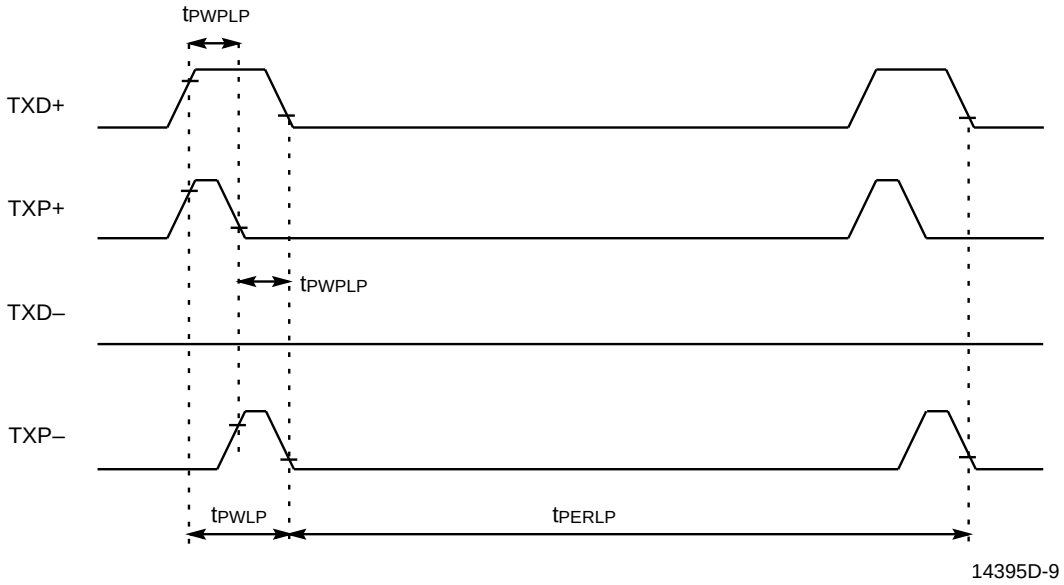
1. *Parameter not tested.*
2. *Uses switching test load.*
3. *DO pulses narrower than t_{PWODO} (min) will be rejected; pulses wider than t_{PWODO} (max) will turn internal DO carrier sense on.*
4. *DO pulses narrower than t_{PWKDO} (min) will maintain internal DO carrier sense on; pulses wider than t_{PWKDO} (max) will turn internal DO carrier sense off.*
5. *RXD pulses narrower than t_{PWKRD} (min) will maintain internal RXD carrier sense on; pulses wider than t_{PWKRD} (max) will turn internal RXD carrier sense off.*

SWITCHING WAVEFORMS



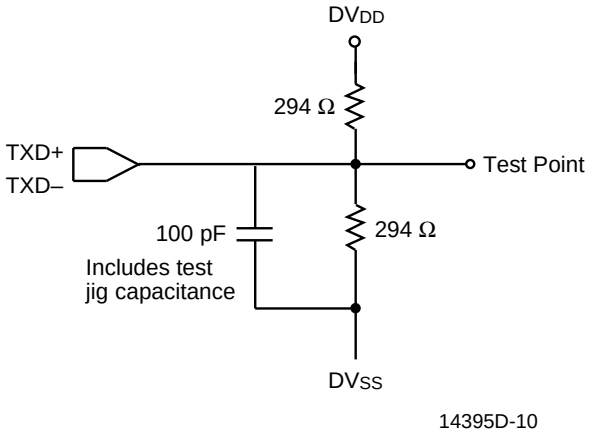
Transmit Timing

SWITCHING WAVEFORMS

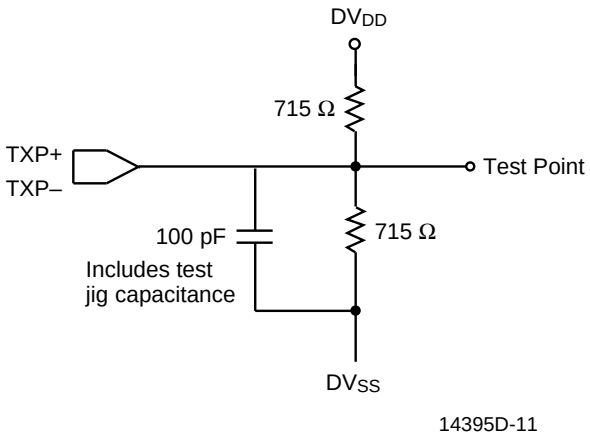


TP Idle Link Test Pulse

SWITCHING TEST CIRCUITS

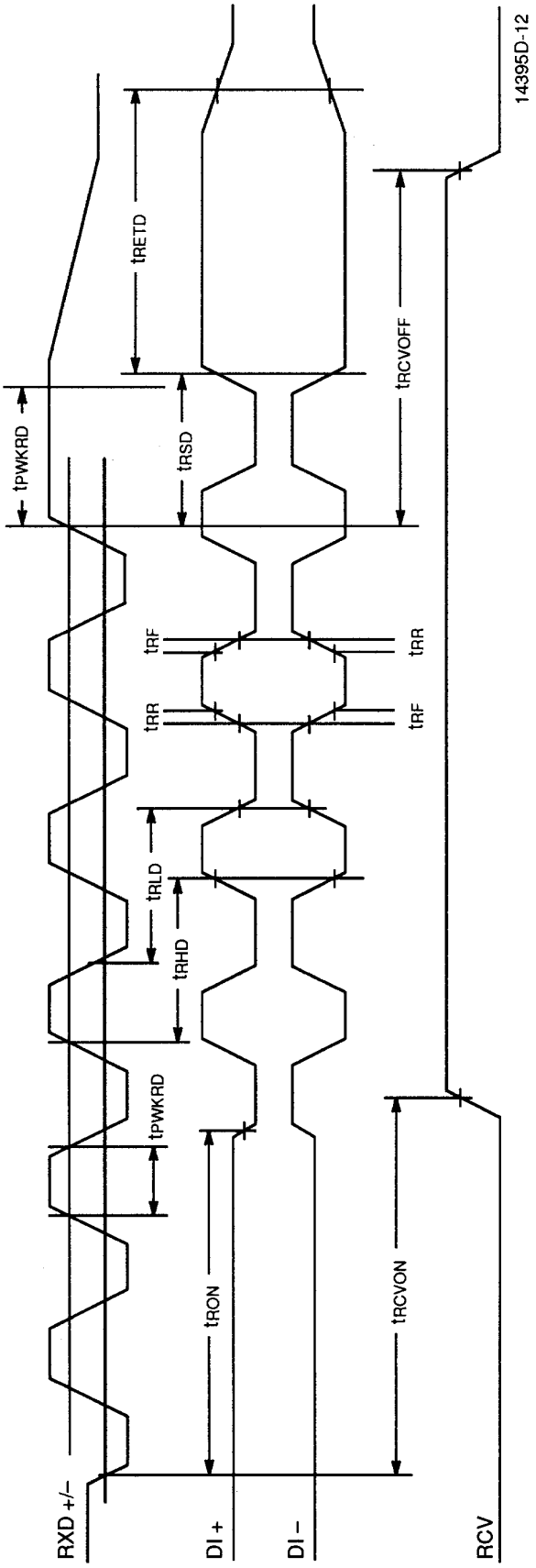


TXD Switching Test Circuit



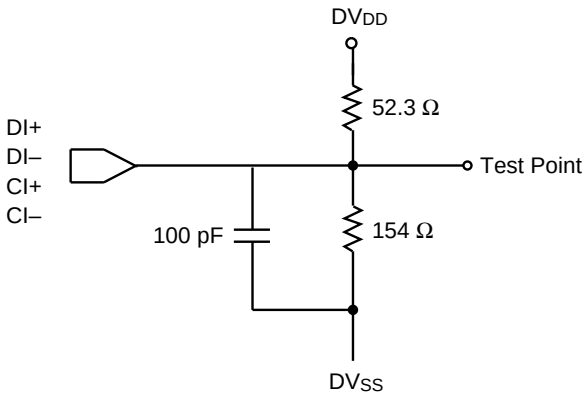
TXP Switching Test Circuit

SWITCHING WAVEFORMS

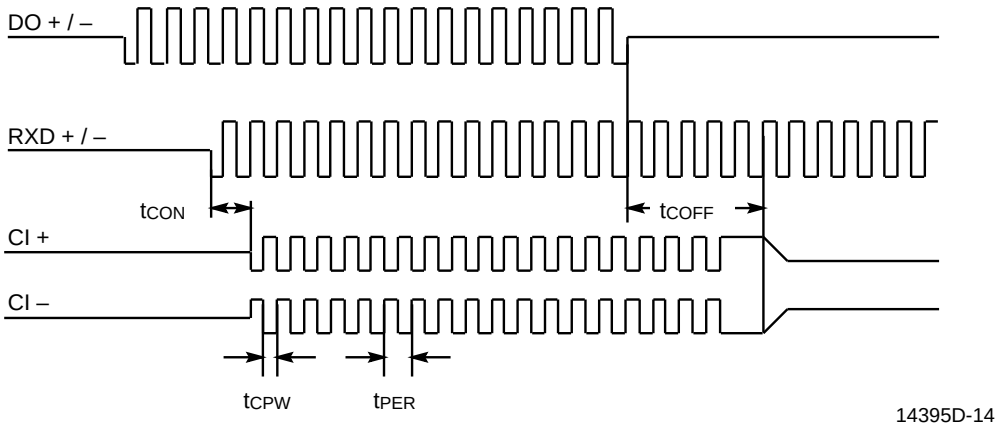


Receive Timing

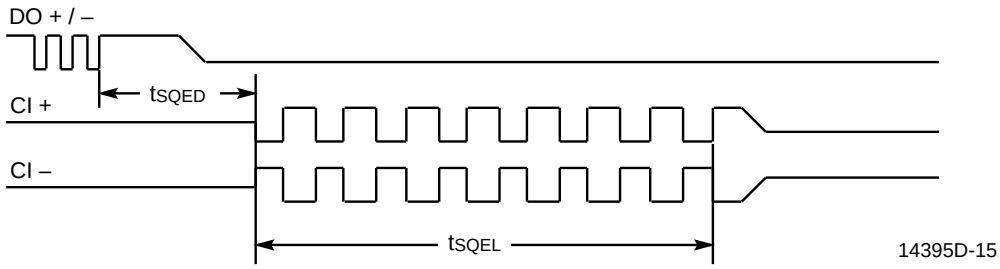
RECEIVE TEST CIRCUIT



AUI DI, CI Switching Test Circuit



Collision Timing



SQE Test Timing ($\overline{\text{SQE Test}}$ Pin Connected to V_{SS})

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