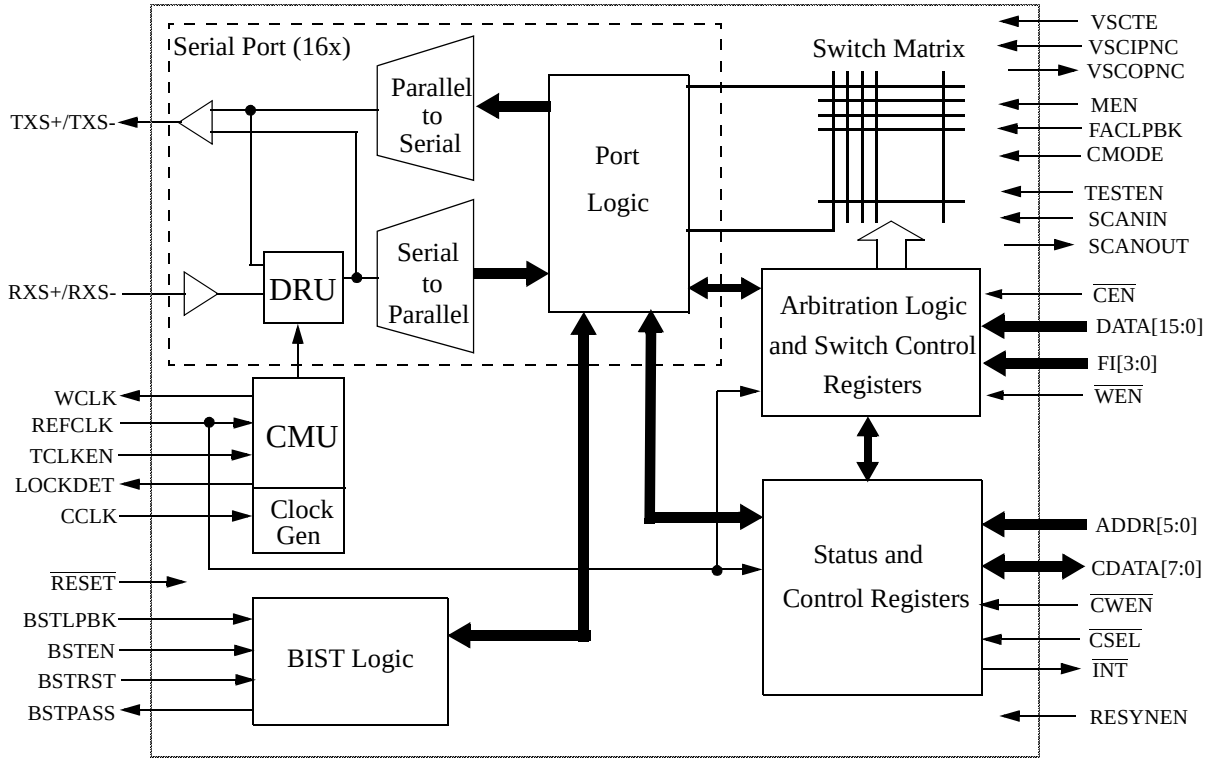
Data Sheet
VSC880

High Performance 16x16 Serial Crosspoint Switch

Features

- 16x16 Synchronous Serial Crosspoint Switch
- Serial Data Rates: 2.0Gb/s
- 32Gb/s Aggregate Data Bandwidth
- Parallel Switches Can Increase Data Bandwidth in Multiples of 32Gb/s
- Designed in Conjunction with the VSC870 Backplane Transceiver
- Automatic Word and Cell Synchronization to the Transceiver
- Two Modes of Operation: Distributed Control Self-routing *Packet Mode* and Central Control *Cell Mode*
- Multicast Supported in All Modes
- Supports Variable Length Packets in Packet Mode
- Built-in Flow Control Channel in Packet Mode
- Supports Cell Synchronization in Cell Mode
- Parallel CPU Interface and Parallel Switch Configuration Interface
- Loopback, Built-in Self Test and Scan Functions
- 5V Tolerant TTL Inputs
- Dual 3.3V/2.5V or Dual 3.3V/2.0V Power Supplies
- Serial Port Quadrants Can be Powered Down
- Available in 304 BGA Package

VSC880 Block Diagram



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High Performance 16x16
Serial Crosspoint Switch

Data Sheet
VSC880

General Description

The VSC880 is a 16x16 serial crosspoint switch with serial data rates at 2.125Gb/s. The VSC880 has been designed to operate with the VSC870 backplane transceiver to establish a synchronous high performance switching system with an aggregate bandwidth of 32Gb/s. The switch chip transmits the master word clock (62.5Mb/s), and master cell clock (if used) to all port cards through the serial data channels. The transceivers automatically perform bit alignment, word alignment and cell alignment to the switch chip. The transceiver and switch chip have been optimized for both self-routing and cell-based systems and include special commands for connection requests (self-routing) and cell synchronous operation (cell based). In addition, a parallel CPU interface can be used to control internal modes and read status information from the switch. A 20-bit interface can also be used to program the switch matrix in 4 clock cycles. The switch chip runs off of a 3.3V/2.5V or 3.3V/2.0V power supplies. The serial I/O buffers contain on-chip termination resistors (see Application Note 34).

Pin Descriptions

Pin	*Name*	*I/O*	*Freq Type*	*Description*
TXS[15:0]+/ TXS[15:0]-	Transmit Serial Outputs	O	2.125Gb/s LVDS	16 high speed serial differential transmit channels
RXS[15:0]+/ RXS[15:0]-	Receive Serial Inputs	I	2.125Gb/s LVDS	16 high speed serial differential receive channels
DATA[15:0]	Configuration Data Input	I	62.5Mb/s TTL	Parallel input signals used to program the switch matrix in 4 clock cycles when the signal $\overline{\text{CEN}}$ is LOW.
FI[3:0]	Force IDLE Input	I	62.5Mb/s TTL	Parallel input signals used to program force IDLE words at the switch matrix output in 4 clock cycles when the signal $\overline{\text{CEN}}$ is LOW.
$\overline{\text{CEN}}$	Configure Enable	I	62.5Mb/s TTL	When $\overline{\text{CEN}}$ is held LOW, the inputs DATA[15:0] and FI[3:0] can be used to program the switch matrix in 4 word clock cycles timed to the $\overline{\text{WEN}}$ signal.
$\overline{\text{WEN}}$	Write Enable	I	62.5Mb/s TTL	If $\overline{\text{CEN}}$ is LOW, this signal provides a synchronization pulse for loading switch configuration data into DATA[15:0] and FI[3:0].
ADDR[5:0]	Data Address	I	62.5Mb/s TTL	The address to read and write data through parallel interface CDATA[7:0].
$\overline{\text{CSEL}}$	Chip Select	I	62.5Mb/s TTL	This signal allows several switch chips to share an 8 bit data bus connected to CDATA[7:0]. If $\overline{\text{CSEL}}$ is LOW, data will be read or written to CDATA[7:0]. If $\overline{\text{CSEL}}$ is HIGH, the outputs will be high impedance and the inputs disabled.
CDATA[7:0]	Status Data Output	B	62.5Mb/s TTL	Bidirectional CPU interface for the status and control registers. If $\overline{\text{CSEL}}$ is LOW, the data will be read or written into this port. If $\overline{\text{CSEL}}$ is HIGH, the outputs will be high impedance and the inputs will be disabled.
$\overline{\text{CWEN}}$	Control Write Enable	I	62.5Mb/s TTL	This signal is set HIGH to read the internal status registers through the parallel interface CDATA[7:0]. It is set LOW to write into this interface.

Pin	Name	I/O	Freq Type	Description
RESYNEN	Resynch Enable	I	<1MHz TTL	If RESYNEN is HIGH, all links that have a link error condition will be reinitialized. This will override the internal control register settings.
$\overline{\text{INT}}$	Interrupt	O	<1MHz TTL	If $\overline{\text{INT}}$ is LOW, a receive error has occurred in one of the links that has it's output enable (OE) bit set HIGH and interrupt control register bit set HIGH.
MEN	Reserved	I	<1MHz TTL	This signal is reserved for future use and should be set LOW during normal operation.
FACLPBK	Facility Loop Back	I	<1MHz TTL	If this signal is set HIGH, all serial inputs are looped back to their serial outputs. This will override the internal control register setting.
CMODE	Cell Mode	I	<1MHz TTL	CMODE is set HIGH for Cell Mode operation.
TESTEN	Scan Test Enable	I	<1MHz TTL	This signal is used in ATE testing to measure propagation delay. It is also used in ATE testing of the BIST logic. Set to logic LOW in normal operation.
SCANIN	Scan Data In	I	62.5Mb/s TTL	The input signal for measuring propagation delay on the ATE tester.
SCANOUT	Scan Data Out	O	62.5Mb/s TTL	The output signal for measuring propagation delay on the ATE tester. When TESTEN is set LOW, the longer delay path is enabled.
WCLK	Word Clock	O	62.5MHz TTL	This is the word clock output.
REFCLK	Reference Clock	I	62.5MHz TTL	This is the reference clock and the source of the system wide word clock period.
TCLKEN	Test Clock Enable	I	<1MHz TTL	This input is set HIGH in test mode, so that the CMU is bypassed and the REFCLK becomes the bit clock. This signal is for ATE test only. Set LOW in normal operation.
CCLK	Cell Clock	I	62.5MHz TTL	This is the source of the system wide cell clock. It is internally synchronized to the REFCLK. In Packet mode, set this signal HIGH to enable external switch configuration for BIST.
$\overline{\text{RESET}}$	Reset	I	<1MHz TTL	Global chip reset (active LOW)
BSTLPBK	Built-in Self Test Loop Back	I	<1MHz TTL	When BSTLPBK is set HIGH and TESTEN is LOW, all serial data output signals are looped back to their serial data inputs. If BSTLPBK is set HIGH and TESTEN is HIGH, only ports 0-7 are placed in loopback.
BSTEN	Built-in Self Test Enable	I	<1MHz TTL	When BSTEN is HIGH, at-speed built-in self testing is enabled.
BSTRST	Built-in Self Test Reset	I	<1MHz TTL	The BSTRST signal is set HIGH to reset the PRBS generator and comparator.
BSTPASS	Built-in Self Test Pass	O	<1MHz TTL	The BSTPASS signal is HIGH if BTSEN is HIGH and the PRBS comparator detects the correct pattern in built-in self test mode.

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Pin	*Name*	*I/O*	*Freq Type*	*Description*
LOCKDET	CMU Lock Detect	O	<1MHz TTL	This signal is LOW while the CMU is acquiring lock.
VSCTE	NOR Chain Test Enable	I	<1MHz TTL	Used for ATE testing of the parametric NOR chain in the I/O frame. Set to logic LOW during normal operation.
VSCIPNC	NOR Chain Input	I	<1MHz TTL	Used for ATE testing of the parametric NOR chain in the I/O frame. Set to logic LOW during normal operation.
VSCOPNC	NOR Chain Output	O	<1MHz VECL	Used for ATE testing of the parametric NOR chain in the I/O frame. Leave output open during normal operation.
VDD1, VDD2, VDD3, VDD4	Serial Port Power Supplies	P	3.3V	VDD1 = Serial Port 0-3 power supply VDD2 = Serial Port 4-7 power supply VDD3 = Serial Port 8-11 power supply VDD4 = Serial Port 12-15 power supply
VDDA	CMU Power Supply	P	3.3V	Clean power supply for CMU
VSSA	CMU Ground	P	0V	Clean ground for CMU
VMM	Core Power Supply	P	2 ~ 2.5V	Core power supply

Functional Description

The VSC880 switch can be used in conjunction with the VSC870 transceivers to support two modes of operation: Packet Mode and Cell Mode. In Packet mode, the chip set provides a switching system to support variable length, self-routing data packets. In Cell Mode, the chip set provides a cell synchronous switching system with a user defined scheduler. In this mode, it can support only fixed length data packets (cells). Routing decisions are carried out in the scheduler and crosspoint configuration is synchronized to a cell clock. The scheduler configures the switch matrix using the parallel interface. To conserve power, each serial port quadrant can be powered down if not used.

The following section gives a detailed functional description of the operation of the switch chip. Most of the discussion includes some of the transceiver operation (see the VSC870 data sheet). The two major operation modes are described separately in the *Packet Mode* and the *Cell Mode* sections.

1.0 Common Features

1.1 Synchronization

1.1.1 Link Characteristic

The serial link is used to connect the switch chip to transceivers. These links operate at 2.125 Gb/s and are initialized simultaneously at power up, or separately when a link error occurs. A link is first bit synchronized, then word synchronized and, if CMODE is HIGH, cell synchronized. In Packet or Cell mode, the switch acts as the master, generating the bit clock along with the word and cell boundary information. The transceivers act as slaves, recovering the bit clock, word clock and cell clock. The transceiver also contains redundant serial inputs and outputs which can be used with a redundant switch chip.

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1.1.2 Data Scrambling

To allow the VSC870 CRU to recover the bit clock, a 15% edge transition density must be guaranteed on the serial data links. All command words and connection request words contain this required density. In order to get this density on data words, scrambling must be employed by the transceiver (see VSC870 data sheet).

1.1.3 Bit Synchronization

In Packet Mode and Cell Mode, the switch acts as the source of the bit clock. It multiplies the local 62.5MHz reference clock by 34 to generate a 2.125GHz clock and uses this clock to serialize the 32-bit word and 2 overhead bits. The transceiver receives and feeds this serial data stream to a digital CRU to recover the bit clock and deserialize the data stream to a 32-bit word plus 2 overhead bits at 62.5MHz. The transceiver also uses this recovered clock to serialize its transmit words that are sent to the switch. In this way, the switch and all the transceivers are frequency-locked to one clock source which is provided by the reference clock on the switch card. Because of this, the switch chip needs to recover only the phase information on the serial receive channel using a data recovery unit (DRU). The DRU is designed as a delay lock loop and remains phase-locked to the incoming data stream as long as the temperature does not change by more than 20°C after link initialization. If this temperature variation is exceeded, a link error may occur causing the link to reinitialize. Because of this, system reset should be held until the system reaches temperature stability before starting the link initializing process.

1.1.4 Word Synchronization

During power up or at reset, the transceiver can initiate the word synchronization process. First, the transceiver sends reset patterns to the switch to request that the switch starts the initialization process. The switch, upon receiving this request, will send out special ALIGN words. The transceiver receives this serial data stream and word aligns to this ALIGN word by adjusting its own word boundary one bit at a time. Upon detecting the correct word alignment, it starts the transmit word alignment process. In this process, the transceiver continuously sends ALIGN words to the switch. The switch uses its own word clock (REFCLK) to detect this ALIGN word. If the transmitters word is not aligned to the switch chip word clock when it arrives at the switch, the switch chip continues to send out ALIGN words. After receiving 32 ALIGN words from the switch chip, the transceiver changes its transmit word boundary by 1 bit position and repeats the process (this limits the distance from the transceiver to the switch to less than 180ns one way). If the switch detects the transceivers ALIGN word correctly, it sends IDLE words to the transceiver to signal that the transmitter has now word synchronized with the switch. It also clears the internal registers LERR, TERR, DERR and CERR and sets the signal $\overline{\text{INT}}$ HIGH if all the enabled serial channels are successfully initialized (see section 1.4).

1.1.5 Cell Synchronization

If CMODE is set HIGH, after the word synchronization process completes, the transceiver starts the cell synchronization process. In this process, the transceiver detects the received cell clock (CCLK) sent from the switch embedded in the alignment word. The switch delays the global cell clock to adjust out the pipeline delay from the transceiver to the switch. The switch chip does this by connecting each port to itself during link initialization. By sending an ALIGN words to itself, the transceiver can adjust the transmit clock until it is properly phase shifted relative to the global cell clock. If cells are sent from the transceiver aligned to this transmit cell clock, they will arrive at the switch aligned to the master cell clock which is originated at the switch. For this alignment process to work, the minimum cell size is 8 words (32 bytes).

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1.1.6 Link Error Detection

There are four types of link errors that can be flagged on the receive serial links. Link errors are detected using IDLE words. If a link error is detected, a bit in the LERR register is set HIGH for that particular channel (see section 1.4). After every 8 link errors, a bit in the TERR register is set HIGH. If the DRU goes out of range, a bit in the DERR register is set HIGH. If the last word in the cell period is an IDLE word and it does not have bits B[1:0] set HIGH to designate a cell clock, a bit in the CERR register will be set HIGH. If an error bit is set in any of these registers, the $\overline{\text{INT}}$ signal can be programmed to go LOW and/or the link can be programmed to automatically start link initialization depending on the value loaded into the Interrupt Control Register (see section 1.4). These error register bits will be cleared if the link is reinitialized, or the registers are read. If the signal RESYNEN is set HIGH, link initialization will begin immediately upon the detection of any of these errors. If the switch is used without IDLE words, the user is responsible for detecting parity error conditions and restarting the link initialization process.

1.2 Data Encoding Format

To provide self-routing and cell synchronization, the transceiver and switch require special word formats. Depending on the mode that the switch is used in, different word types are recognized by the switch. In both the Packet and Cell Modes, the switch processes both data words and command words. They have the same format in both modes and will be described in following section. The format for the connection request words and header words are described later in the *Packet Mode* section.

1.2.1 Data Word Format on the Serial Data Lines

The data word format as seen at the serial output of the transceiver or switch chip is shown below. Two overhead bits are added by the transceiver or switch chip to designate a data word to the receiving switch chip or transceiver. The serial data is transmitted with the MSB first.

33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00
B B 1 0	D D D D 31 30 29 28	D D D D 27 26 25 24	D D D D 23 22 21 20	D D D D 19 18 17 16	D D D D 15 14 13 12	D D D D 11 10 09 08	D D D D 07 06 05 04	D D D D 03 02 01 00
	---------- Data Payload ----------							

Where:
B[1:0]If Packet Mode, 01=Flow control channel,
10=Flow control channel,
11=Acknowledge from switch chip or header word to switch chip
If Cell Mode, 01, 10, 11 = data
D[31:0]32 bit data payload

1.2.2 Command Word Format on the Serial Data Lines

The command word format as seen at the serial output of the transceiver or switch chip is shown below. Two overhead bits are added by the transceiver or switch to designate a command word (00) to the receiving switch chip or transceiver. The serial data is transmitted with the MSB first. In Packet Mode, the IDLE word from the switch always returns the current output connections for the port.

33 32	31 30 29	28 27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00
0 0	1 B B 1 0	C C C C C 04 03 02 01 00 -- Command --	D D D D 15 14 13 12	D D D D 11 10 09 08	D D D D 07 06 05 04	D D D D 03 02 01 00 -- Data --	1 0 1 0	1 0 1 0

Where:

B[1:0]00=Undefined (during normal operation) or alignment word

01=Flow control channel,

10=Flow control channel,

11=Acknowledge (from switch chip only) or link initialization reset or cell clock in cell mode

C[4:0]Command type

00XXX=Link Control (00000=ALIGN word, 00111=IDLE word)

01XX0=Command word for transceiver (01000=set DLYEN/CCKIN value)

10XX0=Command word for switch

11XX0=Command word for receiving port card (TBD)

D[15:0]Optional data payload

Default=1010101010101010

IDLE Word from switch=Current switch outputs this port is connected to

D[15] is for port 0, D[0] is for port 15

If C[4:0]=01000, D[3:0]=DLYEN/CCKIN value

1.2.3 IDLE Words

IDLE words are the default word used on the serial channel when none of the other word types are present. In most cases, these words are automatically generated by the transceiver or switch chip. In Packet Mode, IDLE words are inserted between packets and the IDLE word from the switch always returns the current output connections for the port that is receiving the IDLEs. These connection bits will be in the same location as in the CRQ word. In cell mode, IDLEs will be transmitted from the switch chip if the force IDLE (FI) bit is set in the control registers. IDLE words are also used to detect link error conditions. If the switch chip detects an IDLE word, it uses a bit mask to verify the proper bit pattern within the word.

1.3 Loopback

The VSC880 supports a loopback function at the serial interfaces which is used in built-in self-test mode. If the BSTLPBK signal is set HIGH and TESTEN is set LOW, the serial transmit data is looped back to the serial receive side for all 16 channels. If the BSTLPBK signal is set HIGH and TESTEN is set HIGH, the serial transmit data is looped back to the serial receive side for channels 0-7 only. If the FACLPBK signal is set HIGH, the serial receive signal is looped back to the serial output for all 16 channels. Each channel can also be programmed to be looped back separately from serial input to serial output by using the control registers described below. The VSC880 does not support simultaneous BIST and facilty loopback functions (either FACLPBK pin or LPBK[15:0] register).

1.4 Internal Register Definitions

The internal status and control registers are defined in the following table. The address signal ADDR[5:0] is used along with $\overline{\text{CSEL}}$ and $\overline{\text{CWEN}}$ to read or write data through the CDATA[7:0] interface. $\overline{\text{CWEN}}$ is set LOW to write and HIGH to read from this port. If $\overline{\text{CSEL}}$ is HIGH, the outputs become high impedance and the inputs become

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disabled. All data transfer timing is asynchronous to REFCLK. The Interrupt Control Register is written by the user to mask certain operations. If ICE is set HIGH, the $\overline{INT}$ output pin will go LOW if any error bit is set in the CERR register. If RCE is set HIGH, the link will automatically start link initialization if any error bit is set in the CERR register. The corresponding pins can be used for the DERR, TERR and LERR registers. If the $\overline{INT}$ signal goes LOW, the Interrupt Status Register can be read to determine which of the four registers received an error.

The CDEL[3:0] bits are used to program a value for the cell clock delay (see section 3.0). The switch matrix status information can be read from the C*N* and FI registers. A serial link can be forced to reinitialize by writing a HIGH into the RSY register. A serial output can be logically disabled by writing a HIGH into the OE register. A serial input can be forced to loop back directly to a serial output by writing a HIGH into the LPBK register. All registers are cleared upon RESET. Also, the LERR, TERR, DERR and CERR registers are cleared on reading.

Figure 1: Status and Control Register Definition

		CDATA[7:0] Bit Position								
ADDR[5:0]	***R/W***	***7***	***6***	***5***	***4***	***3***	***2***	***1***	***0***	
X 0 0 0 0 0	R					CE	DE	TE	LE	Interrupt Status Register
X 0 0 0 0 1	R/W	RCE	RDE	RTE	RLE	ICE	IDE	ITE	ILE	Interrupt Control Register
X 0 0 0 1 0	R/W				BIST	CDEL[3:0]				BIST and Count Register
X 0 0 0 1 1										
X 0 0 1 0 0	R	CERR[7:0]								CCLK error register LSB
X 0 0 1 0 1	R	CERR[15:8]								CCLK error register MSB
X 0 0 1 1 0	R	DERR[7:0]								DRU error register LSB
X 0 0 1 1 1	R	DERR[15:8]								DRU error register MSB
X 0 1 0 0 0	R	TERR[7:0]								Error threshold register LSB
X 0 1 0 0 1	R	TERR[15:8]								Error threshold register MSB
X 0 1 0 1 0	R	LERR[7:0]								Link error register LSB
X 0 1 0 1 1	R	LERR[15:8]								Link error register MSB
0 0 1 1 0 0	R/W	C0[3:0]				C8[3:0]				Output0/Output8 Config
0 0 1 1 0 1	R/W	C1[3:0]				C9[3:0]				Output1/Output9 Config
0 0 1 1 1 0	R/W	C2[3:0]				C10[3:0]				Output2/Output10 Config
0 0 1 1 1 1	R/W	C3[3:0]				C11[3:0]				Output3/Output11 Config
0 1 0 0 0 0	R/W	C4[3:0]				C12[3:0]				Output4/Output12 Config
0 1 0 0 0 1	R/W	C5[3:0]				C13[3:0]				Output5/Output13 Config
0 1 0 0 1 0	R/W	C6[3:0]				C14[3:0]				Output6/Output14 Config

		CDATA[7:0] Bit Position								
ADDR[5:0]	***R/W***	***7***	***6***	***5***	***4***	***3***	***2***	***1***	***0***	
0 1 0 0 1 1	R/W	C7[3:0]				C15[3:0]				Output7/Output15 Config
1 0 1 1 0 0	R	S0[3:0]				S8[3:0]				Output0/Output8 Status
1 0 1 1 0 1	R	S1[3:0]				S9[3:0]				Output1/Output9 Status
1 0 1 1 1 0	R	S2[3:0]				S10[3:0]				Output2/Output10 Status
1 0 1 1 1 1	R	S3[3:0]				S11[3:0]				Output3/Output11 Status
1 1 0 0 0 0	R	S4[3:0]				S12[3:0]				Output4/Output12 Status
1 1 0 0 0 1	R	S5[3:0]				S13[3:0]				Output5/Output13 Status
1 1 0 0 1 0	R	S6[3:0]				S14[3:0]				Output6/Output14 Status
1 1 0 0 1 1	R	S7[3:0]				S15[3:0]				Output7/Output15 Status
X 1 0 1 0 0	R/W	FI[7:0]								Force IDLEs LSB
X 1 0 1 0 1	R/W	FI[15:8]								Force IDLEs MSB
X 1 0 1 1 0	R/W	RSY[7:0]								Resynch LSB
X 1 0 1 1 1	R/W	RSY[15:8]								Resynch MSB
X 1 1 0 0 0	R/W	OE[7:0]								Output Enable LSB
X 1 1 0 0 1	R/W	OE[15:8]								Output Enable MSB
X 1 1 0 1 0	R/W	LPBK[7:0]								Loopback LSB
X 1 1 0 1 1	R/W	LPBK[15:8]								Loopback MSB

Where:

CE	Cell clock error	RCE	Resynch on cell error
ICE	Interrupt on cell error		
DE	DRU error	RDE	Resynch on DRU error
IDE	Interrupt on DRU error		
TE	Threshold error	RTE	Resynch on thresh error
ITE	Interrupt on threshold error		
LE	Link error	RLE	Resynch on link error
ILE	Interrupt on link error		

BIST Set this bit HIGH to test the BIST circuitry

CDEL[3:0] Cell clock delay

CERR[15:0]Cell clock error register, bit 0 is channel 0 etc, Cleared on read

DERR[15:0]DRU error register, bit 0 is channel 0 etc. Cleared on read

TERR[15:0]Threshold error register, bit 0 is channel 0 etc. Cleared on read

LERR[15:0]Link error register, bit 0 is channel 0 etc, Cleared on read

C*N*[3:0]Switch configuration data. *N* is the output port number, [3:0] is the input port connected. Default = 0xF.

S*N*[3:0]Output status data. *N* is the output port number, S*N*[3:2] = 00 for normal operation.
01 for out of synch
10 for word synch in progress
11 for cell synch in progress
S*N*[1] = Output busy in packet mode
S*N*[0] = Connection valid in packet mode

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FI[15:0]Force IDLE register, bit 0 is channel 0 etc
RESY[15:0]Resynch register, bit 0 is channel 0 etc
OE[15:0]Output enable register, bit 0 is channel 0 etc
LPBK[15:0]Facility loopback register, bit 0 is channel 0 etc

1.5 Parallel CPU Interface

There is a parallel 8 bit CPU interface on the VSC880 that can be used to read and write the status and control registers described above. This is an asynchronous interface that was design to operate with many common micro controllers that are available. The functional timing diagrams for a write and a read are shown in the following figures. Timing information can be found in the AC Characteristics section of this data sheet.

Figure 2: CPU Interface Functional Write Cycle Timing

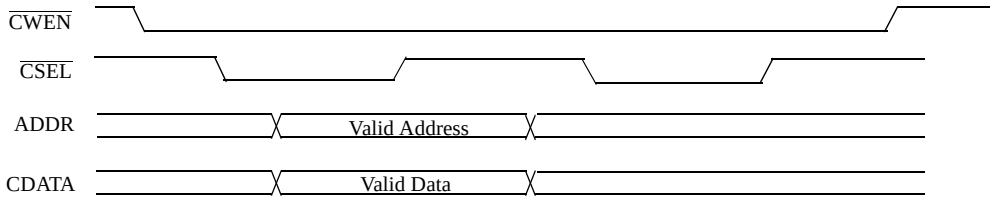
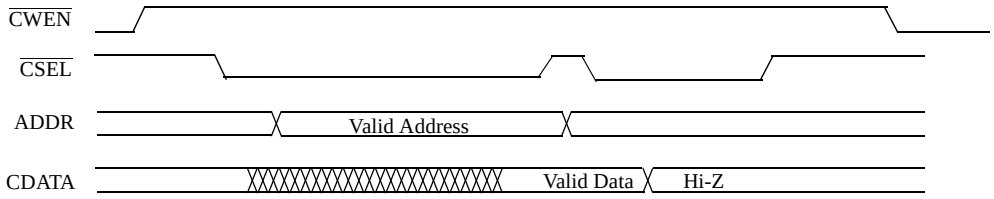


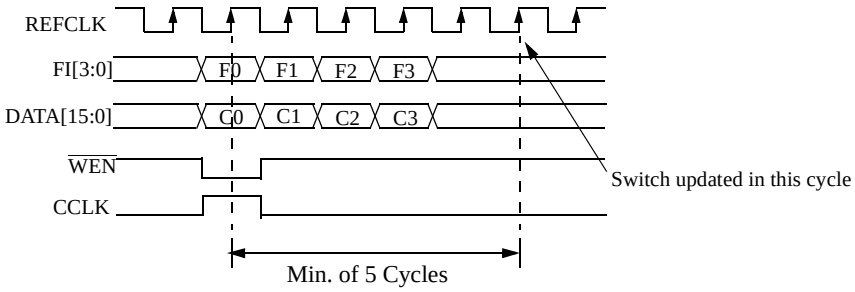
Figure 3: CPU Interface Functional Read Cycle Timing



1.6 Parallel Configuration Interface

In addition to reading and writing the switch configuration using the CPU interface as described above, the entire switch matrix can be reprogrammed in 4 word clocks by setting the $\overline{\text{CEN}}$ signal LOW. If $\overline{\text{CEN}}$ is set LOW, the parallel interface DATA[15:0] contains a 16 bit switch configuration input port, the inputs FI[3:0] load the FI bits and the $\overline{\text{WEN}}$ signal becomes a programming signal as shown in the figure below. It takes 4 word clocks to load all 64 bits of switch configuration data and 16 FI bits into holding registers. All data transfer timing is relative to REFCLK. After data has been loaded, and if CCLK is HIGH, all 80 bits of data are strobed into the switch matrix and FI control logic. Otherwise, the configuration information is stored in holding registers until the next CCLK pulse strobes it in. Since the CCLK signal is delayed internally in the switch, it can be asserted as early as the $\overline{\text{WEN}}$ signal pulse to strobe in the configuration information.

Figure 4: Switch Configuration Interface Functional Timing ($\overline{CEN}$=0)



The switch configuration data for each port is as follows:

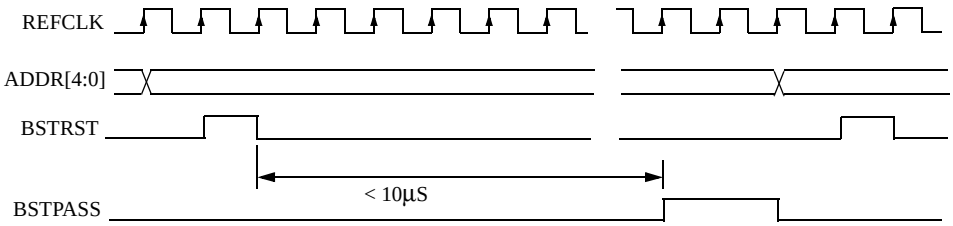
F0[3:0] = FI[port9], FI[port8], FI[port1], FI[port0]
F1[3:0] = FI[port11], FI[port10], FI[port3], FI[port2]
F2[3:0] = FI[port13], FI[port12], FI[port5], FI[port4]
F3[3:0] = FI[port15], FI[port14], FI[port7], FI[port6]
C0[15:0] = Port9[3:0], Port8[3:0], Port1[3:0], Port0[3:0]
C1[15:0] = Port11[3:0], Port10[3:0], Port3[3:0], Port2[3:0]
C2[15:0] = Port13[3:0], Port12[3:0], Port5[3:0], Port4[3:0]
C3[15:0] = Port15[3:0], Port14[3:0], Port7[3:0], Port6[3:0]

Where FI[portN] is the Force IDLE bit for port N and PortN[3:0] is the input port number to be connected to output port N.

1.7 Built-in Self-Test

The switch has built-in self-test logic that can be used to verify the high-speed circuitry as well as the switch matrix while operating at full speed. The built-in self-test mode is enabled by setting the built-in self-test enable (BSTEN) signal HIGH. If the signal BSTLPBK is set HIGH and TESTEN is set LOW, it loops all 16 serial outputs back to the Data Recovery Unit (DRU) at the serial inputs. An internal Pseudo Random Bit Sequence (PRBS) generator connected to the switch matrix at port 0. The random data is sent to port 0, passed through the switch matrix, looped back through the serial interface and returned to the data comparator. If this data matches the correct pattern, BSTPASS is set HIGH. By configuring port 0 to connect to other ports (ports 1 through 15) through the switch matrix using the parallel configuration interface, the rest of the serial channels (one port at a time) can be tested in turn. For example, port 0 can be connected to port 1 by configuring the switch matrix. The PRBS generator transmits the random data through port 0 to port 1, and the random data is then looped back from port 1 to port 0 and the data comparator. To test all 16 ports, the user will need to configure the switch matrix 16 times to test all ports.

Figure 5: Built-in Self-Test Functional Timing



The signal BSTRST is used to reset the PRBS pattern, and there is a comparator that sets the signal BSTPASS HIGH if the test was successful. The functional timing diagram above shows a typical test sequence. The PRBS pattern generator can also be tested by itself by setting the control register bit BIST HIGH. This loops the output of the pattern generator directly back to the comparator circuit. This test will be typically run before running the tests described above. In this case, the signals BSTEN, BSTRST and BSTPASS will operate as shown in the Figure 5 above.

The BIST test can be run on no more than two ports at a time, for example: port 0⟶port 3⟶port 8⟶port 0.

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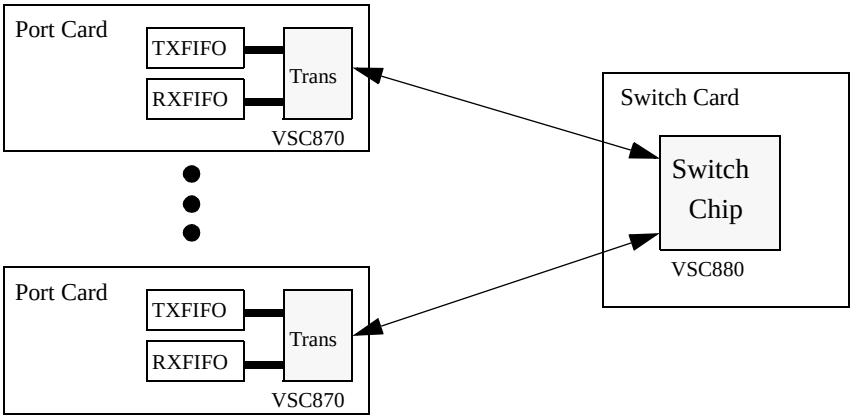
2.0 Packet Mode

2.1 Overview

In Packet Mode (CMODE=LOW), command words can be sent through the transceiver to the switch chip requesting connection to one or multiple output channels. Acknowledge (ACK) information will be returned to the transceiver from the switch allowing the port card to start transmitting data. In this mode of operation, no controller chip is connected to the switch chip as the switch chip handles all arbitration for connection requests. Details on how the transceiver operates in Packet Mode mode can be found in the VSC870 data sheet and the applications note 31: "Design Guide for a Packet Based Switch with Distributed Control". A picture of a self routing system is shown below. The minimum packet size in this mode of operation is 4 words or 16 bytes.

Figure 6: Packet Mode System



2.2 Data Encoding Format

The data word and command word formats are described in section 1.0. In this section the header word and Connection Request (CRQ) word format at the serial input and serial output of the switch are described.

2.2.1 Header word Format on the Serial Data Lines

The header word format as seen at the serial output of the transceiver or switch chip is shown below. Two overhead bits are added to designate a header word to the receiving chip. The serial data is transmitted with the MSB first. If multiple headers are sent in a row, the VSC870 will convert all but the first one into IDLEs.

33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00
A A 1 0	0 B B 1 1 0	0 1 1 0	D D D D 19 18 17 16	D D D D 15 14 13 12	D D D D 11 10 09 08	D D D D 07 06 05 04	D D D D 03 02 01 00	1 0 1 0
			---------- Data Payload ----------					

Where:
A[1:0]11=to switch chip, 00=from switch chip
B[1:0]00=Undefined,
01=Flow control channel,
10=Flow control channel,
11=Acknowledge to transceiver
D[19:0]20 bit data payload

2.2.2 CRQ Word Format on the Serial Data Lines to the Switch

The CRQ command word format as seen at the output of the transceiver is shown below. Two overhead bits are added by the transceiver to designate a CRQ word to the receiving switch chip. The signal ARB, AOA and BRK are used to control modes of operation in the switch chip. The serial data is transmitted with the MSB first.

33 32	31 30 29 28 27	26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00
0 0	0 B B 1 0 1 0	A A B R O R B A K	C C C C 00 01 02 03	C C C C 04 05 06 07	C C C C 08 09 10 11	C C C C 12 13 14 15	D D D D 03 02 01 00 --Data--	1 0 1 0
			------ Connection Bits ------					

Where:
B[1:0]00=Undefined,
01=Flow control channel,
10=Flow control channel,
11=Undefined
ARB1=Multi Queue arbitration
AOA1=Acknowledge on all connections granted, 0=Acknowledge on any connections granted
BRK 1=Break previous connection, 0=Do not break previous connection
C[0:15] Connection request bit map. Set bit high for each output requested
D[3:0] User defined data sent by transmitting port card

2.2.3 CRQ Word Format on the Serial Data Line From the Switch

The CRQ command word format as seen at the output of the switch chip is shown below. Two overhead bits are added by the switch chip to designate a command word (00) to the transceiver. This word is sent on to the receiving port card when an ACK is sent to the transmitting port card. The command word contains the current active connections for this input in the switch chip. The serial data is transmitted with the MSB first.

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33 32	31 30 29 28 27 26 25	24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00
0 0	0 B B 1 0 1 0 1 0	B R K	M M M M 00 01 02 03	M M M M 04 05 06 07	M M M M 08 09 10 11	M M M M 12 13 14 15	D D D D 03 02 01 00	1 0 1 0
			------ Active Connections ------				--Data--	

Where:
B[1:0]00=Undefined,
01=Flow control channel,
10=Flow control channel,
11=Acknowledge
BRK 1=This is the CRQ word for the next packet. This bit is used to break the current connection.
M[0:15]Current outputs the transmitting channel is connected to
D[3:0] User defined data sent by transmitting port card

2.3 Receiver Operation

In Packet Mode, the receiver looks for connection request (CRQ) words from the transceiver. All data words and IDLE words are passed on directly to the switch matrix. If BRK is HIGH, the current connection will be broken before processing the new connection request word. When BRK is LOW, the switch does not break current connections when making a new request. When AOA is HIGH, the switch will send an ACK only if the current switch connections match the C[0:15] bit field. When AOA is LOW, an ACK is sent back to the transceiver when any connection in the C[0:15] bit field is granted. In both cases, a response word is also returned to the transceiver from the switch. The response word can be embedded into an IDLE word or CRQ word that is sent back to the transceiver. If the transceiver makes a CRQ that requires a response (i.e., a multicast CRQ), the switch uses the flow control channel to force an IDLE word into the receiving data stream by forcing the internal ready to receive (RTR) signal low for one word clock (see the VSC870 data sheet).

The bit field C[0:15] is used to designate the output channels that are to be acted upon for a connection request operation. To request an output to connect to, set the corresponding bit HIGH. Multiple bits can be set HIGH at the same time for multicast. The sending port card can include 4 bits of data (D[3:0]) in the CRQ word that will be passed on to the destination port card. Two example word sequences from the transceiver on the serial interface are shown in the Figure 7. The two overhead bits (BB) are used for signaling on data words (see the VSC870 date sheet).

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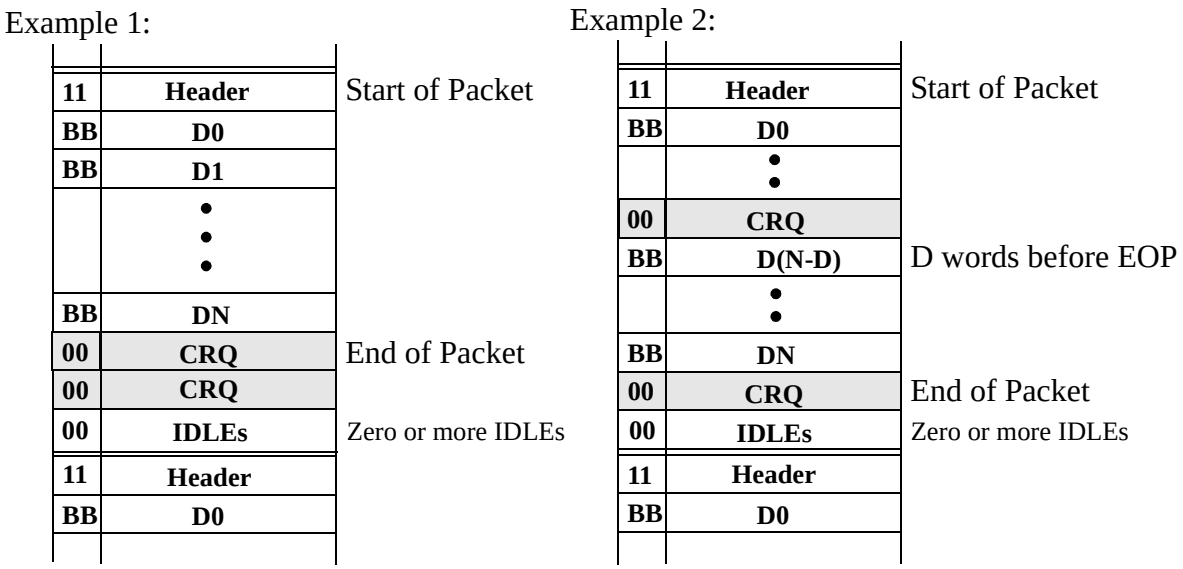
Figure 7: Packet Transmission Format from Transceiver



2.4 Arbitration

In Packet Mode, if multiple inputs request a connection to the same output, arbitration is performed. Connection requests come into the switch chip on each word clock, and the arbitration process takes two word clock cycles. Arbitration is round-robin with the last connection to an output getting the lowest priority for that output. For multicast, if BRK is LOW, arbitration will only be performed on the requested connections that are not currently granted. If a port is in the out of synch state, any connection request to this port will be always granted.

In order to improve bandwidth utilization, a system wide mode of operation can be used where the switch matrix reconfiguration time is delayed D word clocks after the time arbitration results are determined. This allows the user logic to receive arbitration results ahead of time so the port cards do not have to block data while waiting for these results. If the CRQ word is inserted into the current data packet D words before the end of the packet, arbitration results will be known at the port card just as the first word of the next data packet is ready for transmission, thus improving bandwidth utilization. The number D is selected based on the round trip delay from the time the port submits a CRQ until an ACK is received and the FIFO is ready to send a data word. This value of D is a system wide value and must be used by all port cards. D should be set to a maximum value equal to the round trip delay (typically 8 word clocks).

For Multi Queue connection requests from the transceiver (ARB = 1), the switch chip performs two levels of arbitration during two word clock cycles. The first level determines which of the requested outputs are available and holds these outputs. The second level chooses one winner from the available outputs then releases the rest. Because outputs can be blocked during the first level of arbitration, all Muti Queue CRQ commands are held at the switch chip and continue to request outputs until a connection is granted or a header word is detected. If a header word is detected at the transceiver, a repeated sequence of CRQ words is sent to the switch until a connection is granted. The port number of the granted output is returned to the port card using the two overhead bits (see VSC870 data sheet).

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2.5 Transmitter Operation

In Packet Mode, the transmitter sends out data words that come from the switch matrix, adding the appropriate overhead bit information for acknowledges, response bits and flow control. Acknowledges are used to signal the transceiver that a connection request has been granted (see the VSC870 data sheet). The response bits are used with the Multi Queue connection request word. The flow control channel is used to pass state information from the receiving port card to the transmitting port card. The switch redirects the flow control signals to the correct output using the current switch connection state information. In the case of multicast where there is more than one receiver, these channels are logically ORed before being sent back to the transmitter. The flow control channel is also used to send response bits from the switch to the transceiver for multi queue mode (see VSC870 data sheet).

Response words are required by the transceiver in Packet Mode. These response words are simply IDLE words or CRQ words in the data stream that are going back to the transceiver containing port connection status information. If the transceiver receives a connection request word that requires a response, it can use the flow control channel to force an IDLE word into the data stream. When this IDLE arrives at the switch, the switch adds the response data.

2.6 Disconnect Operation

A disconnect can be made to occur automatically after a packet is transmitted through the switch if the packet is followed by either a CRQ (Connection Request) associated with a new packet, or a null CRQ followed by a null header word. The CRQ associated with the new packet typically has the BRK bit set. This breaks down the old connection before it tries to establish the new connection through arbitration. This new connection is made only when the switch receives the header word. When the old connection is broken, the associated output ports are freed up, becoming available for new connections. The null CRQ is a CRQ with the BRK bit set, and has no output port selected. In this case, the switch chip will break down the old connection(s) and will not establish any new connections. The null CRQ word must be followed by a null (empty) header word. The switch will send IDLE words to the transceivers which have not established a new connection. During the packet transmission, if the sending link goes out of synch, the switch will terminate the connection and send an end of packet word (CRQ with the BRK bit set LOW) to the destination port followed by IDLE words. In this case, the receiving transceiver will receive only one CRQ instead of the two normally received.

2.7 Flow Control Channel

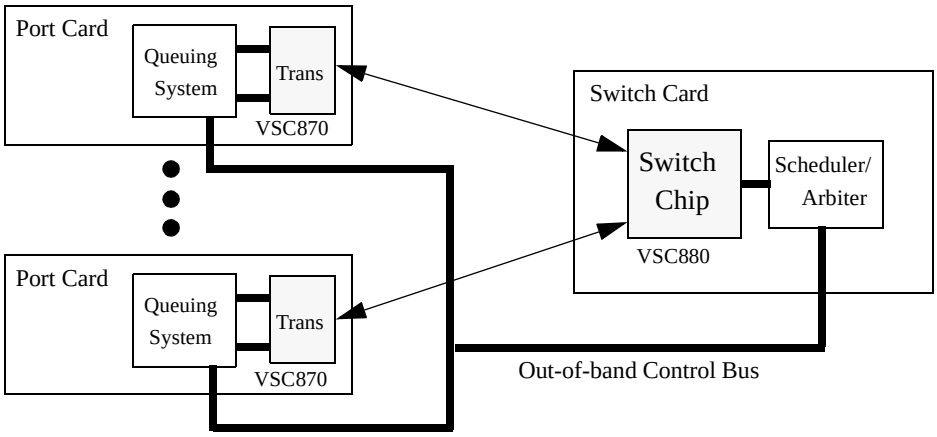
The VSC880 can support a back pressure mechanism by providing a flow control channel. The flow control channel is time shared with the signaling between the switch chip and the transceiver for acknowledgment and response bits. Therefore, it can only guarantee to pass the state information from input pin at the receiving port card through the switch and to the output pin at the transmitting port card. The main application for this flow control channel is to prevent the FIFO on the receiving side from overflowing. By using this channel, when the receive FIFO is almost full, the transmit FIFO will be disabled from sending data. During the time the switch is sending an ACK or response bits back to the port cards, these flow control bits are dropped by the switch. During a multicast transmission, the flow control channels are ORed in the switch. If a port is in an out of synch state, no flow control back pressure is exerted from this output.

3.0 Cell Mode

3.1 Overview

In Cell Mode (CMODE = HIGH), a more sophisticated arbitration scheme can be supported by using the VSC870 and the VSC880 switch in conjunction with a central (user defined) scheduler. In this mode, only fixed length data packets (cells) can be supported. A cell clock is connected to the switch chip, and the switch chip distributes the cell clock to all connected transceivers. The transceivers adjust their transmit cell clocks so that all transceivers send the first word of a cell at such time that it arrives at the switch chip aligned to the switch cell clock (see serial link operation above). In this mode, messages containing port card queue information are sent to the central scheduler using an out of band control bus. Arbitration and flow control information are then sent back to the port cards through the out of band control bus. The scheduler then configures the switch matrix by using the parallel interface. A picture of a cell based system is shown below. Multiple switch chips can be used in parallel to increase system bandwidth (see Application Note 32 “Design Guide for a Cell Based Switch with Central Control”).

Figure 8: Cell Based System



3.2 Data Encoding Format

The data word and command word formats are described in section 1.0. Command words use the overhead bits set to 00. Data words can have overhead bits 01, 10 or 11. The user can use these bits for signaling to the receiving port card. Information such as start of frame and end of frame can be passed through the switch in this manner.

3.3 Receiver Operation

If CMODE is HIGH, the receiver at each port examines the two overhead bits (B[1:0]) of the received word to determine the word type. If the word is a command word sent from the port card, the switch will respond based on the type of command specified in the C[4:0] bit field. If an IDLE word arrives at the end of the cell clock period and it does not have an embedded cell clock, a cell clock error is flagged. If it is a data word, it is sent to the switch fabric to be routed to its destination along with the user defined overhead bits.

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3.4 Transmitter Operation

If CMODE is HIGH and the force IDLE register is set LOW, the transmitter sends data words from the switch fabric. If the force IDLE register is set HIGH, IDLE words are transmitted. At the end of the cell clock period, bits B[1:0] in all IDLE words are set to 11 to embed the cell clock marker. For data words, user defined overhead bits are passed on to the destination as is.

3.5 Delaying The Cell Clock

If out-of-band messaging is used between the port cards and the switch card, there will be a phase offset between the cell clock (CCLK) on the switch card, and the transmit cell clock (RTM/TCLK) on the port card. A cell clock delay value can be programmed into the control register CDEL[3:0] to set the time the switch is configured after receiving a cell clock. This adds 1-14 word clocks worth of delay between CCLK input to the switch chip and the cell clock sent to the transceivers from the switch chip. In this way, the transmit cell clock (RTM/TCLK) on the transceivers can be aligned to the cell clock at the switch chip (CCLK). For a typical system design where the transceiver is less then 20” from the switch chip, the default value of 5 can be used. See Application Note 32 for more details.

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AC Characteristics

Table 1: LVDS and TTL Outputs

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
$T_{R,TTL}$	TTL Output Rise Time	2.5			ns	10-90% @ 50pF
$T_{F,TTL}$	TTL Output Fall Time	2.5			ns	10-90% @ 50pF
$T_{R,LVDS}$	LVDS Output Rise Time		100		ps	20-80%
$T_{F,LVDS}$	LVDS Output Fall Time		100		ps	20-80%

Figure 9: Parallel Data Input Timing Diagram

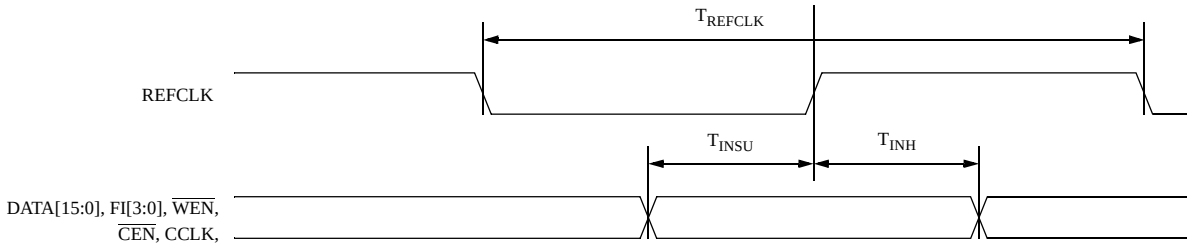

Table 2: Transmit Data Input Timing Table

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{REFCLK}	Reference (word) clock period		16		ns
F_{REFCLK}	Reference clock frequency stability			100	ppm
J_{REFCLK}	Reference clock input jitter			7	ps RMS
T_{INSU}	Parallel data setup time with respect to REFCLK	1			ns
T_{INH}	Parallel data hold time with respect to REFCLK	2			ns
T_{SKEW}	REFCLK to REFCLK skew using parallel switch chips			1	ns

Note: Duty cycle for T_{REFCLK} is 50% +/- 10% worst case

Figure 10: Parallel Data Output Timing Diagram

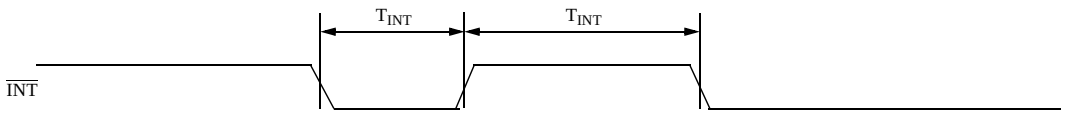

Table 3: Receive Data Output Timing Table

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{INT}	Interrupt pulse width	15			ns
T_{RESET}	$\overline{RESET}$, RESYNEN pulse width	64			ns

Figure 11: CPU Interface Write Cycle Timing

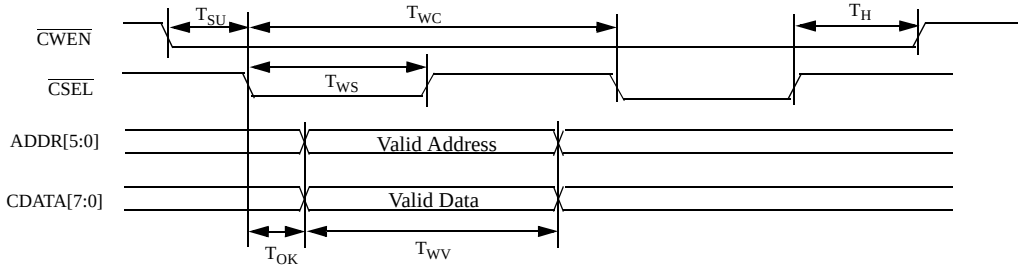

Figure 12: CPU Interface Read Cycle Timing

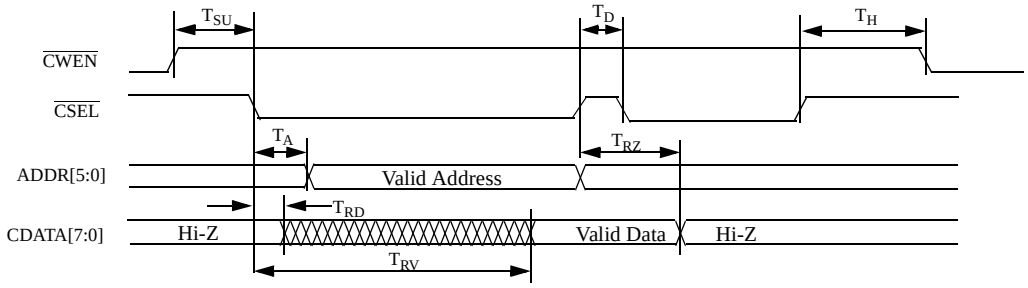

Table 4: CPU Interface Timing Table

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{OK}	CSEL falling edge to valid address			5	ns
T_D	$\overline{CSEL}$ inactive between read cycles	10			ns
T_{SU}	$\overline{CWEN}$ valid to $\overline{CSEL}$ falling edge	5			ns
T_H	$\overline{CSEL}$ active to $\overline{CWEN}$ change	5			ns
T_{WV}	Valid data and address during a write	45			ns
T_{WS}	$\overline{CSEL}$ low time during a write	20			ns
T_{WC}	$\overline{CSEL}$ cycle time during a write	55			ns
T_{RV}	$\overline{CSEL}$ active to valid data	15		45	ns
T_{RZ}	$\overline{CSEL}$ deactivate to high impedance data			5	ns
T_{RD}	$\overline{CSEL}$ active to low impedance data	0			ns

DC Characteristics

Table 5: LVDS and TTL Inputs and Outputs

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	I_{OH} = -6.0 mA
V_{OL}	Output LOW voltage (TTL)	—	—	0.4	V	I_{OL} = +6.0 mA
V_{OCM}	O/P Common Mode Range (LVDS)	1.2	—	2.1	V	At Min ΔV_{OUT}
ΔV_{OUT}	Differential Output Voltage (LVDS)	400	—	1000	mV	100Ω across input
V_{ICM}	I/P Common Mode Range (LVDS)	0.8	—	2.5	V	At Min ΔV_{IN}
ΔV_{IN}	Differential Input Voltage (LVDS)	200	—	1600	mV	—
V_{IH}	Input HIGH voltage (TTL)	2.0	—	V_{DD}+1.0	V	—
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	—	500	µA	V_{IN} =2.4V
I_{IL}	Input LOW current (TTL)	- 50	—	—	µA	V_{IN} = 0.4V
I_{OZB}	Bi-directional (TTL) HIGH current 3-State Output OFF			500	µA	V_{OUT}=2.4V

Hot Swap

The LVDS input and output buffers are subject to hot swap events while being connected and disconnected from the passive backplane. If the input is powered down but still receiving a signal from an output, the input must tolerate extra input current and power. If the input is powered up but has no input connection, it must go to a valid logic state. The Table 6 below lists the LVDS I/O parameters that relate to hot swap condition.

Table 6: Hot Swap LVDS I/O Parameters

Parameters	*Description*	*Value*	*Units*	*Conditions*
I_{CO}	LVDS maximum current delivered per output pin	10	mA	Normal Operation
I_{CI}	LVDS maximum current allowed per input pin	40	mA	V_{DD} = 0V
P_{CI}	LVDS maximum added power per output pin	60	mW	V_{DD} = 0V on VSC870
V_{CDL}	LVDS input default logic state	LOW	—	Input Open

Power Dissipation

Table 7: Power Supply Currents

Parameter	*Description*	*(Max)*	*Units*
I_{DD}	Power supply current from V_{DD}, V_{DDA} (V_{DD}, V_{DDA} = 3.3V + 5%)	1000	mA
I_{DDA}	Power supply current from V_{DDA} (V_{DDA} = 3.3V + 5%)	200	mA
I_{DDX}	Power supply current from each serial data quadrant V_{DDX} (V_{DDX} = 3.3V + 5%)	750	mA
I_{MM}	Power supply current from V_{MM} (V_{MM} = 2.5V + 5%)	6800	mA
P_{DS}	Power dissipation (V_{DD} = 3.3V+5%, V_{MM} = 2.5V+5%, all quadrants powered)	30.7	W
P_{DD}	Power dissipation (V_{DD} = 3.3V+5%, V_{MM} = 2.0V+5%, all quadrants powered)	28.1	W

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Absolute Maximum Ratings(1)

Power Supply Voltage (V_{DD}) Potential to GND ..... -0.5V to +4V
Power Supply Voltage (V_{MM}) Potential to GND ..... -0.5V to +4V
DC Input Voltage (LVDS inputs) ..... -0.5V to V_{DD} + 1.0V
DC Input Voltage (TTL inputs) ..... -0.5V to 5.5V
DC Input Voltage (TTL inputs for CDATA[7:0]) ..... -0.5V to V_{DD} + 1.0V
DC Output Voltage (TTL outputs) ..... -0.5V to V_{DD} + 1.0V
Output Current (TTL outputs) ..... +/-50mA
Output Current (LVDS outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C

NOTE: (1) Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{DD}) ..... +3.3V ±5 %
Power Supply Voltage (V_{MM}) ..... (+2.0V to +2.5V) ±5 %
Extended Commercial Operating Temperature Range(1) (T) ..... 0°C to 85°C

NOTE: (1) Lower limit of specification is ambient temperature and upper limit is case temperature.

Package Pin Descriptions

Signal	*Pin*
NC	A01
VSS	A02
VSS	A03
VSS	A04
NC	A05
REFCLK	A06
CCLK	A07
VSS	A08
DATA[2]	A09
DATA[5]	A10
DATA[6]	A11
DATA[10]	A12
DATA[13]	A13
DATA[14]	A14
FI[1]	A15
VSS	A16
$\overline{\text{WEN}}$	A17
BSTRST	A18
NC	A19
VSS	A20
VSS	A21
VSS	A22
NC	A23
VSS	B01
VSS	B02
VSS	B03
NC	B04
NC	B05
NC	B06
TCLKEN	B07
VMM	B08
DATA[1]	B09
DATA[3]	B10
DATA[8]	B11
DATA[9]	B12
DATA[11]	B13
FI[0]	B14

Signal	*Pin*
FI[2]	B15
VMM	B16
BSTLPBK	B17
NC	B18
NC	B19
NC	B20
VSS	B21
VSS	B22
VSS	B23
NC	C01
VSS	C02
NC	C03
NC	C04
NC	C05
VSS	C06
VMM	C07
$\overline{\text{RESET}}$	C08
DATA[0]	C09
DATA[4]	C10
DATA[7]	C11
VMM	C12
DATA[12]	C13
DATA[15]	C14
FI[3]	C15
$\overline{\text{CEN}}$	C16
VMM	C17
VSS	C18
NC	C19
VSS	C20
NC	C21
VSS	C22
NC	C23
VMM	D01
NC	D02
VDD1	D03
NC	D04
VSSA	D05

Signal	*Pin*
VDDA	D06
NC	D07
VMM	D08
VDD	D09
VMM	D10
VMM	D11
VDD1	D12
VMM	D13
VMM	D14
VDD	D15
VMM	D16
BSTEN	D17
VDD	D18
VSS	D19
NC	D20
VDD4	D21
NC	D22
VMM	D23
RXS[0]-	E01
VSS	E02
TXS[0]+	E03
VDD1	E04
VDD4	E20
TXS[15]+	E21
VSS	E22
RXS[15]-	E23
VSS	F01
RXS[0]+	F02
VDD1	F03
TXS[0]-	F04
TXS[15]-	F20
VDD4	F21
RXS[15]+	F22
VSS	F23
TXS[1]+	G01
VSS	G02
RXS[1]-	G03

Signal	*Pin*
VDD1	G04
VDD4	G20
RXS[14]-	G21
VSS	G22
TXS[14]+	G23
VDD1	H01
TXS[1]-	H02
VDD1	H03
RXS[1]+	H04
RXS[14]+	H20
VDD4	H21
TXS[14]-	H22
VDD4	H23
RXS[2]-	J01
VSS	J02
TXS[2]+	J03
VDD1	J04
VDD4	J20
TXS[13]+	J21
VSS	J22
RXS[13]-	J23
NC	K01
RXS[2]+	K02
VDD1	K03
TXS[2]-	K04
TXS[13]-	K20
VDD4	K21
RXS[13]+	K22
VSS	K23
RXS[3]-	L01
RXS[3]+	L02
NC	L03
VSS	L04
VSS	L20
NC	L21
RXS[12]+	L22
RXS[12]-	L23

Signal	Pin
VMM	M01
VDD1	M02
TXS[3]-	M03
TXS[3]+	M04
TXS[12]+	M20
TXS[12]-	M21
VDD4	M22
VMM	M23
VMM	N01
VDD2	N02
TXS[4]-	N03
TXS[4]+	N04
TXS[11]+	N20
TXS[11]-	N21
VDD3	N22
VMM	N23
RXS[4]-	P01
RXS[4]+	P02
VSS	P03
NC	P04
VSS	P20
NC	P21
RXS[11]+	P22
RXS[11]-	P23
NC	R01
RXS[5]+	R02
VDD2	R03
TXS[5]-	R04
TXS[10]-	R20
VDD3	R21
RXS[10]+	R22
VSS	R23
RXS[5]-	T01
VSS	T02
TXS[5]+	T03
VDD2	T04
VDD3	T20
TXS[10]+	T21
VSS	T22

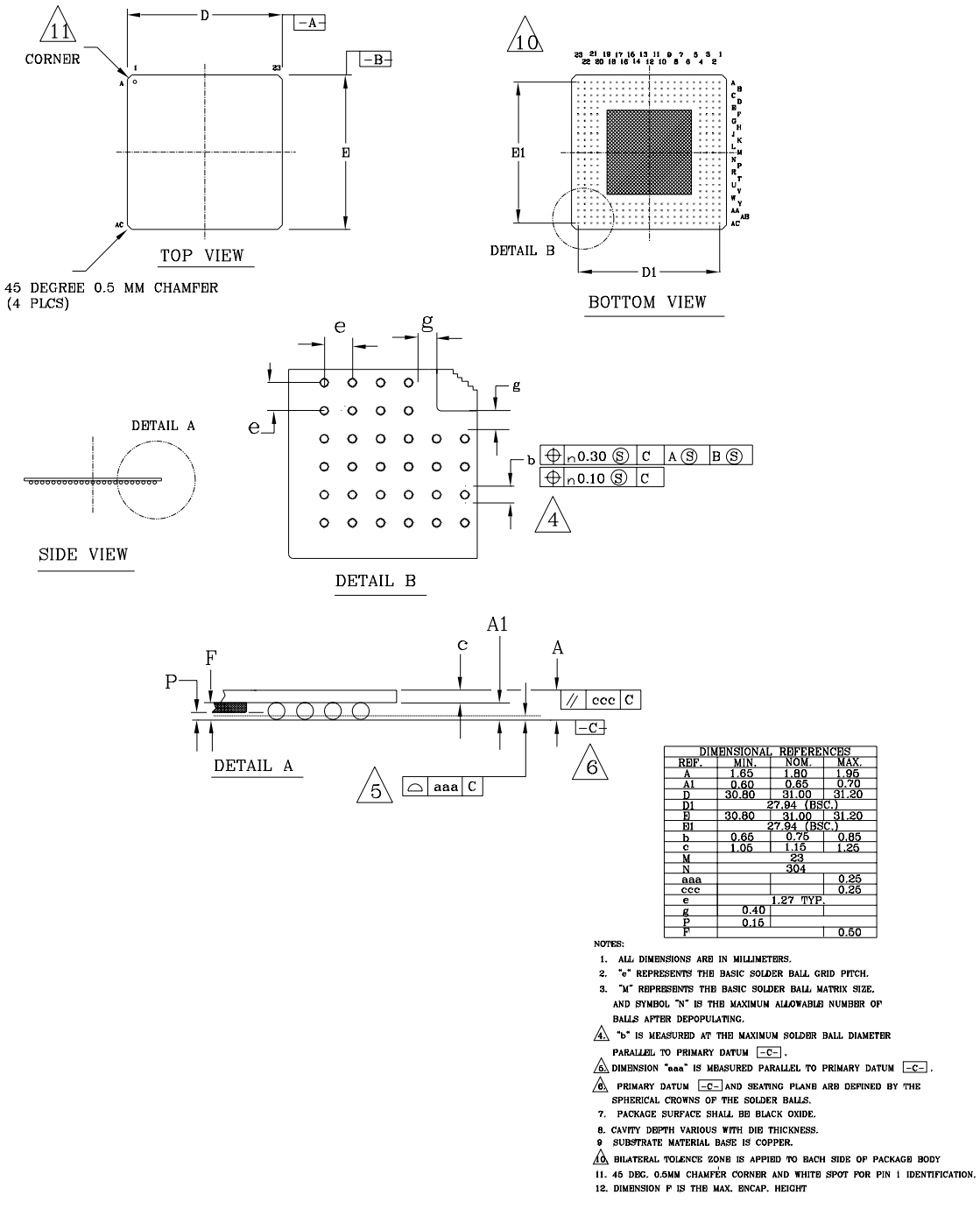
Signal	Pin
RXS[10]-	T23
VDD2	U01
TXS[6]-	U02
VDD2	U03
RXS[6]+	U04
RXS[9]+	U20
VDD3	U21
TXS[9]-	U22
VDD3	U23
TXS[6]+	V01
VSS	V02
RXS[6]-	V03
VDD2	V04
VDD3	V20
RXS[9]-	V21
VSS	V22
TXS[9]+	V23
VSS	W01
RXS[7]+	W02
VDD2	W03
TXS[7]-	W04
TXS[8]-	W20
VDD3	W21
RXS[8]+	W22
VSS	W23
RXS[7]-	Y01
NC	Y02
TXS[7]+	Y03
VMM	Y04
VSS	Y05
VDD	Y06
SCANOUT	Y07
VDD	Y08
VDD	Y09
VMM	Y10
VMM	Y11
VSS	Y12
VMM	Y13
VMM	Y14

Signal	Pin
VDD	Y15
VDD	Y16
CDATA[4]	Y17
VDD	Y18
VSS	Y19
VMM	Y20
TXS[8]+	Y21
NC	Y22
RXS[8]-	Y23
VMM	AA01
VDD2	AA02
VMM	AA03
VSS	AA04
VSCIPNC	AA05
VSS	AA06
VSS	AA07
LOCKDET	AA08
NC	AA09
SCANIN	AA10
TESTEN	AA11
VMM	AA12
ADDR[3]	AA13
ADDR[0]	AA14
NC	AA15
CDATA[1]	AA16
VSS	AA17
VSS	AA18
NC	AA19
NC	AA20
VMM	AA21
VDD3	AA22
VMM	AA23
NC	AB01
VSS	AB02
VSS	AB03
NC	AB04
VSCOPNC	AB05
NC	AB06
WCLK	AB07

Signal	Pin
VMM	AB08
NC	AB09
FACLPBK	AB10
RESYNEN	AB11
VSCTE	AB12
ADDR[4]	AB13
$\overline{\text{CSEL}}$	AB14
NC	AB15
VMM	AB16
CDATA[2]	AB17
CDATA[5]	AB18
CDATA[7]	AB19
NC	AB20
VSS	AB21
VSS	AB22
VSS	AB23
VSS	AC01
VSS	AC02
VSS	AC03
VSS	AC04
NC	AC05
BSTPASS	AC06
$\overline{\text{INT}}$	AC07
VSS	AC08
MEN	AC09
NC	AC10
CMODE	AC11
ADDR[5]	AC12
ADDR[2]	AC13
ADDR[1]	AC14
$\overline{\text{CWEN}}$	AC15
VSS	AC16
CDATA[0]	AC17
CDATA[3]	AC18
CDATA[6]	AC19
VSS	AC20
VSS	AC21
VSS	AC22
VSS	AC23

Package Information

304 BGA Package



DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	1.65	1.80	1.95
A1	0.60	0.65	0.70
D	30.80	31.00	31.20
D1		27.94 (BSC.)	
E	30.80	31.00	31.20
E1		27.94 (BSC.)	
b	0.65	0.75	0.85
c	1.05	1.15	1.25
M		23	
N		304	
aaa			0.25
ccc			0.25
e		1.27 TYP.	
g	0.40		
P	0.15		
F			0.50

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "M" REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE, AND SYMBOL "N" IS THE MAXIMUM ALLOWABLE NUMBER OF BALLS AFTER DEPOPULATING.
4. "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM -C-.
5. DIMENSION "aaa" IS MEASURED PARALLEL TO PRIMARY DATUM -C-.
6. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. PACKAGE SURFACE SHALL BE BLACK OXIDE.
8. CAVITY DEPTH VARIOUS WITH DIE THICKNESS.
9. SUBSTRATE MATERIAL BASE IS COPPER.
10. BILATERAL TOLENCE ZONE IS APPIED TO EACH SIDE OF PACKAGE BODY
11. 45 DEG. 0.5MM CHAMFER CORNER AND WHITE SPOT FOR PIN 1 IDENTIFICATION.
12. DIMENSION F IS THE MAX. ENCAP. HEIGHT

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Package Thermal Characteristics

The VSC880 is packaged in a thermally enhanced 31mm 304TBGA with an embedded heat sink. The heat sink surface configurations are shown in the package drawings. With natural convection, the junction to case thermal resistance is estimated to be 0.45°C/W. The approximate air flow versus thermal resistance relationship is shown in Table 12.3. Note: The VSC880 is not guaranteed to operate under cold start conditions. If the ambient temperature is 0°C, 15 seconds after power is applied, the case temperature will be at least 30°C, at which point it will be at thermal equilibrium and ready for operation.

Table 8: Theta Junction-to-Ambient versus Air Velocity

Air Velocity (LFPM)	*Junction-to-Ambient Thermal Resistance (°C/W)*	
	Low Conductivity 2-Layer Board	*High Conductivity 4-Layer Board*
0	17.5	13.0
100	15.0	11.0
200	13.0	10.0
400	11.0	9.0
600	10.0	8.0

Ordering Information

The order number for this product is formed by a combination of the device number and package type.

VSC880 xx

Device Type
High Performance 16x16
Serial Crosspoint Switch

Package
TY: 304 BGA
Extended Commerical Temperature: 0°C ambient to +85°C case

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