

# SN74LS165

## 8-Bit Parallel-to-Serial Shift Register

The SN74LS165 is an 8-bit parallel load or serial-in register with complementary outputs available from the last stage. Parallel inputting occurs asynchronously when the Parallel Load ( $\overline{PL}$ ) input is LOW. With  $\overline{PL}$  HIGH, serial shifting occurs on the rising edge of the clock; new data enters via the Serial Data (DS) input. The 2-input OR clock can be used to combine two independent clock sources, or one input can act as an active LOW clock enable.

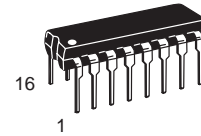
### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			–0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

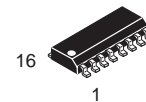


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### LOW POWER SCHOTTKY



PLASTIC  
N SUFFIX  
CASE 648



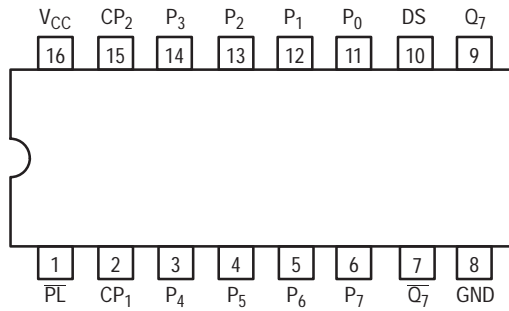
SOIC  
D SUFFIX  
CASE 751B

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS165N	16 Pin DIP	2000 Units/Box
SN74LS165D	16 Pin	2500/Tape & Reel

# SN74LS165

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

CP <sub>1</sub> , CP <sub>2</sub>	Clock (LOW-to-HIGH Going Edge) Inputs
DS	Serial Data Input
PL	Asynchronous Parallel Load (Active LOW) Input
P <sub>0</sub> – P <sub>7</sub>	Parallel Data Inputs
Q <sub>7</sub>	Serial Output from Last State
Q̄ <sub>7</sub>	Complementary Output

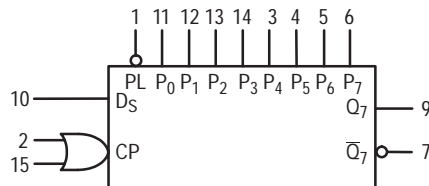
### LOADING (Note a)

	HIGH	LOW
CP <sub>1</sub> , CP <sub>2</sub>	0.5 U.L.	0.25 U.L.
DS	0.5 U.L.	0.25 U.L.
PL	1.5 U.L.	0.75 U.L.
P <sub>0</sub> – P <sub>7</sub>	0.5 U.L.	0.25 U.L.
Q <sub>7</sub>	10 U.L.	5 U.L.
Q̄ <sub>7</sub>	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

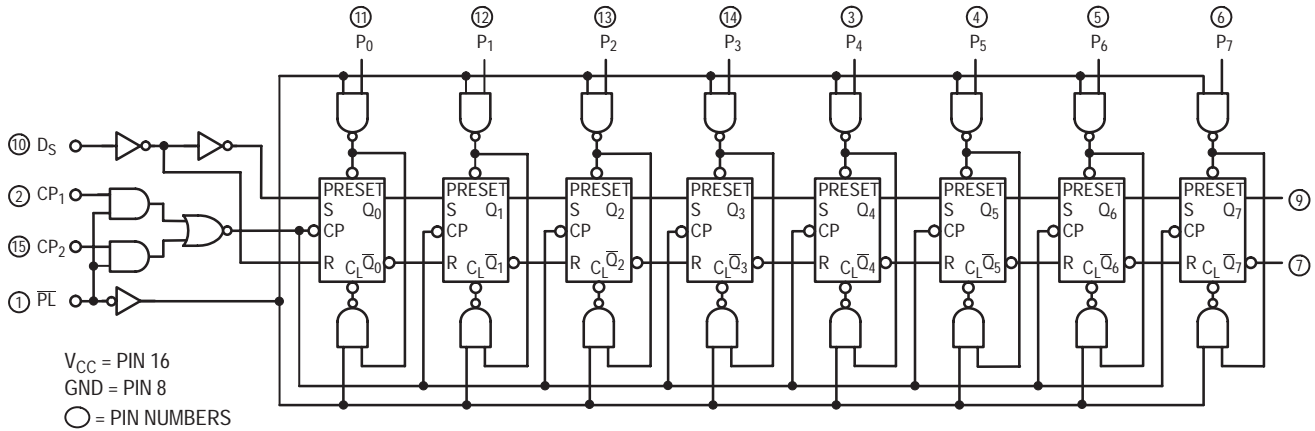
### LOGIC SYMBOL



V<sub>CC</sub> = PIN 16  
GND = PIN 8

# SN74LS165

## LOGIC DIAGRAM



### FUNCTIONAL DESCRIPTION

The SN74LS165 contains eight clocked master/slave RS flip-flops connected as a shift register, with auxiliary gating to provide overriding asynchronous parallel entry. Parallel data enters when the  $\overline{P_L}$  signal is LOW. The parallel data can change while  $\overline{P_L}$  is LOW, provided that the recommended setup and hold times are observed.

For clock operation,  $\overline{P_L}$  must be HIGH. The two clock inputs perform identically; one can be used as a clock inhibit

by applying a HIGH signal. To avoid double clocking, however, the inhibit signal should only go HIGH while the clock is HIGH. Otherwise, the rising inhibit signal will cause the same response as a rising clock edge. The flip-flops are edge-triggered for serial operations. The serial input data can change at any time, provided only that the recommended setup and hold times are observed, with respect to the rising edge of the clock.

### TRUTH TABLE

$\overline{P_L}$	CP		CONTENTS								RESPONSE
	1	2	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Q <sub>7</sub>	
L	X	X	P <sub>0</sub>	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	P <sub>4</sub>	P <sub>5</sub>	P <sub>6</sub>	P <sub>7</sub>	Parallel Entry
H	L	$\overline{\text{---}}$	D <sub>S</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Right Shift
H	H	$\overline{\text{---}}$	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Q <sub>7</sub>	No Change
H	$\overline{\text{---}}$	L	D <sub>S</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Right Shift
H	$\overline{\text{---}}$	H	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Q <sub>7</sub>	No Change

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

# SN74LS165

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current Other Inputs P <sub>L</sub> Input			20 60	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
	Other Inputs P <sub>L</sub> Input			0.1 0.3	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current Other Inputs P <sub>L</sub> Input			-0.4 -1.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			36	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Input Clock Frequency	25	35		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay P <sub>L</sub> to Output		22 22	35 35	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to Output		27 28	40 40	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay P <sub>7</sub> to Q <sub>7</sub>		14 21	25 30	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay P <sub>7</sub> to Q <sub>7</sub>		21 16	30 25	ns	

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>W</sub>	CP Clock Pulse Width	25			ns	V <sub>CC</sub> = 5.0 V
t <sub>W</sub>	P <sub>L</sub> Pulse Width	15			ns	
t <sub>S</sub>	Parallel Data Setup Time	10			ns	
t <sub>S</sub>	Serial Data Setup Time	20			ns	
t <sub>S</sub>	CP <sub>1</sub> to CP <sub>2</sub> Setup Time <sup>1</sup>	30			ns	
t <sub>H</sub>	Hold Time	0			ns	
t <sub>rec</sub>	Recovery Time, P <sub>L</sub> to CP	45			ns	

<sup>1</sup>The role of CP<sub>1</sub> and CP<sub>2</sub> in an application may be interchanged.

**DEFINITION OF TERMS:**

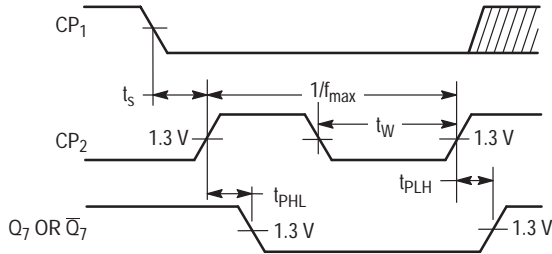
**SETUP TIME ( $t_s$ )** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

**HOLD TIME ( $t_h$ )** — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure

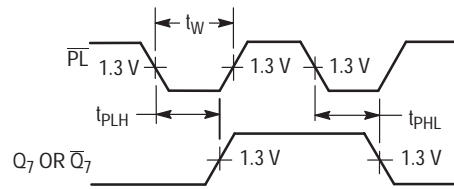
continued recognition. A negative hold time indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

**RECOVERY TIME ( $t_{rec}$ )** — is defined as the minimum time required between the end of the  $\overline{PL}$  pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer loaded Data to the Q outputs.

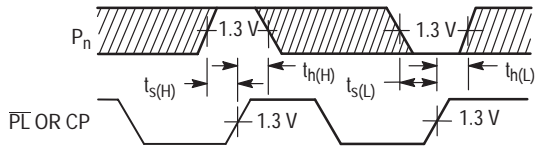
**AC WAVEFORMS**



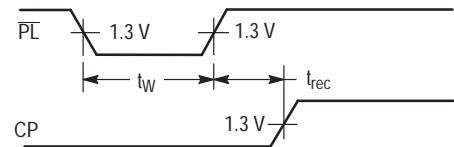
**Figure 1.**



**Figure 2.**



**Figure 3.**

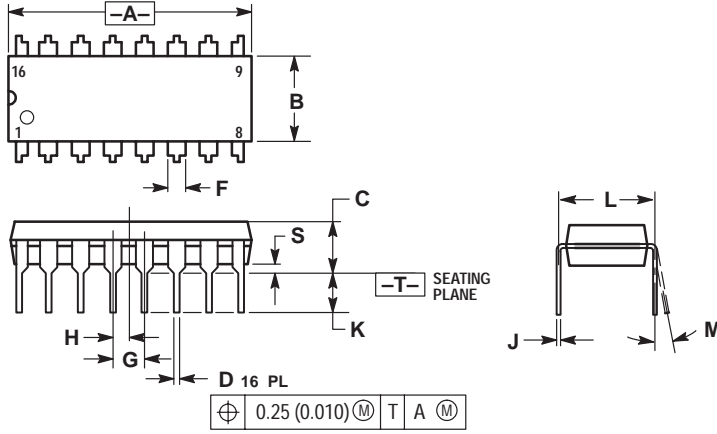


**Figure 4.**

# SN74LS165

## PACKAGE DIMENSIONS

**N SUFFIX**  
**PLASTIC PACKAGE**  
**CASE 648-08**  
**ISSUE R**



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0° 10°		0° 10°	
S	0.020	0.040	0.51	1.01

# SN74LS165

## PACKAGE DIMENSIONS

### D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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