

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC4062

DUAL J-FET INPUT LOW-POWER OPERATIONAL AMPLIFIER

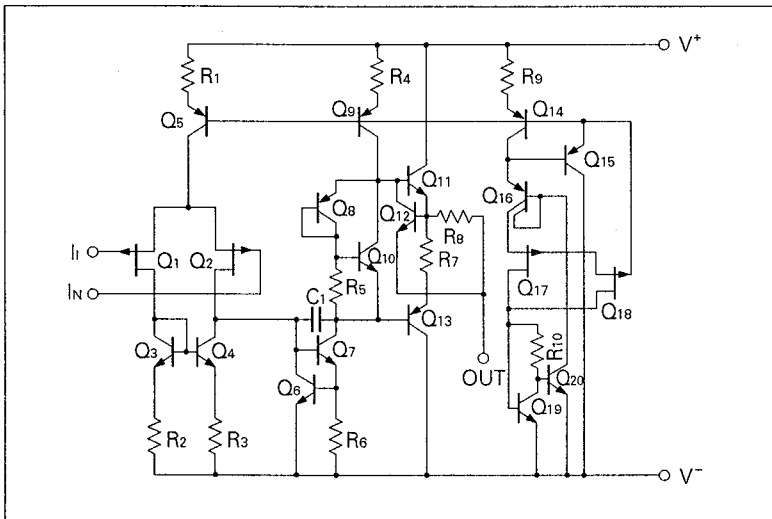
DESCRIPTION

The μPC4062 is a low-power, J-FET input, operational amplifier featuring low supply voltage operation from ±2 V. Supply current of μPC4062 is 1/10 the supply current of a μPC4082 op-amp. With very low input bias current characteristics, the μPC4062 is an excellent choice for hand-held measurement equipment and other low-power application circuits.

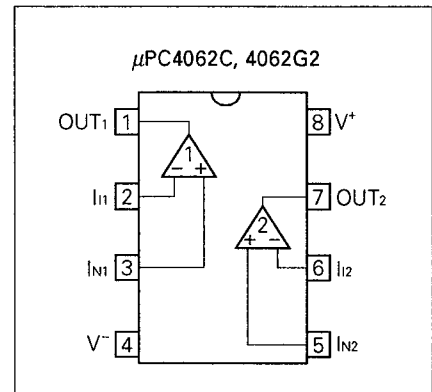
FEATURES

- Low supply current: 400 μA (TYP.)
- Very low input bias and offset currents
- High input impedance...J-FET Input Stage
- Low supply voltage operation
- Output short circuit protection
- Internal frequency compensation

EQUIVALENT CIRCUIT (1/2 Circuit)



CONNECTION DIAGRAM (Top View)



ORDERING INFORMATION

| PART NUMBER | PACKAGE | QUALITY GRADE |
|-------------|-----------------------------|---------------|
| μPC4062C | 8 PIN PLASTIC DIP (300 mil) | Standard |
| μPC4062G2 | 8 PIN PLASTIC SOP (225 mil) | Standard |

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specifications of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25\text{ }^\circ\text{C}$)

| PARAMETER | | SYMBOL | μ PC4062 | UNIT |
|--|---------------------|-------------|----------------------------|------------------|
| Voltage between V^+ and V^- (Note 1) | | $V^+ - V^-$ | -0.3 to +36 | V |
| Differential Input Voltage | | V_{ID} | ± 30 | V |
| Input Voltage (Note 2) | | V_I | $V^- - 0.3$ to $V^+ + 0.3$ | V |
| Output Voltage (Note 3) | | V_O | $V^- - 0.3$ to $V^+ + 0.3$ | V |
| Power Dissipation | C Package (Note 4) | P_T | 350 | mW |
| | G2 Package (Note 5) | | 440 | mW |
| Output Short Circuit Duration (Note 6) | | | Indefinite | sec |
| Operating Temperature Range | | T_{opt} | -20 to +80 | $^\circ\text{C}$ |
| Storage Temperature Range | | T_{stg} | -55 to +125 | $^\circ\text{C}$ |

Note 1. Reverse connection of supply voltage can cause destruction.

Note 2. The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.

Note 3. This specification is the voltage which should be allowed to supply to the output terminal from external without damage or destructive. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The output voltage of normal operation will be the Output Voltage Swing of electrical characteristics.

Note 4. Thermal derating factor is $-5.0\text{ mV} / ^\circ\text{C}$ when ambient temperature is higher than $55\text{ }^\circ\text{C}$.

Note 5. Thermal derating factor is $-4.4\text{ mV} / ^\circ\text{C}$ when ambient temperature is higher than $25\text{ }^\circ\text{C}$.

Note 6. Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings, Note 4 and Note 5.

RECOMMENDED OPERATING CONDITIONS

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|--------------------------------|-----------------------|---------|------|----------|------|
| Supply Voltage | V^\pm | ± 2 | | ± 16 | V |
| Output Current (SOURCE) | $I_{O\text{ SOURCE}}$ | | | 5 | mA |
| Output Current (SINK) | $I_{O\text{ SINK}}$ | | | 3.5 | mA |
| Capacitive Load ($A_v = +1$) | C_L | | | 100 | pF |

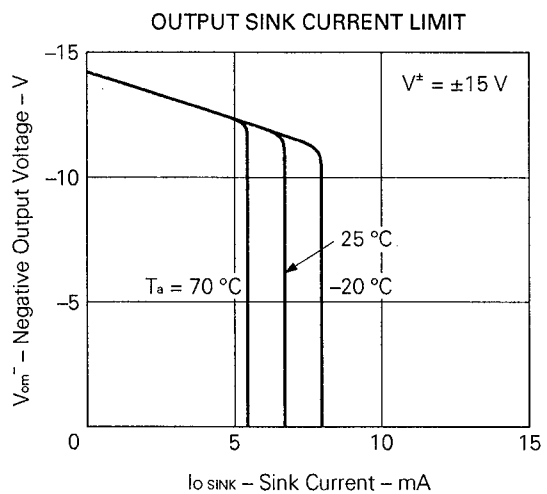
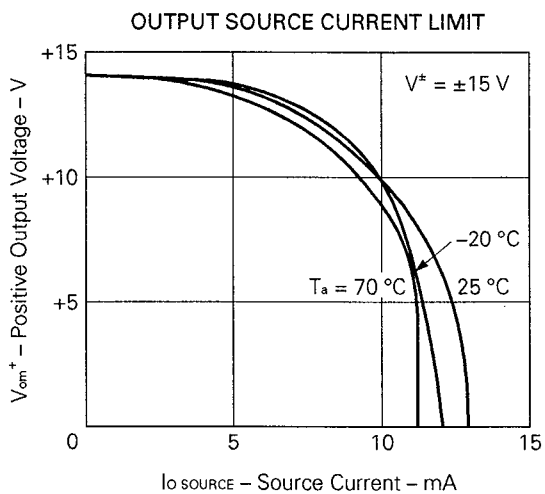
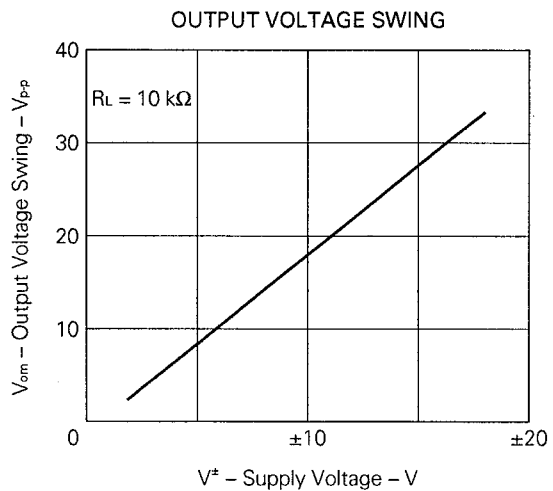
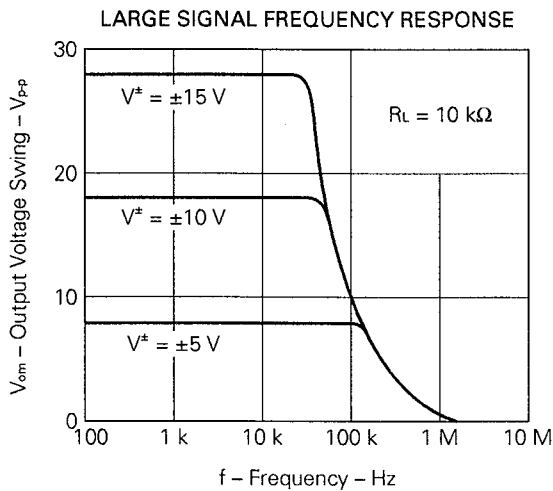
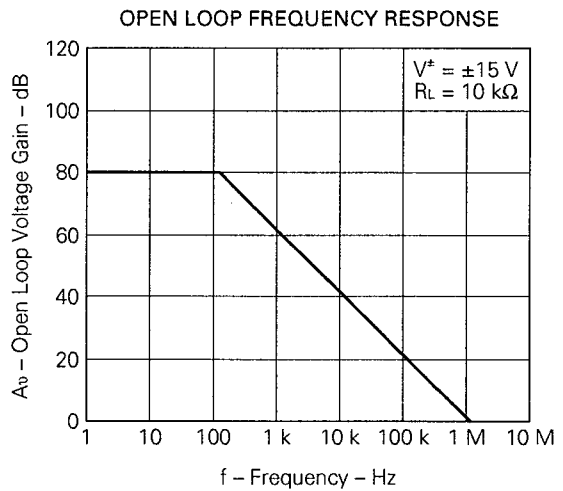
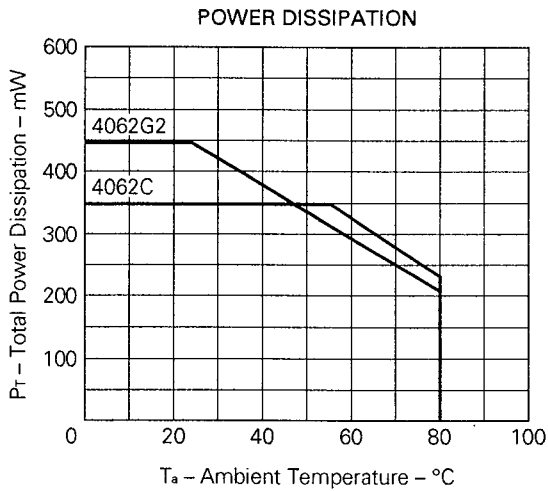
ELECTRICAL CHARACTERISTICS ($T_a = 25\text{ }^\circ\text{C}$, $V^\pm = \pm 15\text{ V}$)

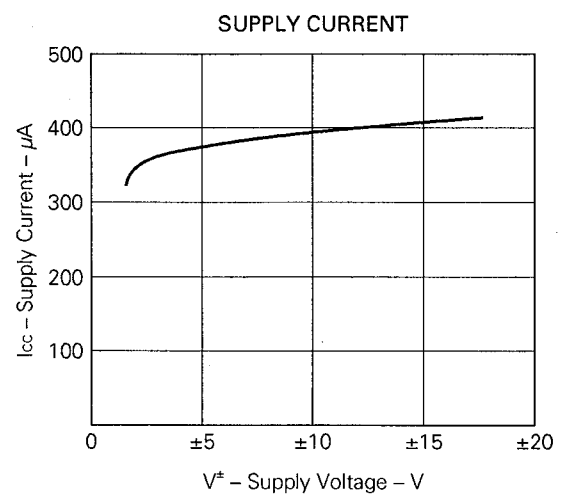
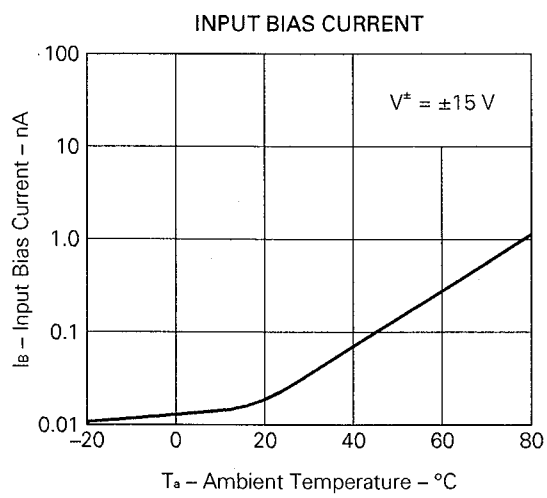
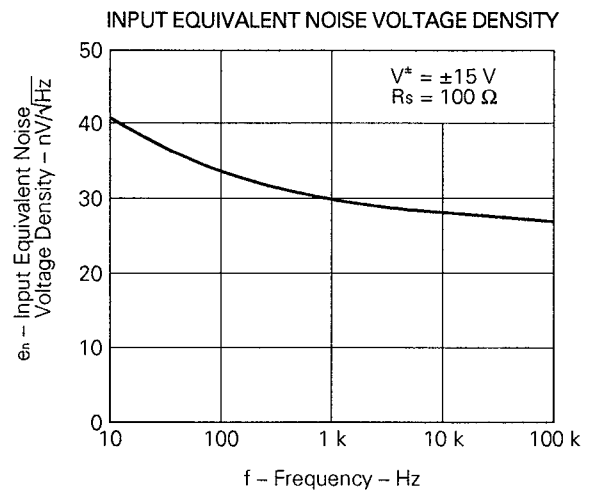
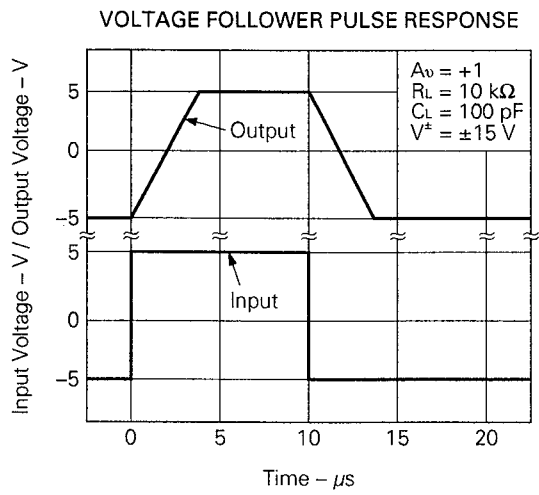
| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | CONDITION |
|--|--------------------------|----------|----------------|----------|------------------------------|---|
| Input Offset Voltage | V_{io} | | ± 2 | ± 10 | mV | $R_s \leq 50\ \Omega$ |
| Input Offset Current (Note 7) | I_{io} | | ± 5 | ± 50 | pA | |
| Input Bias Current (Note 7) | I_B | | 10 | 100 | pA | |
| Large Signal Voltage Gain | A_v | 3 | 9 | | V/mV | $R_L \geq 10\ \text{k}\Omega$, $V_o = \pm 10\ \text{V}$ |
| Supply Current | I_{cc} | | 400 | 500 | μA | $I_o = 0\ \text{A}$, Both Amplifiers |
| Common Mode Rejection Ratio | CMR | 70 | 90 | | dB | |
| Supply Voltage Rejection Ratio | SVR | 70 | 90 | | dB | |
| Output Voltage Swing | V_{om} | ± 12 | +14.0 -13.6 | | V | $R_L \geq 10\ \text{k}\Omega$ |
| Common Model Input Voltage Range | V_{icM} | ± 12 | +15 -13 | | V | |
| Slew Rate | SR | | 3 | | V/ μs | $A_v = 1$ |
| Unity Gain Frequency | f_{unity} | | 1 | | MHz | |
| Input Equivalent Noise Voltage Density | e_n | | 30 | | nV/ $\sqrt{\text{Hz}}$ | $R_s = 100\ \Omega$, $f = 1\ \text{kHz}$ |
| Channel Separation | | | 120 | | dB | |
| Input Offset Voltage | V_{io} | | | ± 15 | mV | $R_s \leq 50\ \Omega$, $T_a = -20\ \text{to}\ +70\ ^\circ\text{C}$ |
| Average V_{io} Temperature Drift | $\Delta V_{io}/\Delta T$ | | ± 10 | | $\mu\text{V}/^\circ\text{C}$ | $T_a = -20\ \text{to}\ +70\ ^\circ\text{C}$ |
| Input Offset Current (Note 7) | I_{io} | | | ± 2 | nA | $T_a = -20\ \text{to}\ +70\ ^\circ\text{C}$ |
| Input Bias Current (Note 7) | I_B | | | 3.5 | nA | $T_a = -20\ \text{to}\ +70\ ^\circ\text{C}$ |

Note 7. Input bias currents flow into IC. Because each currents are gate leak current of P-channel J-FET on input stage.

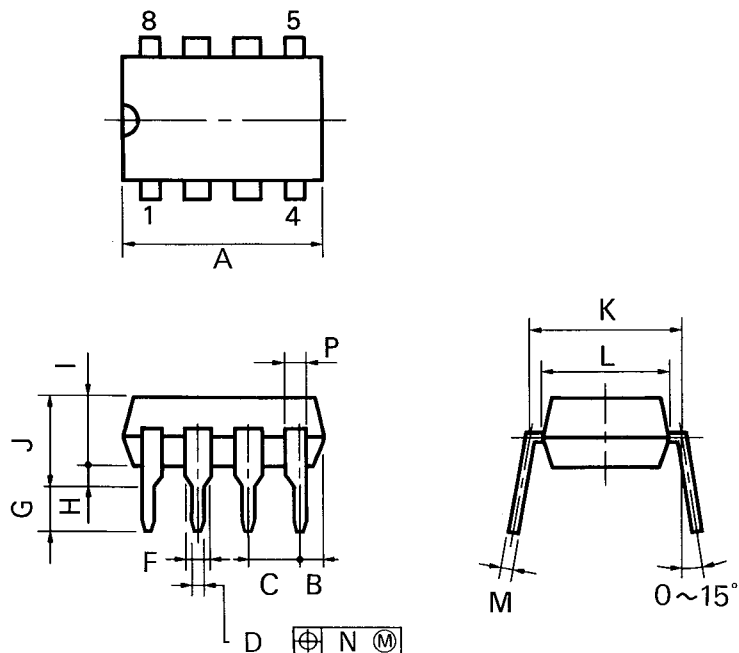
And that are temperature sensitive. Short time measuring method is recommendable to maintain the junction temperature close to the ambient temperature.

TYPICAL PERFORMANCE CHARACTERISTICS ($T_a = 25^\circ\text{C}$, TYP.)





8PIN PLASTIC DIP (300 mil)



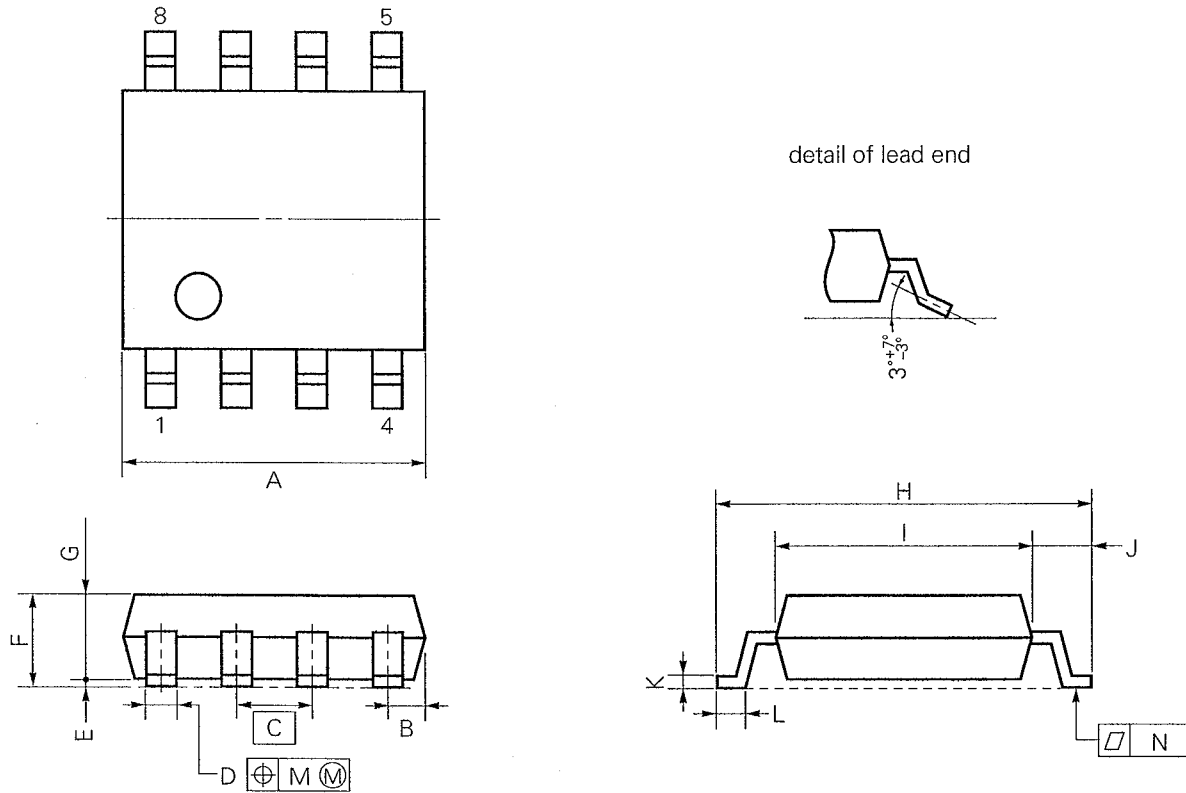
P8C-100-300B,C

NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| A | 10.16 MAX. | 0.400 MAX. |
| B | 1.27 MAX. | 0.050 MAX. |
| C | 2.54 (T.P.) | 0.100 (T.P.) |
| D | 0.50 ^{+0.10} | 0.020 ^{+0.004} _{-0.005} |
| F | 1.4 MIN. | 0.055 MIN. |
| G | 3.2 ^{+0.3} | 0.126 ^{+0.012} |
| H | 0.51 MIN. | 0.020 MIN. |
| I | 4.31 MAX. | 0.170 MAX. |
| J | 5.08 MAX. | 0.200 MAX. |
| K | 7.62 (T.P.) | 0.300 (T.P.) |
| L | 6.4 | 0.252 |
| M | 0.25 ^{+0.10} _{-0.05} | 0.010 ^{+0.004} _{-0.003} |
| N | 0.25 | 0.01 |
| P | 0.9 MIN. | 0.035 MIN. |

8 PIN PLASTIC SOP (225 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S8GM-50-225B-2

| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| A | 5.37 MAX. | 0.212 MAX. |
| B | 0.78 MAX. | 0.031 MAX. |
| C | 1.27 (T.P.) | 0.050 (T.P.) |
| D | 0.40 ^{+0.10} _{-0.05} | 0.016 ^{+0.004} _{-0.003} |
| E | 0.1±0.1 | 0.004±0.004 |
| F | 1.8 MAX. | 0.071MAX. |
| G | 1.49 | 0.059 |
| H | 6.5±0.3 | 0.256±0.012 |
| I | 4.4 | 0.173 |
| J | 1.1 | 0.043 |
| K | 0.15 ^{+0.10} _{-0.05} | 0.006 ^{+0.004} _{-0.002} |
| L | 0.6±0.2 | 0.024 ^{+0.008} _{-0.009} |
| M | 0.12 | 0.005 |
| N | 0.15 | 0.006 |

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.
 Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

[μPC4062G2]

| Soldering method | Soldering conditions | Recommended condition symbol |
|------------------------|--|------------------------------|
| Infrared ray reflow | Peak package's surface temperature: 230 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 1, Exposure limit*: None | IR30-00-1 |
| VPS | Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 1, Exposure limit*: None | VP15-00-1 |
| Wave soldering | Solder temperature: 260 °C or below, Flow time: 10 seconds or below Number of flow process: 1, Exposure limit*: None | WS15-00-1 |
| Partial heating method | Terminal temperature: 300 °C or below, Flow time: 10 seconds or below, Exposure limit*: None | |

*: Exposure limit before soldering after dry-pack package is opened.
 Storage conditions: 25 °C and relative humidity at 65 % or less.

Note: Do not apply more than a single process at once, except for "Partial heating method."

TYPES OF THROUGH HOLE DEVICE

[μPC4062C]

| Soldering method | Soldering conditions | Recommended condition symbol |
|------------------|--|------------------------------|
| Wave soldering | Solder temperature: 260 °C or below, Flow time: 10 seconds or below | |

[MEMO]

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Application examples recommended by NEC Corporation.

Standard: Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tools, Industrial robots, Audio and Visual equipment, Other consumer products, etc.

Special: Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.