

# MOS FIELD EFFECT TRANSISTOR $\mu$ PA1721

# SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

### **DESCRIPTION**

The  $\mu$ PA1721 is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

### **FEATURES**

· Low on-resistance

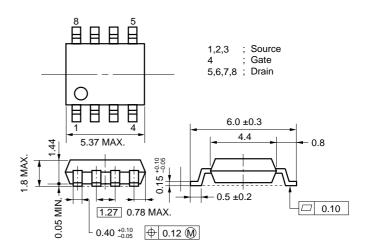
$$\begin{split} &R_{DS(on)1} = 10.5 \text{ m}\Omega \text{ MAX. (VGs} = 10 \text{ V, ID} = 5.0 \text{ A)} \\ &R_{DS(on)2} = 14.0 \text{ m}\Omega \text{ MAX. (VGs} = 4.5 \text{ V, ID} = 5.0 \text{ A)} \\ &R_{DS(on)3} = 17.0 \text{ m}\Omega \text{ MAX. (VGs} = 4.0 \text{ V, ID} = 5.0 \text{ A)} \end{split}$$

- Low Ciss: Ciss = 2200 pF TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

### ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1721G	Power SOP8

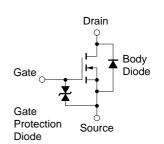
### PACKAGE DRAWING (Unit: mm)



### ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (Vgs = 0 V)	Voss	30	V	
Gate to Source Voltage (Vps = 0 V)	Vgss	±20	V	
Drain Current (DC)	ID(DC)	±10	Α	
Drain Current (pulse) Note1	D(pulse)	±40	Α	
Total Power Dissipation $(T_A = 25^{\circ}C)^{Note2}$	Рт	2.0	W	
Channel Temperature	Tch	150	°C	
Storage Temperature	$T_{stg}$	-55 to +150	°C	

### **EQUIVALENT CIRCUIT**



**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1 %

2. Mounted on ceramic substrate of 1200 mm<sup>2</sup> x 2.2 mm

**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.



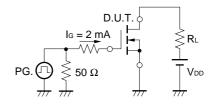
### ELECTRICAL CHARACTERISTICS (TA = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	Vgs = 10 V, ID = 5.0 A		8.0	10.5	mΩ
	RDS(on)2	Vgs = 4.5 V, ID = 5.0 A		10.0	14.0	mΩ
	RDS(on)3	Vgs = 4.0 V, ID = 5.0 A		12.0	17.0	mΩ
Gate to Source Cut-off Voltage	VGS(off)	VDS = 10 V, ID = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	yfs	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5.0 A	7.0	14.0		S
Drain Leakage Current	IDSS	Vps = 30 V, Vgs = 0 V			10	μΑ
Gate to Source Leakage Current	Igss	Vgs = ±20 V, Vps = 0 V			±10	μΑ
Input Capacitance	Ciss	Vps = 10 V		2200		pF
Output Capacitance	Coss	Vgs = 0 V		710		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		270		pF
Turn-on Delay Time	t <sub>d(on)</sub>	ID = 5.0 A		30		ns
Rise Time	tr	VGS(on) = 10 V		90		ns
Turn-off Delay Time	t <sub>d(off)</sub>	VDD = 15 V		90		ns
Fall Time	<b>t</b> f	$R_G = 10 \Omega$		50		ns
Total Gate Charge	Q <sub>G</sub>	ID = 10 A		39		nC
Gate to Source Charge	Qss	VDD = 24 V		6.3		nC
Gate to Drain Charge	Q <sub>GD</sub>	Vgs = 10 V		10.0		nC
Body Diode Forward Voltage	VF(S-D)	IF = 10 A, VGS = 0 V		0.8		V
Reverse Recovery Time	trr	IF = 10 A, VGS = 0 V		40		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ μs		50		nC

### TEST CIRCUIT 1 SWITCHING TIME

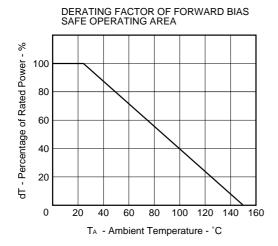
# PG. $\bigcap_{RG} R_G = 10 \Omega$ $\tau = 1 \mu s$ Duty Cycle $\leq 1 \%$

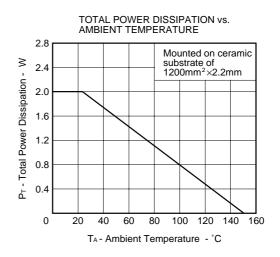
### **TEST CIRCUIT 2 GATE CHARGE**

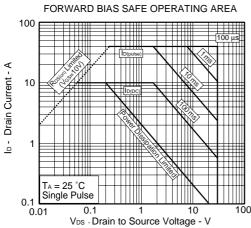




### **★** TYPICAL CHARACTERISTICS (TA = 25 °C)

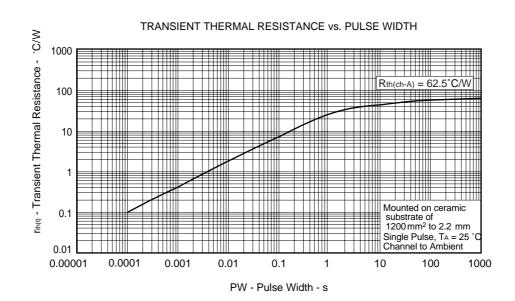






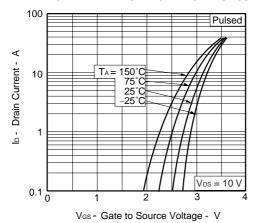
### Note

Mounted on ceramicsubstrate of 1200 mm<sup>2</sup> × 2.2 mm

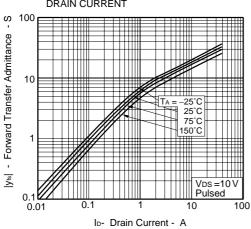


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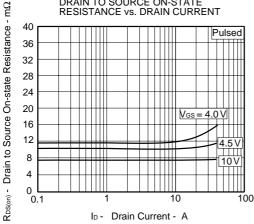
#### FORWARD TRANSFER CHARACTERISTICS



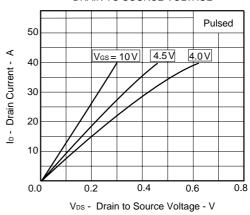
# FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



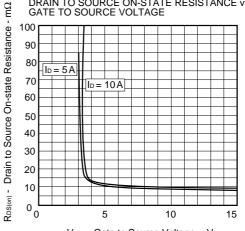
### DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT 40



# DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

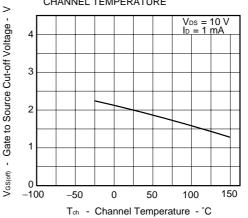


# DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

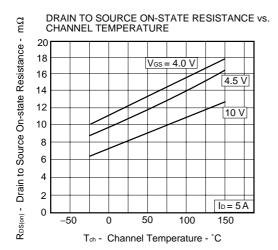


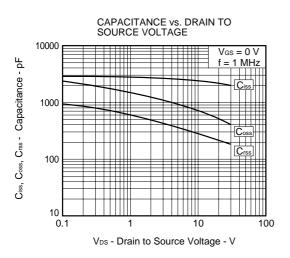
V<sub>GS</sub> - Gate to Source Voltage - V

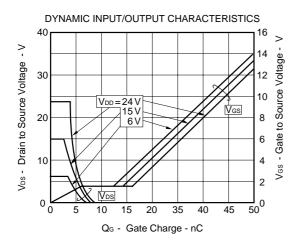
# GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

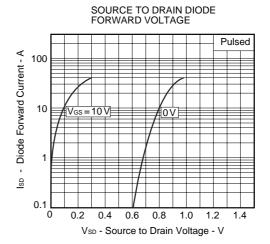


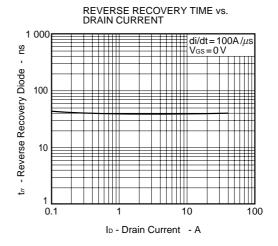












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