NEC

MOS INTEGRATED CIRCUIT

μPD75P308

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD75P308 is a model of the μPD75308 equipped with a one-time PROM or EPROM instead of an internal mask ROM.

Two types are available as the μPD75P308. The one-time PROM type is ideal for production of a small quantity of many different types of application systems as data can only be written once to the one-time PROM of this type. Programs can be written and rewritten to the built-in EPROM type making it ideal for system evaluation.

Detailed functions are described in the followig user's manual. Be sure to read it for designing.

μPD75308 User's Manual: IEM-5016

FEATURES

- μPD75308 compatible
- Memory capacity
  - Program memory (PROM): 8064 x 8 bits
  - Data memory (RAM): 512 x 4 bits
- Can be connected to a pull-up resistor through software: Ports 0-3, 6, 7
- Open-drain input/output: Ports 4 and 5
- Single power source: 5V ± 5%

ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD75P308GF-3B9	80-pin plastic QFP (14 x 20 mm)	One-time PROM
μPD75P308K	80-pin ceramic WQFN (LCC w/window)	EPROM

QUALITY GRADE ★

Part Number	Package	Quality Grade
μPD75P308GF-001-3B9	80-pin plastic QFP (14 x 20 mm)	Standard
μPD75P308K	80-pin Ceramic WQFN (LCC w/window)	Standard

Please refer to "Quality Grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The function common to the one-time PROM and EPROM types of product is referred to as PROM throughout this document.

The information in this document is subject to change without notice.

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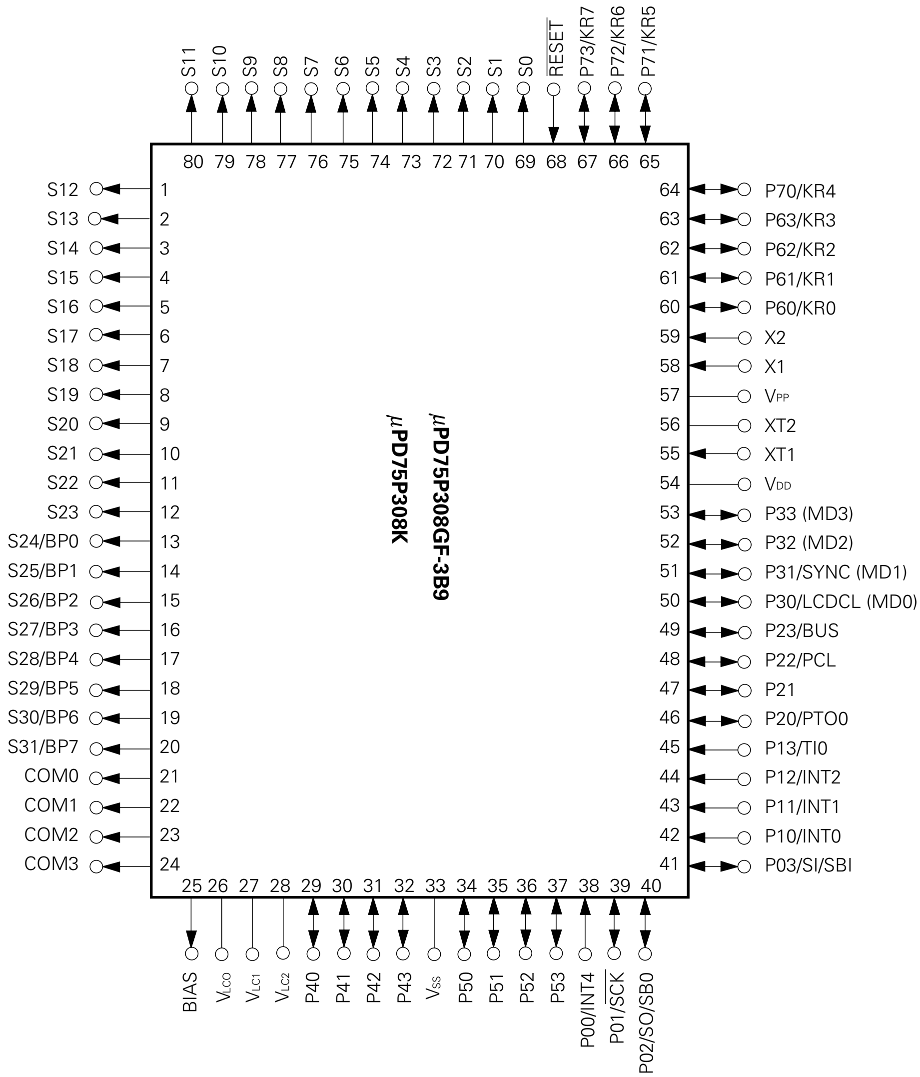
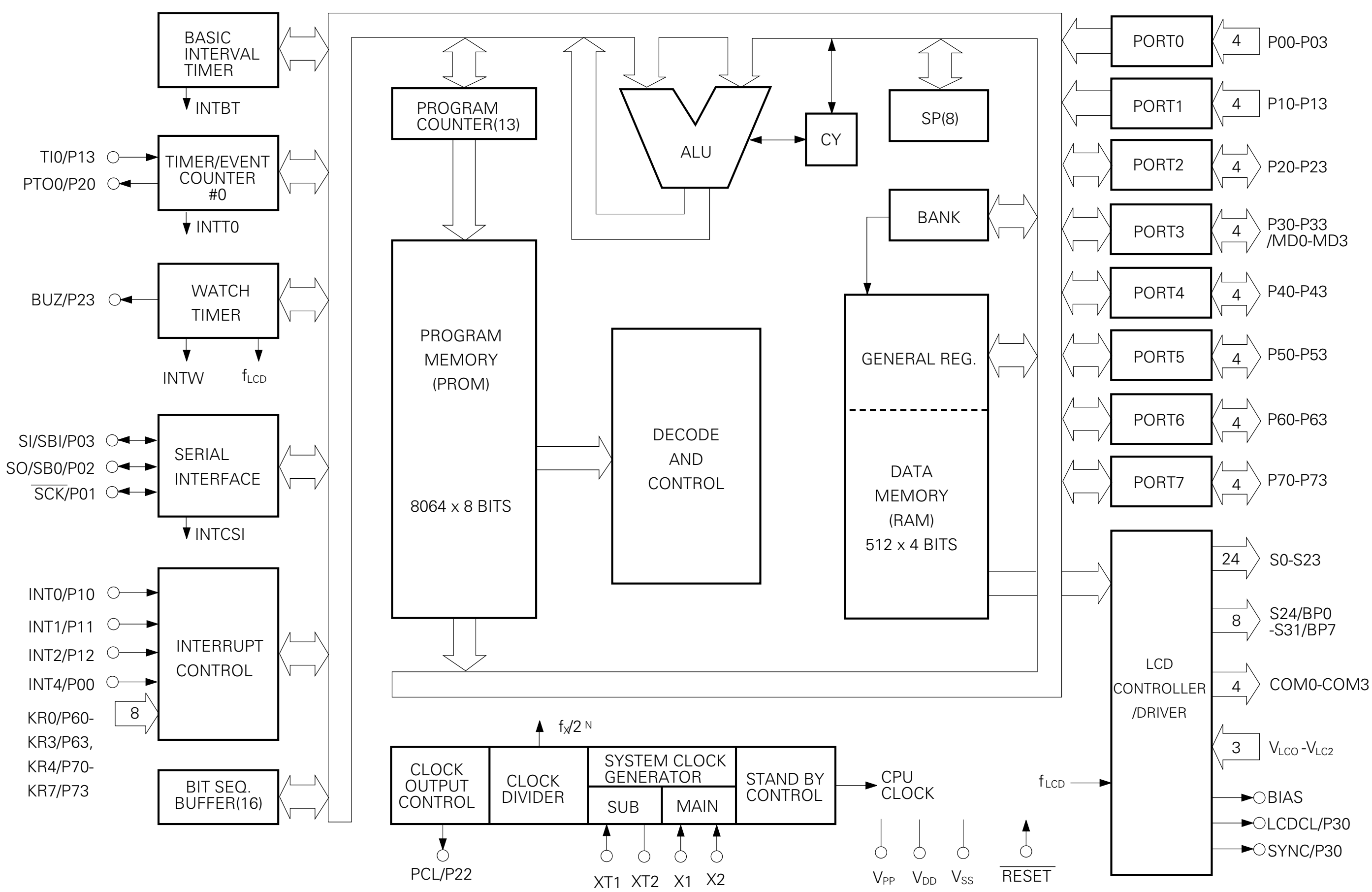
Date Published November 1993 P
Printed in Japan

The mark ★ shows major revised points.

PIN CONFIGURATION



BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

1.1 PORT PINS

Pin Name	Input/Output	Also Served As	Function	8-Bit I/O	When Reset	Input/ Output Circuit TYPE*1
P00	Input	INT4	4-bit input port (PORT0) Pull-up resistors can be specified in 3-bit units for the P01 to P03 pins by software.	X	Input	Ⓑ
P01	Input/Output	$\overline{SCK}$				Ⓕ-A
P02	Input/Output	SO/SB0				Ⓕ-B
P03	Input/Output	SI/SBI				Ⓜ-C
P10	Input	INT0	With noise elimination function 4-bit input port (PORT1) Internal pull-up resistors can be specified in 4-bit units by software.	X	Input	Ⓑ-C
P11		INT1				
P12		INT2				
P13		TI0				
P20	Input/Output	PTO0	4-bit input/output port (PORT2) Internal pull-up resistors can be specified in 4-bit units by software.	X	Input	E-B
P21		—				
P22		PCL				
P23		BUZ				
P30*2	Input/Output	LCDCL, MD0	Programmable 4-bit input/output port (PORT3) This port can be specified for input/output in bit units. Internal pull-up resistors can be specified in 4-bit units by software.	X	Input	E-B
P31*2		SYNC, MD1				
P32*2		MD2				
P33*2		MD3				
P40-43*2	Input/Output	—	N-ch open-drain 4-bit input/output port (PORT4) Data input/output pin for writing and verifying of program memory (PROM) (lower 4 bits)	○	High impedance	M-A
P50-P53*2	Input/Output	—	N-ch open-drain 4-bit input/output port (PORT5) Data input/output pin for writing and verifying of program memory (PROM) (upper 4 bits)		High impedance	M-A
P60	Input/Output	KR0	Programmable 4-bit input/output port (PORT6) This port can be specified for input/output in bit units. Internal pull-up resistors can be specified in 4-bit units by software.	○	Input	Ⓕ-A
P61		KR1				
P62		KR2				
P63		KR3				
P70	Input/Output	KR4	4-bit input/output port (PORT7) Internal pull-up resistors can be specified in 4-bit units by software.		Input	Ⓕ-A
P71		KR5				
P72		KR6				
P73		KR7				
BP0	Output	S24	1-bit output port (BIT PORT) Shared with a segment output pin.	X	*3	G-C ★
BP1		S25				
BP2		S26				
BP3		S27				
BP4	Output	S28				
BP5		S29				
BP6		S30				
BP7		S31				

*1: Circles indicate schmitt trigger inputs.

2: Can directly drive LED.

3: For BP0-7, V_{LC1} indicated below are selected as the input source.
However, the output level is changed depending on BP0-7 and the V_{LC1} external circuits.

1.2 NON PORT PINS

Pin Name	Input/Output	Also Served As	Function	When Reset	Input/ Output Circuit TYPE*1
TI0	Input	P13	Timer/event counter external event pulse input	—	Ⓑ-C
PTO0	Output	P20	Timer/event counter output	Input	E-B
PCL	Input/Output	P22	Clock output	Input	E-B
BUZ	Input/Output	P23	Fixed frequency output (for buzzer or for trimming the system clock)	Input	E-B
$\overline{SCK}$	Input/Output	P01	Serial clock input/output	Input	Ⓕ-A
SO/SB0	Input/Output	P02	Serial data output Serial bus input/output	Input	Ⓕ-B
SI/SB1	Input/Output	P03	Serial data input Serial bus input/output	Input	Ⓜ-C
INT4	Input	P00	Edge detection vector interrupt input (either rising or falling edge detection is effective)	—	Ⓑ
INT0	Input	P10	Edge detection vector interrupt input (detection edge can be selected)	—	Ⓑ-C
INT1		P11			
INT2	Input	P12	Edge detection testable input (rising edge detection)	—	Ⓑ-C
KR0-KR3	Input/Output	P60-P63	Testable input/output(parallel falling edge detection)	Input	Ⓕ-A
KR4-KR7	Input/Output	P70-P73	Testable input/output(parallel falling edge detection)	Input	Ⓕ-A
S0-S23	Output	—	Segment signal output	*3	G-A
★ S24-S31	Output	BP0-7	Segment signal output	*3	G-C
COM0-COM3	Output	—	Common signal output	*3	G-B
V_{LC0}-V_{LC2}	—	—	LCD drive power	—	—
BIAS	—	—	External dividing resistor disconnect output	High-impedance	—
LCDCL*2	Input/Output	P30	Externally expanded driver clock output	Input	E-B
SYNC*2	Input/Output	P31	Externally expanded driver sync clock output	Input	E-B
X1, X2	Input	—	To connect the crystal/ceramic oscillator to the main system clock generator. When inputting the external clock, input the external clock to pin X1, and the reverse phase of the external clock to pin X2.	—	—
XT1	Input	—	To connect the crystal oscillator to the subsystem clock generator. When the external clock is used, in XT1 inputs the external clock. In this case, pin XT2 must be left open. Pin XT1 can be used as a 1-bit input (test) pin.	—	—
XT2	—	—			
$\overline{RESET}$	Input	—	System reset input (low level active)	—	Ⓑ
MD0-MD3	Input/Output	P30-P33	To select mode when writing/verifying of program memory (PROM)	Input	E-B
V_{PP}	—	—	Program voltage application when writing and verifying of program memory (PROM) Connect to V_{DD} during the normal operation Apply +12.5V when writing/verifying EPROM	—	—
V_{DD}	—	—	Positive power supply	—	—
V_{SS}	—	—	GND	—	—

*1: Circles indicate schmitt trigger inputs.

2: These pins are provided for future system expansion. At present, these pins are used only as pins P30 and P31.

3: For these display output, V_{LCX} indicated below are selected as the input source.

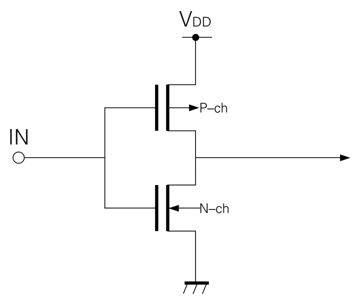
S0 to S31: V_{LC1}, COM0 to COM2: V_{LC2}, COM3: V_{LC0}

However, display output level varies depending on the particular display output and V_{LCX} external circuit.

1.3 PIN INPUT/OUTPUT CIRCUITS

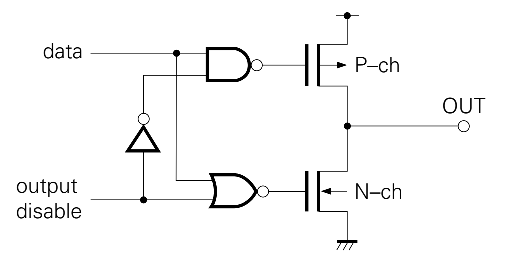
The following shows a simplified input/output circuit diagram for each pin of the μPD75P308.

TYPE A (for TYPE E–B)



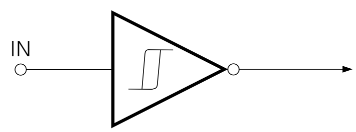
Input buffer of CMOS standard

TYPE D (for TYPE E–B, F-A)



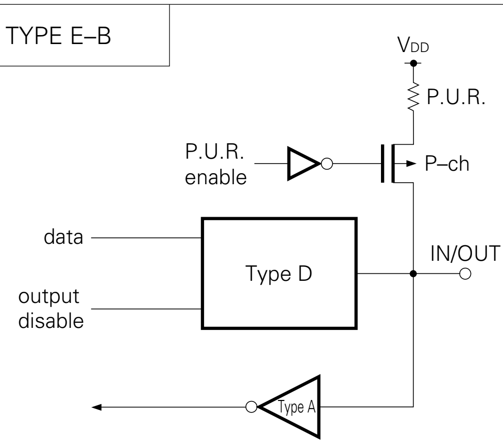
Push–pull output that can be set in a output high–impedance state (both P–ch and N–ch are off)

TYPE B



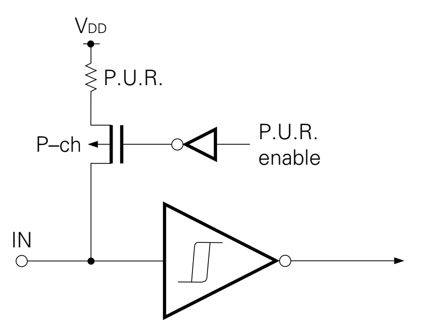
Schmitt trigger input with hysteresis characteristics

TYPE E–B



P.U.R. : Pull–Up Resistor

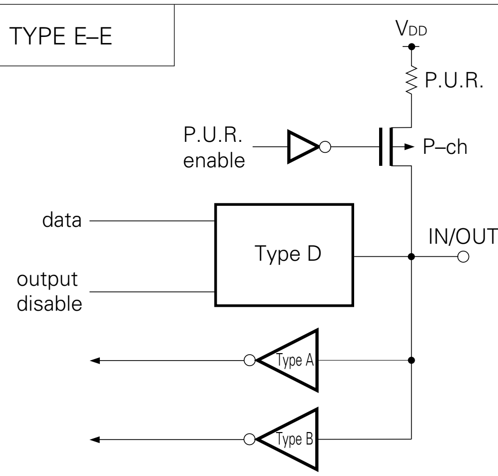
TYPE B–C



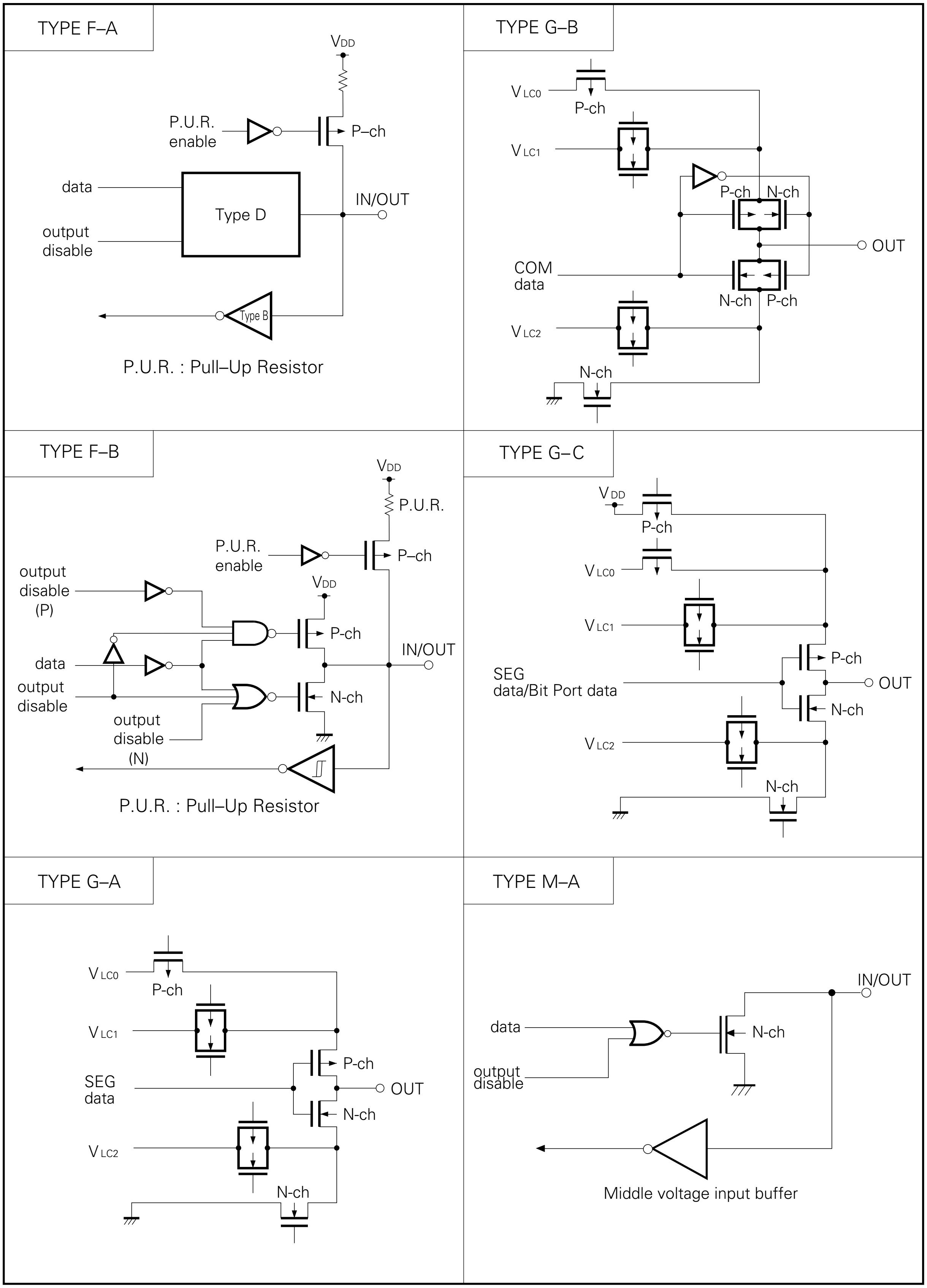
P.U.R. : Pull–Up Resistor

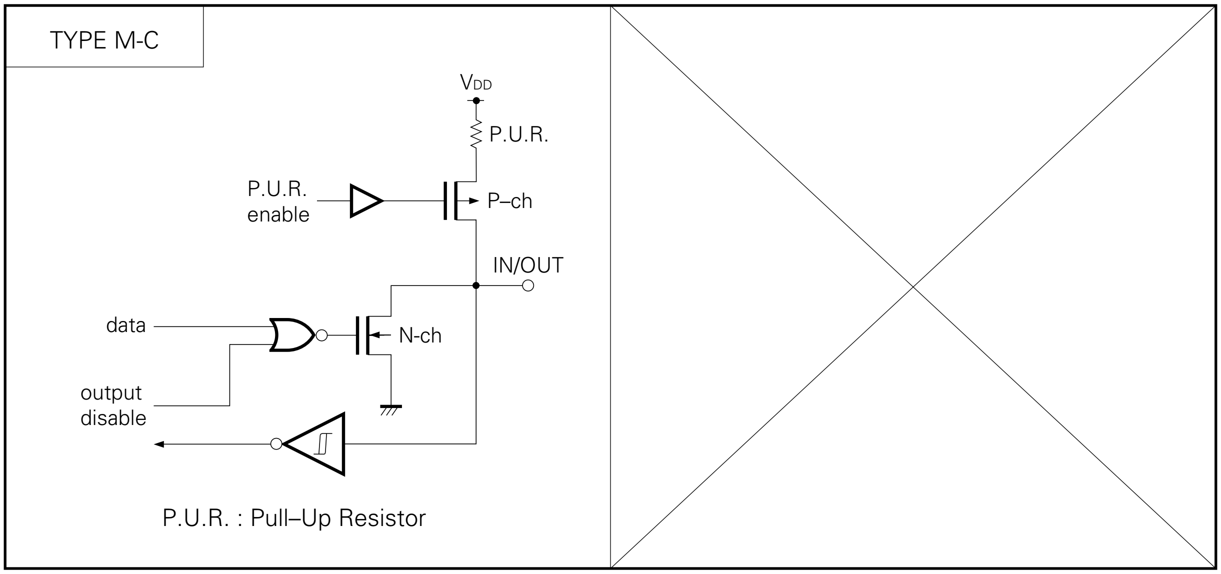
Schmitt trigger input with hysteresis characteristics

TYPE E–E



P.U.R. : Pull–Up Resistor


TYPE F–A
VDD
P.U.R.
enable
P–ch
data
Type D
IN/OUT
output
disable
Type B
P.U.R. : Pull–Up Resistor
TYPE G–B
V LC0
P-ch
V LC1
P-ch
N-ch
OUT
COM
data
N-ch
P-ch
V LC2
N-ch
TYPE F–B
VDD
P.U.R.
P.U.R.
enable
P–ch
output
disable
(P)
VDD
P-ch
IN/OUT
data
output
disable
N-ch
output
disable
(N)
P.U.R. : Pull–Up Resistor
TYPE G–C
V DD
P-ch
V LC0
V LC1
P-ch
SEG
data/Bit Port data
OUT
N-ch
V LC2
N-ch
TYPE G–A
V LC0
P-ch
V LC1
P-ch
SEG
data
OUT
N-ch
V LC2
N-ch
TYPE M–A
IN/OUT
data
N-ch
output
disable
Middle voltage input buffer



1.4 NOTES ON USING P00/INT4 AND $\overline{\text{RESET}}$ PINS

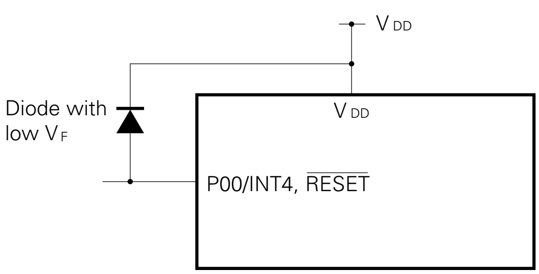
In addition to the functions shown in sections 1.1 and 1.2, the P00/INT4 and $\overline{\text{RESET}}$ pins also have a function to set a test mode (for IC testing) in which the internal operations of the μPD75P308 are tested.

When a voltage higher than V_{DD} is applied to either of these pins, the test mode is set. This means that, even during ordinary operation, the μPD75P308 may be set in the test mode if a noise exceeding V_{DD} is applied.

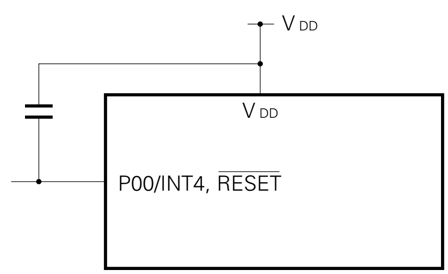
For example, if the wiring length of the P00/INT4 or $\overline{\text{RESET}}$ pin is too long, noise superimposed on the wiring line of the pin may cause the above problem.

Therefore, keep the wiring length of these pins as short as possible to suppress the noise; otherwise, take noise preventive measures as shown below by using external components.

- Connect diode with low V_F between V_{DD} and P00/INT4, $\overline{\text{RESET}}$ pin



- Connect capacitor between V_{DD} and P00/INT4, $\overline{\text{RESET}}$ pin



2. DIFFERENCES BETWEEN μPD75P308 AND μPD75308

The μPD75P308 is a model of the μPD75308 and is equipped with a PROM instead of a mask ROM. Programs can be rewritten to the PROM of the μPD75P308. Table 2-1 shows the differences between the μPD75P308 and μPD75308. You should fully consider these differences when you debug or produce your application system on an experimental basis by using the PROM model, and then proceed to mass-produce the system by using the mask ROM model.

For the details of the CPU and the internal hardware, refer to μPD75308 User's Manual (IEM-5016).

Table 2-1 Differences between μPD75P308 and μPD75308

Item		μPD75P308K	μPD75P308GF	μPD75308GF
Program Memory		• EPROM • 0000H-1F7FH • 8064 x 8 bits	• PROM (one-time model) • 0000H-1F7FH • 8064 x 8 bits	• Mask ROM • 0000H-1F7FH • 8064 x 8 bits
Pull-up Resistor	Ports 4, 5	Not provided		Mask option
Dividing Resistor for LCD Driving Power Supply		Not provided		Mask option
Pin Connection	Pins 50-53	P30/MD0-P33/MD3		P30-P33
	Pin 57	V_{PP}		NC
★ Electrical Specifications		Current dissipations and operating temperature ranges differ between μPD75P308 and μPD75308. For detail, refer to the specification documents of each mode.		
Operating Voltage Range		5V±5%		2.7-6.0V
Package		80-pin ceramic WQFN (LCC w/window)	80-pin plastic QFP (14 x 20 mm)	
★ Others		Noise immunity and noise radiation differ because circuit scale and mask layout are different.		

★ *Note:* The noise immunity and noise radiation differ between the PROM and mask ROM models. To replace the PROM model with the mask ROM model in the course of experimental production to mass production, evaluate your system by using the CS mode (not ES model) of the mask ROM model.

3. WRITING AND VERIFYING PROM (PROGRAM MEMORY)

The program memory of the μPD75P308 is a PROM of 8064 x 8 bits. To write data to or verify the contents of this PROM, the pins listed in the table below are used. Note that no address input pins are provided because the address is updated by the clock input through the X1 pin.

Pin Name	Function
V_{PP}	Applies voltage when program memory is written/verified (normally, at V_{DD} potential)
X1, X2	These pins input clock that updates address when program memory is written/verified. To X2 pin, input signal 180º out of phase in respect to signal to X1 pin.
MD0-MD3	These pins select operation mode when program memory is written/verified.
P40-P43 (Lower 4) P50-P53 (Upper 4)	These pins input/output 8-bit data when program memory is written/verified.
V_{DD}	Power supply voltage application pin. Apply 5V ± 5% to this pin during normal operation and 6V when program memory is written/verified.

Note 1: Always cover the erasure window of the μPD75P308K with a light-opaque film except when the contents of the program memory are erased.

2: The one-time PROM model μPD75P308GF is not equipped with a window and therefore, the contents of the program memory of this model cannot be erased by exposing it to ultraviolet rays.

3.1 OPERATION MODES FOR WRITING/VERIFYING PROGRAM MEMORY

When +6V is applied to the V_{DD} pin of the μPD75P308 with +12.5V applied to the V_{PP} pin, the μPD75P308 is set in the program memory write/verify mode. In this mode, the following operation modes can be set by using the MD0-MD3 pins. At this time, pull down the levels of all the other pins to V_{SS}.

Operating Mode Specification						Operating Mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address 0 clear mode
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	x	H	H	Program inhibit mode

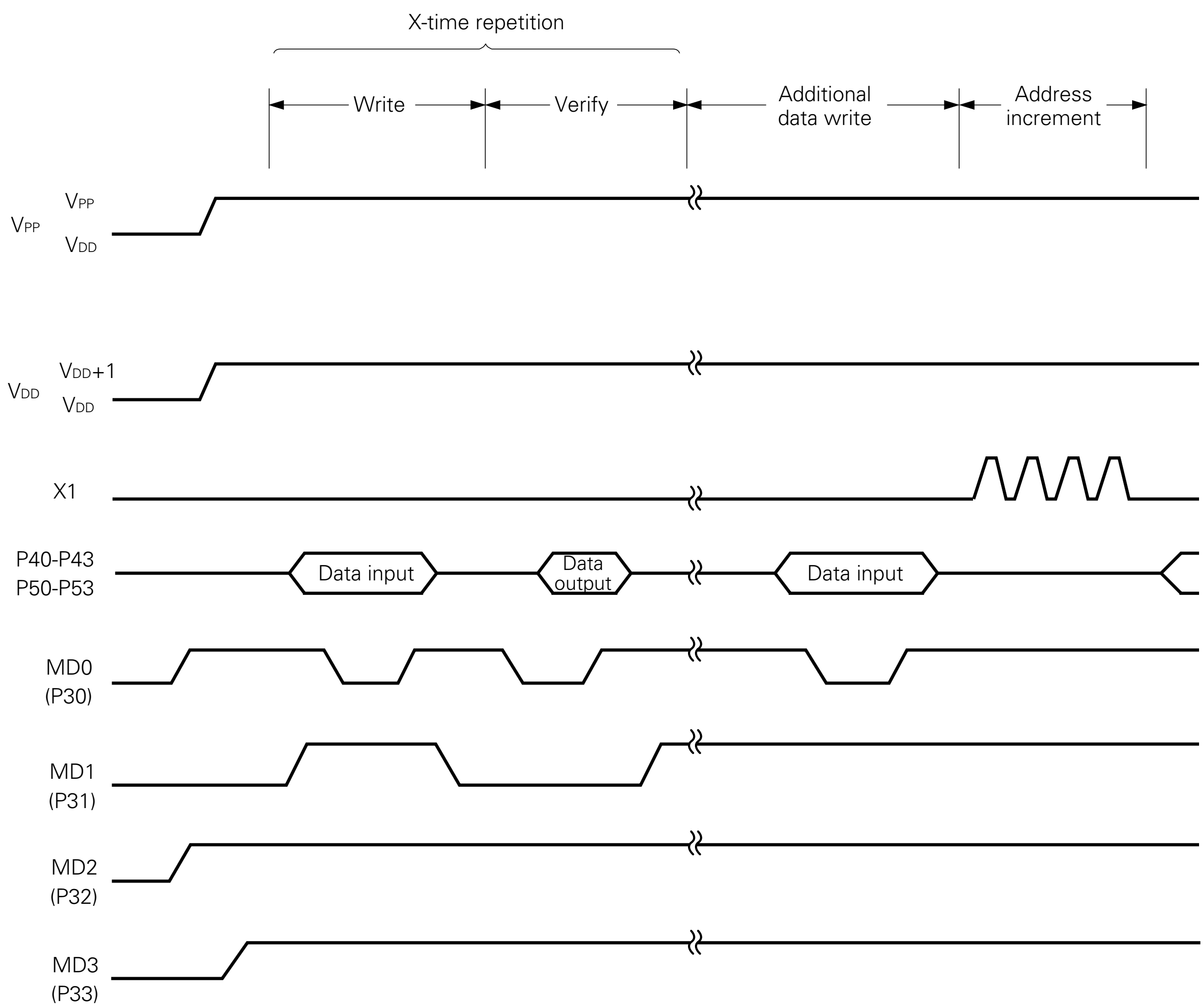
x: L or H

3.2 PROGRAM MEMORY WRITE PROCEDURE

The program memory write procedure is as follows. High-speed program memory write is possible.

(1) Ground the unused pins through pull-down resistors. The X1 pin must be low.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) Wait for 10 microseconds.
(4) Set program memory address 0 clear mode.
(5) Supply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
(6) Set program inhibit mode.
(7) Write data in 1-millisecond write mode.
(8) Set program inhibit mode.
(9) Set verify mode. If data has been written connectly, proceed to step (10). If data has not yet been written, repeat steps (7) to (9).
(10) Write additional data for (the number of times data was written (X) in steps (7) to (9)) times 1 milliseconds.
(11) Set program inhibit mode.
(12) Supply a pulse to the X1 pin four times to update the program memory address by 1.
(13) Repeat steps (7) to (12) to the last address.
(14) Set program memory address 0 clear mode.
(15) Change the voltages of V_{DD} and V_{PP} pins to 5 V.
(16) Turn off the power supply.

Steps (2) to (12) are illustrated below.

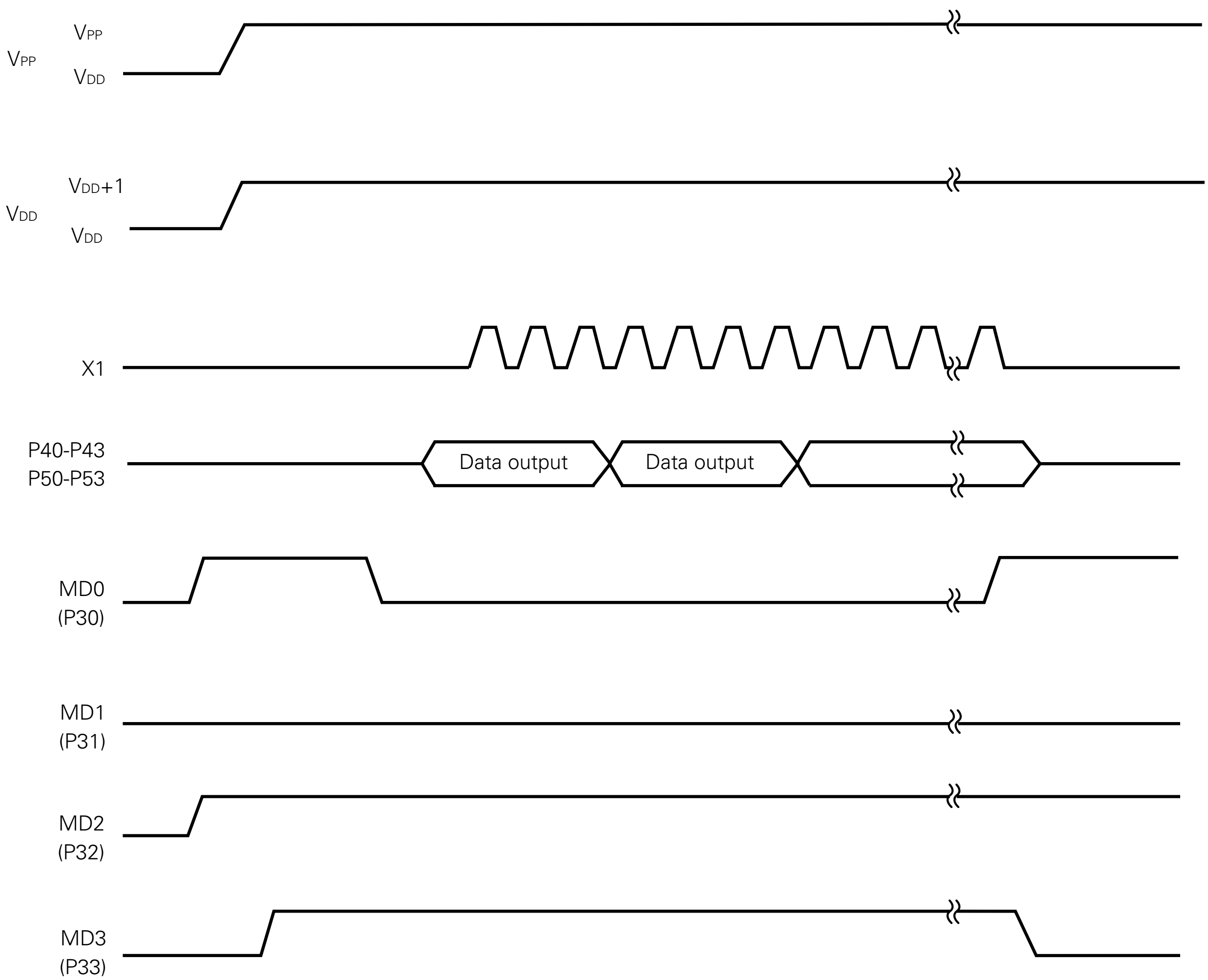


3.3 PROGRAM MEMORY READ PROCEDURE

The contents of the program memory can be read in the following procedure.

(1) Ground the unused pins through pull-down resistors. The X1 pin must be low.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) Wait for 10 microseconds.
(4) Set program memory address 0 clear mode.
(5) Supply 6 V to the V_{DD} pin and 12.5 V to the V_{PP} pin.
(6) Set program inhibit mode.
(7) Set verify mode. Data of each address is sequentially output each time a clock pulse is input to the X1 pin four times.
(8) Set program inhibit mode.
(9) Set program memory address 0 clear mode.
(10) Change the voltages of V_{DD} and V_{PP} pins to 5 V.
(11) Turn off the power supply.

Steps (2) to (9) are illustrated below.



3.4 ERASURE (μPD75P308K ONLY)

The contents of the data programmed to the μPD75P308 can be erased by exposing the window of the program memory to ultraviolet rays.

The wavelength of the ultraviolet rays used to erase the contents is about 250 nm, and the quantity of the ultraviolet rays necessary for complete erasure is 15 $W.s/cm^2$ (= ultraviolet ray intensity x erasure time).

When a commercially available ultraviolet ray lamp (wavelength: 254 nm, intensity: 12 mW/cm^2) is used, about 15 to 20 minutes is required.

Note 1: The contents of the program memory may be erased when the μPD75P308 is exposed for a long time to direct sunlight or the light of fluorescent lamps. To protect the contents from being erased, mask the window of the program memory with the light-opaque film supplied as an accessory with the UV EPROM products.

2: To erase the memory contents, the distance between the ultraviolet ray lamp and the μPD75P308 should be 2.5 cm or less.

Remarks: The time required for erasure changes depending on the degradation of the ultraviolet ray lamp and the surface condition (dirt) of the window of the program memory.

4. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

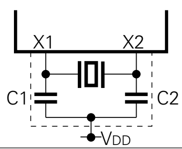
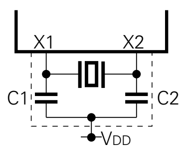
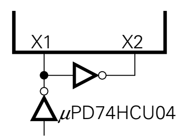
Parameter	Symbol	Conditions		Rating	Unit
Supply Voltage	V_{DD}			-0.3 to +7.0	V
Supply Voltage	V_{PP}			-0.3 to +13.5	V
Input Voltage	V_{I1}	Other than ports 4 or 5		-0.3 to V_{DD}+0.3	V
	V_{I2} *1	Ports 4 and 5	Open-drain	-0.3 to +11	V
Output Voltage	V_O			-0.3 to V_{DD}+0.3	V
High-Level Output Current	I_{OH}	1 Pin		-15	mA
		All pins		-30	mA
Low-Level Output Current	I_{OH} *2	One pin	Peak value	30	mA
			Effective value	15	mA
		Total of ports 0, 2, 3, 5	Peak value	100	mA
			Effective value	60	mA
		Total of ports 4, 6, 7	Peak value	100	mA
			Effective value	60	mA
Operating Temperature	T_{opt}			-10 to +70	°C
Storage Temperature	T_{stg}			-65 to +150	°C

*1: The impedance of the power source (pull-up resistor) must be 50 KΩ minimum when a voltage higher than 10V is applied to ports 4 and 5.

2: Effective value = Peak value x $\sqrt{\text{Duty}}$

MAIN SYSTEM CLOCK OSCILLATOR CIRCUIT CHARACTERISTICS

(T_a = -10 to +70°C, V_{DD} = 5 to ±5 V)

Oscillator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic[*3]		Oscillation frequency (f_{XX})[*1]		1.0		5.0[*4]	MHz
		Oscillation stabilization time[*2]	After V_{DD} came to MIN. of oscillation voltage range			4	ms
Crystal		Oscilaltion frequency (f_{XX})[*1]		1.0	4.19	5.0[*4]	MHz
		Oscillation stabilization time[*2]				10	ms
External Clock		X1 input frequency (f_X)[*1]		1.0		5.0[*4]	MHz
		X1 input high-, low-level widths (t_{XH}, t_{XL})		100		500	ns

* 1: The oscillation frequency and X1 input frequency are indicated only to express the characteristics of the oscillator circuit.
For instruction execution time, refer to AC Characteristics.

2: Time required for oscillation to stabilize after V_{DD} reaches the minimum value of the oscillation voltage range or the STOP mode has been released.

3: The oscillators below are recommended.

★ 4: When the oscillation frequency is 4.19 MHz < fx ≤ 5.0 MHz, do not select PCC = 0011 as the instruction execution time: otherwise, one machine cycle is set to less than 0.95 μs, falling short of the rated minimum value of 0.95 μs.

★ **Caution: When using the oscillation circuit of the main system clock, wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacity:**

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over the other signal lines. Do not route the wiring in the vicinity of lines through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillator circuit at the same potential as V_{DD}. Do not connect the power source pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

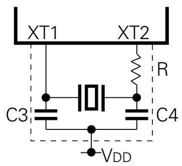
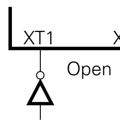
RECOMMENDED OSCILLATION CIRCUIT CONSTANTS

MAIN SYSTEM CLOCK: CERAMIC OSCILLATOR (T_a = -10 to +70°C)

Manufac-turer	Product Name	External Capacitance [pF]		Oscillation Voltage Range [V]	
		C1	C2	MIN.	MAX.
Murata Mfg. Co., Ltd.	CSA 2.00MG	30	30	4.75	5.25
	CSA 4.19MG	30	30	4.75	5.25
	CSA 4.19MGU	30	30	4.75	5.25
	CST 4.19MG	30 pF (internal)	30 pF (internal)	4.75	5.25

SUBSYSTEM CLOCK OSCILLATOR CIRCUIT CHARACTERISTICS

(T_a = -10 to +70°C, V_{DD} = 5 V ±5%)

Oscillator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Crystal		Oscillation frequency (f_{XT})		32	32.768	35	kHz
		Oscillation stabilization time*			1.0	2	s
External Clock		XT1 input frequency (f_{XT})		32		100	kHz
		XT1 input high-, low-level widths (t_{XTH}, t_{XTL})		5		15	μs

*: Time required for oscillation to stabilize after V_{DD} reaches the minimum value of the oscillation voltage range.

Caution: When using the oscillation circuit of the subsystem clock, wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacity: ★

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over the other signal lines. Do not route the wiring in the vicinity of lines through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillator circuit at the same potential as V_{DD}. Do not connect the power source pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

The amplification factor of the subsystem clock oscillation circuit is designed to be low to reduce the current dissipation and therefore, the subsystem clock oscillation circuit is influenced by noise more easily than the main system clock oscillation circuit. When using the subsystem clock, therefore, exercise utmost care in wiring the circuit.

CAPACITANCE (T_a = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{IN}	f = 1 MHz			15	pF
Output Capacitance	C_{OUT}	Pins other than thosemeasured are at 0 V			15	pF
Input/Output Capacitance	C_{IO}				15	pF

DC CHARACTERISTICS (T_a = -10 to +70°C, V_{DD} = 5V ±5%)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V_{IH1}	Ports 2, 3		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7, $\overline{RESET}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4, 5	Open-drain	0.7 V_{DD}		10	V
	V_{IH4}	X1, X2, XT1		V_{DD}-0.5		V_{DD}	V
Low-Level Input Voltage	V_{IL1}	Ports 2, 3, 4, 5		0		0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7, $\overline{RESET}$		0		0.2 V_{DD}	V
	V_{IL3}	X1, X2, XT1		0		0.4	V
High-Level Output Voltage	V_{OH1}	Ports 0, 2, 3, 6, 7 BIAS	I_{OH} = -1mA	V_{DD}-1.0			V
	V_{OH2}	BP0-7	I_{OH} = -100μA*1	V_{DD}-2.0			V
Low-Level Output Voltage	V_{OL1}	Ports 0, 2, 3, 6, 7	Ports 3, 4, 5 I_{OL} = 15mA		0.4	2.0	V
			I_{OL} = 1.6mA			0.4	V
	V_{OL2}	SB0, 1 Open-drain	Pull-up R ≥ 1kΩ			0.2V_{DD}	V
	V_{OL3}	BP0-7	I_{OL} = 100μA*1			1.0	V
High-Level Input Leakage Current	I_{LIH1}	V_{IN} = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1, X2, XT1			20	μA
	I_{LIH3}	V_{IN} = 10V	Ports 4, 5			20	μA
Low-Level Input Leakage Current	I_{LIL1}	V_{IN} = 0V	Other than below			-3	μA
	I_{LIL2}		X1, X2, XT1			-20	μA
High-Level Output Leakage Current	I_{LOH1}	V_{OUT} = V_{DD}	Other than below			3	μA
	I_{LOH2}	V_{OUT} = 10V	Ports 4.5			20	μA
Low-Level Output Leakage Current	I_{LOL}	V_{OUT} = 0V				-3	μA
Internal Pull-Up Resistor	R_{LI}	Ports 0, 1, 2, 3, 6, 7 (except P00) V_{IN} = 0V		15	40	80	KΩ
LCD Drive Voltage	V_{LCD}			2.5		V_{DD}	V
LCD Output Voltage Deviation *2 (Common)	V_{ODC}	I_0 = ±5 μA	V_{LCD0} = V_{LCD} V_{LCD1} = V_{LCD} x $\frac{2}{3}$ V_{LCD2} = V_{LCD} x $\frac{1}{3}$ 2.7 V ≤ V_{LCD} ≤ V_{DD}	0		±0.2V	V
LCD Output Voltage Deviation *2 (Segment)	V_{ODS}	I_0 = ±1 μA		0		±0.2V	V
Supply Current *3	I_{DD1}	4.19MHz crystal oscillator C1 = C2 = 22pF *4	*6		5	15	mA
	I_{DD2}		HALT mode		500	1500	μA
	I_{DD3}	32 kHz crystal oscillator *5			350	1000	μA
			HALT mode		35	100	μA
	I_{DD4}	XT1 = 0V STOP mode			0.5	20	μA

* 1: When using two of BP0-BP3 and two of BP4-BP7 for output at the same time.
2: "Voltage deviation" means the difference between the ideal segment or common output value (V_{LCDn}: = 0, 1, 2) and output voltage.
3: Currents for the built-in pull-up resistor are not included.
4: Including when the subsystem clock is operated.
5: When operated with the subsystem clock by setting the system clock control register (SCC) to 1001 to stop the main system clock operation.
6: When operand in the high-speed mode with the processor clock control register (PCC) set to 0011.

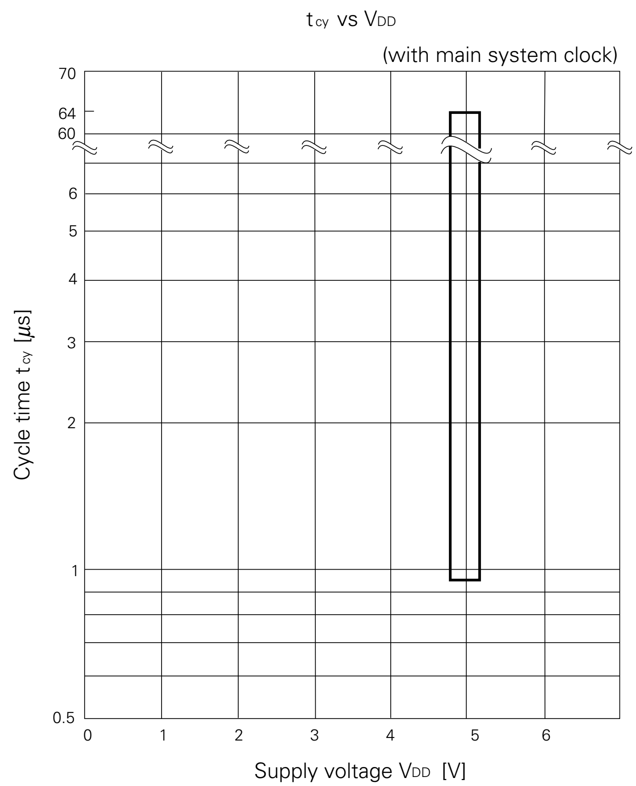
AC CHARACTERISTICS (T_a = -10 to + 70°C, V_{DD} = 5V ±5%)

Operation Other Than Serial Transfer

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU Clock Cycle Time*1 (Minimum Instruction Execution Time = 1 Machine Cycle)	t_{CY}	w/main system clock	0.95		64	μs
		w/subsystem clock	114	122	125	μs
TI0 Input Frequency	f_{TI}		0		1	MHz
TI0 Input High-, Low-Level Widths	t_{TIH}, t_{TIL}		0.48			μs
Interrupt Input High-, Low-Level Widths	t_{INTH}, t_{INTL}	INT0	*2			μs
		KR0-7, INT1, 2, 4	10			μs
$\overline{\text{RESET}}$ Low-Level Width	t_{RSL}		10			μs

* 1: The CPU clock (Φ) cycle time is determined by the oscillation frequency of the connected oscillator, system clock control register (SCC), and processor clock control register (PCC).
The figure on the right is cycle time t_{CY} vs. supply voltage V_{DD} characteristics at the main system clock.

2: $2t_{CY}$ or $128/f_{XX}$ depending on the setting of the interrupt mode register (IM0).



SERIAL TRANSFER OPERATION

TWO-LINE AND THREE-LINE SERIAL I/O MODES ($\overline{SCK}$: internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY1}		Output	1600			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KH1}, t_{KL1}		Output	$t_{KCY1}/2-50$			ns
SI Set-Up Time (vs. $\overline{SCK}$↑)	t_{SIK1}			150			ns
SI Hold Time (vs. $\overline{SCK}$↑)	t_{KSI1}			400			ns
$\overline{SCK}$ ↓ → SO Output Delay Time	t_{KSO1}	$R_L = 1k\Omega$, $C_L = 100pF$*				250	ns

★ *: R_L and C_L are load resistance and load capacitance of the SO output line.

TWO-LINE AND THREE-LINE SERIAL I/O MODES ($\overline{SCK}$: external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY2}		Input	800			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KH2}, t_{KL2}		Input	400			ns
SI Set-Up Time (vs. $\overline{SCK}$↑)	t_{SIK2}			100			ns
SI Hold Time (vs. $\overline{SCK}$↑)	t_{KSI2}			400			ns
$\overline{SCK}$ ↓ → SO Output Delay Time	t_{KSO2}	$R_L = 1k\Omega$, $C_L = 100pF$*				300	ns

★ *: R_L and C_L are load resistance and load capacitance of the SO output line.

SBI MODE ($\overline{SCK}$: internal clock output (master))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY3}		1600			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL3} t_{KH3}		$t_{KCY}/2$ -50			ns
SB0, 1 Set-Up Time (vs. $\overline{SCK}$↑)	t_{SIK3}		150			ns
SB0, 1 Hold Time (vs. $\overline{SCK}$↑)	t_{KSI3}		$t_{KCY}/2$			ns
$\overline{SCK}$↓ → SB0, 1 Output Delay Time	t_{KSO3}	R_L = 1kΩ, C_L = 100pF*	0		250	ns
$\overline{SCK}$↑ → SB0, 1↓	t_{KSB}		t_{KCY}			ns
SB0, 1↓ → $\overline{SCK}$↓	t_{SBK}		t_{KCY}			ns
SB0, 1 Low-Level Width	t_{SBL}		t_{KCY}			ns
SB0, 1 High-Level Width	t_{SBH}		t_{KCY}			ns

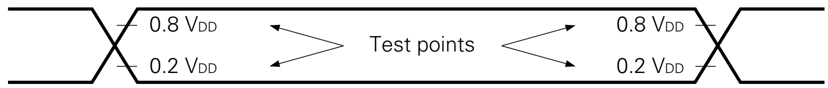
*: R_L and C_L are load resistance and load capacitance of the SO output line. ★

SBI MODE ($\overline{SCK}$: external clock output (master))

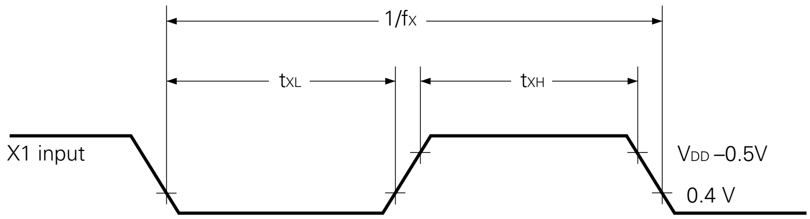
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY4}		1600			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL4} t_{KH4}		400			ns
SB0, 1 Set-Up Time (vs. $\overline{SCK}$↑)	t_{SIK4}		100			ns
SB0, 1 Hold Time (vs. $\overline{SCK}$↑)	t_{KSI4}		$t_{KCY}/2$			ns
$\overline{SCK}$↓ → SB0, 1 Output Delay Time	t_{KSO4}	R_L = 1kΩ, C_L = 100pF*	0		300	ns
$\overline{SCK}$↑ → SB0, 1↓	t_{KSB}		t_{KCY}			ns
SB0, 1↓ → $\overline{SCK}$↓	t_{SBK}		t_{KCY}			ns
SB0, 1 Low-Level Width	t_{SBL}		t_{KCY}			ns
SB0, 1 High-Level Width	t_{SBH}		t_{KCY}			ns

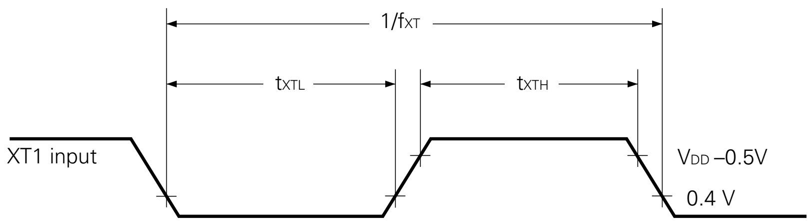
*: R_L and C_L are load resistance and load capacitance of the SO output line. ★

AC TIMING TEST POINT (excluding X1 and XT1 inputs)

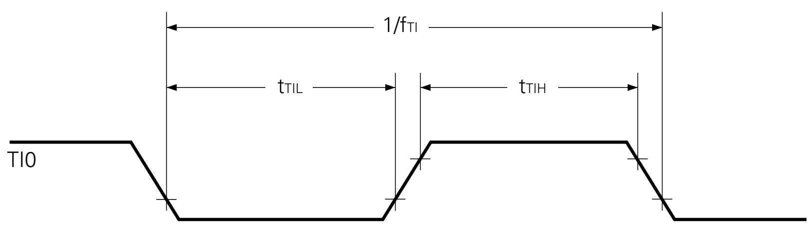


CLOCK TIMING



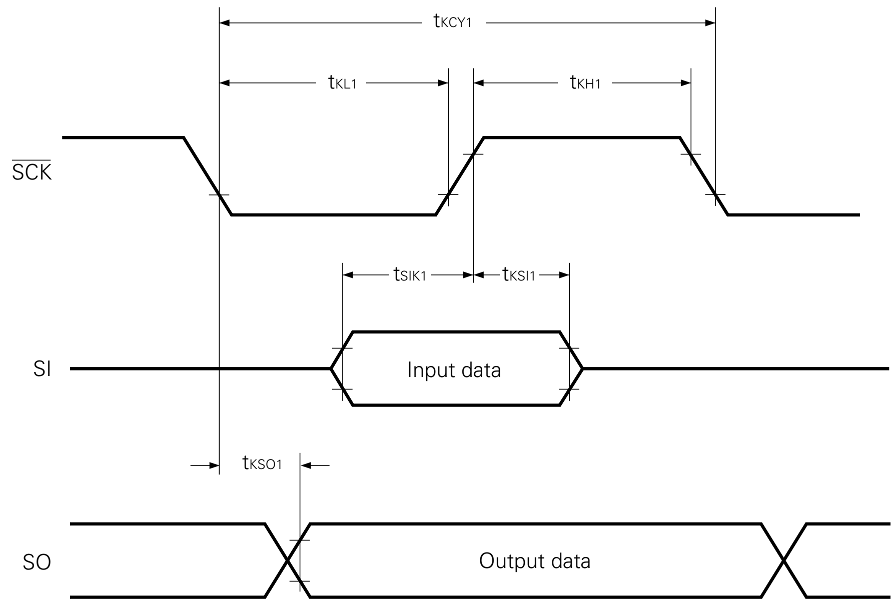


TI0 TIMING

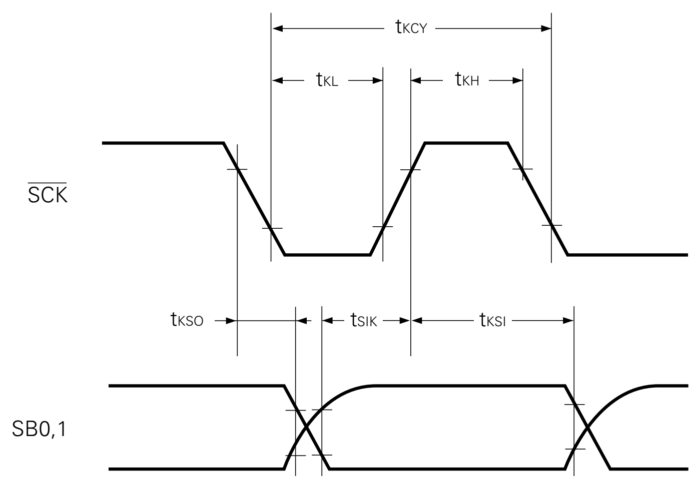


SERIAL TRANSFER TIMING

THREE-LINE SERIAL I/O MODE:

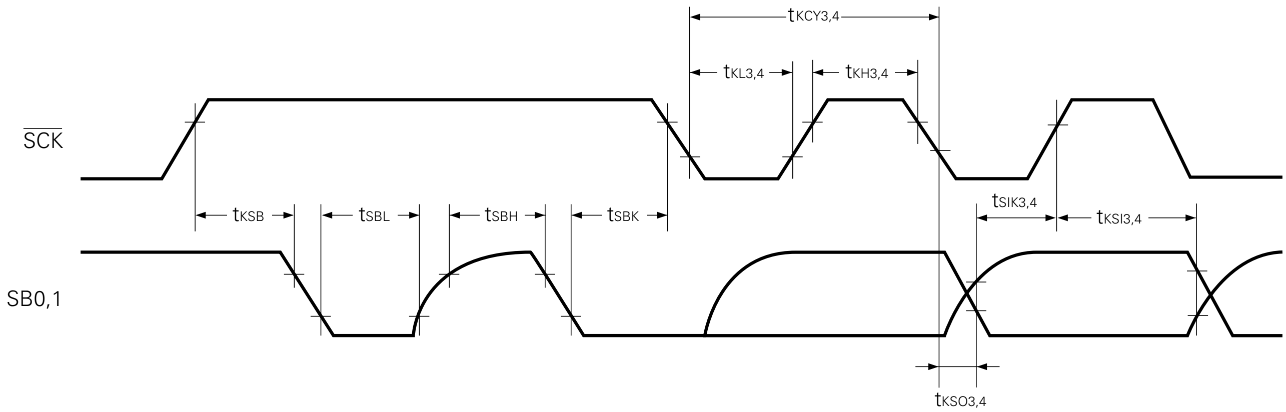


TWO-LINE SERIAL I/O MODE:

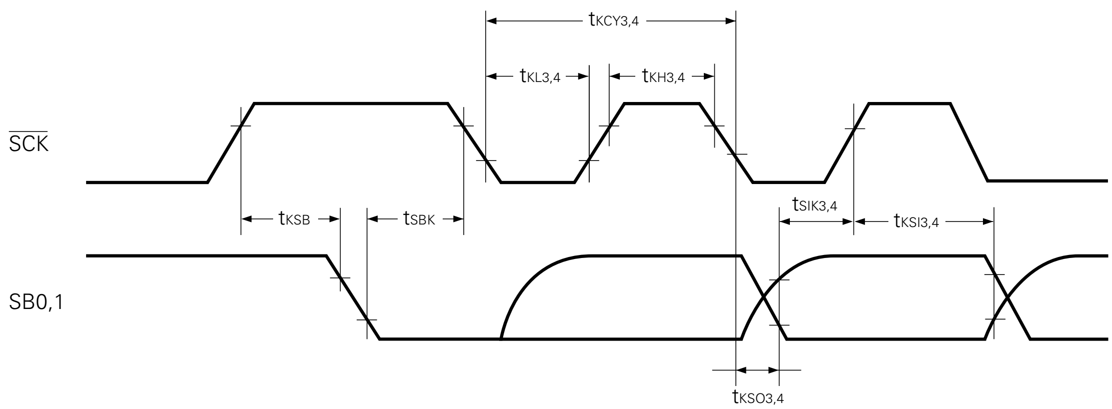


SERIAL TRANSFER TIMING

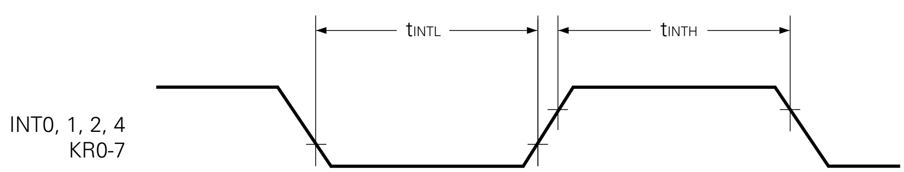
BUS RELEASE SIGNAL TRANSFER



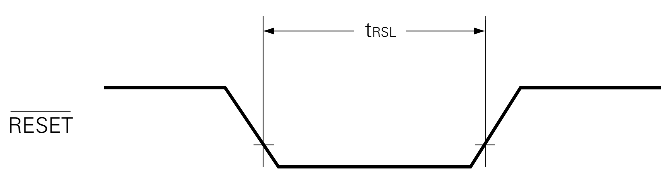
COMMAND SIGNAL TRANSFER



INTERRUPT INPUT TIMING



RESET INPUT TIMING



LOW-VOLTAGE DATA RETENTION CHARACTERISTICS OF DATA MEMORY IN STOP MODE

(T_a = -10 to +70°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data Retention Supply Voltage	V_{DDDR}		2.0		6.0	V
Data Retention Supply Current*1	I_{DDDR}	V_{DDDR} = 2.0V		0.1	10	μA
Release Signal Set Time	t_{SREL}		0			μs
Oscillation Stabilization Wait Time*2	t_{WAIT}	Released by $\overline{RESET}$		$2^{17}/f_X$		ms
		Released by interrupt		*3		ms

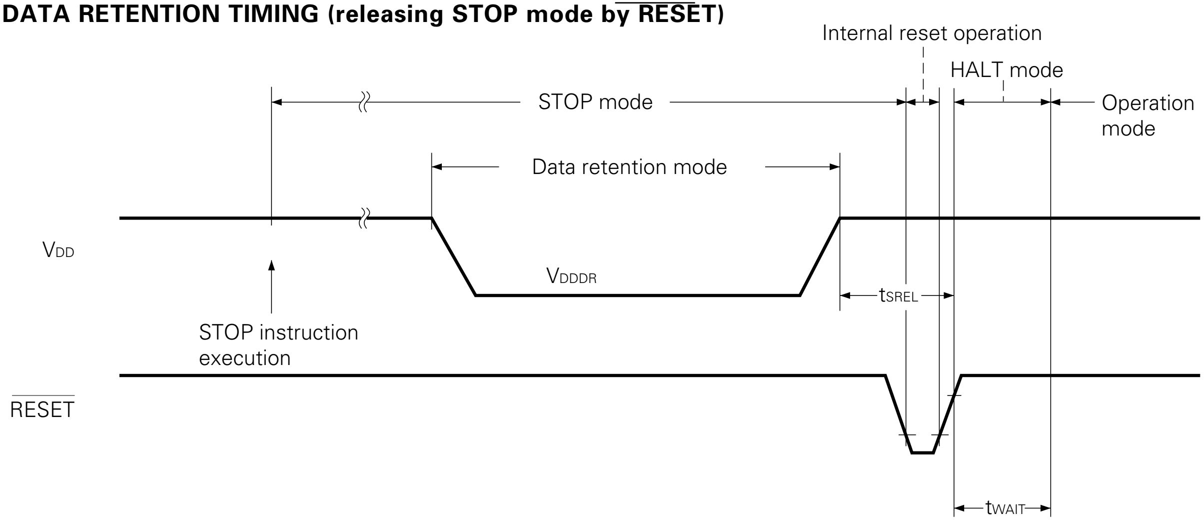
*1: Does not include current folowing through internal pull-up resistor

2: The oscillation stabilization wait time is the time during which the CPU is stopped to prevent unstable operation when oscillation is started.

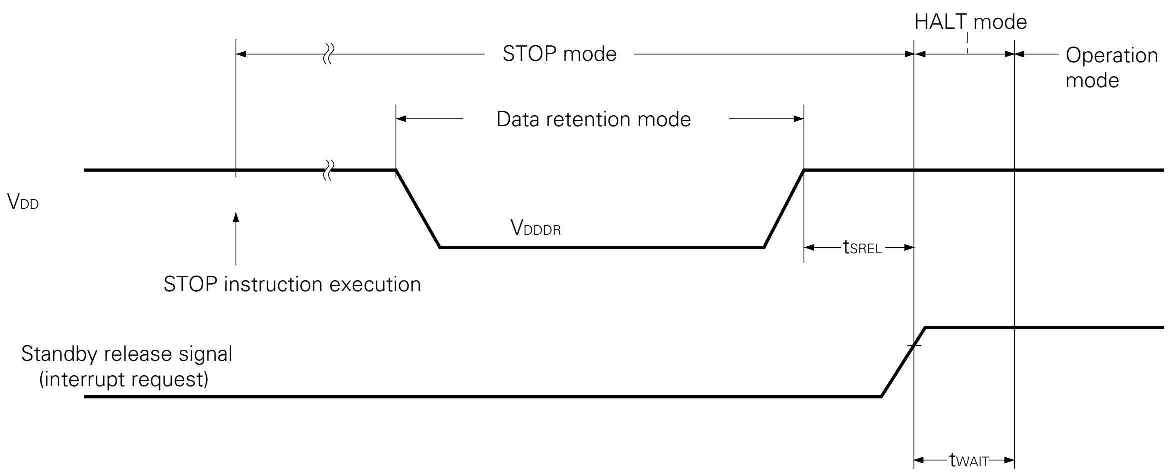
3: Depends on the setting of the basic interval timer mode register (BTM) as follows:

BTM3	BTM2	BTM1	BTM0	WAIT time ( ): fx = 4.19 MHz
—	0	0	—	$2^{20}/f_X$ (approx. 250 ms)
—	0	1	—	$2^{17}/f_X$ (approx. 31.3 ms)
—	1	0	—	$2^{15}/f_X$ (approx. 7.82 ms)
—	1	1	—	$2^{13}/f_X$ (approx. 1.95 ms)

DATA RETENTION TIMING (releasing STOP mode by $\overline{RESET}$)



DATA RETENTION TIMING (standby release signal: releasing STOP mode by interrupt)



DC PROGRAMMING CHARACTERISTICS (T_a = 25 ±5°C, V_{DD} = 6.0±0.25V, V_{PP} = 12.5±0.3V, V_{SS} = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V_{IH1}	Other than X1 or X2	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	X1 and X2	V_{DD} −0.5		V_{DD}	V
Low-Level Input Voltage	V_{IL1}	Other than X1 or X2	0		0.3 V_{DD}	V
	V_{IL2}	X1 and X2	0		0.4	V
Input Leakage Current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			10	μA
High-Level Output Voltage	V_{OH}	I_{OH} = −1 mA	V_{DD} −1.0			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} Supply Current	I_{DD}				30	mA
V_{PP} Supply Current	I_{PP}	MD0 = V_{IL}, MD1 = V_{IH}			30	mA

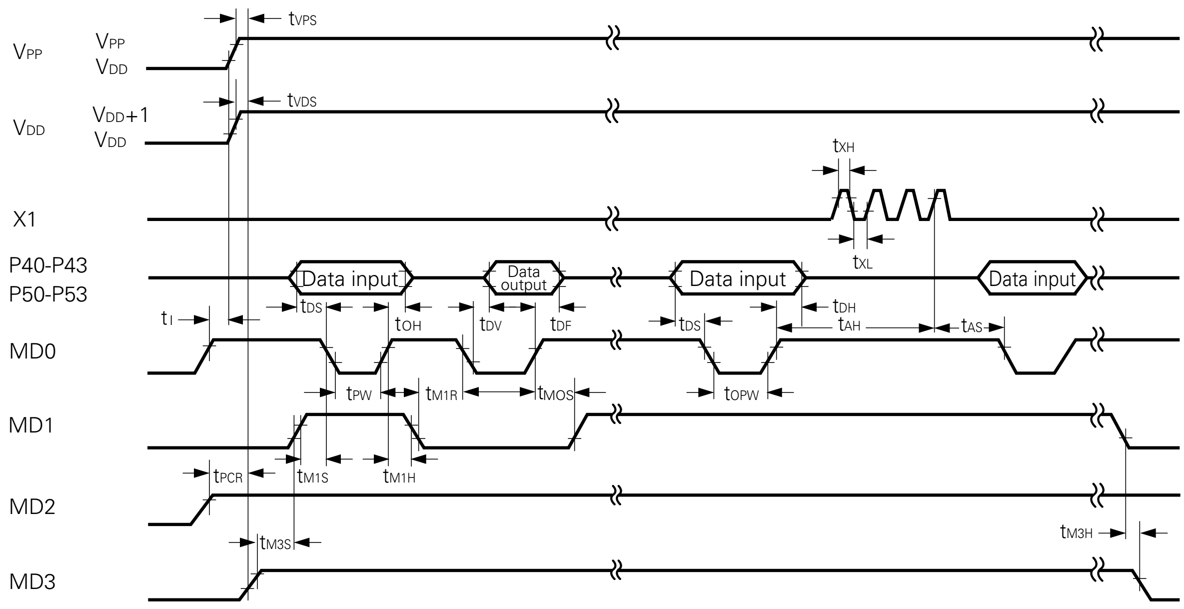
Notes 1: V_{PP} must not exceed +13.5 V, including the overshoot.
2: Apply V_{DD} before V_{PP} and disconnect it after V_{PP}.

AC PROGRAMMING CHARACTERISTICS (T_a = 25±5°C, V_{DD} = 6.0±0.25V, V_{PP} = 12.5±0.3V, V_{SS} = 0V)

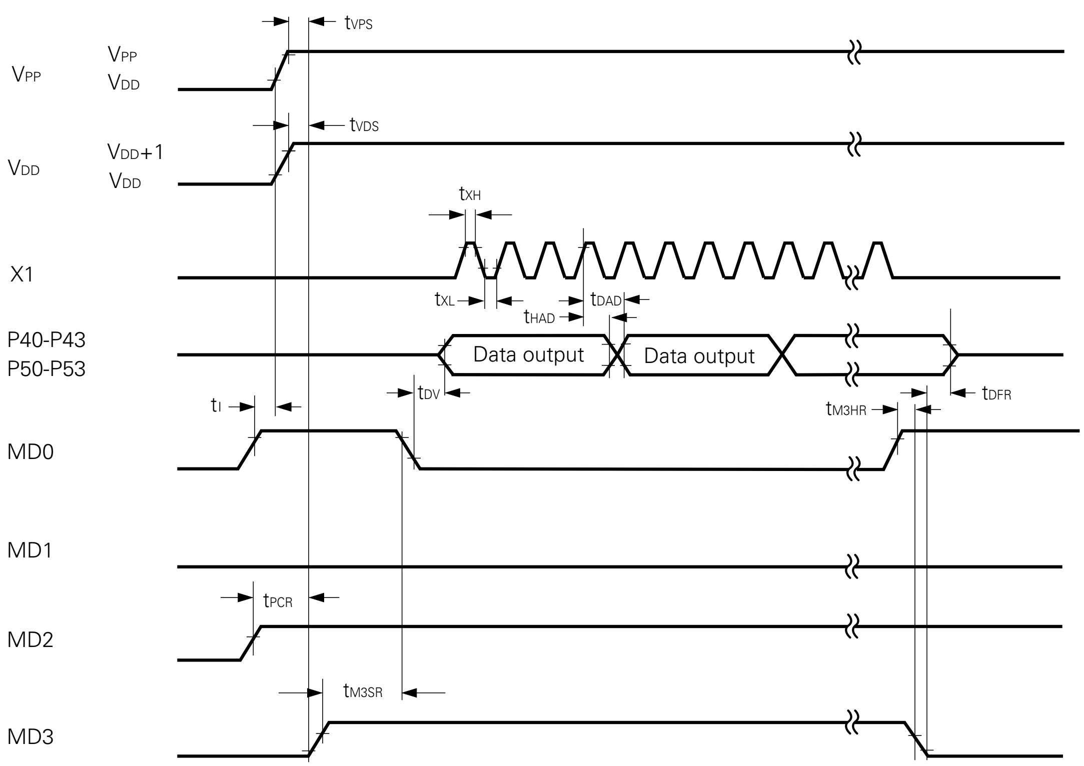
Parameter	Symbol	*1	Conditions	MIN.	TYP.	MAX.	Unit
Address Set-Up Time*2 (vs.MD0↓)	t_{AS}	t_{AS}		2			μs
MD1 Set-Up Time (vs. MD0↓)	t_{M1S}	t_{OES}		2			μs
Data Set-Up Time (vs. MD0↓)	t_{DS}	t_{DS}		2			μs
Address Hold Time*2 (vs.MD0↑)	t_{AH}	t_{AH}		2			μs
Data Hold Time (vs. MD0↑)	t_{DH}	t_{DH}		2			μs
MD0 ↑→ Data Output Float Delay Time	t_{DF}	t_{DF}		0		130	ns
V_{PP} Set-Up Time (vs. MD3↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} Set-Up Time (vs. MD3↑)	t_{VDS}	t_{VCS}		2			μs
Initial Program Pulse Width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional Program Pulse Width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 Set-Up Time (vs. MD1↑)	t_{MOS}	t_{CES}		2			μs
MD0 ↓→ Data Output Delay Time	t_{DV}	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 Hold Time (vs. MD0↑)	t_{M1H}	t_{OEH}	t_{M1H} + t_{M1R} ≥ 50 μs	2			μs
MD1 Recovery Time (vs. MD0↓)	t_{M1R}	t_{OR}		2			μs
Program Counter Reset Time	t_{PCR}	–		10			μs
X1 Input High-/Low- Level Width	t_{XH},t_{XL}	–		0.125			μs
X1 Input Frequency	f_X	–				4.19	MHz
Initial Mode Set Time	t_I	–		2			μs
MD3 Set-Up Time (vs. MD1↑)	t_{M3S}	–		2			μs
MD3 Hold Time (vs. MD1↓)	t_{M3H}	–		2			μs
MD3 Set-Up Time (vs. MD0↓)	t_{M3SR}	–	When data is read from program memory	2			μs
★ Address*2 → Data Output Delay Time	t_{DAD}	t_{ACC}	When data is read from program memory			2	μs
Address*2 → Data Output Hold Time	t_{HAD}	t_{OH}	When data is read from program memory	0		130	ns
MD3 Hold Time (vs. MD0↑)	t_{M3HR}	–	When data is read from program memory	2			μs
★ MD3 ↓→ Data Output Float Delay Time	t_{DFR}	–	When data is read from program memory			2	μs

***1**: These symbols are the corresponding μPD27C256 symbols.
2: The internal address signal is incremented by 1 at the fourth rising edge of X1 input. The internal address is not connected to any pin.

PROGRAM MEMORY WRITE TIMING

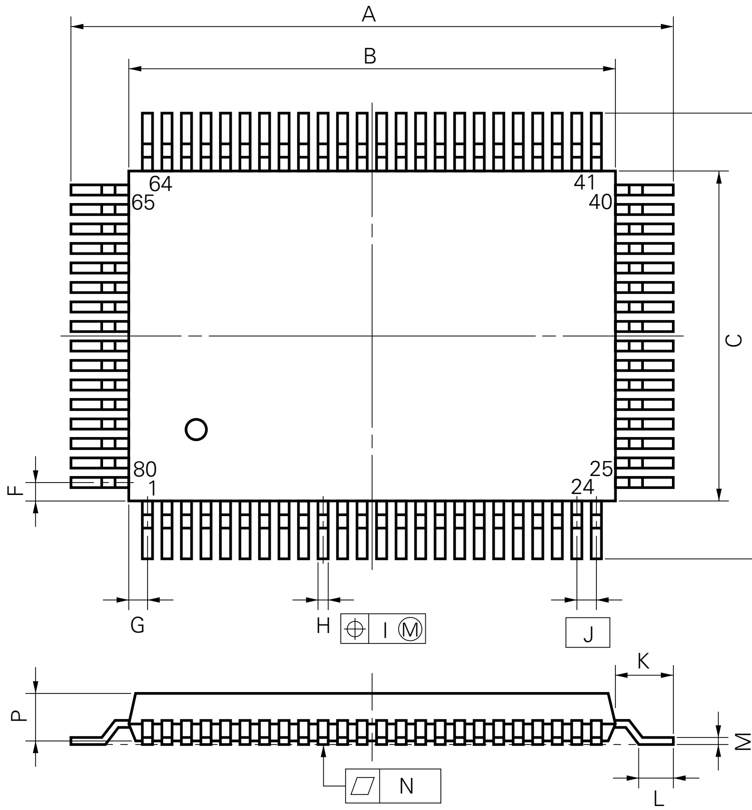


PROGRAM MEMORY READ TIMING

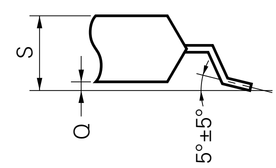


5. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×20)



detail of lead end



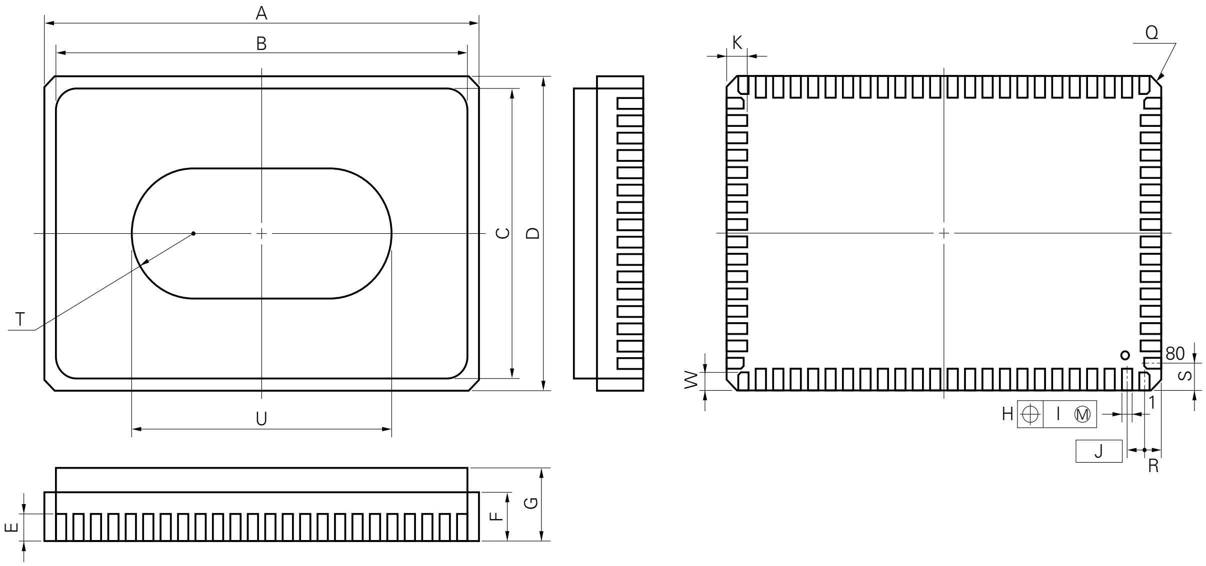
P80GF-80-3B9-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

80 PIN CERAMIC WQFN



X80KW-80A-1

NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	20.0±0.4	$0.787^{+0.017}_{-0.016}$
B	19.0	0.748
C	13.2	0.520
D	14.2±0.4	0.559±0.016
E	1.64	0.065
F	2.14	0.084
G	4.064 MAX.	0.160 MAX.
H	0.51±0.10	0.020±0.004
I	0.08	0.003
J	0.8 (T.P.)	0.031 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
Q	C 0.5	C 0.020
R	0.8	0.031
S	1.1	0.043
T	R 3.0	R 0.118
U	12.0	0.472
W	0.75±0.2	$0.030^{+0.008}_{-0.009}$

★ 6. RECOMMENDED SOLDERING CONDITIONS

It is recommended that μPD75P308 be soldered under the following conditions.

For details on the recommended soldering conditions, refer to Information Document "Semiconductor Devices Mounting Manual" (IEI-616).

The soldering methods and conditions are not listed here, consult NEC.

Table 6-1 Soldering Conditions

μPD75P308GF-3B9: 80-pin plastic QFP (14 x 20 mm)

Soldering Method	Soldering Conditions	Symbol for Recommended Condition
Wave Soldering	Soldering bath temperature: 260°C max., time: 10 seconds max., number of times: 1, pre-heating temperature: 120°C max. (package surface temperature), maximum number of days: 2 days*, (beyond this period, 16 hours of pre-baking is required at 125°C).	WS60-162-1
Infrared Reflow	Package peak temperature: 230°C, time: 30 seconds max. (210°C min.), number of times: 1, maximum number of days: 2 days* (beyond this period, 16 hours of pre-baking is required at 125°C)	IR30-162-1
VPS	Package peak temperature: 215°C, time: 40 seconds max. (200°C min.), number of times: 1, maximum number of days: 2 days* (beyond this period, 16 hours of pre-baking is required at 125°C)	VP15-162-1
Pin Partial Heating	Pin temperature: 300°C max., time: 3 seconds max. (per side)	—

*: Number of days after unpacking the dry pack. Storage conditions are 25°C and 65%RH max.

Caution: Do not use two or more soldering methods in combination (except the pin partial heating method).

Notice

A model that can be soldered under the more stringent conditions (infrared reflow peak temperature: 235°C, number of times: 2, and an extended number of days) is also available. For details, consult NEC.

APPENDIX A. DEVELOPMENT TOOLS

The following development support tools are readily available to support development of systems using μPD75P308:

PROM writing tools

Hardare	IE-75000-R[*1] IE-75001-R	In-circuit emulator for 75K series
	IE-75000-R-EM[*2]	Emulation board for IE-75000-R and IE-75001-R
	EP-75308GF-R EV-9200G-80	Emulation prove for μPD75P308GF, provided with 80-pin conversion socket, EV-9200G-80.
	PG-1500	PROM programmer
	PA-75P308GF	PROM programmer adapter solely used for μPD75P308GF. It is connected to PG-1500.
	PA-75P308K	PROM programmer adapter solely used for μPD75P308K. It is connected to PG-1500.
Software	IE Control Program	Host machine • PC-9800 series (MS-DOS™ Ver.3.30 to Ver.5.00A[*3]) • IBM PC/AT™ (PC DOS™ Ver.3.1)
	PG-1500 Controller	
	RA75X Relocatable Assembler	

*1: Maintenance product
2: Not provided with IE-75001-R
3: Ver.5.00/5.00A has a task swap function, but this function cannot be used with this software.

Remarks: For development tools from other companies, refer to 75X Series Selection Guide (IF-151).

★ APPENDIX B. RELATED DOCUMENTS

GENERAL NOTES ON CMOS DEVICES

① STATIC ELECTRICITY (ALL MOS DEVICES)

Exercise care so that MOS devices are not adversely influenced by static electricity while being handled.

The insulation of the gates of the MOS device may be destroyed by a strong static charge. Therefore, when transporting or storing the MOS device, use a conductive tray, magazine case, or conductive buffer materials, or the metal case NEC uses for packaging and shipment, and use grounding when assembling the MOS device system. Do not leave the MOS device on a plastic plate and do not touch the pins of the device.

Handle boards on which MOS devices are mounted similarly .

② PROCESSING OF UNUSED PINS (CMOS DEVICES ONLY)

Fix the input level of CMOS devices.

Unlike bipolar or NMOS devices, if a CMOS device is operated with nothing connected to its input pin, intermediate level input may be generated due to noise, and an inrush current may flow through the device, causing the device to malfunction. Therefore, fix the input level of the device by using a pull-down or pull-up resistor. If there is a possibility that an unused pin serves as an output pin (whose timing is not specified), each pin should be connected to V_{DD} or GND through a resistor.

Refer to “Processing of Unused Pins” in the documents of each devices.

③ STATUS BEFORE INITIALIZATION (ALL MOS DEVICES)

The initial status of MOS devices is undefined upon power application.

Since the characteristics of an MOS device are determined by the quantity of injection at the molecular level, the initial status of the device is not controlled during the production process. The output status of pins, I/O setting, and register contents upon power application are not guaranteed. However, the items defined for reset operation and mode setting are subject to guarantee after the respective operations have been executed.

When using a device with a reset function, be sure to reset the device after power application.

[MEMO]

The devices listed in this document are not suitable for uses in aerospace equipment, submarine cables, nuclear reactor control systems and life support systems. If customers intend to use NEC devices for above applications or they intend to use "Standard" quality grade NEC devices for the applications not intended by NEC, please contact our sales people in advance.
Application examples recommended by NEC Corporation

Standard: Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tools, Industrial robots, Audio and Visual equipment, Other consumer products,etc.

Special: Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime system, etc.

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