1998.11.30 Ver.B

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change

MITSUBISHI LSIs
M5M54R04AJ-10,-12,-15

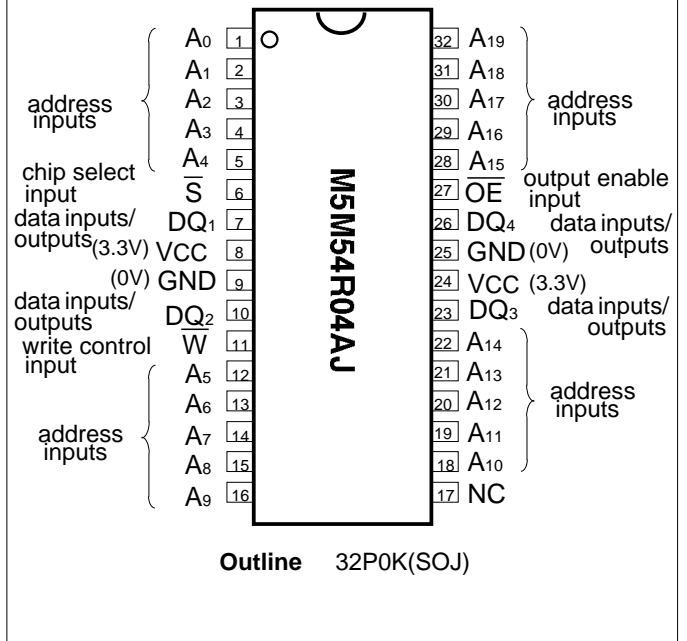**4194304-BIT (1048576-WORD BY 4-BIT) CMOS STATIC RAM**

DESCRIPTION

The M5M54R04AJ is a family of 1048576-word by 4-bit static RAMs, fabricated with the high performance CMOS silicon gate process and designed for high speed application.

These devices operate on a single 3.3V supply, and are directly TTL compatible. They include a power down feature as well.

FEATURES

- Fast access time   M5M54R04AJ-10 ... 10ns(max)
  M5M54R04AJ-12 ... 12ns(max)
  M5M54R04AJ-15 ... 15ns(max)

- Single +3.3V power supply
- Fully static operation : No clocks, No refresh
- Common data I/O
- Easy memory expansion by $\overline{S}$
- Three-state outputs : OR-tie capability
- OE prevents data contention in the I/O bus
- Directly TTL compatible : All inputs and outputs

APPLICATION

High-speed memory units
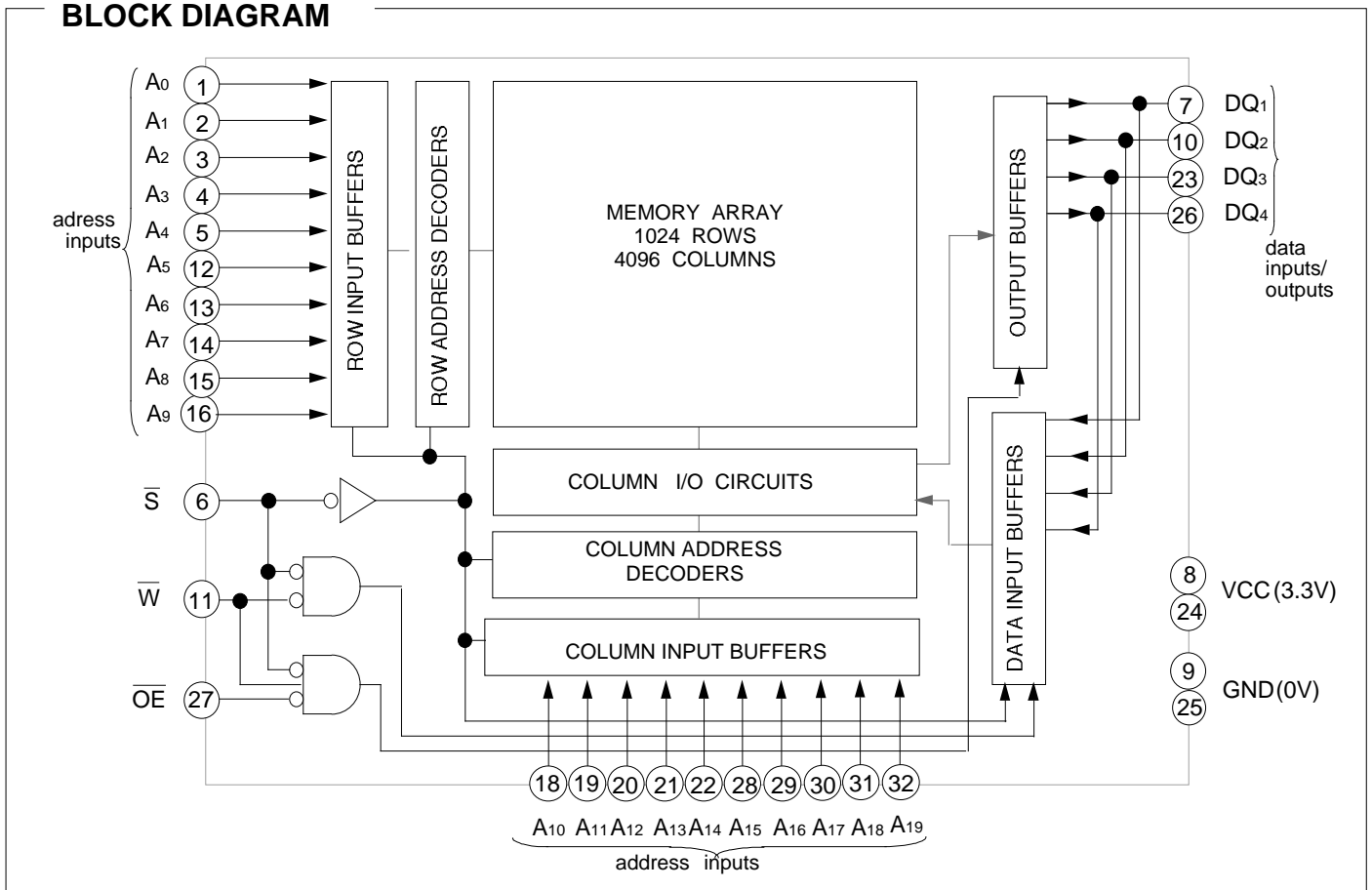
PIN CONFIGURATION (TOP VIEW)

address inputs	A_0	1	32 A_{19}	address inputs
	A_1	2	31 A_{18}	
	A_2	3	30 A_{17}	
	A_3	4	29 A_{16}	
	A_4	5	28 A_{15}	
chip select input	$\overline{S}$	6	27 $\overline{OE}$	output enable input
data inputs/outputs	DQ_1	7	26 DQ_4	data inputs/outputs
(3.3V)	VCC	8	25 GND (0V)	
(0V)	GND	9	24 VCC (3.3V)	
data inputs/outputs	DQ_2	10	23 DQ_3	data inputs/outputs
write control input	$\overline{W}$	11	22 A_{14}	address inputs
	A_5	12	21 A_{13}	
address inputs	A_6	13	20 A_{12}	
	A_7	14	19 A_{11}	
	A_8	15	18 A_{10}	
	A_9	16	17 NC	

M5M54R04AJ

Outline   32P0K(SOJ)

PACKAGE

M5M54R04AJ   : 32pin 400mil SOJ

BLOCK DIAGRAM

MEMORY ARRAY
1024 ROWS
4096 COLUMNS

ROW INPUT BUFFERS
ROW ADDRESS DECODERS
OUTPUT BUFFERS
DATA INPUT BUFFERS
COLUMN I/O CIRCUITS
COLUMN ADDRESS DECODERS
COLUMN INPUT BUFFERS

adress inputs: A_0 (1), A_1 (2), A_2 (3), A_3 (4), A_4 (5), A_5 (12), A_6 (13), A_7 (14), A_8 (15), A_9 (16)

$\overline{S}$ (6) $\overline{W}$ (11) $\overline{OE}$ (27)

data inputs/outputs: (7) DQ_1, (10) DQ_2, (23) DQ_3, (26) DQ_4

(8)(24) VCC (3.3V)
(9)(25) GND (0V)

(18)(19)(20)(21)(22)(28)(29)(30)(31)(32)
A_{10} A_{11} A_{12} A_{13} A_{14} A_{15} A_{16} A_{17} A_{18} A_{19}
address inputs

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FUNCTION

The operation mode of the M5M54R04AJ is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set-up before the write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of $\overline{W}$ or $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high impedance state, and the data bus

contention problem in the write cycle is eliminated.

A read cycle is excuted by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state ($\overline{S}$=L).

When setting $\overline{S}$ at high level, the chip is in a non-selectable mode in which both reading and writing are disable. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$.

Signal-$\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissapation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand by
L	L	X	Write	Din	Active
L	H	L	Read	Dout	Active
L	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		- 2.0* ~ 4.6	V
V_I	Input voltage	With respect to GND	- 2.0* ~ VCC+0.5	V
V_O	Output voltage		- 2.0* ~ VCC	V
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
$T_{stg(bias)}$	Storage temperature(bias)		- 10 ~ 85	°C
T_{stg}	Storage temperature		- 65 ~ 150	°C

* Pulse width _3ns, In case of DC: - 0.5V

DC ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3V $^{+10\%}_{-5\%}$, unless otherwise noted)

Symbol	Parameter	Condition			Min	Typ	Max	Unit
V_{IH}	High-level input voltage				2.0		Vcc+0.3	V
V_{IL}	Low-level input voltage						0.8	V
V_{OH}	High-level output voltage	I_{OH}= - 4mA			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8mA					0.4	V
I_I	Input current	V_I= 0 ~ Vcc					2	uA
$|I_{OZ}|$	Output current in off-state	$V_{I(\overline{S})}$=V_{IH} $V_{I/O}$= 0 ~ Vcc					2	uA
I_{CC1}	Active supply current (TTL level)	$V_{I(\overline{S})}$=V_{IL} other inpus=V_{IH} or V_{IL} Output-open(duty 100%)	AC	10ns cycle			190	mA
				12ns cycle			180	
				15ns cycle			160	
			DC				90	
I_{CC2}	Stand by current (TTL level)	$V_{I(\overline{S})}$=V_{IH}	AC	10ns cycle			90	mA
				12ns cycle			70	
				15ns cycle			60	
			DC				40	
I_{CC3}	Stand by current	$V_{I(\overline{S})}$=Vcc_0.2V other inputs V_I_0.2V or V_I_Vcc - 0.2V					10	mA

Note 1: Direction for current flowing into an IC is positive (no mark).

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CAPACITANCE (Ta=0~70°C, Vcc=3.3V $^{+10\%}_{-5\%}$,unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
C_I	Input capacitance	V_I=GND, V_I=25mVrms,f=1MHz			7	pF
C_O	Output capacitance	V_O=GND, V_O=25mVrms,f=1MHz			8	pF

Note 2: C_I,C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V $^{+10\%}_{-5\%}$,unless otherwise noted)

(1)MEASUREMENT CONDITION

Input pulse levels …………………….…… VIH=3.0V, VIL=0.0V
Input rise and fall time ……………………………………… 3ns
Input timing reference levels …………………… VIH=1.5V, VIL=1.5V
Output timing reference levels ……………… VOH =1.5V, VOL=1.5V
Output loads …………………………………………… Fig.1,Fig.2

Fig.1 Output load

Fig.2 Output load for t_{en}, t_{dis}

(2)READ CYCLE

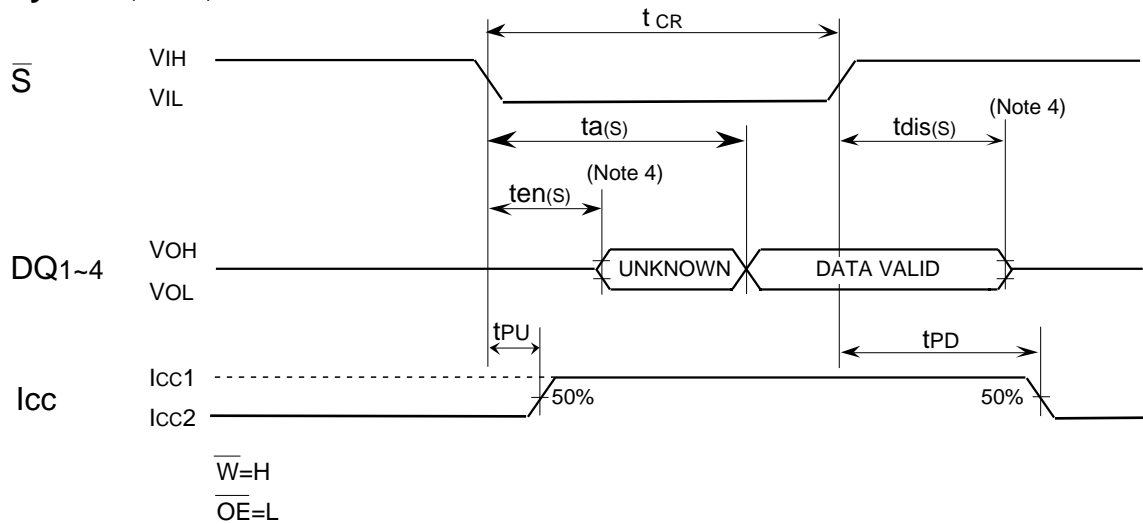| Symbol	Parameter	Limits						Unit
		M5M54R04AJ-10		M5M54R04AJ-12		M5M54R04AJ-15		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	10		12		15		ns
$t_{a(A)}$	Address access time		10		12		15	ns
$t_{a(S)}$	Chip select access time		10		12		15	ns
$t_{a(OE)}$	Output enable access time		5		6		7	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high	0	5	0	6	0	7	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	5	0	6	0	7	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	2		3		3		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		1		1		ns
$t_{v(A)}$	Data valid time after address change	2		3		3		ns
t_{PU}	Power-up time after chip selection	0		0		0		ns
t_{PD}	Power-down time after chip selection		10		12		15	ns

(3)WRITE CYCLE

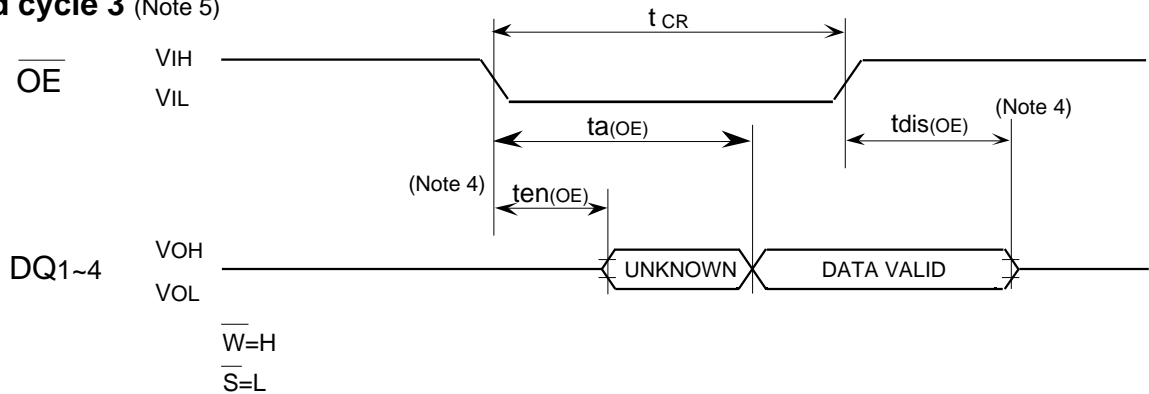| Symbol	Parameter	Limits						Unit
		M5M54R04AJ-10		M5M54R04AJ-12		M5M54R04AJ-15		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	10		12		15		ns
$t_{w(W)}$	Write pulse width ($\overline{OE}$ low)	10		12		15		ns
$t_{w(W)}$	Write pulse width($\overline{OE}$ high)	8		10		10		ns
$t_{su(A)}1$	Address setup time($\overline{W}$)	0		0		0		ns
$t_{su(A)}2$	Address setup time($\overline{S}$)	0		0		0		ns
$t_{su(S)}$	Chip select setup time	8		10		10		ns
$t_{su(D)}$	Data setup time	5		6		7		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{rec(W)}$	Write recovery time	1		1		1		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0	5	0	6	0	7	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	5	0	6	0	7	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0		0		0		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		0		0		ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ High	8		10		10		ns

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(4)TIMING DIAGRAMS

Read cycle 1

$A_{0\sim19}$ — VIH / VIL

t_{CR}

$DQ_{1\sim4}$ — VOH / VOL

$t_{a(A)}$, $t_{v(A)}$, $t_{v(A)}$

PREVIOUS DATA VALID | UNKNOWN | DATA VALID

$\overline{W}$=H
$\overline{S}$=L
$\overline{OE}$=L

Read cycle 2 (Note 3)

$\overline{S}$ — VIH / VIL

t_{CR}

$t_{a(S)}$, $t_{dis(S)}$ (Note 4)

$t_{en(S)}$ (Note 4)

$DQ_{1\sim4}$ — VOH / VOL

UNKNOWN | DATA VALID

t_{PU}, t_{PD}

Icc — Icc1 / Icc2

50%   50%

$\overline{W}$=H
$\overline{OE}$=L
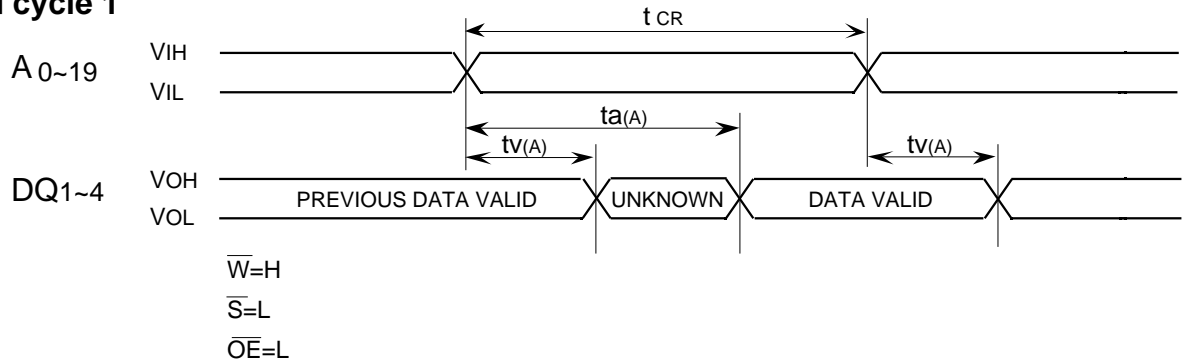
Note 3. Addresses valid prior to or coincident with $\overline{S}$ transition low.
    4. Transition is measured ±500mv from steady state voltage with specified loading in Figure 2.
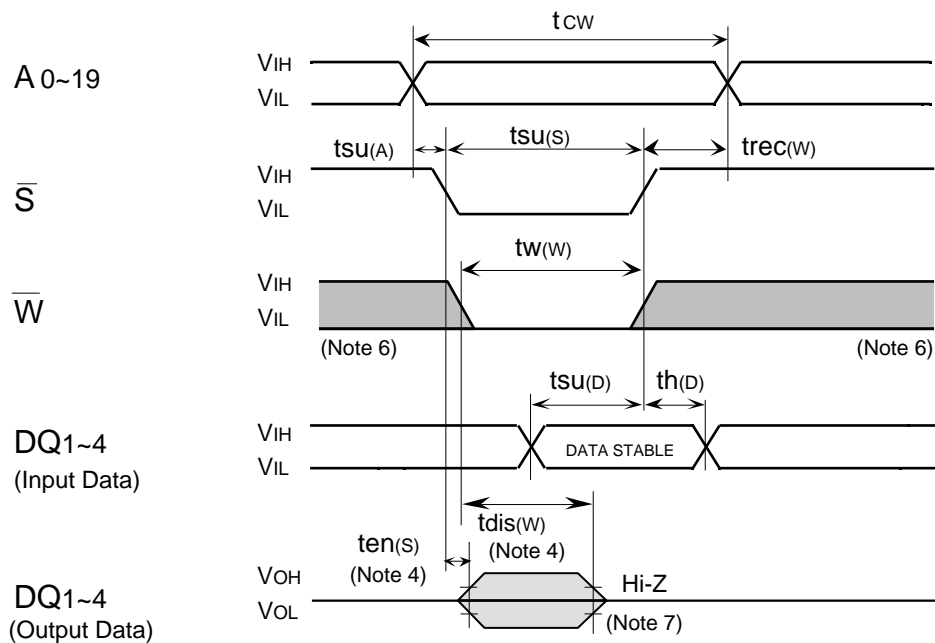
Read cycle 3 (Note 5)

$\overline{OE}$ — VIH / VIL

t_{CR}

$t_{a(OE)}$, $t_{dis(OE)}$ (Note 4)

(Note 4) $t_{en(OE)}$

$DQ_{1\sim4}$ — VOH / VOL

UNKNOWN | DATA VALID

$\overline{W}$=H
$\overline{S}$=L

Note 5. Addresses and $\overline{S}$ valid prior to $\overline{OE}$ transition low by (ta(A)-ta(OE)), (ta(S)-ta(OE))

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Write cycle ($\overline{\text{W}}$ control mode)
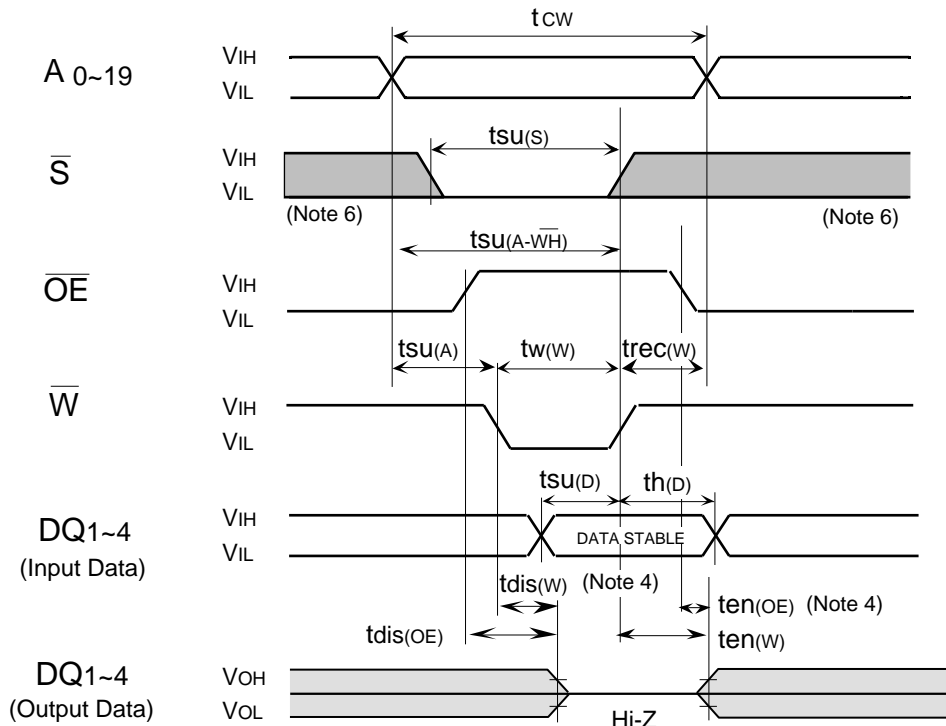
Write cycle($\overline{\text{S}}$ control)

Note 6: Hatching indicates the state is don't care.

7: When the falling edge of $\overline{\text{W}}$ is simultaneous or prior to the falling edge of $\overline{\text{S}}$, the output is maintained in the high impedance.

8: ten,tdis are periodically sampled and are not 100% tested.

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