DATA SHEET

TDA1313; TDA1313T
Stereo continuous calibration DAC (CC-DAC)

Objective specification
File under Integrated Circuits, IC01

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Philips Semiconductors

PHILIPS

Stereo continuous calibration DAC (CC-DAC)

TDA1313; TDA1313T

FEATURES

- 4/8 × oversampling (multiplexed/simultaneous input) possible
- Voltage output (capable of driving headphone)
- Space saving package (SO16 or DIL16)
- Low power consumption
- Wide dynamic range (16-bit resolution)
- Continuous Calibration concept
- Easy application:
  - single 3 to 5.5 V supply rail
  - output voltage is proportional to the supply voltage
  - integrated current-to-voltage converter
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range (−40 °C to +85 °C)
- Compatible with most current Japanese input format multiplexed/simultaneous, two's complement and CMOS)
- No zero crossing distortion
- Cost efficient
- High signal-to-noise ratio
- Low total harmonic distortion.

GENERAL DESCRIPTION

The TDA1313; 1313T is a voltage driven digital-to-analog converter, and is of a new generation of DACs which incorporates the innovative technique of Continuous Calibration (CC). The largest bit-currents are repeatedly generated from one single current reference source. This duplication is based upon an internal charge storage principle having an accuracy which is insensitive to ageing, temperature and process variations.

The TDA1313; 1313T is fabricated in a 1.0 μm CMOS process and features an extremely low power dissipation, small package size and easy application. Furthermore, the accuracy of the intrinsic high coarse-current combined with the implemented symmetrical offset decoding method preclude zero-crossing distortion and ensures high quality audio reproduction. Therefore, the CC-DAC is eminently suitable for use in (portable) digital audio equipment.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1313[1]	16	DIL	plastic	SOT38GG
TDA1313T[2]	16	SO16	plastic	SOT109AG

Notes

1. SOT38-1; 1996 August 15.
2. SOT109-1; 1996 August 15.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V; at code 0000H	–	8	9.5	mA
V_{FS}	full scale output voltage	V_{DD} = 5 V	3.8	4.2	4.6	V
(THD+N)/S	total harmonic distortion plus noise	at 0 dB signal level	–	–88	–81	dB
			–	0.004	0.009	%
		at 0 dB signal level; see Fig.8	–	–70	–	dB
			–	0.03	–	%
		at –60 dB signal level	–	–36	–28	dB
			–	1.6	4.0	%
		at –60 dB; A-weighted	–	–38	–	dB
			–	1.3	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	93	98	–	dB
t_{CS}	current setting time to ±1LSB		–	0.2	–	µs
BR	input bit rate at data input		–	–	18.4	Mbits/s
f_{BCK}	clock frequency at clock input		–	–	18.4	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (V_{OL}; V_{OR})		–	400	–	ppm
T_{amb}	operating ambient temperature		–40	–	+85	°C
P_{tot}	total power dissipation	V_{DD} = 5 V; at code 0000H	–	40	53	mW
		V_{DD} = 3 V; at code 0000H	–	15	–	mW

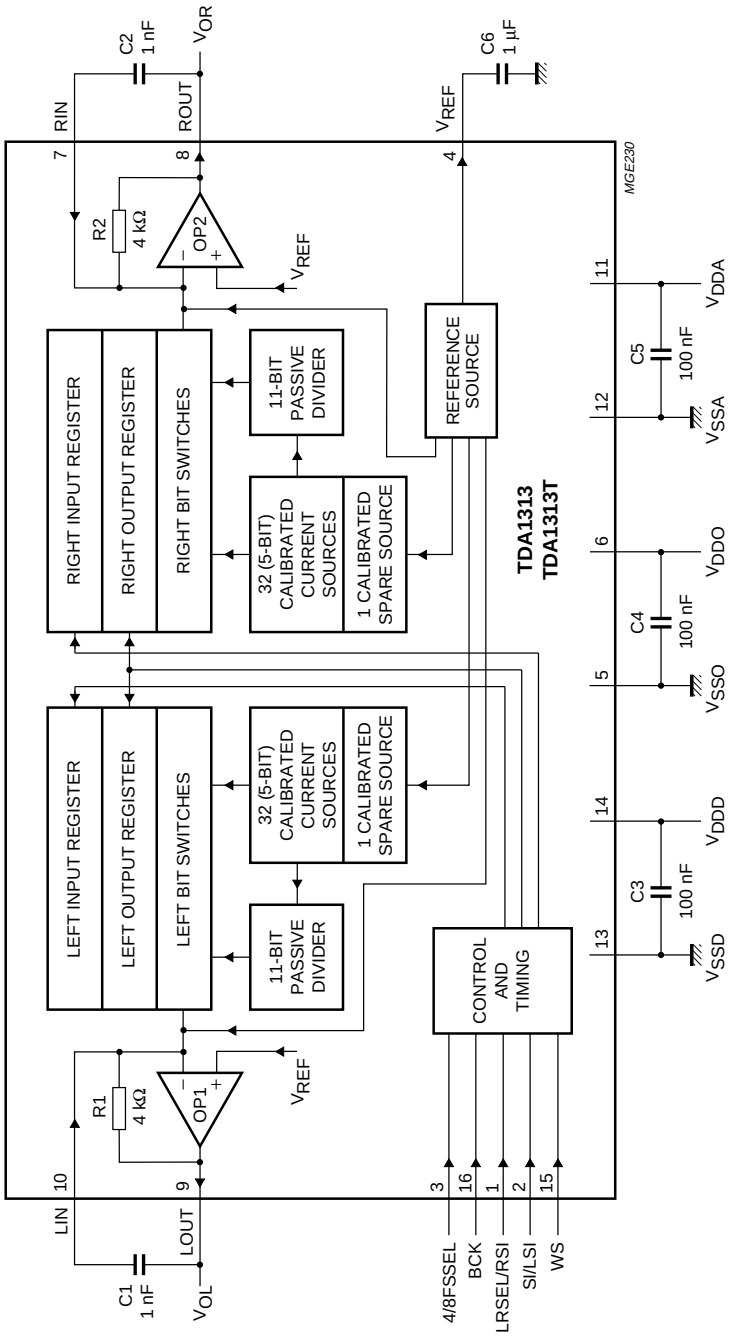


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LRSEL/RSI	1	left/right select; right serial input
SI/LSI	2	serial input; left serial input
4/8FSSEL	3	4/8 oversampling select
V_{REF}	4	reference voltage output
V_{SSO}	5	operational amplifier ground
V_{DDO}	6	operational amplifier supply voltage
RIN	7	right analog input
ROUT	8	right analog output
LOUT	9	left analog output
LIN	10	left analog input
V_{DDA}	11	analog supply voltage
V_{SSA}	12	analog ground
V_{SSD}	13	digital ground
V_{DDD}	14	digital supply voltage
WS	15	word select
BCK	16	bit clock input

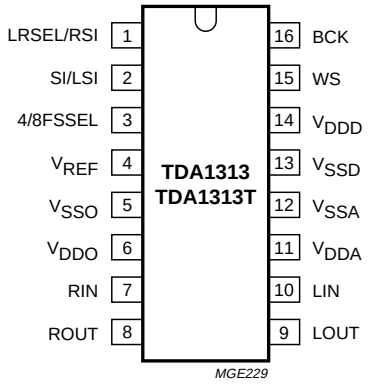


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The basic operation of the continuous calibration DAC is illustrated in Fig.3. The figure shows the calibration and operation cycle. During calibration of the MOS current source (Fig.3a) transistor M1 is connected as a diode by applying a reference current. The voltage V_{gs} on the intrinsic gate-source capacitance C_{gs} of M1 is then determined by the transistor characteristics. After calibration of the drain current to the reference value I_{REF}, the switch S1 is opened and S2 is switched to the other position (Fig.3b). The gate-to-source voltage V_{gs} of M1 is not changed because the charge on C_{gs} is preserved. Therefore, the drain current of M1 will still be equal to I_{REF} and this exact duplicate of I_{REF} is now available at the I_O terminal.

In the TDA1313; 1313T, 32 current sources and one spare current source are continuously calibrated (see Fig.1). The spare current source is included to allow continuous converter operation. The output of one calibrated source is connected to an 11-bit binary current devider which consists of 2048 transistors. A symmetrical offset decoding principle is incorporated and arranges the bit switching in such a way that the zero-crossing is performed by switching only the LSB currents.

The TDA1313; T (CC-DAC) accepts serial input data format of 16 bit word length. The most significant bit (bit 1) must always be first. The timing is illustrated in Fig.4 and the input data formats are illustrated in Figs 5 and 6.

Data is placed in the right and left input registers (Fig.1). The data in the input registers is simultaneously latched to the output registers which control the bit switches.

V_{REF} and V_{FS} are proportional to V_{DD}.

Where: $V_{DD1}/V_{DD2} = V_{FS1}/V = V_{REF1}/V_{REF2}$

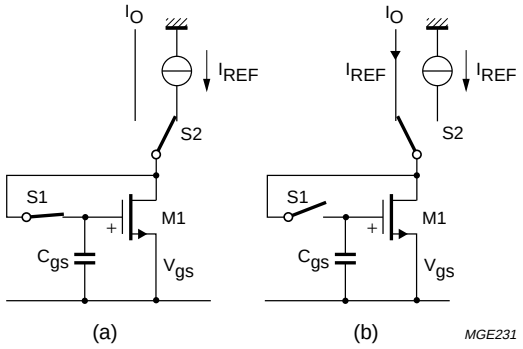


Fig.3 Calibration principle; (a) calibration (b) operation.

Table 1 Mode application

4/8FSSEL	LRSEL/RSI	MODE	FIGURE
0	1	4FS/left = HIGH	6
0	0	4FS/left = LOW	6
1	data right	8FS	5

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–	6.0	V
T_{XTAL}	maximum crystal temperature		–	+150	°C
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{ES}	electrostatic handling	note 1	–2000	+2000	V
		note 2	–200	+200	V

Notes

1. Human body model: C = 100 pF; R = 1500 Ω; 3 zaps positive and negative.
2. Machine model: C = 200 pF; L = 0.5 μH; R = 10 Ω; 3 zaps positive and negative.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	DIL16	75 K/W
	SO16	120 K/W

CHARACTERISTICS

$V_{DDD} = V_{DDA} = V_{DDO} = 5$ V; $T_{amb} = 25$ °C; measured in Fig.7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		3.0	5.0	5.5	V
I_{DD}	total supply current	at code 0000H	–	8.0	9.5	mA
I_{DDD}	digital supply current	at code 0000H; no clock running	–	0.2	–	mA
I_{DDA}	analog supply current		–	4.6	5.5	mA
I_{DDO}	operational amplifier supply current		–	3.4	4	mA
PSRR	power supply ripple rejection	at code 0000H; note 1	–	30	–	dB
Digital inputs; pins WS, BCK, 4/8FSSEL, LRSEL/RSI and SI/LSI						
$\lvert I_{IL} \rvert$	input leakage current LOW	$V_I = 0.V$	–	–	10	µA
$\lvert I_{IH} \rvert$	input leakage current HIGH	$V_I = 5.5$ V	–	–	10	µA
f_{BCK}	clock frequency		–	–	18.4	MHz
BR	bit rate data input		–	–	18.4	Mbits/s
f_{WS}	word select input frequency		–	–	384	kHz
Timing (see Fig.4)						
t_r	rise time		–	–	12	ns
t_f	fall time		–	–	12	ns
t_{CY}	bit clock cycle time		54	–	–	ns
t_{BCKH}	bit clock pulse width HIGH		15	–	–	ns
t_{BCKL}	bit clock pulse width LOW		15	–	–	ns
$t_{SU;DAT}$	data set-up time		12	–	–	ns
$t_{HD:DAT}$	data hold time to bit clock		10	–	–	ns
$t_{HD:WS}$	word select hold time		10	–	–	ns
$t_{SU;WS}$	word select set-up time		12	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog outputs; pins V_{OL} and V_{OR}						
V_{FS}	full-scale voltage		3.8	4.2	4.6	V
TC_{FS}	full-scale temperature coefficient		–	±400	–	ppm
R_L	load resistance		3	–	–	kΩ
C_L	load capacitance		–	–	200	pF
V_{REF}	reference output voltage		3.16	3.33	3.5	V
V_{DC}	output DC voltage		2.25	2.5	2.75	V
(THD+N)/S	total harmonic distortion plus noise	at 0 dB signal level; note 2	–	–88	–81	dB
			–	0.004	0.009	%
		at 0 dB signal level; see Fig.8	–	–70	–	dB
			–	0.03	–	%
		at –60 dB signal level; note 2	–	–36	–28	dB
			–	1.6	4.0	%
		at –60 dB signal level; A-weighted; note 2	–	–38	–	dB
			–	1.3	–	%
		at 0 dB signal level; f = 20 Hz to 20 kHz	–	–84	–70	dB
			–	0.006	0.03	%
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
α	channel separation		86	95	–	dB
		see Fig.8	–	70	–	dB
$\lvert\delta I_O\rvert$	unbalance between outputs	note 2	–	0.2	0.3	dB
$\lvert t_d\rvert$	time delay between outputs		–	±0.2	–	µs
S/N	signal-to-noise ratio at bipolar zero	A-weighted; at code 0000H	93	98	–	dB

Notes

1. V_{ripple} = 1% of the supply voltage; f_{ripple} = 100 Hz.
2. Measured with 1 kHz sinewave generated at a sampling rate of 384 kHz.

QUALITY SPECIFICATION

In accordance with UZW-BO/FQ-0601.

TEST AND APPLICATION INFORMATION

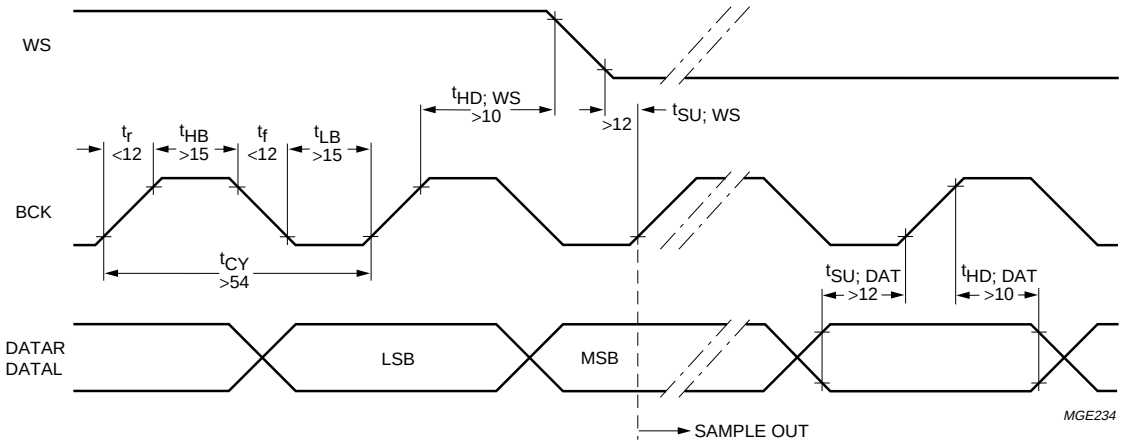


Fig.4 Timing of input signals.

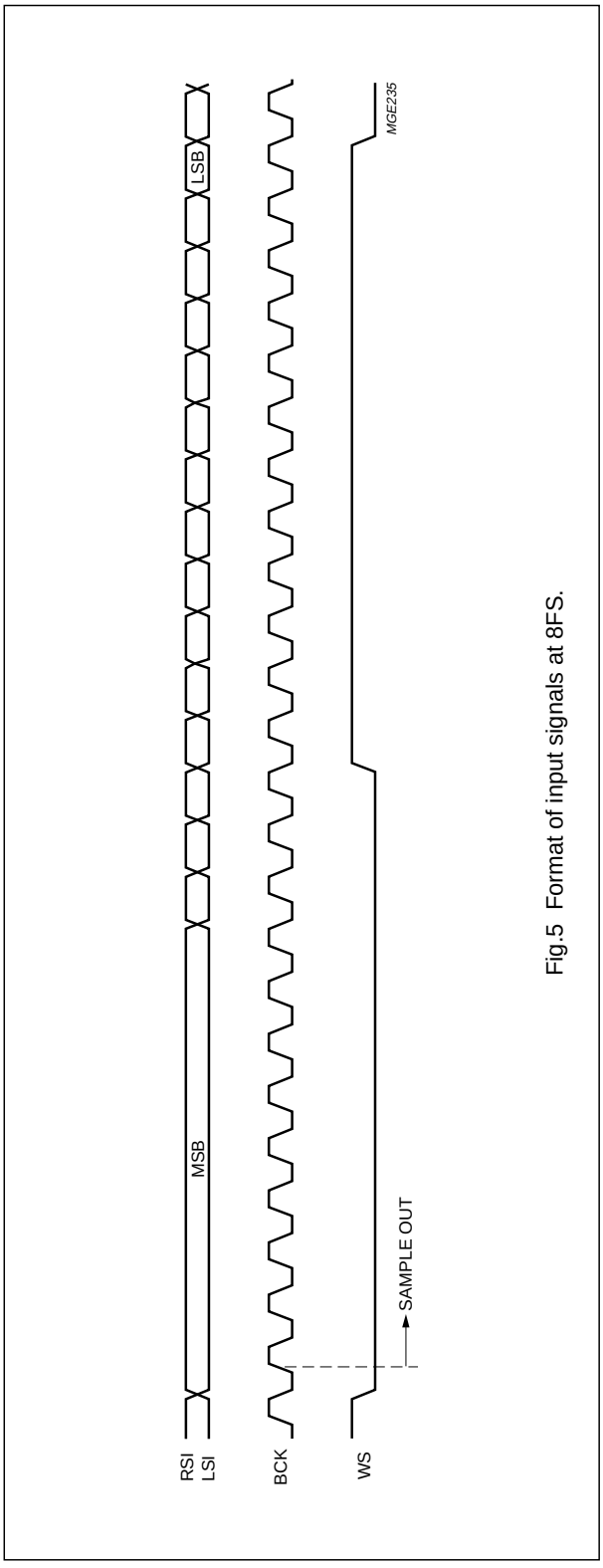


Fig.5 Format of input signals at 8FS.

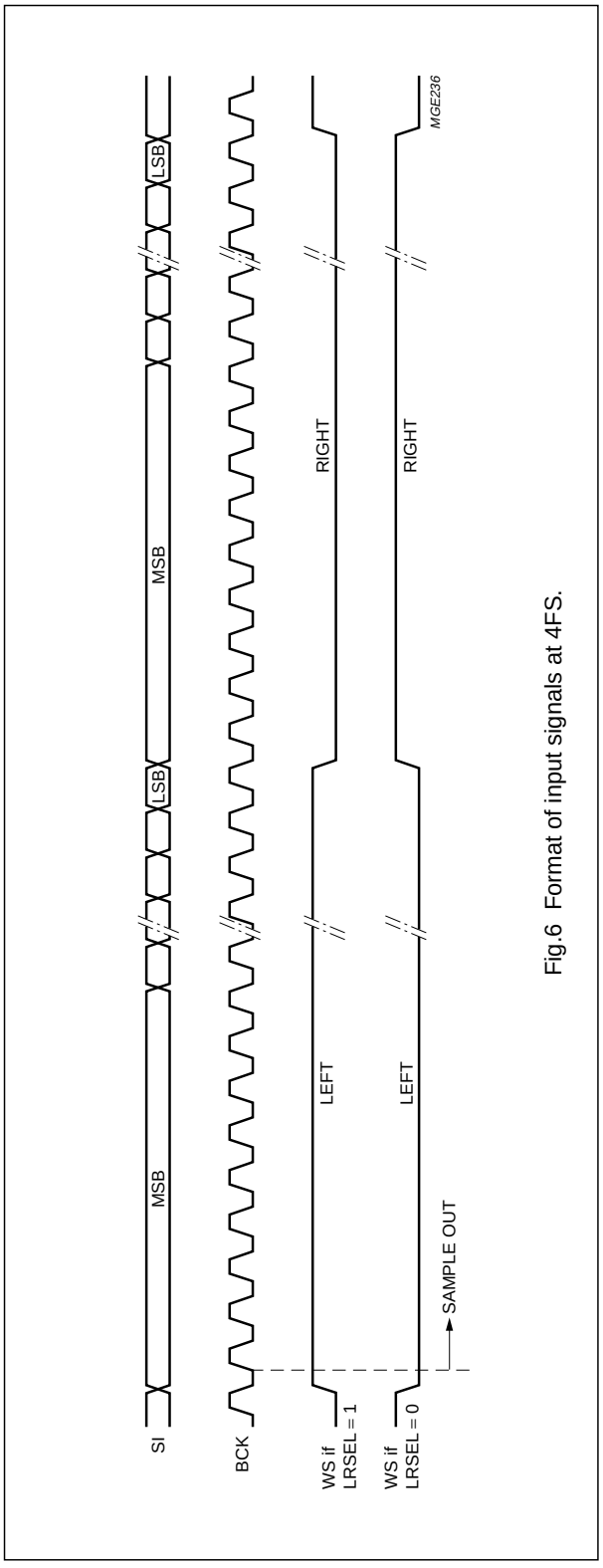


Fig.6 Format of input signals at 4FS.

APPLICATION INFORMATION

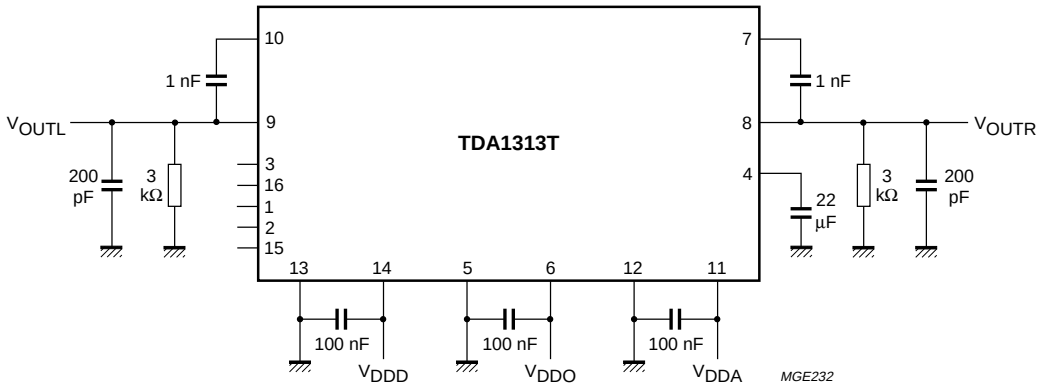


Fig.7 TDA1313T as line driver with 3 kΩ/200 pF load.

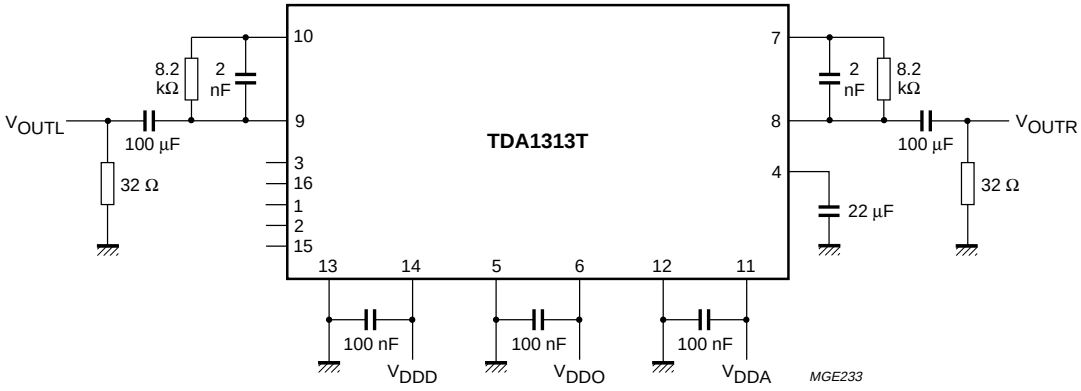
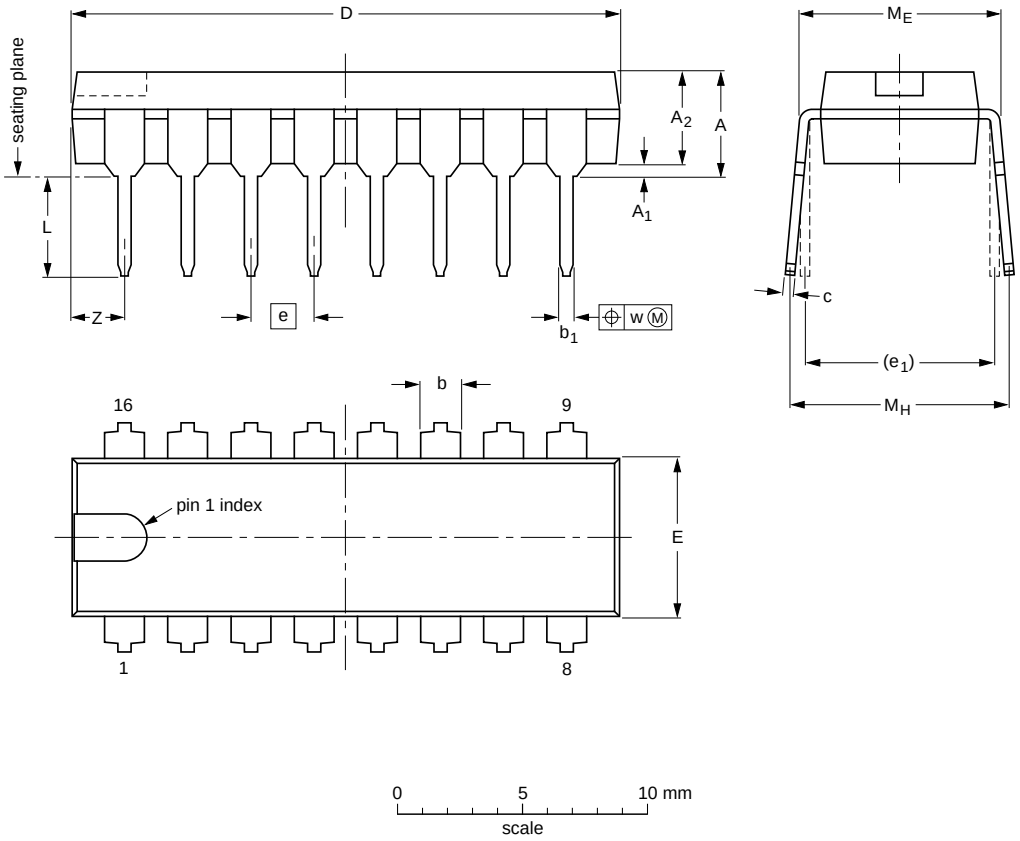


Fig.8 TDA1313T as headphone driver with 32 Ω load.

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

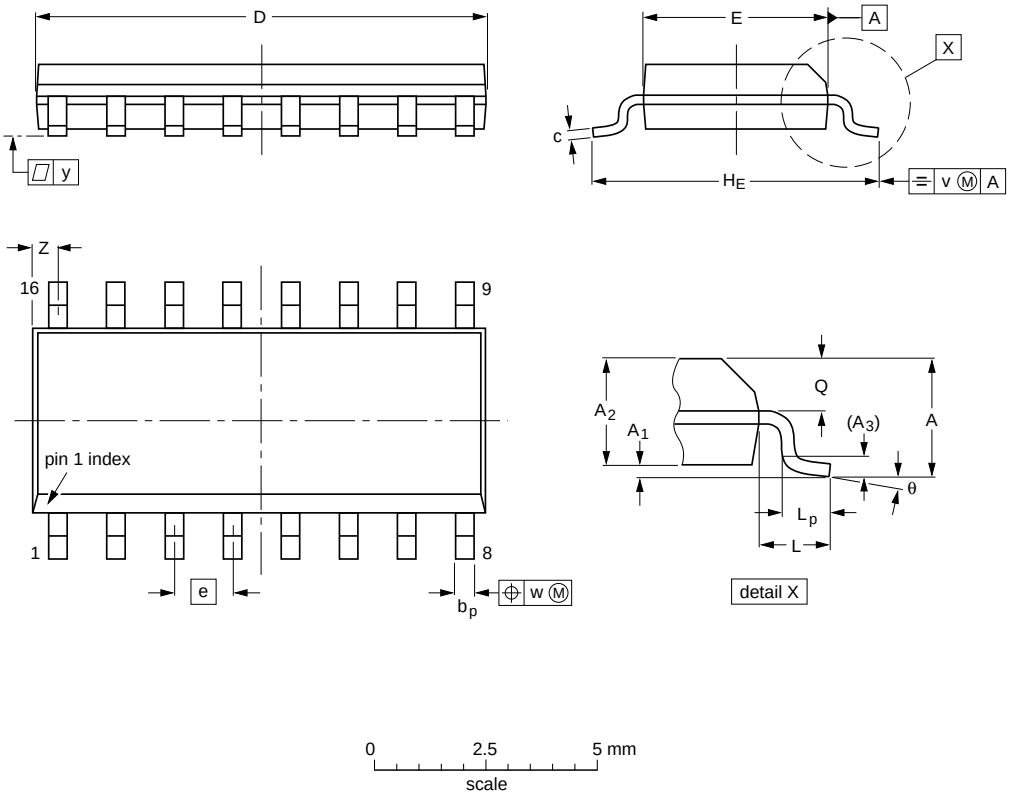
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.